SEMICONDUCTOR MANUFACTURING TEST STRUCTURES

The motivation to use test structures is best captured by a statement made by Lord Kelvin in 1883: "When you can measure what you are speaking about, and express it in numbers, you know something about it; but when you cannot measure it, when you cannot express it in numbers, your knowledge is of a meager and unsatisfactory kind." This philosophy has been employed in semiconductor manufacturing to quantify the process in terms that relate to fabrication performance and facilitate transfers to new locations. The test structures can be deployed in-line as well as at end of line electrical testing, where subcircuit components are tested, and are now viewed as an essential diagnostic and control tool during fabrication processing. Since a test structure is designed to relay information about the particular process or device in question, a universal test structure does not exist. Consequently, this article presents a subset of the more commonly applied test structures, though it must be acknowledged that as new circuits are devised so too must new test structures be created.

SHEET RESISTANCE

The most fundamental measurement made in semiconductor testing is that of resistance. Three terms arise when describing this: resistance, resistivity, sheet resistance. These are frequently (and mistakenly) interchanged. The *resistivity* of a material, usually denoted by ρ, with units of Ω-cm, is a property of, and unique to, that material. The relationship of resis-

tivity to resistance and sheet resistance is shown in Fig. 1. Passing a current between faces A and B and measuring a voltage V_{AB} yields a *resistance* value, $R = V_{AB}/I_{AB}$. For a given thickness of material, T, a quantity, R_S, the *sheet resistance,* can be defined as $R_S = R/T$. In semiconductor processing, the value T is defined by the layer thickness, such as polysilicon or metal, or the diffused layer defined by the junction depth. The sheet resistance may vary in the vertical plane, particularly for diffused resistors, and is given by

$$R_s = \frac{1}{\sigma} = \frac{1}{\frac{1}{T}\int_0^T qC(z)\mu(z)\,dz}$$

where σ is the conductivity, $C(z)$ is the carrier concentration in the z direction, q is the charge on an electron, and $\mu(z)$ is the carrier mobility.

The procedure used to measure resistivity was advanced by L. J. van der Pauw (1), who showed that the specific resistivity of an arbitrary shape can be measured without knowing the current flow pattern providing the contacts are small and placed on the circumference of the sample and that the sample is constant in thickness and contains no isolated holes. A current, I_{ab}, is applied between contacts a and b, and a voltage, V_{cd}, is measured between c and d. A value, $R_{ab,dc}$, is defined as $(V_c - V_d)/I_{ab}$. Similarly, $R_{bc,da}$ is defied as $(V_a - V_d)/I_{bc}$. The resistivity can be expressed as

$$R_s = f\left[\frac{\pi T R(\pm I)}{\ln 2}\right]$$

where f is a function of the ratio $R_{ab,cd}/R_{bc,da}$ only and satisfies

$$\cosh\left[\frac{r-1}{r+1}\frac{\ln 2}{f}\right] = \frac{1}{2}\exp\left(\frac{\ln 2}{f}\right)$$

where

$$r = \frac{(V_{dc}+V_{cd})(I_{da}+I_{ad})}{(I_{ab}+I_{ba})(V_{cb}+V_{bc})}$$

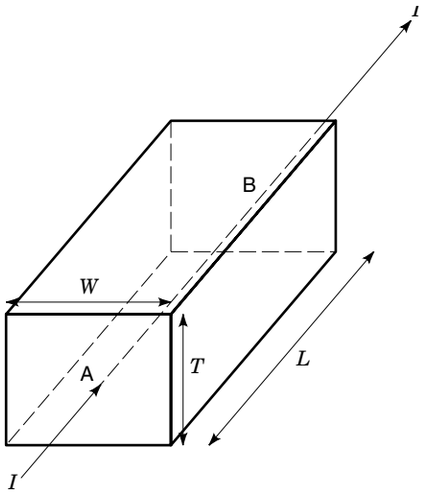

Figure 1. Current is forced into face A and out of face B. The measured resistance is a function of the length, L, width, W, and thickness, T, of the block.

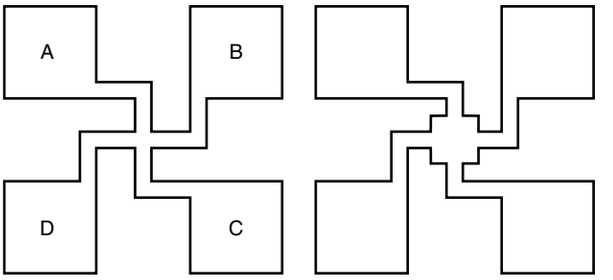

Figure 2. (left) Standard van der Pauw structure. The resistance at the center of the cross is measured using the 4 contact pads, A, B, C, D; (right) alternative van der Pauw structure. The larger block in the middle lessens the sensitivity to non-uniformities in the film.

The practical implementation of this is seen in the Greek cross structure [Fig. 2(left)] and provides a procedure for measuring sheet resistance (2). The commonly adopted procedure is as follows:

1. Force current $I_{ab}(+I)$ *into* terminal a and *out of* terminal b, and measure a voltage, $V_{dc}(+I)$, between terminals c and d.
2. Force a current $I_{ab}(-I)$ *into* b and *out of* a, and measure voltage $V_{dc}(-I)$ between terminals c and d.
3. Force current $I_{ad}(+I)$ *into* terminal a and *out of* terminal d, and measure a voltage, $V_{bc}(+I)$, between terminals c and b.
4. Force a current $I_{ad}(-I)$ *into* d and *out of* a, and measure voltage $V_{bc}(-I)$ between terminals c and b.

The first two measurements yield the value of the zero degree resistance as

$$R_0 = [V_{dc}(+I)/I_{ab}(+I) + V_{dc}(-I)/I_{ba}(-I)]$$

(Note that both $V_{dc}(-I)$ and $I_{ba}(-I)$ are negative.) Similarly, the 90° position resistance is

$$R_{90} = [V_{cb}(+I)/I_{da}(+I) + V_{cb}(-I)/I_{da}(-I)]$$

(Note that both $V_{cb}(-I)$ and $I_{da}(-I)$ are negative.) The average resistance is given by

$$R = [R_0 + R_{90}]/2$$

Using the van der Pauw theorem, the sheet resistance is given as

$$R_S = f[\pi R(\pm I)/\ln 2]$$

where f is as defined previously and is usually taken as 1. In fact, f is related to F_A, the asymmetry factor by

$$F_A = [R_0(\pm I) - R_{90}(\pm I)]/R(\pm I)]$$

If F_A is less than 10%, f is found to be within 0.1% of I.

Two other useful parameters can be calculated. F_0 is defined as

$$F_0 = \frac{\text{abs}[R_0(+I) - R_0(-I)] + \text{abs}[R_{90}(+I) - R_{90}(-I)]}{2R(\pm I)}$$

F_0 is the zero offset factor and should be small to ensure that the offset voltages are negligible.

It is essential when performing resistance measurements to establish the Ohmic regime. To quantify this, a linearity factor, F_L, may be calculated as

$$F_L = \frac{R(\pm nI) = R(\pm I)}{R(\pm I)}$$

where n is an integer. This region exists between the low-level noise and the high current joule heating and may reasonably be expected to extend over several decades of forced current.

The technique has been applied to measure resistances between 0.01 Ω/sq and 10^6 Ω/sq. Variations on the Greek cross structure exist, and general rules established for their layout (3) detail some of these. In designing a Greek cross structure, the arm width to length ratio should be greater than 2 to minimize errors. Further, since voltage sensed is at the center of the cross, crosses of the type shown in Fig. 2(left) are better suited when average sheet resistance measurements are required and the type shown in Fig. 2(right) when localized sheet resistances are sought. (Where the material consists of a grain structure, the size of the grains can lead to highly variable results when the grain size is greater than the linewidth.)

Though not a test structure itself, a silicon sample is often measured using a four-point probe to determine the resistivity and, from van der Pauw's work, the sheet resistance. A current source forces current through the outer two probes, which are co-linear with the inner two probes, which themselves are used to measure voltage. The resistivity is given by

$$\rho = \left(\frac{\pi d}{\ln 2}\right)\frac{V_M}{I_S}$$

and so the sheet resistance is given by

$$R_S = \left(\frac{\pi}{\ln 2}\right)\frac{V_M}{I_S}$$

The factor

$$\left(\frac{\pi}{\ln 2}\right)$$

is the conversion factor (= 4.53) often quoted in commercial 4-point probe systems.

LINEWIDTH

The width of a conducting line is one of the critical measurements in semiconductor metrology. The SEMI (Semiconductor and Equipment Materials International) definition of linewidth states "at a given cross-section of the line, the distance between the air-line material boundaries at some specified height above the interface between the patterned layer in which the line is formed and the underlying layer." Further, it is acknowledged that the result is dependent on the method used to measure the linewidth, be it optical, electrical, or by electron microscopy, which in itself poses a difficulty in defining linewidth standards (4). Routinely measured by optical systems, the linewidth is usually correlated to the distance between two points in output signal of the measurement equipment, and the expression "full width at half maximum" is often employed to identify these points. The electrical linewidth is defined as "the effective conductive path width of a patterned uniform conducting film whose length is typically much larger than its width." The conducting line may suffer from edge roughness and variable slope, which will likely be captured by the optical and scanning electron microscope (SEM) methods as these focus on a small section of the line. The electrical measurement, however, averages these out, providing an extremely repeatable value of linewidth, whereby three sigma values of around 2 nm may be expected. Since the line must be conducting, the electrical method cannot measure photoresist images, which continues to use optical and electron microscope techniques. (See also the section titled "Optical Structures.")

Linewidths of conducting layers may be measured electrically using a linewidth bridge structure. The general shape is shown in Fig. 3. Current, I_S, is forced between taps C and D and voltage V_M measured between taps A and B. Consistent with the approach in measuring sheet resistance, the current should be reversed and the average of the two measurements taken. The *electrical* or effective linewidth is computed as

$$W = R_S L_{AB}\frac{I_S}{V_M}$$

Some general rules regarding the taps should be observed:

1. The tap spacing is center-to-center, L_{AB}. L_X is incorrect.
2. All voltage taps should be identical in layout.
3. Voltage taps should be on the same side of the line.
4. The tap should extend on one side of the line only.
5. The tap should be placed more than twice the channel width from a discontinuity.
6. Tap width should be as small as possible, provided that overetch does not cause the structure to fail.
7. The tap length should be greater than half the width.

The length of the line is usually drawn at least one order of magnitude greater than the width. The split cross bridge structure (5) is a variation of the standard bridge and is a self-verification structure as it uses the pitch, which must remain constant, as an assurance tool. There may, however, be a difference between the width of an isolated line and one of a series of parallel lines, designed at minimum pitch. Inherent in all of this is the assumption of uniformity in the lateral dimension, though deviations from the above theory

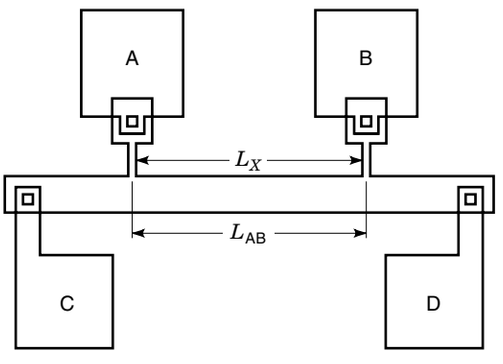

Figure 3. A Linebridge structure to measure electrical linewidth.

can exist and sheet resistance itself can, in some circumstances, be width dependent. The line-shortening effect of the voltage taps on the extracted width can be compensated by the addition of dummy taps (6), which lie either side of the line in question, enabling bridge lengths to be decreased and tap widths to be arbitrarily increased. This powerful feature means that short lines can be measured; thus local effects such as nonuniformities in the line can be evaluated.

MISALIGNMENT

Layer-to-layer alignment (or registration overlay and feature placement) is critical in many cases, and several techniques exist to measure this. While optical instruments are the preferred tool to measure overlay where the layers are visible because of the low measurement cost, good repeatability, and the ability to measure nonconductive layers, they are prone to systematic errors known as tool-induced shift (TIS) and wafer-induced shift (WIS). TIS may be traced to the equipment and WIS to the asymmetries of the optical cross sections of the features caused by the fabrication process (7). Optical misalignment structures are discussed in a following section.

A variety of electrical test structures is available: the van der Pauw [Fig. 4(a)], the differential linebridge (referred to in a slightly different form as a Stickman structure) [Fig. 4(b)], and the sliding wire potentiometer [Fig. 4(c)].

As with the measurement of linewidth, the effects of the voltage taps can be mitigated to produce very high precision structures, accurate down to nanometer level on the sliding wire potentiometer, that have been quantified and incorporated into the *MOATS* test structure (8). Approximate comparisons suggest optical reproducibility of 10 nm compared to MOATS values of <10 nm uncertainty and <2 nm reproducibility for conductive films. A variety of other techniques exist to measure registration. Optical and electrical verniers are commonly used. Electrical verniers rely on digital measurements that quantify the misalignment by testing for electrical continuity and offer ease of testing but suffer from high pad count—a problem common to all alignment structures generally. Standard electrical verniers provide $(N - 1)$ connections for the use of N pads. The incorporation of diodes to passive electrical verniers can increase this to $N(N - 1)$ (9) by using the diodes to restrict the flow through parallel parasitic paths in the vernier.

In the case of polysilicon gate to active area misalignment, the structures are not electrically connected, but polysilicon can be biased to switch off the channel and the standard differential line bridge used. An alternative approach is to employ nonorthogonal intersection of the polysilicon to the active area, which can increase sensitivity by altering the angle of overlap (10). For diffused emitter-base registration, a modified bridge potentiometer can use the difference between intrinsic and extrinsic base regions to quantify alignment (11).

CONTACT RESISTANCE

Ohmic contacts between metals and semiconductors are defined as interfaces that possess current-voltage characteristics with a linear region for both directions of current flow through the contact over a wide range of temperatures. However, to be useful in semiconductor applications a further criterion is that the resistance must be sufficiently small such that the effect on device performance is negligible. The contact resistivity, ρ_c, is defined as the ratio of the voltage across the layer, v_c, and the current density there, j_c, and is measured in Ω-cm^2. (The contact resistance, R_C, is defined as the contact resistivity per unit area.) A common approach to assess contact resistance has been to measure the resistance of a series of connected contacts in a so-called contact chain, and, using the known values of sheet resistances of the two layers, an average value of the contact resistance can be obtained. Usually performed as a two-terminal test, this procedure suffers the limitations of a non-Kelvin measurement (i.e., including tap and probe to pad resistances in the measurements). Further, the computed value returns only the front contact resistance as opposed to the *interfacial* and *end contact* resistances. The Berger (12) structure shown in Fig. 5 was developed to separate the bulk resistance from the interface resistance. Three contacts are made to a diffused region where the width of the contact is made as close to the diffused width as possible. Two

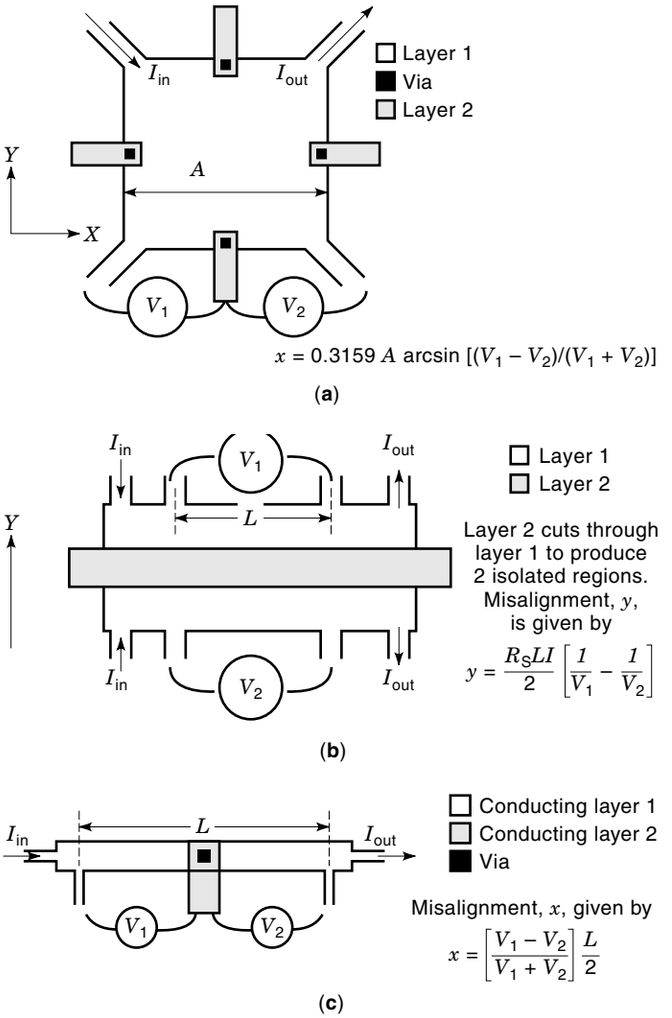

Figure 4. (a) Misalignment, x, given as shown. Top and bottom results should be averaged. Symmetrical conditions yield the y misalignment. (b) The differential linebridge. (c) Sliding wire potentiometer.

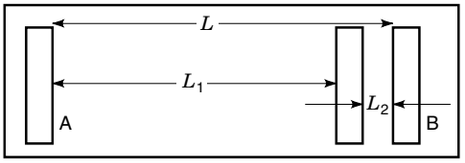

Figure 5. The Berger contact resistance structure.

contacts are placed close together, while the third is separated by a much greater distance. Current is forced and voltage measured, to produce three resistance values. The total resistance, R_t, is given as

$$R_t = R_S \frac{L}{W} + 2R_c$$

Similarly, the separately measured resistances R_1 and R_2 can provide R_c and R_S as

$$R_c = \frac{R_1 L_2 - R_2 L_1}{2(L_2 - L_1)}$$

$$R_S = \frac{(R_2 - R_1)W}{(L_2 - L_1)}$$

Alternatively, the six terminal cross Kelvin structure shown in Fig. 6 can be used to measure R_C as well as evaluating the contact layer uniformly. Current is forced from the lower layer (taps 1 or 3) through the contact to the upper (tap 5), and voltage is sensed via two different pads, one lower (either 2 or 4) and one upper (tap 6). By averaging these results contact misalignment errors can be minimized.

The measured contact resistance is affected by the configuration of the oversized area at the contact window. To compensate for misalignment, the conducting layer is oversized to accommodate the contact window. If the oversize is maintained in the linewidth, then the structure is defined as L type. If the oversize exists solely around the contact window, then the structure is defined as D type. Both structures exaggerate the contact resistance, an effect more noticeable at low ρ_c values. A self-aligned six-terminal structure has been presented, but it requires two masks to define the lower layer.

OPTICAL STRUCTURES

While electrical techniques are generally applicable to conducting structures and are generally preferred because of the advantages of speed, automation, and interpretation, optical test structures do not suffer from this limitation. (Correlation between the two is often desirable.) Optical structures are necessary to align layers and can be used to measure the very same alignment. Commonly used structures are the box-in-box, frame-in-frame, and bars-in-bars devices, all of which place an outer square on the first photo and an inner square on the second photo. The misalignment can be accurately quantified by the relative offsets measured in the x and y directions. The measurement techniques of available tools vary: Some systems analyze a pixel image of a uniformly illuminated target; others may employ interferrometric techniques. Optical verniers are also routinely used, whereby the misalignment of one layer to the previous can be read directly from the printed image.

Checkerboard structures, made up of incremental overlay of identically sized squares, are often used as a resolution assessment and etch monitor. Here squares of a particular size are designed in off-set columns such that the bottom corner of one square just touches the top corner of another. This column pair is duplicated in the $+x$ direction, simultaneously incrementing the size of the square by a small predetermined unit, and in the $-x$ direction, reducing the square size by the same amount. In all cases the pitch is maintained, so that the degree of overlap and underlap varies in a linear fashion. Since the human eye is particularly adept at picking out straight lines, the column that shows the squares just touching is easily identified. If an overetch has occurred, then the line of contact moves to the right by that amount of overetch, which in turn is related to the designed overlap increment. This structure can be easily calibrated when the standard etch measurements are made and subsequently used with no need for measurement equipment.

Akin to this is the Murray dagger (13), which comprises a wedge cut into a single layer such that the size of the gap is calibrated to its position along the wedge. The size of the opening, then, is simply read from the calibrated scale along the side and any variations in the pattern transfer procedure result in a change in the position of the end of the wedge.

Recent developments have employed the use of holograms (14) to yield information on the pattern transfer process. This has the advantage of employing nondestructive testing on the actual circuit and can be applied to nonconducting layers such as photoresist. By comparing the characteristics of a holographic image to the expected image, a fast response can be obtained using a simple test set-up. However, this process is immature compared to the more established techniques and has yet to find widespread use.

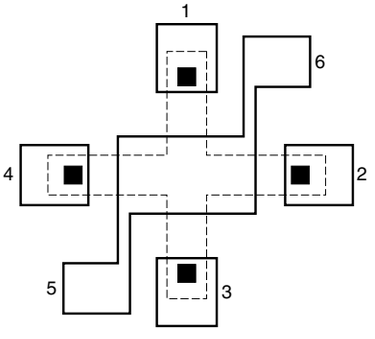

Figure 6. The six-terminal contact resistance structure.

RELIABILITY

Device reliability is generally accepted as following the bathtub trend, with high infant mortality followed by a low failure rate over a long period of time before finally reaching wearout. (Plotting the number of failures against time follows a "U" or "bathtub" shape.) Predicting the lifetime of these devices using accelerated testing is a particularly difficult task as the end result is, in essence, statistical in nature. Accelerating factors include temperature, electric field, current density, moisture and chemical contamination, and mechanical stress. Many test structures make use of an Arrhenius relationship of temperature and reaction rate. Fast techniques have been developed

to evaluate the metal system and are known by their acronyms:

TRACE—Temperature-ramps Resistance Analysis to Characterize Electromigration

BEM—Breakdown Energy of Metal

SWEAT—Standard Wafer-level Electromigration Acceleration Test

WIJET—Wafer-level Isothermal Joule heated Electromigration Test

CAFÉ—Constant Acceleration Factor Electromigration.

All suffer from the lack of confidence in extrapolation of results to long-term prediction.

A common failure of metal tracks is electromigration (EM), caused by momentum transfer as electrons collide with atoms. While the electrons themselves do not possess enough energy to cause the atom to relocate to an adjacent vacancy site, they do increase the probability. Because there are more vacancies at grain boundaries, most of the EM occurs there and the net result is in the direction of electron flow. This has been shown to be a function of both current density and temperature, and the mean time to failure (MTF) is defined in Black's equation:

$$\frac{1}{\mathrm{MTF}} = AJ^n \exp\left[\frac{-E_a}{kT}\right]$$

where E_a is the activation energy, J is the current density, k is Boltzmann's constant, T is the absolute temperature, and A is a constant. The value of n can vary between 1 and 7. The activation energy varies according to metal composition. Both thermal gradients and mechanical stress gradients can cause preferential self-diffusion of the metal and so can enhance or retard the EM depending on the direction. (A noticeable effect is seen when the width of the line under stress is smaller than the grain size of the metal and is described as having a bamboo structure.) The stress can be induced by temperature or current. However, as the current contributes to the heating through Joule heating, only a common stress can be defined using self-heated structures. Typically an acceleration factor is calculated as the ratio of the MTF for two different current and temperature conditions. This acceleration factor is then held constant for different tests.

In its simplest form the American Society for Testing and Materials (ASTM) EM test structure forces a current along a long (on the order of 1 mm) metal track and measures the voltage using Kelvin taps. A modification of this is seen in the SWEAT structure (Fig. 7), in which the reduced line length between taps may reduce defect sensitivity and large thermal gradients may occur at the transition between regions. The lines under test must be greater than one Blech length (defined as the threshold value of the product of the length and current density at which EM ceases to occur) and may be heated by polysilicon resistors. The test is controlled by a predetermined increase in voltage or an open circuit condition, the latter being a destructive test.

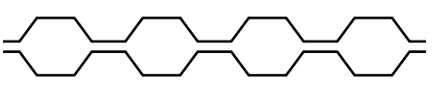

Figure 7. The SWEAT structure.

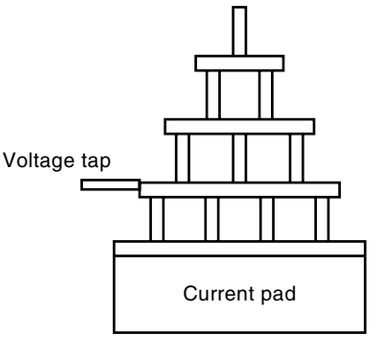

Figure 8. The Tower of Babel structure.

The ASTM and SWEAT structures are susceptible to premature failure caused by the abrupt change from bamboo to multigrain microstructure. They are also candidates for the reservoir effect, in which one large area of metal may act as an infinite source of material to the test stripe, replenishing any regions depleted due to EM. The Babel tower structure is an attempt to resolve these issues and is shown in Fig. 8. Each segment contains one or more lines of equal width, with the segments indexed until the last contains lines that are each carrying a small proportion of the total current, thus maintaining the low thermal gradient at that point but increasing the EM resistance so that there is a lower probability of failure compared with the test stripe. The test structures are usually located on both planar and nonplanar substrates, as the stepped topography is known to reduce the lifetime.

In addition to single-layer EM test structures, via (or contact) structures are necessary. This usually comprises a Kelvin measurement of a series of contact chains, with the current alternating between the two conducting layers. Intermediate taps may be used to calibrate the effect of increasing the number of vias.

Dielectric Breakdown

Dielectric breakdown can be achieved through voltage or current ramping. Usually applied to thin gate oxides, the test structure comprises of a capacitor that is stressed under certain bias conditions. Breakdown can be a function of time, voltage, or current and is used to monitor oxide quality. Low-voltage breakdowns signify pinholes in the oxide, with later breakdowns identified with weak spots and the final group assessing the oxide quality. This test structure is applied in a variety of ways.

As a defect monitor, an array of capacitors is necessary and a suitable algorithm is required to provide statistical validity. A modified form of the capacitor has been implemented as a wafer surface charge monitor (CHARM) applied to implant and etch processes in which a potentially damaging plasma is present. The device structure of the CHARM monitor is a floating-gate MOS EEPROM transistor with a thin oxide between the floating-gate electrode and source. The structure is further enhanced by the addition of a large charge-collecting metal plate. Analogous to this are the antenna structures, which compare edge effects and area effects

by splitting the large plate into fingers, thus altering the periphery/area ratio. This is particularly useful in monitoring gate oxide thinning at the LOCOS edge by alternating the fingers of the antenna with the gaps in the diffusion regions or at the gate edge by running the stripes over one large diffusion. Often reference devices are used, which are formed by shorting the gate and other terminals through the use of fuses, creating equipotentials that prevent charge buildup. The fuses can be blown once processing is complete. Defects in the gate oxide may not produce instant breakdown, but rather cause a thinning of the gate, thus increasing the electric field and accelerating the wearout of the oxide.

Capacitance-Voltage Structures

The metal-oxide-silicon capacitor is frequently used as a test structure in a variety of different applications. The first of these assesses oxide integrity by simple breakdown tests or by the standard reliability tests. A second application examines mobile ion drift through the oxide and is used to evaluate process cleanliness. The device is fabricated on a test wafer typically using only two or three process steps, and a voltage sweep is made and the capacitance measured. Since the doped silicon will invert at a particular sweep voltage, forming a variable capacitor in series with the oxide capacitor, a characteristic capacitance-voltage (CV) trace is observed. Heating the sample while applying a voltage a stress will relocate charged contaminant in the oxide and alter the subsequent CV profile, thus quantifying the amount of mobile ions produced during the processing. Further information on the condition of the oxide/silicon interface can be obtained using the same technique.

Since the CV profile is formed by first depleting and then inverting the underlying silicon, it is possible to perform dopant profiling using this technique. This has proved popular for three important reasons: It measures the electrically active profile, is nondestructive, and can be easily automated. The theory assumes the validity of the *depletion approximation* and is consequently limited to an accuracy of a few deBye lengths of the surface, severely limiting its application to deep submicron devices.

Variations on these techniques can be applied to the same structure, including current-voltage, *I-V*, and capacitance-time, *C-t*, tests. Reference 15 provides a comprehensive text on the subject.

YIELD STRUCTURES

Since the problem of yield prediction is statistical in nature, yield test structure design must incorporate placement, frequency, and interpretation of the data as part of the overall picture. As well as quantifying the defects, it is essential to identify the location, the size, and the step in the process at which they appeared. Consequently a prioritization becomes necessary, with a Pareto-style approach to tackle the problems in a systematic order. The transistor yield can be modeled as function of the chip area and feature size (or critical area in the chip), the chip size, and the size and number of the defects, and it takes an exponential form.

Evolutionary refinements to the first approximation of a Poisson distribution have resulted in commonly used models such those produced by Stapper and by Murphy, as shown, and subsequent variations on these.

$$\begin{aligned} &\text{Poisson} && Y = \exp(-DA) \\ &\text{Stapper} && Y = (1 + DA/\alpha)^{-\alpha} \\ &\text{Murphy} && Y = (1 - \exp(-DA))/DA \end{aligned}$$

where D is the defect density, A is the critical area, and α is a constant between 0 and 1.

Ideally the test structure should reflect the chip itself, and the most efficient way to generate the test vehicle is to deconstruct the process and build a monitor that can identify each layer. Many yield structures consist of a large meandering track (often simply referred to as a meander) of electrically continuous material and rely on detecting an open or short circuit condition caused by the presence of a killer defect. Figure 9 shows such a structure that can test for track continuity and track shorting. This serpentine or meander structure can be adapted to examine contact defects and junction leakage and maintains the philosophy of the Kelvin design. Further, the structure can be easily modified to examine step coverage and interlayer shorts.

Electron microscopy can be employed in the analysis of these yield type structures, using voltage contrast to distinguish between charged floating conductor shapes from charge-drained grounded shapes in terms of visual contrast and thus combined with a knowledge of the circuit structure highlight the location of the defect. This has the advantage that it can be used *in-line,* prior to probing capability, and provides resolution beyond that of optical structures. Further, since it checks for electrical connectivity, nonkiller defects are ignored (though the potential for the defect to *become* a killer defect is always present).

Silicon-level defects are best examined using parallel arrays of transistors, incorporating electrical commonality, and can be used to examine dielectric and junction leakage. Memory devices such as SRAMs (or DRAMs) are commonly used vehicles that can operate in this mode and identify the location of the defect to the accuracy of the size of the SRAM itself. A standard approach is to fabricate a batch of SRAM wafers at a predetermined frequency. Another approach is to locate test drop-ins at discrete points over the wafer, sacrificing silicon real estate on each product wafer and interpreting the results to provide information on the rest of the wafer. About 2 to 10 drop-ins are common, and recent results suggest that placement should be around the edge of

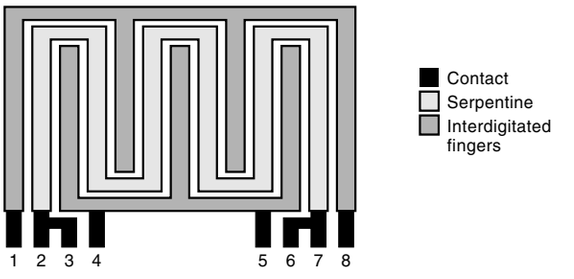

Figure 9. Current is forced between 2 and 7 and voltage measured between 3 and 4. Open circuit signifies a break in the track. Bridging or leakage between tracks can be quantified by measuring leakage current between 1 and 3, and 3 and 4 (similarly between 5 and 6, and 6 and 8).

the wafers and at the center. Test structures placed in the scribe lines offer the advantage of whole wafer mapping but suffer from area constraints. The large array typically required by yield monitors can be divided into subchips in an approach that uses fast digital testing to locate and identify defect type between conducting layers (16).

PARAMETER EXTRACTION

Perhaps the most important test structure is the transistor. Knowing the fundamental transistor characteristics and tuning them to the computer-aided design (CAD) model facilitates successful design. The designer simulates the circuit before the design is fabricated. The simulation tool uses a set of equations which describes the behavior of the devices used in the circuit. The numbers used in the model equations depend on the technology or process used to fabricate the devices (e.g., the transistor threshold voltage is a function of the processing). To supply these numbers, parameter extraction is performed, whereby measurements are made on discrete devices and process of model fitting follows. The transistor is the focus of the bulk of the work, but all discrete devices are modeled. Many different models exist, though the test structures used to extract these parameters show a greater degree of commonality (17).

Typically a range of standard transistor geometries is deployed to identify the geometry dependence of the parameters, the difference between the drawn and fabricated sizes, and the separation of edge and periphery effects. This approach assumes a validity in geometric scaling of devices. For MOS devices this usually means an array comprising the gate length and gate width (Fig. 10), and for bipolar devices the emitter length and emitter width. It is desirable to include minimum-size transistors and reduce this further by the variation seen in the fabricated dimension. Common contacts can be made for the gate and the source (or collector), and it is preferable to orient the structures in the same direction to minimize any systematic discrepancies. If nonstandard structures are used in the design, it is essential to include these in the test chip, where cell library components are often also incorporated, as are high-frequency characterization structures using unique pad connections for two-port measurements and using microwave probes and including dummy structures to de-embed parasitic inductances and capacitances. While the approach of varying transistor sizes is common, it is not unique: Another approach is to use one transistor only, to extract parameters to fit to the model, since it can be argued that the relationship of the special structures used for measurement to the transistor is open to interpretation. Though parameter extraction provides a set of values for the CAD model, the results are often single valued. To predict the circuit performance, knowledge of the statistical spread of the parameters is essential, which results in a time-consuming task of making many measurements and subsequent curve fitting. The resulting distribution of SPICE model parameters can then be employed to evaluate circuit corner models, ensuring successful circuit operation at all points in the fabrication specification range.

Device matching is critical for precision analog applications (such as A/D or D/A converters) and will be exacerbated particularly for advanced audio and video mixed signal circuits. The degree of mismatch is a function of the device layout, and so the array used for parameter extraction can be augmented for use in quantifying matching. Generally, MOSFET matching is attributed to two sources: stochastic mismatch related to random physical spatial variations and systematic mismatch related to nonrandom errors caused by such components as asymmetrically placed transistors or linearly graded parameters across mask and/or wafer. For stochastic mismatch, the general mismatch law, which states that the standard deviation of the percentage change in measured parameter is inversely proportional to the square root of the area, guides the designer toward "larger is better," though the presence of a systematic variation may work in opposition to this rule. Evaluation of matching is usually performed by placing devices close together (as they would be in actual design) or built up by common centroid cross-coupled pairs, as demonstrated by the QUAD layout, in which the matched pair is split into four unit devices, diametrically opposed such that

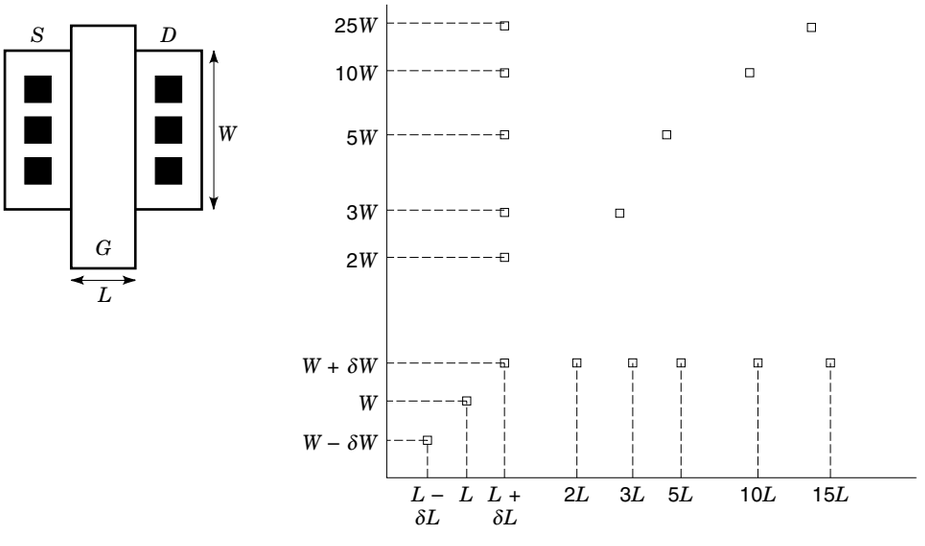

Figure 10. A typical array of transistor length and width dimensions used in the parameter extraction procedure. L and W are the nominal length and width values. Integral multiples of these values define the array of transistor. Also included are slight variations (δ) in each of L and W.

one matching transistor is actually an average of two of the four available.

SUMMARY

While the common areas of test structure design have been reported, a plethora of application-specific test structures exist. The fields of sensors and micromachining are examples of this, producing many novel structures. As technologies evolve, so too do test structures and they are therefore likely to remain an essential tool in semiconductor fabrication.

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SEMICONDUCTOR MEMORIES. See SRAM CHIPS.

SEMICONDUCTOR PHASE SHIFTERS, MICROWAVE. See MICROWAVE PHASE SHIFTERS.

SEMICONDUCTOR PROCESS CONTROL. See PROCESS CONTROL.