tions for fabrication equipment or operators, to design knowledge about a process under development or optimization. Process representation is of particular importance in the semiconductor field because of the process-intensive nature of semiconductors. That is, the key characteristics of semiconductor products are highly dependent on the specific details of the process used to manufacture them.

There are many ways to describe or document a semiconductor process, and the process flow representation can be variously thought of as a language (if it has a textual form), a data structure, or, if sufficiently powerful and comprehensive, a knowledge base. Initially, when little is known about a process, an overview with many details hidden or unstated is desirable. This allows a big picture of the process so that at least the intent of the process can be understood. A circuit or device designer will generally be concerned with the various material layers, how they are patterned (what masks to specify), what regions are implanted with dopants, and so on. Physical realization of the process requires synthesis of a process flow to achieve the designers' intent and typically involves computer simulation of key process steps. A presentation of the process similar to a programming flowchart shows the main flow of control. All of the detailed exceptions, such as what happens when something out of the ordinary occurs, are hidden. Figure 1 shows the initial sequence of steps of a hypothetical but typical process. The process starts with a silicon wafer of known characteristics, and a pad oxide is grown followed by a nitride growth or deposition. A photomask step is used to pattern a protective resist layer on the wafer so that the subsequent etch step will selectively remove the nitride on specific areas of the wafer. Actual fabrication will generally require expansion of this simplified process flow and provide details in both sequence structure (substeps) and equipment-specific processing parameters. In the typical nitridation step, for example, the wafer is first cleaned and then the nitride material is deposited, using a particular schedule of gas flows and temperatures, often called a recipe, in a particular furnace. Afterward, the thickness of the deposited nitride may be measured as a standard part of the complete nitridation step.

In a real factory, there are, of course, other details that are important, some of which are often not written down. Such implicit details may be part of the knowledge, experience, and training of the fabrication operators, the equipment specialist

SEMICONDUCTOR PROCESS REPRESENTATION

Semiconductor chip manufacturers, foundries, research laboratories, and other enterprises all use some sort of representation of the semiconductor fabrication process in order to make or design semiconductor devices and integrated circuits (IC). In their most elementary form, such representations may be textual or graphical and intended solely for human interpretation. Of much greater use, however, are highly structured or formalized representations that can be understood and manipulated by a collection of computer programs. The purpose of such a process flow representation is to capture key information for one or more purposes in the life of a fabrication process or semiconductor product, from early con- **Figure 1.** Semiconductor process representation involves multiple ceptualization through design and manufacture. Such infor- levels of detail. Shown here is a simplified sequential process flow for mation ranges from manufacturing details, including instruc- the selective creation of active areas where transistors will be formed.

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tion provides a common interface to various applications. A process representation may be created by a user through a combination of graphical user interfaces or editors operating on textual process descriptions and may draw process steps from one or more process libraries that could reside either locally or be accessed via a computer network. The process representation may be utilized or integrated with applications supporting fabrication or simulation.

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A complete software process flow representation system IC; software programs then use these data to accomplish fab-
consists of four basic elements: the information model, user intervalses.
The second key element of a proc and programmatic interfaces, a base collection or library of The second key element of a process representation system
represents and a set of annihilation programs that use or map is the mechanism or interface for capturi processes, and a set of application programs that use or man-
age the process representation, as shown in Fig. 2. These ele-
ments enable the process representation to act as a general. a process flow in a prespecified tex ments enable the process representation to act as a general- a process flow in a prespecified textual format or language,
nurmose unified means for expressing what is already known which is then read and interpreted by com purpose, unified means for expressing what is already known which is then read and interpreted by computer. Graphical about the process, or what is learned about a process in the user interfaces (GUI) are generally preferred by users who
course of design simulation or manufacturing itself. A uni-
are not programmers; the GUI helps guide a course of design, simulation, or manufacturing itself. A uni-
fied process representation is one in which the knowledge signer in the creation and modification of process steps and fied process representation is one in which the knowledge about the process is represented coherently and in a uniform the assembly of these steps into correct process flows. In addi-
fashion in order to bridge and integrate related activities tion to human interfaces, well-defin fashion in order to bridge and integrate related activities (e.g., process design and manufacture). A unified process rep-
resentation organizes the various levels of detail that are es-
tude of manufacturing or computer-aided design (CAD) resentation organizes the various levels of detail that are essential to the making of an IC and provides a comprehensive systems to use and manipulate process information. framework for knowledge about process steps. The third element of a working process representation sys-

type and format of process information that can be expressed. available processes for one or more particular fabrication

or engineer, or of the equipment developer and manufacturer. describing both process structure (e.g., linear sequences of The details may be embodied in multiple places, so that which process steps or hierarchical decompositions of complex prodetails are used depends on when and where the ICs are cesses) and the organization of process details (e.g., details made. The matrix of a water during a process as it is sub-With computer representations for the process flow at vari-
jected to specific gas flows, thermal treatments, etc.). Examous levels of detail, software programs that use process infor- ples of the information expressed by a process representation include the process structure, control structure, simulation results, desired effect on the wafer, processing models, equip- • simulation ment operation or microprograms, scheduling data, and test-• safety checks ing and yield results. Once a process representation is struc-
• instruction formatting and the structured around such a model, application programs can be • instruction formatting tured around such a model, application programs can be

• data collection

• data reduction

• data reduction

• control

• control • process analysis and diagnosis transforms them, and produces wafers as outputs. Alterna- • scheduling tively, the representation can be viewed as data that include
knowledge as to specifications, documentation, and the ma-• rule-based or intent-based process synthesis knowledge as to specifications, documentation, and the ma-
chines or other resources required to manufacture the product

The first element is an information model that specifies the tem is a collection of process libraries, which provide the In particular, the information model defines the methods for facilities (fabs). Such libraries may also include unit process steps and reusable subprocess modules that can be integrated hand, many process representations do not impose a strict by a process designer to create new complete manufacturing hierarchy and provide for arbitrary levels of process sequencprocesses. ing (e.g., each process step can be decomposed into smaller

without a supporting set of computer integrated manufactur- detail is desired). For example, while a unit process step ing (CIM) or CAD applications to enable the accomplishment might be a thermal operation in a furnace, it is often desirof actual fabrication or design goals. able to break this into smaller sequences of time blocks or

as well as user and application program interfaces and pro- the process. cess libraries, are discussed in detail. These form the generic Several process representations have also been proposed core of a process representation system. More advanced issues that deal explicitly with more sophisticated process sequencand the current state of the art regarding the integration of ing requirements. One example is timing constraints on the process representations with CAD and CIM applications, as execution of process steps. It is often critical that one process well as industry standardization efforts, are then described. step be immediately followed with zero or finite delay by the

Process Sequence

Generic Process Model Complete IC manufacturing processes are frequently thought of as being divided into smaller sequences of steps or modules In addition to process sequence information, details about in turing process as composed of sequences of process building

sented in a hierarchical or tree structure, as illustrated in process flow consists of process modules made up of unit pro- ment at various points cess steps, which each occur on a specific piece of equipment), generic process model. cess steps, which each occur on a specific piece of equipment). generic process model.
Such fixed bierarchies have been found to beln communities During a process step, a wafer (or several wafers) is conof users structure and share complex processes. On the other

process step. Each substep can be decomposed into an ordered se-

Finally, a process flow representation is of limited value process steps as needed to describe the process to whatever In the following sections, process flow information models, events where temperatures or gas flows are changed during

next step (e.g., polysilicon deposition after a gate oxidation), **INFORMATION MODEL INFORMATION MODEL** and attributes on a process step have been used to express such requirements (e.g., tagging a process to indicate that all The information model is fundamental to creating a shared

understanding of terms and definitions in a formal process

understanding of terms and definitions in a formal process

representation. At its most basic, a semic

(e.g., well formation, active area definition, metalization). dividual process steps are needed. The second key idea in a Therefore, a fundamental "chunking" abstraction capability of process representation is that specific information can be as-
process representations is the ability to describe a manufac-
sociated with process steps at vari process representations is the ability to describe a manufac-
turing process steps at various points in the process
turing process as composed of sequences of process building hierarchy; this information is usually capture blocks or components. The process step that express detailed or aggre-Because each component may itself have subcomponents gate information at the appropriate point in the process. An σ , subprocess steps), process flows are typically repre- example of a scheduling-related attribute is the (e.g., subprocess steps), process flows are typically repre- example of a scheduling-related attribute is the time required Fig. 3. This hierarchical decomposition also enables modular the time-required attributes associated with the process process development, as the same process step (e.g., clean step's subcomponents. To help organize and structure desteps, thin oxidations, resist development) is often used at tailed unit process information, a generic model for semiconseveral points in the same process flow or across multiple pro- ductor processing, as conceptually pictured in Fig. 4, has been
cess flows. In some process representations, the number of defined. The process representation cess flows. In some process representations, the number of defined. The process representation then supports the speci-
levels (and terminology at each level) is predefined (e.g., a) fication of desired states of the wafer levels (and terminology at each level) is predefined (e.g., a fication of desired states of the wafer, environment, or equip-
process flow consists of process modules made up of unit pro- ment at various points during fabr

Such fixed hierarchies have been found to help communities During a process step, a wafer (or several wafers) is con-
of users structure and share complex processes. On the other tained within some physical environment tha erated as a result of settings on a fabrication machine within a facility. These settings are, in turn, controlled or dictated by a program or recipe. The layering in Fig. 4 indicates a number of boundaries: between the wafer and the wafer environment, between the wafer environment and machine/facility, between the machine/facility and settings (as well as readings), and finally between settings/readings and control programs. This conceptual layering is loosely guided by the **Figure 3.** A hierarchical or tree decomposition for a masked implant physical containment that exists during the processing (i.e., process step Each substep can be decomposed into an ordered segment of a masked within wat quence of smaller substeps. These can affect another only through one of the boundaries

fying groups or categories of state information and interfaces between and varying scope of the problem domain, however, modern
those states as they occur during IC manufacture.

shown in Fig. 4 or through a chain of such interfaces. Each knowledge about processes for new and different purposes).
Process representation implementations may be divided affected through interaction with the surrounding or en-

This partial decoupling of entities (or the states of those indirectly (e.g., as a delta or change in state that the step is

are on the surface of the wafer that enable safety or design
rule checks) or further modeling (e.g., representations of indi-
vidual devices to sufficient detail that desired process and de-
vidual devices to sufficient de clude surface topography, bulk dopant concentrations, thin film stresses, and other geometric and parametric properties **USER AND PROGRAM INTERFACES** of the wafer. A typical desired change in wafer state is the addition or removal of a thin film of specified thickness or
properties (e.g., deposit a 0.5 μ m silicon dioxide layer). This
is also sometimes termed the *effect* that a process has (or is
desired to have) on a wafer.

subjected to during processing. This treatment can be de- **Human Interfaces** scribed as functions in position and time of temperature, partial pressures of ambient gases, and so on. These parameters Two different approaches (or a hybrid of these approaches) are typically thermodynamically intensive, a property that have been widely used to enable engineers and operators to helps to distinguish them from machine state parameters. specify process steps and flows. On one end of the spectrum

Machine/Facility. The machine state might include the current machine setup and configurations during operation, such as valve positions or the voltages across plates in plasma equipment. The machine resides within a facility that has attributes such as gases, airborne contaminants, and staff.

Settings and Readings. Settings correspond to the desired positions of knobs or other controls and may vary discretely or continuously as a function of time in response to operator or automated instructions. Examples of readings are the current shown on a meter of an ion implanter and a temperature derived from a furnace thermocouple.

Implementing the Information Model

A great deal of progress has been made in identifying a ge neric process model for unit process steps, as well as generic Figure 4. A conceptual model for semiconductor fabrication, identi-
process sequencing mechanisms. Because of the complexity process representation implementations use process modeling. and representation techniques that are extensible (that is, capable of easily being extended to accommodate new kinds of

may evolve over time due to internal interactions or as it is Process representation implementations may be divided
affected through interaction with the surrounding or en-
into three basic types: programming language base closed entities.
This nartial decoupling of entities (or the states of those based approaches, such as FABLE (developed at Stanford) entities) motivates a generic model of the semiconductor pro-
cess to enable identification and differentiation among catego-
itly represented as a program in a specialized programming cess to enable identification and differentiation among catego- itly represented as a program in a specialized programming
ries of state information, corresponding to the partitioning language to be executed. In knowledgeries of state information corresponding to the partitioning language to be executed. In knowledge-based approaches, the
shown in Fig. 4. In general a state description may be speci-
process representation is treated as a g shown in Fig. 4. In general, a state description may be speci-
fied directly (e.g., to indicate the desired or resulting state) or resentation problem: the Stanford MKS and PDS systems are fied directly (e.g., to indicate the desired or resulting state) or resentation problem; the Stanford MKS and PDS systems are
indirectly (e.g., as a delta or change in state that the step is examples of this approach. The intended to accomplish). combine the benefits of the other two. The MIT PFR is an example of the hybrid type; a textual form can be used to **Wafer State.** Of key interest is the state of the wafer at the specify processes (or the same textual form can be used as an explanation of the process as well as at intermediate points in interchange format to exchange p completion of the process as well as at intermediate points in interchange format to exchange process information between
the process flow While potentially infinite in complexity and different systems). A sample of this f the process flow. While potentially infinite in complexity and different systems). A sample of this flow representation is
detail, the process representation typically captures only shown in Fig. 5. Other systems have als further processing (e.g., states that indicate what materials adopts a language-based front end with an object-based back
are on the surface of the water that enable safety or design end or application programming interfac

Wafer Environment or Treatment. The wafer environment faces to the process flow, followed by issues in computer-ac-
captures the relevant physical environment that the wafer is

SEMICONDUCTOR PROCESS REPRESENTATION 143

(define cmos-baseline (flow (:documentation "CMOS Baseline Process") (:body initial-epi well-formation active-area-definition field-formation channel-formation source-drain-definition bpsg-passivation contact-definition metal-definition)))) (define well-formation (flow (:body n-well-formation p-well-formation))) (define n-well-formation (flow (:body stress-relief-oxide lpcvd-silicon-nitride n-well-pattern nitride-plasma-etch n-well-ion-implant resist-ash))) (define p-well-formation (flow (:body n-well-cover-oxide nitride-wet-etch (define n-well-cover-oxide p-well-ion-implant (flow well-drive (:documentation well-oxide-wet-etch))) "Grows a thick cover oxide using a thermal treatment") (:permissible-delay :minimal) (define active-area-definition rca-clean (flow (operation (:body stress-relief-oxide (:body lpcvd-silicon-nitride (:change-wafer-state active-area-pattern (:oxidation :thickness (:angstroms (:mean 5100 :range 250)))) nitride-plasma-etch (:treatment p-field-pattern (thermal-r. (thermal-rampup-treatment :final-temperature 950) p-field-ion-implant (thermal-dryox-treatment :temperature 950 :time (:minutes 30)) resist-ash))) (thermal-wetox-treatment :temperature 950 :time (:minutes 175)) (thermal-dryox-treatment :temperature 950 :time (:minutes 30)) (define field-formation (thermal-rampdown-treatment :start-temperature 950)) (flow (:machine Thick-Oxidation-Tube) (:body n-field-pattern (:settings :recipe 240))))) n-field-ion-implant resist-ash field-oxide (define (thermal-rampup-treatment final-temperature) nitride-wet-etch))) (sequence (:thermal :temperature 800 (define channel-formation :time (:minutes 20) :ambient :N2) (flow (:thermal :temperature 800 (:body stress-relief-oxide-wet-etch :time (:minutes 10) :ambient :N2) dummy-gate-oxide (:thermal :temperature 800 :ambient :N2
n-channel-definition (:minutes (/ (- final-te time (:minutes (/ (- final-temperature 800) 10.0)) p-channel-definition :temp-rate 10) dummy-gate-wet-etch (:thermal :temperature final-temperature gate))) :time (:minutes 10) :ambient :N2)))

> **Figure 5.** Sample process flow representation. Here a textual programming language format is used to capture key information about a process flow.

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engineers editing text files that express process steps as Architecture (CORBA) also enable remote network access to somewhat like subroutines or procedures, with the ability to such information from multiple applications implemented in identify variables and parameters in those steps to enable widely different programming languages. At present, examgeneralization or reuse of those steps in different process ples of such interfaces have been demonstrated, and the semiflows. From the very earliest work on programming languages conductor industry is working to define standard interface for semiconductor process representation (e.g., the Stanford definition language (IDL) specifications so that independently FABLE system), the need to represent multiple abstraction developed utilities and systems can interoperate. levels or views for process information was recognized, leading to language descriptions that are somewhat different from **PROCESS LIBRARIES** those in conventional programming languages (e.g., through

The definition of standard program interfaces is of critical The full power of a process representation is only realized concern for the development and integration of the many ap-
when a collection of computer programs or concern for the development and integration of the many ap-
plication of computer programs or applications is
plication programs that need access to process information. available to accomplish the wide range of tasks that plication programs that need access to process information. available to accomplish the wide range of tasks that need pro-
At this stage, most contemporary process representations cess information. For example, various pro At this stage, most contemporary process representations cess information. For example, various programs may pro-
adopt an object-based approach. Each process component typ-
duce reports or subsets of information from a fu ically has multiple views that contain attributes (or name- pository or process flow for different purposes or targeted to value pairs) that can be accessed and manipulated. Clearly, specific types of users, such as process designers, managers, one set of these attributes must capture the process sequence schedulers, equipment suppliers, control engineers, and othor hierarchy. Other views typically align with the generic pro- ers connected to a fabrication process. Among the most comcess model or with other sets of attributes needed to accom- mon of these report generators are programs that create a plish specific tasks. Conventional object and object attribute paper or electronic traveler or run sheet that provides sumcreation, access, and mutation methods are typically pro- marized process sequence, equipment to run on, key process

Historically, many such programming interfaces have been cific wafers or lots that travel through the fab. language and implementation specific. Generic object models When ICs are fabricated, the run sheet or traveler follows and standard interface description languages, however, en- along with each batch or wafer lot and contains the sequence able the specification of language-neutral interfaces to com- of processing steps need to produce the IC. In a computerized mon data stores. Indeed, approaches such as the Object Man- manufacturing system, the traveler may be a computer record

lies the programming language analogy and approach, with agement Group (OMG) Common Object Request Broker

the definition of different code branches or blocks that are
 \pm t can be argued that process knowledge capture alone is sufficient of a property
and the preservation of a three extreme of the spectrum lies the fieled at

APPLICATION PROGRAMS Program Interfaces

duce reports or subsets of information from a full process revided. **parameter information**, and room for measurements for spe-

The run sheet is typically augmented with some of the key processing. details that are unique to the machines being used or to the As part of the process execution, modern CIM systems will product being manufactured. These augmentations may in- often download detailed operating specifications or programs clude, for example, the recipe number to be used for a particu- on fabrication equipment. While a few research systems have lar machine, summaries of expected results (e.g., the thick- integrated generic process step specification with individual ness of an oxide to be grown), and measurements to be taken. equipment program download, at present most CIM systems Data concerning the processing and the resulting wafer state and process representations act more as a holding place for are usually collected throughout the actual processing. At these detailed recipes (e.g., by uploading a recipe developed times these data are recorded on the run sheet itself, while in directly on the tool). The more complete integration of deother cases the measurements are recorded in computer files tailed equipment recipe process representations remains a or records, and the filename or data path is noted on the trav- goal for the future. eler. In a more sophisticated implementation, the electronic In addition to process execution, the CIM system must run sheet is itself an interactive computer application, both gather measurement information for use in future decision providing processing instructions from the process flow and making, debugging of the process, as well as quality manage-

cess information well before a factory is constructed. Process flow information is also needed in factory design and planning **APPLICATION: SIMULATION** (e.g., capacity planning to define equipment set requirements

of the product mix desired as well as detailed process knowledge. Interactions between sequential machine operations can **Operational Modeling** be simulated or otherwise determined from the process, and
material transport systems can be designed and tested based
on process flow knowledge.
to f an existing or contemplated IC fab, descriptions of
the process are req

plex endeavor, and the representation of the process plays a More detailed information may also be useful, including time critical role in the CIM system that accomplishes this task. dependencies based on batching, setup, or other handling, Indeed, some CIM systems, such as the Computer-Aided Fab- and other resources required, including operators, handling rication Environment (CAFE) system developed at MIT, have equipment or tooling, and materials or consumables. Because been constructed with the process representation as the key a substantial volume of such process information may be reorganizing or integrating mechanism. In other modern CIM quired for operational modeling and facility management desystems (e.g., those provided by Consilium, Promis, Texas In- cision making, it is highly desirable that information be repstruments, and Fastech), a process representation interacts resented in a form that discrete event or operational with the CIM system in three key areas: flow and resource simulation and modeling tools can use so that reentry of this scheduling, recipe execution, and data collection and analysis. information can be avoided.

The CIM system must manage the flow of material and information in the facility. In addition to details about the **Process Modeling** physical process (as described in the generic process model), the process representation must also indicate those resources To model the physical processes at work in semiconductor fabthat are needed to accomplish each process step. Typically, rication, a great deal of detailed unit process information is these resources are specific equipment (or classes of equip- typically required. Physical process simulators generally opment) that are to be used in the step, as well as mask, tooling, erate from the treatment view of a process step (that is, the or materials required at that step. Other resources may also description of the physical environment of the wafer during be indicated; the time required to complete the step is of clear processing). However, a complete physical description of the

process representation. Systems, equipment, and operators to execute the specified

accepting data input from operators or equipment. ment and continual improvement. Again, the process representation plays a central role; the process representation will **APPLICATION: FACTORY DESIGN** by pically indicate precisely what metrology is required and link that information with the corresponding process step and In modern fabs, CIM systems fundamentally depend on pro-
cess information (among a great deal of other information).
Less well known, but important to note, is the need for pro-

to meet production goals for various mixes of products and
processes).
Answering the simple question of which machine types will
be needed in a new facility requires knowledge of the process.
Determination of the capacity

subset of a complete process description and typically in-**APPLICATION: COMPUTER INTEGRATED MANUFACTURING** cludes at a minimum the sequence or flow of process steps, with clear identification of the specific equipment (or classes The management of a modern IC fab is an enormously com- of equipment) needed for each step, and the time required.

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a multitude of alternative and unique representations of the (and record that environment in the appropriate view of a process. Each simulation tool has typically defined its own file process step). Another simulator might be able to summarize format or user interface for expression of those details of the the effect of the treatment as a change in wafer state. In the process that it needs. An early approach that sought to bridge reverse direction, synthesis tools or utilities could also generthose gaps was proposed by MacDonald et al., where simula- ate more detailed descriptions from abstract specifications.
tor statements were inserted into comments fields in the pro- For example, for a desired treatment, a tor statements were inserted into comments fields in the pro-
cost routes descriptions in a preexisting CIM system en-
could generate the detailed recipe or settings needed to create cess routes descriptions in a preexisting CIM system, en-
abling in-fab process engineers to perform simulations to a desired environment around a fabrication tool, given the abling in-fab process engineers to perform simulations to a desired environment around a fabrication tool, given the
assist in process diagnosis and improvement. In this ap-
constraints of existing equipment in a particula assist in process diagnosis and improvement. In this ap- constraints of existing equipment in a particular facility. The proach, the process sequence or flow is shared between fabri- representation and capture of the full spectrum of process in-
cation and simulation but process details must be entered in formation between both fabrication a both step recipes and simulation statements (that is, no other improved process development in other ways as well. Direct
narameter coupling between the manufacturing and CAD in-
comparison of simulation with historical me parameter coupling between the manufacturing and CAD in-
formation was achieved: only the correspondence of steps was haps including measurements or characterization data spanformation was achieved; only the correspondence of steps was haps including measurements or characterization data span-
achieved). Another approach was reported by Durbeck et all ining original process development as well achieved). Another approach was reported by Durbeck et al. ning original process development as well as manufacturing)
in which an on-line specification management system primar- can accelerate yield learning and diagnosis ily targeted at managing process libraries with engineering tal systems have achieved substantial integration (e.g., the check off and subsequent generation of run sheets was ex. CAFE CIM system developed at MIT), support check off and subsequent generation of run sheets was ex-
tended to generate parameterized simulator input decks. In grated capability is not yet present in commercial systems. tended to generate parameterized simulator input decks. In this case, process details are entered only once into the system; and these values automatically propagate to the views or descriptions needed for simulation. The approach remains **STANDARDIZATION** limited, however, in that it is only possible to emit or generate

timestep information. One approach is to encode such inforlator would examine wafer state and process specification in- ment of formation and generate simulator information with annoual systems. formation and generate simulator information with appropriate gridding or model information (perhaps by consultation of additional simulator-specific library information). In either case, it is recognized that implementations must deal with **BIBLIOGRAPHY** existing simulators that are not ideal but rather require more than simple wafer state or treatment information. D. Akkus, *Process Advisors: Process Synthesis for Arbitrary Initial*

content shared between both fabrication and design require-
Massachusetts Inst. Technol., Cambridge, MA, 1991. ments provides additional benefits and opportunities. A data D. S. Boning et al., A general semiconductor process modeling framerepresentation with well-defined levels of abstraction enables work, *IEEE Trans. Semicond. Manuf.,* **5**: 266–280, 1992. multiple types of simulators and other CAD tools beyond D. Durbeck, J.-H. Chern, and D. S. Boning, A system for semiconduc-

environment adequate to predict process results may not be those that simply produce wafer descriptions for later device available. Moreover, even if such a description is available simulation. Indeed, a picture emerges of the process represenin principle, it may be outside the modeling capability of a tation as a dynamic representation where new knowledge particular simulator. Hence, more limited or ad hoc models, about the process is stored as it is created by CAD tools or requiring significant empirical calibration, are often used in experiments. For example, equipment simulation may be able simulation. to take detailed equipment state or recipe information and The central historical difficulty has been the existence of predict what treatment or environment the wafer will see cation and simulation, but process details must be entered in formation between both fabrication and simulation enables
hoth step recipes and simulation statements (that is no other improved process development in other wa in which an on-line specification management system primar-
ily targeted at managing process libraries with engineering tal systems have achieved substantial integration (e.g., the

files for use in conventional process simulators.
Several process representations have been focused on sup-
standards for process representation, but none have yet Several process representations have been focused on sup-
standards for process representations have been focused on sup-
achieved widespread acceptance. The most promising ap-
 $\frac{1}{2}$ porting process simulation environments. In these cases, a achieved widespread acceptance. The most promising ap-
key goal is often to capture process sequence and key process proach to standardization at present seems to key goal is often to capture process sequence and key process proach to standardization at present seems to be through the
narameter details needed for more than one process simula. definition of application programming in parameter details needed for more than one process simula-
tor. A difficult issue has always been the handling of simula- fying how other programs (CIM systems, CAD tools, etc.) mafor. A difficult issue has always been the handling of simula-
for-specific details, such as model coefficients and gridding or published process information. In particular, the OMG CORBA tor-specific details, such as model coefficients and gridding or nipulate process information. In particular, the OMG CORBA
timesten information. One approach is to encode such infor-specification enables platform and prog mation directly into the process flow representation. For ex-
ample Wenstrand enabled multiple simulator views to be de-
ten in various languages and run on computers with different ample, Wenstrand enabled multiple simulator views to be de-
scribed in each process object, with key process parameters operating systems. This is the approach taken, for example, scribed in each process object, with key process parameters operating systems. This is the approach taken, for example,
linked between these steps. An alternative approach is to sug-
by the SEMATECH CIM framework. In addit linked between these steps. An alternative approach is to sug-
gest that such simulator-specific information is best sepa. communication and recipe management standards for upload gest that such simulator-specific information is best sepa- communication and recipe management standards for upload
rated from the intrinsic process information and instead and download of process details are under develo rated from the intrinsic process information and instead and download of process details are under development.
should be treated by intelligent compilation or interpretation. These promise to move the industry toward stan should be treated by intelligent compilation or interpretation These promise to move the industry toward standard process
approaches That is an interpreter for some particular simu. flow representations and enable the deve approaches. That is, an interpreter for some particular simu-
later would examine wafer state and process specification in-
ment of a new generation of intercoperable CIM and CAD

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