PHOTOLITHOGRAPHY

The meteoric rise of semiconductor integrated circuit functionality has drastically changed human lifestyles and elevated living standards around the world. The key process in the manufacturing of semiconductor circuits is optical lithography. As such, improvements in optical lithography have been the driving force behind the extraordinary advances in integrated circuit performance for 30 years (1) (Fig. 1). The number of elements in a circuit has been doubling every eighteen months (Moore's law), and computational power has been increasing even faster (1). Semiconductor industry product roadmaps show this trend continuing (2), or even accelerating in the near future. However, many pundits are predicting that optical lithography improvements are coming to an end. Optical lithography appears to be reaching hard physical limits (3). How much farther will this technology extend semiconductor patterning? This article lays the groundwork for answering this question by explaining terms and concepts in the optical lithography process; the possibilities and challenges for extension; and the possible successor technologies.

Optical lithography plays the major role in the patterning of semiconductor devices. The patterning of materials in multiple layers builds the transistor devices and interconnections that make up integrated circuits (4). The material patterning step is made up of four separate but critically related processes: design, reticle, optical lithography, and etch/implant. In the design process, the desired patterns are created in a computer database. The database specifies the size, shape, and position of all features on each layer of the pattern. Design rules for each product generation determine size and placement limits on features in the design to ensure printability (5). The minimum feature size patterned determines the generation label. Currently, the 0.25 μm generation is in full production with the 0.18 μm generation just beginning initial production.

The database patterns are transferred to an optical mask, or reticle, during the reticle process. The patterned reticle contains clear and opaque regions, corresponding to the design pattern. The optical lithography process uses light to transfer the reticle pattern to a photosensitive polymer layer, the 'photoresist, on a semiconductor wafer that contains material layers to be patterned (Fig. 2) (6,7). Optical lithography transfers the reticle pattern sequentially to the fields on the wafer. Each field contains one or more die, where each die will become an integrated circuit, or chip, when fully manufactured (Fig. 3). The wafer is then used in either the etch or implant process. The etch process uses the polymer as a mask to pattern underlying material layers (Fig. 4). The patterned layers of materials are used to build transistor and interconnect features. The implant process uses the patterned photoresist as a mask to control the positioning of dopant ions implanted into the wafer substrate (Fig. 5). This positioning of the dopants strongly impacts the final device and circuit characteristics.

The optical lithography process is repeated for each field of each layer on each wafer for advanced semiconductor manufacturing. The number of patterning layers per wafer is typically 10 to 20. The number of wafers patterned in a single high-volume fabrication plant, or fab, can be many thousands per week. Each correctly manufactured die contains a precise and valuable semiconductor circuit. Therefore, the challenges of optical lithography are to define patterns quickly and accurately across a field with precise layer-to-layer placement, or overlay, and low defectivity. How well the optical lithography process meets these challenges greatly impacts the production of an integrated circuit (IC) product and its performance.

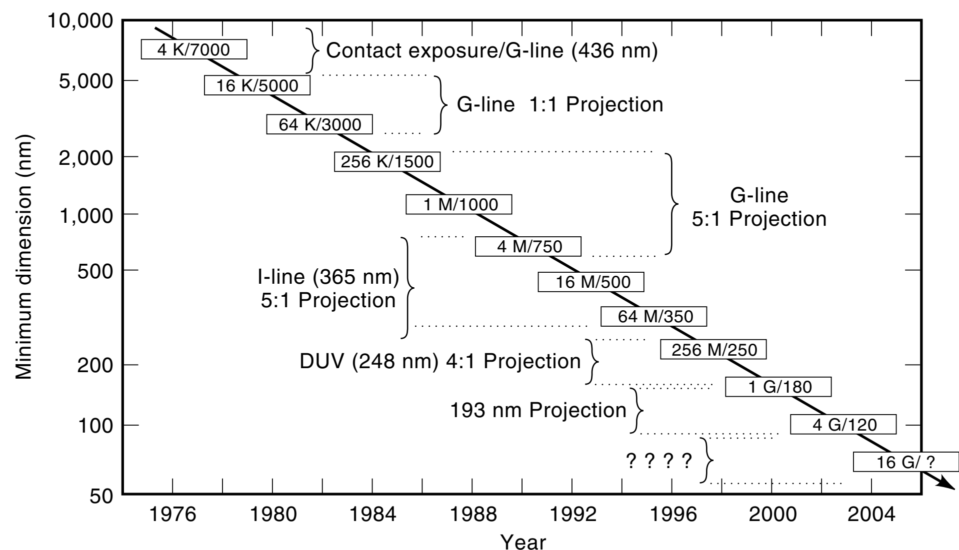

Figure 1. Year of introduction for DRAM technologies showing device memory capacity and minimum feature size. Also shown are the lithographic technologies used to manufacture each generation.

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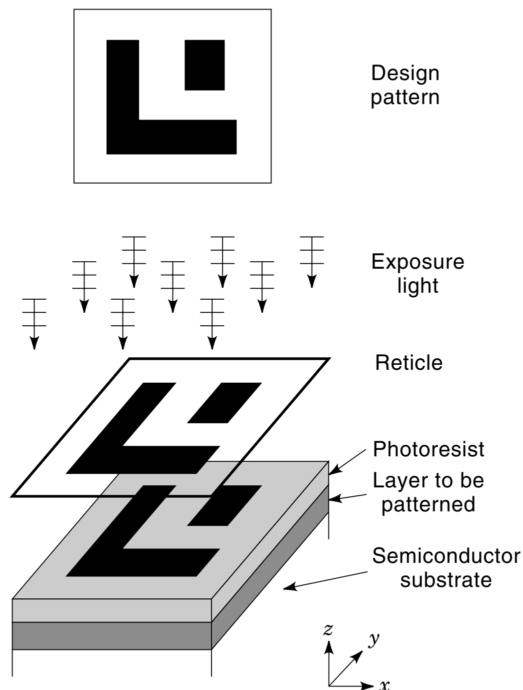


Figure 2. Idealized schematic of optical lithography exposure process. The pattern on the reticle is optically transferred to a photosensitive polymer film, or photoresist.

Specifically, optical lithography performance directly affects device properties such as current drive, current leakage, gate delay, size, and interconnection resistance (8); circuit properties such as area, power dissipation, defectivity, speed and variability of device, and interconnect behavior across the die

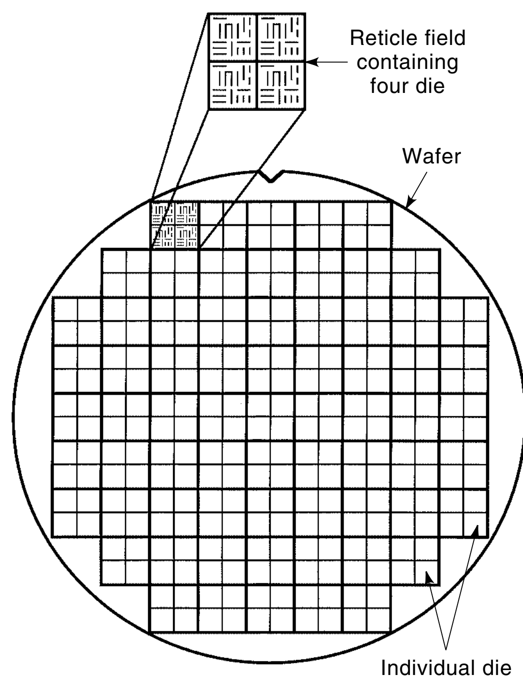


Figure 3. Semiconductor wafer being patterned lithographically by a multiple die reticle. The notch at top provides orientation to the manufacturing equipment during processing.

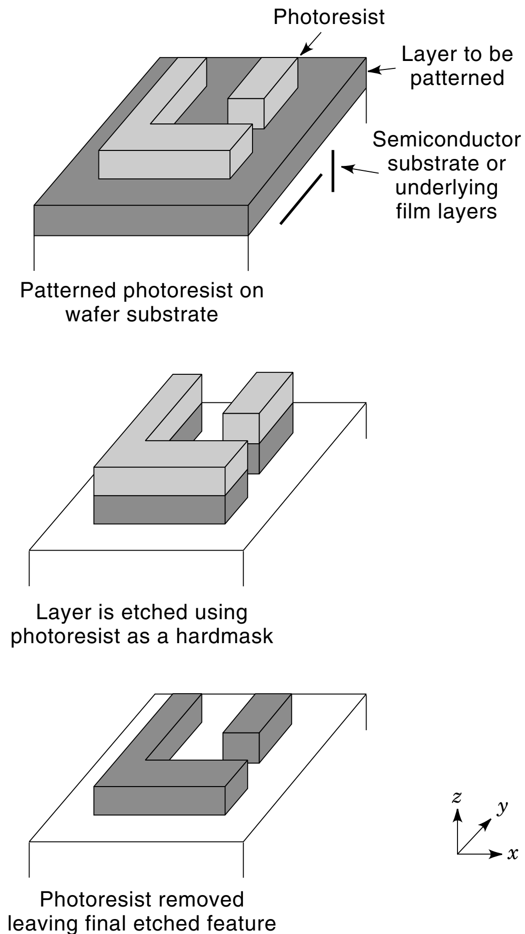


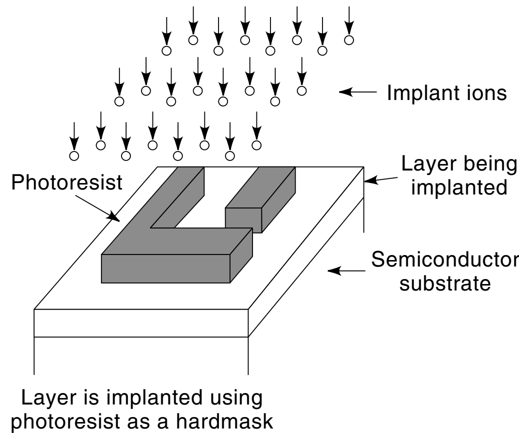
Figure 4. Idealized schematic showing the role of photoresist in the etch process.

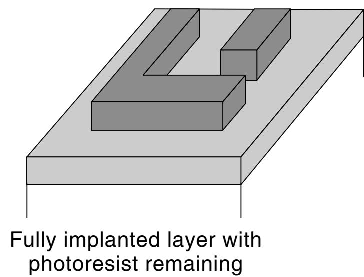
(9); and production properties such as wafers processed per hour, or throughput, process complexity, process development time, die cost, yield, material costs, tool costs, and overall factory cost (10). The success of an IC device, both technical and financial, is strongly determined by the capability of the optical lithography process.

OVERVIEW OF OPTICAL LITHOGRAPHY

The optical lithography process can be defined as the method by light which tools, materials, photoresists, and environment are combined to create patterned photoresist wafers. The optical lithography process is composed of multiple complex subprocesses. These can be classified as wafer substrate preparation, alignment, exposure, development, and metrology. Each subprocess has unique tools, materials, and process steps. The subprocesses are tailored to comprehend design, reticle, optical lithography, and etch/implant process interactions to produce optimum final (etched or implanted) patterning results. In this section, we will assume that the design and reticle processes are completed and introduce the lithography subprocesses in greater detail.

In substrate preparation, the wafer surface is prepared for photoresist, or resist, application. The substrate is defined as the stack of layers, including the semiconductor wafer itself,





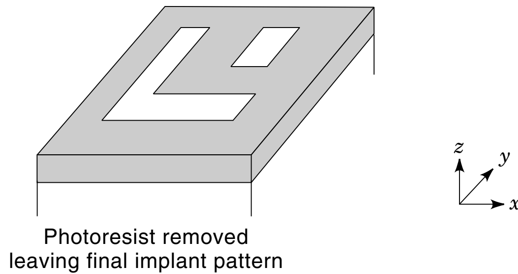


Figure 5. Idealized schematic showing the role of photoresist in the implant process.

on which the resist is applied. The etch or implant process will use the resist to pattern the top layer(s) of material. The wafer is first carefully cleaned to remove any potential contaminants. The wafer surface is then treated with an adhesion promoter before a liquid coating of resist is applied (11). The newly coated wafer is heated, or baked, to remove solvents in the resist and create a physically stable polymer film (11). This is known as the prebake, postapply bake, or softbake step. These operations are performed on a coat and develop tool, a coater track or track. After the substrate is prepared, the wafer is then transferred to an exposure tool, a step and repeat tool or stepper, which is essentially an imaging camera (3). The stepper contains the reticle, an exposure source, imaging optics, and an alignment system. In alignment, the reticle pattern is aligned to the pattern of a previously patterned layer at each wafer exposure field (Fig. 6). Dedicated features on the reticle and on a previously patterned layer are used by the alignment system to ensure accurate positioning before the image transfer occurs.

After alignment, the stepper is used to expose each field on the wafer to transfer the reticle pattern to the resist. During exposure, light from the illumination source is shaped and

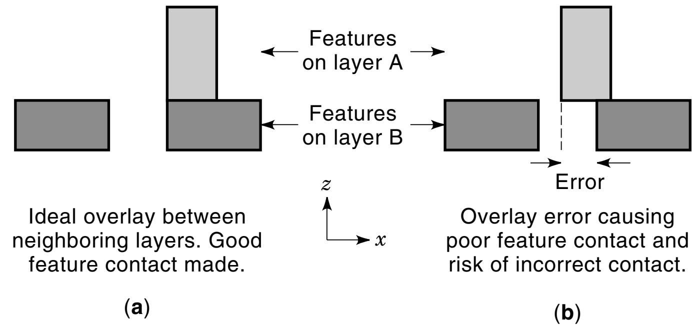


Figure 6. Cross-section view of ideal and nonideal alignment between features on adjacent layers of a device.

directed onto the reticle by the illuminator optics, or condenser. The light transferred through the reticle is focused onto the wafer by the projection optics (12) (Fig. 7). The wafer stage on the stepper moves the wafer into the correct alignment position for each field exposure. Shutters, or blades, restrict the exposure light to the correct wafer field. Sensors on the stepper ensure that the desired exposure energy and optimum wafer focus position are achieved. The clear and opaque patterns on the reticle create exposed and unexposed regions of photoresist. The photochemistry of the resist cre-

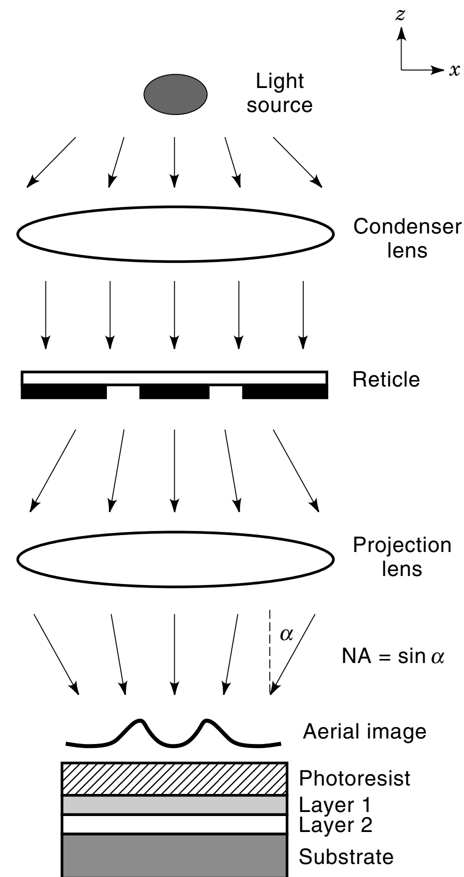


Figure 7. Idealized schematic of a stepper exposing a photoresist coated film stack. The condenser and projection optics are each approximated by a single lens. The projection lens numerical aperture is the sin of the largest angle imaged by the lens onto the wafer.

ates large solubility differences to an aqueous developing solution between these exposed and unexposed regions (6,13).

After exposure, the wafer is transferred back to the track to be baked again, the postexposure bake (6,11,13,14). The postbake reduces the undesirable effects of thin film interference during exposure. In chemically amplified resists the postbake also acts to complete the chemical reactions initiated by exposure. The resist is then introduced to a developing solution, or developer (6,11,13). During development, the highly soluble resist areas are selectively dissolved away to produce the final resist pattern. The wafer is then rinsed in water to remove the developer solution completely. The resist pattern may be subjected to ultraviolet (UV) light and/or an additional bake, the UV bake or hard bake, to increase the resistance to the etchant used during the etch process or to high-energy incident ions in the implant process (15).

After the resist pattern is formed on the wafer, the wafer may be inspected and measured to ensure correct processing (16). In the interest of throughput, only a small sample of the wafers and die on these wafers are typically investigated. If a problem is identified, the resist pattern on the wafer can be removed and re-created, or reworked. Once the inspection and metrology tests have been passed, the wafer is deemed correctly patterned with resist and allowed to continue on to the next process, either etch or implant. Additional inspections and metrology are done after the etch to ensure that the final pattern was formed correctly. If correct, the patterning step is completed.

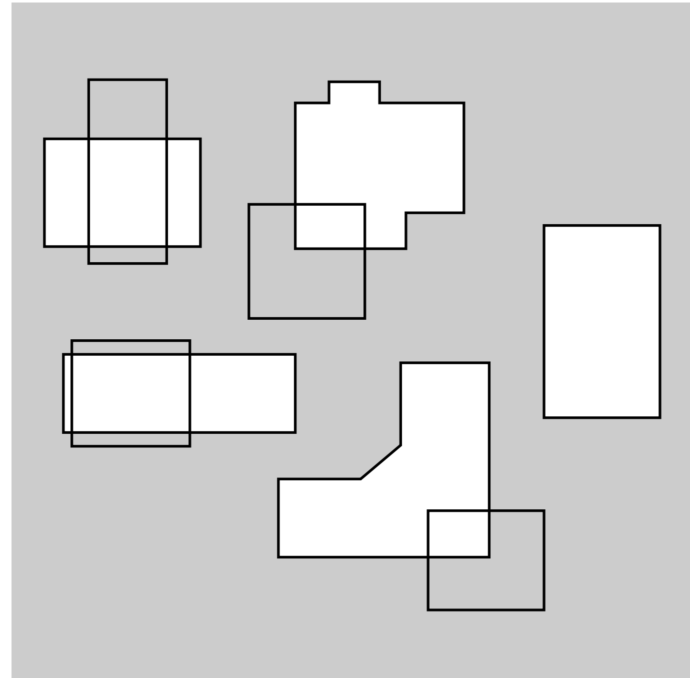


Figure 8. Example of a layout design showing descriptions of features on two layers (solid and transparent features) and the design grid of allowed feature vertices.

PATTERNING ISSUES

Many optical lithography issues impact whether a layer will be deemed to be correctly patterned. These include the designed feature size and shape; the accuracy of the reticle pattern; the optical performance of the stepper; the alignment between patterning layers; the capability of the photoresist; the interactions between the resist and the etch or implant process; the control of the films on the wafer substrate; the ability of metrology to measure and inspect the pattern; and the addition of pattern-altering particles to the wafer at any step in the process. We define the patterning of a die to be correct if dimensions of every feature are within specified tolerances of the designed dimension and also the overlay of every feature to features on the underlying layer(s) is within specified tolerances. These specifications, the sizing and overlay budgets, are given by the ability of the circuit functionality to tolerate patterning deviations. Process latitude measures the ability of the patterning process to tolerate manufacturing deviations and produce size and overlay outputs within the allowed specifications. This section will further explain the important factors of correct optical lithography patterning. It will also describe simulation methods for predicting patterning performance and optical lithography factors critical to financial success in semiconductor manufacturing.

Design

An integrated circuit design contains, in a computer database, the description of the desired pattern features that will make up the circuit. The design describes the ideal size, shape, and relative position of all features on all patterning layers (5,7,17) (Fig. 8). The features are described by the placement of their vertices on a uniform grid of allowed vertex locations. The size of the grid and the design rules determine what features and feature locations are allowed on each layer (17,18). Design rules incorporate knowledge of processing and device capability so that circuits produced using these rules are manufacturable and will function properly (19). For optical lithography, the design rules specify minimum and maximum feature dimensions on each layer; minimum and maximum spacings between features on each layer; and required overlaps or spacings between features on neighboring layers. New design rules are created for each device technology. However, to maximize reuse in the design stage, successive generations of a device technology family will scale down, or shrink, versions of the original design rules with only minor modifications (17).

There are two main classes of designs, logic (Fig. 9) and memory (5) (Fig. 10), although actual circuits generally contain both types. These classes have distinct design characteristics and patterning requirements. Logic, or random logic, designs contain a large number of hand-designed groups of features. Logic designs typically contain a wide array of feature types, such as long lines, short bars, and small squares. They also contain a large variety of local environments for features: dense arrays of features, isolated features, and seemingly randomly placed neighboring features. Memory designs contain one main feature set, or memory cell or bit cell, which is repeated across the design. Therefore, the designed feature types and local environment are extremely limited in comparison to a logic design. These limitations allow the features in the memory cell to be highly optimized for patternability, yield, area consumed, and circuit performance (20). Thus, for a given patterning or manufacturing capabil-

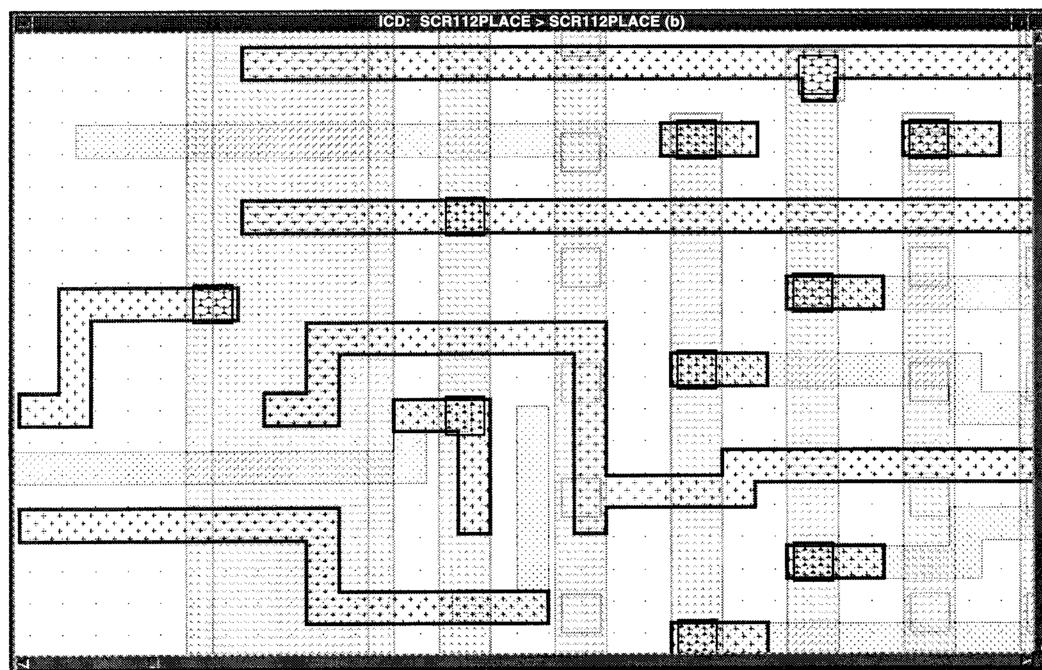


Figure 9. Example portion of a random logic design layout showing multiple patterning layers. Note the wide range of feature geometries.

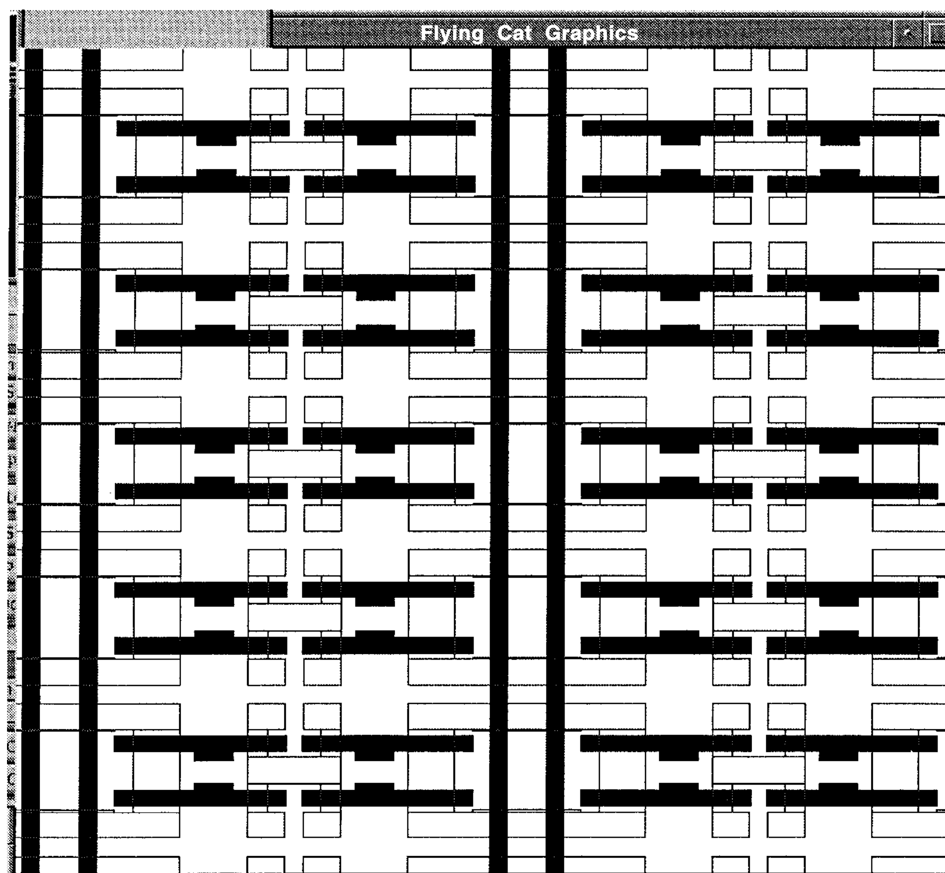


Figure 10. Example portion of a memory design layout showing two patterning layers. The layout of the single memory cell is highly repetitive.

ity, design rules for a memory design may be more aggressive than for a logic design.

Regardless of the design type, the design is stored in computer memory in a format optimized for the design process. Often this format is GDSII (also called GDS, Calma format, or Stream format) (21). Before a design can be transferred onto a reticle, it must be translated into a format for controlling the reticle patterning tool. Typically this is the Mebes format (22). The process of translating the design into the reticle patterning format is called fracture. Fracture also includes any scaling of the design (sizing of the features and the grid together), resizing of particular design features (sizing of the features only), addition of alignment features, and any calibration structures (23). The calibration structures are used by the metrology to determine the deviation from the ideal alignment and sizing of the features on each patterned wafer layer (16). Once fracture is performed, the design data are ready to be used in reticle manufacturing.

Reticle Patterning

A reticle is an optical mask containing the design features (24). It is used to pattern light in the optical lithography exposure of a wafer field. A reticle is composed of clear and opaque (typically chrome) regions on a glass substrate. In addition to the design pattern, the reticle contains alignment features, or marks, for the stepper to align the reticle to the wafer (16). The size of the reticle is typically 5 or 6 in. square (24). The reticle is patterned with the design at a reticle manufacturing factory, or mask shop. In this patterning, chrome is selectively removed to define the pattern by a reticle lithography process. Reticles generally fall into two categories: bright field (where chrome features exist in a mainly clear background), and dark field (where clear features exist in a mainly chrome background) (16).

Reticles are also patterned with a resist exposure and substrate (chrome) etch process. However, the pattern to be transferred is contained only in the fractured design data. The reticle exposure is typically performed by a scanning electron beam (E-beam) or optical laser tool, where the photoresist can be optimized for the exposure tool type. A round exposure spot approximates the fractured design grid size. In a typical reticle exposure process, each design grid point that is designed to be clear on the reticle is exposed by a beam spot. The reticle exposure tools may have one or many scanning beams, but the reticle grid points are exposed individually. Therefore, the exposure time of a reticle ($\sim$1 h to 10 h) is much slower than the relatively instantaneous ($<$1 sec) exposure of a wafer field. Additionally, on many reticle writing tools the exposure time is linearly dependent upon the number of grid points in the design to be exposed. Thus, fine reticle write grids and complicated patterns are often more expensive to pattern.

Reticles are typically patterned at a larger size than the desired wafer pattern size (3) (Fig. 7). Common reticle magnification factors are 1×, 2×, 2.5×, 4×, 5×, and 10×. The reticle pattern is reduced by the magnification factor when imaged onto the wafer. For advanced devices, accurately writing the features and placing them in correct relationship to each other is extremely difficult at 1× reticle magnification. Errors in feature dimension or placement on the reticle will affect the wafer pattern, but these errors are also reduced by the magnification factor. A large magnification factor makes the reticle features easier to manufacture but the design then takes up more area on the reticle. However, control of the feature sizes, the critical dimensions (CD), is still critical. Reticle CD errors often use much of the overall wafer CD budget. Global CD sizing errors, all CDs deviating from their target size by the same percentage, can generally be compensated for by the wafer exposure dose and are of secondary importance (25).

Random reticle CD errors can be classified as width, length, or corner-rounding errors (24,26). Corner rounding is the common inability of the reticle write process to reproduce the sharp edges of features in the design. Severe corner rounding causes line shortening, a length error, typically on narrow rectangular features. Reticle CD errors can be caused by variations in exposure energy, neighboring feature environment (proximity), feature size, reticle substrate, reticle resist variations, and chrome etch (24,26,27). Defects, typically extra or missing chrome, can also cause CD errors, depending upon size and placement.

To ensure usability in wafer patterning, the reticle is inspected for particles and to verify pattern correctness. The pattern verification is done either with die-to-die (for multidie reticles) or die-to-database inspection (24). If a defect is found, and the majority of reticles contain these initially, an attempt will be made to repair the defect (24). Missing chrome spots can be filled in with vapor-deposited metal. Unwanted chrome pieces can be evaporated with a laser or a focused ion beam. The accuracy of the repair procedures is limited and may not be successful in all cases. The correct placement of features on the reticle is also critical. Most systematic placement errors, e.g., all features offset by the same amount, can be corrected for in the stepper during wafer exposure. However, random reticle feature placement errors are a considerable problem for overlay control (24). Larger field sizes increase the difficulty of placement control.

Measurement of registration and CD errors is another important reticle manufacturing step (24,28). Due to throughput restrictions, only a minute fraction of the features on each reticle can be measured accurately. Reticle CD measurements are typically made with an optical microscope using visible light. Once the inspection and metrology determine that the reticle was correctly patterned, a pellicle is applied (24). The pellicle is a transparent film cover that keeps particles away from the reticle surface and out of the focal plane of the light image during wafer exposure. Therefore, the effect of particles which land on the reticle is greatly reduced. After the pellicle has been correctly installed, the reticle is sent to the stepper in the wafer fab.

Optical Performance

A wafer stepper is a tool for illuminating a reticle with light to transfer optically the reticle pattern to the resist on the wafer substrate (3) (Fig. 7). During exposure, diffraction limitations of the stepper optics transform the binary reticle pattern into a smoothly varying light intensity pattern, or aerial image. It is the interaction of the aerial image with the resist chemistry that allows the creation of resist patterns (Fig. 11). The goal of the stepper is to optimize the contrast and positioning of this light image on the wafer. To image and align these exposures correctly, the stepper requires many different

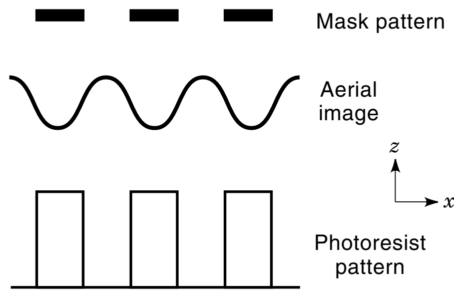


Figure 11. Cross-section view showing a common relationship between the mask pattern, light intensity aerial image, and the resulting photoresist pattern.

optical and mechanical elements. The illumination source provides the light for the exposure. It is typically a mercury vapor lamp or a laser. Mercury vapor sources are often wavelength filtered to one or more atomic transition lines at the 436 nm (G-line), 365 nm (I-line), or 248 nm (deep ultraviolet, or DUV) (3,6,12). The condenser optics image light from the source wavelengths uniformly onto the reticle. These optics control the spatial coherence, the coherence or sigma, of the incident light (29,30). The coherence of the light moderately affects the process latitude of the patterning process. The reticle is held by the reticle stage in the proper position for exposure. The projection optics image the light patterned by the reticle onto the wafer field. The numerical aperture (NA) specifies the maximum angle of light captured by a lens for imaging. The NA of the projection optics greatly impacts the resolution and process latitude of the patterning process (30,31). The projection optics typically also reduce the reticle pattern size upon exposure.

The wafer rests on the wafer stage that moves, or steps, the wafer so each field can be exposed sequentially. Alignment optics are used to ensure the correct reticle and wafer stage horizontal positions for proper alignment of each exposure to a previous patterned layer on the wafer. Focus sensors ensure that the wafer stage is at the proper vertical location, without tilt, for best pattern transfer (3). Dose sensors ensure that the correct amount of light energy is incident upon each wafer field. The exposure dose is used to optimize the size of the resist features (6,13,30) (Fig. 12). Software controls the workings of the different stepper mechanical subsystems and the interaction between the tool and the user. The software is used to create groups of instructions, or exposure recipes, to control and automate the tools' functions. The stepper may also connect directly to the coater track for automatic wafer transfers.

The minimum feature size resolvable for a diffraction limited (ideal lens) optical system is given by $R = K_1 \cdot \lambda/NA$ (3,30). K_1 is a process-dependent factor determined mainly by the resist capability, the tool control, and the process control. Typical values of K_1 are between 0.5 and 0.8. Therefore, the trends in optical lithography are towards lower-lambda, higher-NA imaging systems and smaller K_1 values to allow the printing of smaller features and denser patterns. The sensitivity of the patterning process to expected variations determines the manufacturability of the process. A patterning process can be characterized by its sensitivity to two main process control parameters, focus and exposure energy, also known as exposure or exposure dose (30) (Fig. 12). The usable focus and exposure latitude budgets actually incorporate a number of process variations, many unrelated to the stepper performance. Exposure errors alter resist CDs and limit focus latitude. The parameters that cause effective exposure errors include substrate reflectivity variations, nonuniform illumination intensity, reticle CD errors, resist sensitivity variations, developer variations, and feature proximity effects. Differences in feature size can also reduce the exposure latitude of a process as different exposure doses are required to pattern large and small features correctly. Reticle CD variations of smaller features must also be controlled more tightly than those of larger features (32) (Fig. 13).

Focusing errors, or defocus, lower the definition and contrast of the aerial image, alter the resist CDs, and limit exposure latitude (Fig. 14). The focus latitude, or depth of focus (DOF), expected at a single point in a stepper field is $DOF = K_2 \cdot \lambda/NA^2$ (3,30). K_2 is a tool-, process-, and pattern-size -dependent parameter, where small features have lower focus latitude. A typical value of K_2 is 1.0 for a minimum dimension feature. Therefore, the trends in lambda, NA, and feature size require patterning with lower overall focus margin. Parameters that cause effective focus errors between exposures or across the exposure field include wafer flatness, lens aberrations, substrate topography, stepper focusing errors, stage tilt, and resist thickness variations. Lens aberrations cause imperfections in the image transfer of patterns. The manufac-

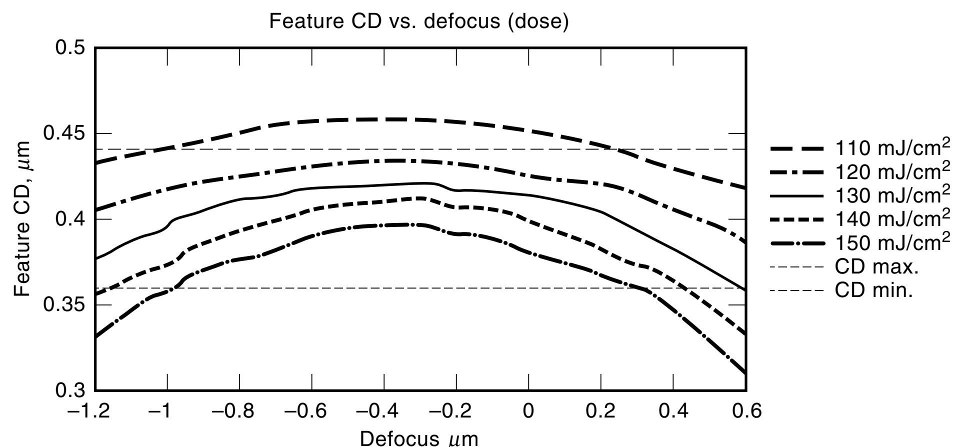


Figure 12. Plot of photoresist feature CD versus I-line stepper defocus as a function of exposure dose. Target CD range is 0.36 μm to 0.44 μum, shown by CD Max and CD Min lines.

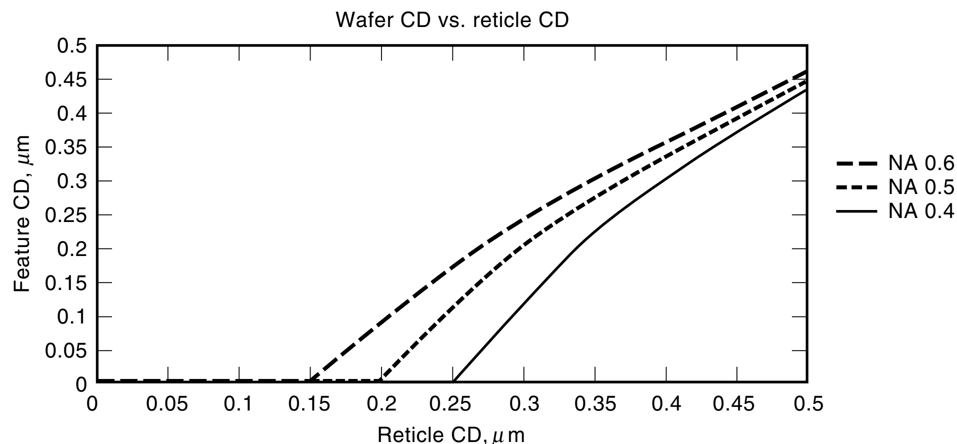


Figure 13. Plot of photoresist feature CD on the wafer versus the 1× chrome feature CD on the reticle as a function of projection lens NA for a DUV stepper.

ture of lenses with high NA, wide field size, and low aberrations is extremely difficult, especially for shorter illumination wavelengths (33).

To improve process control, a new type of stepper is becoming common, the step-and-scan exposure tool, or scanner (34). A scanner exposes only a strip of the reticle (and wafer field) at any time, scanning the exposure across the reticle to complete the image transfer. The stage then steps the next field into position to be exposed by scanning. This method allows smaller lenses and lower aberration imaging. However, image transfer errors due to scattered light, or flare, and mechanical movement are increased. Another latitude improvement technique is optimization of the condenser optics (29,30). Tuning the coherence and spatially filtering the illumination have been shown to improve the process margin for certain feature patterns. Focus latitude can also be expanded by optimizing the mask feature size together with the stepper exposure dose. This allows the feature width to be determined by an aerial image intensity level which is less sensitive to focus variations, the 150-focal point (see Fig. 14).

Photoresists

The goal of the photoresist is to translate the smoothly varying aerial image into a vertical profile relief image. To do this, the photoresist must undergo some physical or chemical change upon exposure to light, which can result in the generation of the relief image through further processing (i.e., it must be photosensitive). However, the photoresist must also resist or withstand further processing, such as ion implantation or plasma etching, in order to protect the regions covered by the resist. In general, there are several requirements that any photoresist must meet to be useful for integrated circuit manufacturing. First, the photoresist must be able to be easily spin coated into defect free thin films that will adhere to a variety of underlying substrates. The resist should have a relatively long shelf life and should give repeatable coating thicknesses with good uniformity. The coated resist films should also be relatively chemically and physically stable. The resist material must have good physical and mechanical properties in order to withstand elevated temperatures and harsh environments, such as corrosive etches, without losing pattern shape or adhesion to the substrate. Next, the resist must possess a high sensitivity to light energy to allow for the desired wafer throughput in the production line. Finally, the resist should have resolution capability that exceeds the CDs of the desired patterns (6).

Resists typically have two main components, a base polymer resin and a photosensitive additive or sensitizer. The polymer resin gives the resist its good film-forming and physical property characteristics, while the sensitizer makes the

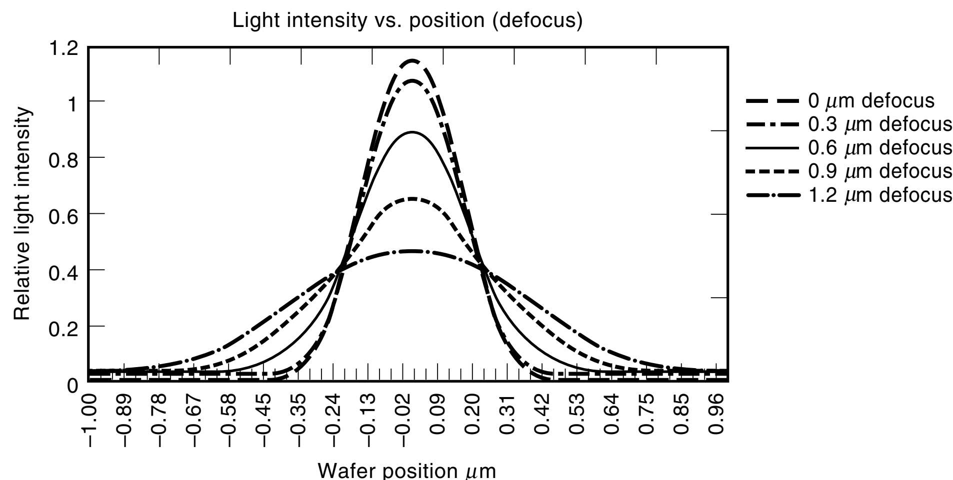


Figure 14. Plot of aerial image light intensity versus position on the wafer as a function of 0.6 NA I-line stepper defocus for a 0.5 μm opening on the reticle (1×).

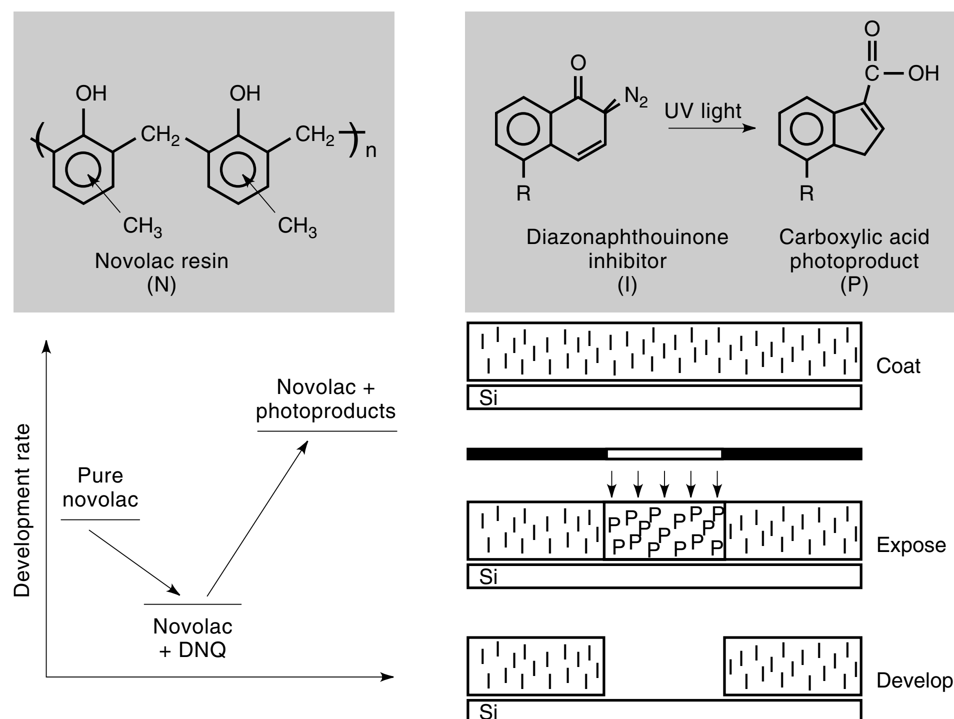


Figure 15. Overview of diazonaphthoquinone-novolac photoresists.

material respond to radiation exposure and allows the material to be imaged. Resists can be either positive or negative tone depending on their response to radiation exposure and development. In positive tone resists, the areas that are exposed to radiation are dissolved away in the development step, leaving behind resist in the unexposed areas (and vice versa for negative resists). Resists can also be classified by their general design as either nonchemically amplified or chemically amplified. Both of these schemes will be explained in more detail.

The current "workhorse" resists for the microelectronics industry are the diazonaphthoquinone-novolac materials (13). These resists are used by exposing them to the G-, H-, or I-line wavelengths. Figure 15 shows an overview of the manner in which these resists function. The polymer resin in these resists is novolac, a copolymer of phenol and formaldehyde. Novolac is soluble in many common organic solvents and can be coated from solution to form high-quality thin films. Novolac is also soluble in aqueous base solutions by virtue of the acidic nature of the phenolic groups on the polymer, giving rise to the common basic developers for these resists. The photoactive compound (PAC) in these resists is substituted diazonaphthoquinones (DNQ). Upon exposure to UV radiation, the DNQ is converted into a carboxylic acid photoproduct, which is itself soluble in basic developers. The presence of the DNQ photoactive compounds in the novolac resin serves to reduce drastically the dissolution rate of the novolac polymer in aqueous base developers. On the other hand, the presence of the carboxylic acid photoproducts of the DNQ in novolac often increases dramatically the dissolution rate of the polymer in basic developers. Thus, by converting the DNQ in the resist film using exposure to UV radiation, it is possible to cause a dramatic change in the development rate of the resist. An important property of these type of resists is the phenomenon known as bleaching. Bleaching refers to the fact that the optical absorbence of the photoproduct is significantly lower than its parent DNQ molecule, which results in the resist becoming more transparent in the ultraviolet as it is exposed. This bleaching phenomenon helps light to propagate through to the bottom of the resist film as the exposure process is carried out. Bleaching increases the nonlinear dependence of the resist's development rate upon remaining PAC. This nonlinear response is critical for converting the smoothly varying aerial image back into a well-defined resist relief image after development.

When resist is exposed over reflective substrates, the formation of standing waves due to interference of the various reflections within the thin resist film can lead to a scalloped-looking PAC profile in the resist at the edge of the feature, which without further processing would be transferred into the final resist relief image (13,30) (Fig. 16). During a postexposure bake, the PAC can diffuse from areas of high concentration in the antinodes of the standing waves into areas of low concentration, thus smoothing out the concentration gradients at the edge of the feature. In this manner, the sidewalls of the relief image can be returned to a smooth vertical profile.

Traditional DNQ-novolac resists were found not to be suitable for 248 nm lithography because of high absorbance and low sensitivity to the limited output of mercury vapor light sources at 248 nm (6). These problems were the basis for the invention of the second major class of resists, the chemically amplified resists (CAR) (6). Figure 17 shows an overview of the manner in which CARs function. Exposure to light generates a catalyst in the resist, typically an acid, which then acts on the surrounding matrix polymer in the presence of heat to catalyze a series of reactions that modify the matrix properties in such a way as to allow for generation of a relief image. This catalytic action serves to increase dramatically the sensitivity of these types of resists. CARs also have their share of

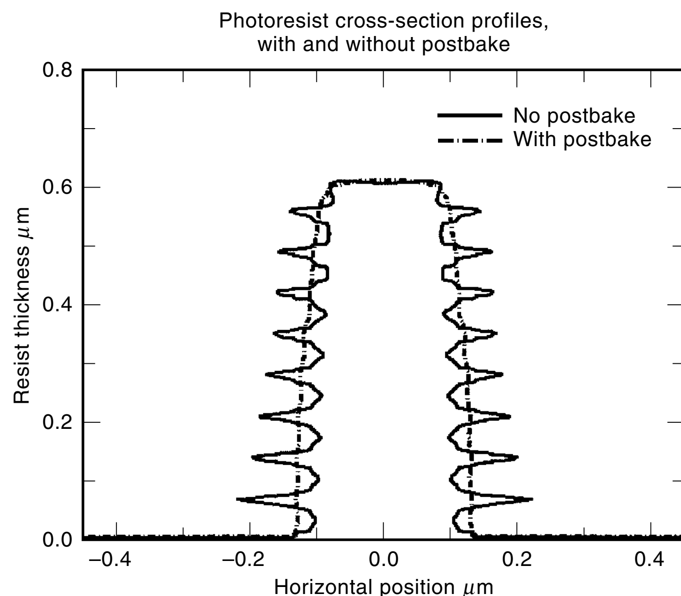


Figure 16. Cross-section view of simulated photoresist profiles patterned on a reflective substrate with and without postexposure bake (postbake). The scalloped photoresist profile in the non-postbake case is due to PAC variations caused by thin film interference. The postbake step diffuses the PAC locally to produce the desired smooth final profile.

problems. During the early implementation of these systems, environmental contamination and acid neutralization of the resist were shown to be major problems. A number of solutions have been proposed to solve this problem, including independent filtration of the air in the exposure tool systems, special top coat layers to protect the resist, and development of new chemically amplified resist systems that have less sensitivity to contamination.

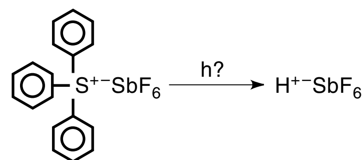
Photoresist Properties

Once a wafer has been patterned with photoresist, it is then ready for further processing, such as etching or ion implantation. It is at this point where the physical properties of the resist become very important in its resistance to the harsh environments and elevated temperatures possible in these processes. There are several criteria that must be met by both the etch process and masking resist to make the combination successful for a particular application. First, the resist must maintain good adhesion throughout the etch process to prevent etching in undesired areas. The resist must also maintain its profile during the process. The etch process must also show a high selectivity between the resist and the underlying material to be etched. This allows relatively thin resist layers (compared to underlying film thickness) to be used as etch masks without being completely consumed during the etch process. Finally, the resist layer must be relatively easy to remove after the etch process is completed (11).

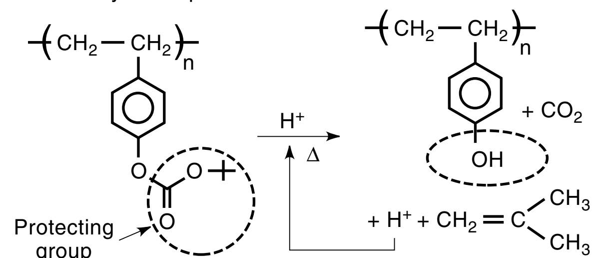
In most cases there is a tradeoff between the selectivity and anisotropy of the etch process that must be balanced. Typically, etching is a plasma process. In plasma etching, or sputtering as it is sometimes called, ions generated in a plasma chamber are accelerated by a potential difference in the chamber toward the wafer and literally chip off atoms as they bombard the surface. Since sputtering is a physical process, this type of plasma etching tends to be nonselective but anisotropic. The high degree of anisotropy is achieved due to the fact that the ions can be accelerated along a single axis. One method used to improve the etch resistance of photoresist masking layers is to use a process known as UV hard baking. In this process, the patterned resist layer is heated and subjected to intense ultraviolet light, which causes the resist polymer to crosslink and thus increase its etch resistance. One can also improve the selectivity of the process at some loss of anisotropy by forming chemically reactive species during the plasma etch that chemically react to etch the surface. This process is often referred to as reactive ion etching, or RIE. There are also many other mechanisms that play roles in the performance of plasma etch processes and that are beyond the scope of this work, such as polymer redeposition and advanced plasma etch processes (4,35,36).

Photoresists can also be used as masking layers for ion implantation. In ion implantation, the masking layer must meet several requirements. Most important, the resist layer

Photoacid generation



Acid-catalyzed deprotection



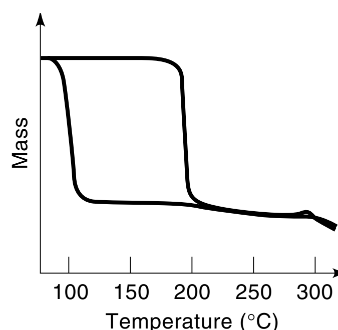


Figure 17. Overview of chemically amplified resist functionality.

must be able physically to block the incoming ions. This typically means that the resist layers used for this process must be substantially thicker than resist layers in other steps of the manufacturing process. Due to this increased thickness, resists for this application require relatively high photospeeds—high sensitivity to exposure energy. A UV hard bake step can again be used to crosslink the resist and thereby increase its ability to stop incoming ions. The implantation of ions into the resist layer can lead to charging on the surface of the resist (4). This buildup of charge can arc to the substrate damaging the device or can deflect other incoming ions, leading to nonuniform doping profiles. Resists also can outgas substantially during ion implantation and can act as a source of secondary electrons in the implanter. During the implantation, the resist becomes more heavily crosslinked and thus can become difficult to remove. Extended exposure to an oxygen plasma, or plasma ashing, is often required to remove such layers.

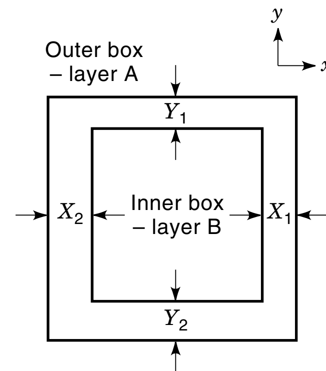


Figure 18. Determination of overlay error between layers A and B by measuring offset between box in box structures in X and Y directions. The offset $x,y = (X2 - X1)/2, (Y2 - Y1)/2$.

Metrology and Inspection

In general, the purpose of a metrology step is either for process control or process analysis. Process control metrology and inspection steps are performed during production to determine if individual parts of the process are meeting their control requirements or whether a layer has been correctly patterned. In process analysis, metrology is used to develop, improve, and test processes; find problem sources; and characterize tool, resist, and material performance (16). To provide results confidently, each metrology step should have adequate resolution, accuracy, and repeatability. Automated metrology tools should also have high throughput, usable software interfaces, and adequate sensitivity to process variations. Using an appropriate sampling plan, metrology for process control requires only moderate sensitivity to determine if the process is operating within allowed variations. Process analysis metrology requires higher sensitivity to show better the effects of process variations from a limited number of samples.

Process control steps are consistently performed during the wafer patterning process, or inline. A low-resolution optical inspection looks for large processing problems such as obvious misprocessing or large defects. A higher-resolution optical field-to-field pattern comparison checks wafers for smaller random defects (16). A top-down scanning electron microscope, or SEM, measures with high accuracy the CDs of test features on a field to ensure that the printed pattern size is correct (16). Adequate CD control is often defined to be +/− 10% of the minimum feature size. Additionally, optical measurements determine the overlay error between different patterning layers (16) (Fig. 18). These measurements are done with a dedicated overlay metrology tool upon specially designed features that overlap layer to layer. Once the metrology and inspection tests have been passed, the wafer is assumed to be correctly patterned. In addition to in-line measurements of wafer patterns, tools (including metrology tools), resists, and materials are periodically measured to ensure correct performance.

Process analysis requires additional metrology steps. A SEM is used for top-down viewing of printed feature shapes and CD measurements. Cross-section SEMs are used to measure and view feature profiles (37). An atomic force microscope, or AFM, is used for extremely high-precision profile measurements (16). Electrical probing is used to obtain quickly many high-accuracy width measurements of etched electrically conducting features or effective transistor gates (16,38,39). Interferometric measurements are made of material and resist film thicknesses.

Ellipsometry is used to determine thickness and optical properties of material and resist films; or to calibrate interferometry (40–42). Metrology performance improvements in these areas are required to ensure continuing lithographic patterning progress.

Overlay

Control of layer-to-layer pattern positioning is critical to the proper functioning of integrated circuits. The terms *overlay* and *alignment* are widely but inconsistently used across the semiconductor industry. In this article, we will define *overlay* to be the layer-to-layer positioning of features, and *alignment* to be the determination of reticle and wafer field positions that makes overlay possible. Improvements in overlay control are a necessary ingredient for increasing pattern density of designs (16). The overlay control of features on one layer to features on another layer must be within specified tolerances (Fig. 6). These tolerances are determined by the ability of the circuit to function with less than ideal overlaps or spacings between features on adjoining layers. A typical value for the maximum allowed overlay error on a layer is one-third of the minimum feature size (16). The first patterning step is performed on an unpatterned, or bare silicon, wafer that contains no alignment features. The stepper merely centers the exposed fields on the wafer. However, the first patterning layer is important to overlay control because it defines a reference pattern.

Overlay control is limited by errors in reticle patterning; alignment of the reticle to the stepper, or reticle alignment; alignment of the wafer to the stepper, or wafer alignment; distortions in pattern transfer to the wafer; and processed induced distortions on the wafer. During reticle patterning, the reticle write tool may not print features at the correct positions relative to each other (24). These errors are known as reticle registration errors. In both reticle and wafer alignment, each alignment system performs either a scanning or static illumination of alignment features, or alignment marks

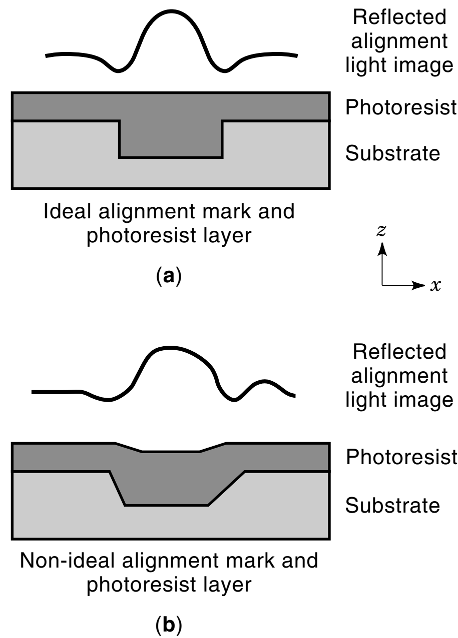


Figure 19. Relationship between reflected light intensity of alignment image from (a) ideal and (b) nonideal alignment marks on the wafer substrate.

(Fig. 19). The reticle marks are typically chrome or clear lines on the reticle. The wafer marks are typically grouped or isolated lines on a previously patterned wafer layer. The alignment signal, the reflected or transmitted light profile of these marks, is analyzed to determine the locations of the alignment marks. Different light detection and signal processing schemes may be used to enhance the accuracy of this determination. Errors in reticle or wafer alignment can occur in the determination of the mark edge positions or from movement inaccuracies of the reticle or wafer stages to these positions. Lens aberrations create overlay errors by distorting the image placement of the reticle pattern during resist exposure (43). Feature sizing errors strongly affect acceptable overlay errors. Dimensions that are too large or too small limit the ability of features on different layers to connect properly with adequate overlay tolerance (Fig. 6).

As wafers distort during semiconductor processing and as pattern transfer is never perfect, good overlay control requires matching the characteristics of previously patterned layers. The patterning errors affecting overlay are either intrafield or wafer based, although the actual error types are similar. The main correctable intrafield, or field, errors are magnification, rotation, and skew. The main correctable wafer, or global or "grid", errors are offset, magnification, rotation, and skew (3) (Fig. 20). Before exposure, the stepper measures multiple alignment structures across the wafer and creates an internal model of the previous layer's field and wafer errors. The stepper then attempts to emulate these errors as closely as possible during resist exposure to minimize layer-to-layer overlay variations (3). This is achieved by adjusting the stage stepping characteristics and lens reduction ratio. In scanning systems, additional corrections can be made for field skew and field magnification differences between the x and y axis. Special overlapping overlay calibration features from the two layers can be measured after patterning to analyze how well the layers were matched (Fig. 18). The stepper matching performance can be optimized based on the results of this analysis.

Because individual steppers or types of steppers have characteristic image placement distortions, worse overlay matching is typically obtained between layers patterned on different tool types than between those patterned on the same tool or same tool type. Therefore, the common cost reduction strategy of using multiple exposure tool types for patterning different layers, or mix and match lithography, creates issues for overlay control (3,44). Because the detection of the alignment signal is critical to overlay accuracy, the integrity of the alignment features is also important (3,45). These features were created during previous patterning steps and have been subjected to all subsequent semiconductor manufacturing steps. These steps include film etching and resist application and may include film deposition, high-temperature annealing, and chemical mechanical polish, or CMP. These steps can introduce undesirable changes or nonuniformities to the alignment features that prevent the alignment signal from being accurately analyzed (Fig. 19). As each alignment analysis method has individual process sensitivities, steppers include multiple alignment options.

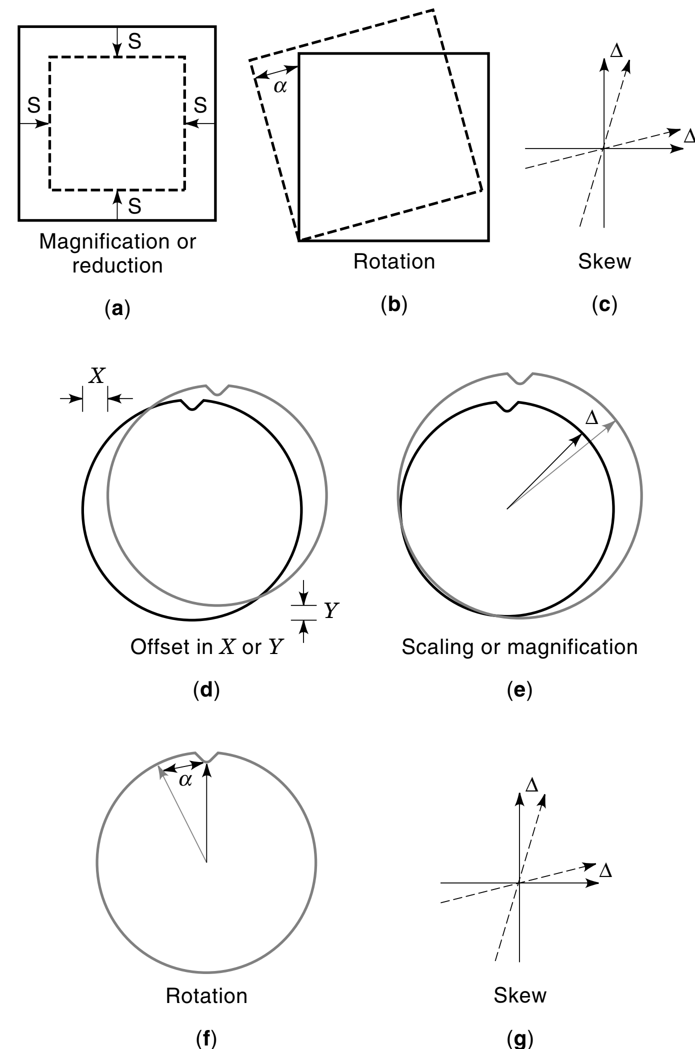


Figure 20. Pictorial description of field and global overlay errors.

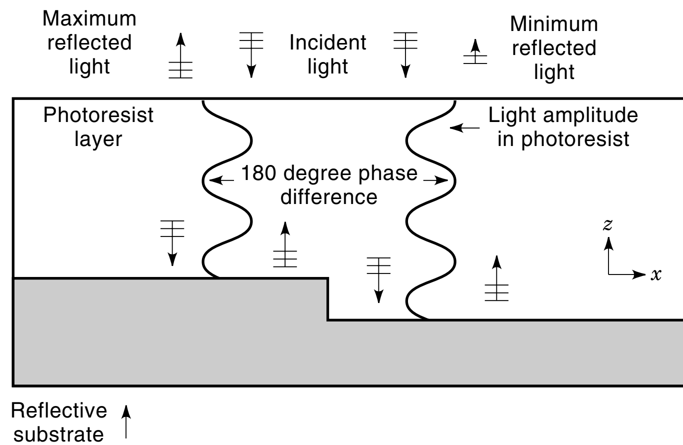


Figure 21. Diagram showing the cause of the CD swing effect where CD varies sinusoidally with resist thickness. Differences in absorbed light energy due to thin film interference create the effective exposure dose differences leading to CD variation.

Substrate Control

Accurate control of substrate films on the wafer is a necessary ingredient for staying within the optical lithography CD and overlay budgets. Control is required because changes in substrate topography, film thickness, resist thickness, film optical properties, or film chemical properties can cause CD and overlay errors. Many of these errors are attributable to thin film interference effects, or swing effects, where the error magnitude is sinusoidally dependent upon film thickness (3,13,30) (Figs. 21 and 22). During resist exposure, light incident upon the wafer may be reflected at the air/resist interface, at the resist/substrate interface, and at any of the interfaces between substrate films. The interaction of incident and reflected light creates vertical standing waves of light intensity locally within the resist layer. These standing waves lead to variations in the energy absorbed by the resist with changes in resist thickness, film thickness, substrate topography, or substrate reflectivity. Often the exposure budget of the patterning process is dominated by these effects. Additionally, nonplanar features on reflective substrates can scatter a significant portion of light laterally, causing undesired exposure of resist areas (3,13,46). This effect is known as reflective notching.

As swing effects are due to variations in the energy coupled into the resist from incident and reflected light, they can be affected by a number of parameters (3,47). Broadband mercury lamp illumination is less sensitive to swing effects than highly narrowed laser illumination. Resists dyed with light-absorbing additives allow less light to reach, and reflect from, the reflective substrate, although this light absorption also tends to limit resist imaging performance. Optimization of the resist thickness to an energy coupling minima or maxima will minimize CD variations due to small changes in resist thickness. An antireflective coating (ARC) on top of the resist can minimize variations in reflected light intensity and, therefore, absorbed light intensity (3,13). The reflectivity of the resist/substrate interface can be lowered with the use of an ARC underneath the resist, (bottom ARC) or by optimizing substrate layer thickness (3,13,48) (Fig. 22). Bottom ARCs are the preferred strategy for improving substrate reflectivity effects as they can eliminate swing effects and reflective notching. Bottom ARCs can be either organic or inorganic films. They work either by desorption of incident light or phase cancellation of reflected light, or by a combination of both. Often process integration issues such as etch requirements will determine an ARC strategy (48).

Due to light absorption in resists, large variations in resist thickness caused by substrate topography create CD errors, even on nonreflective substrates, a so-called bulk absorption effect. The use of CMP on substrate layers will minimize these errors. However, typical variations in CMP depth across fields or wafers can cause substantial substrate thickness variations (49). Although not often considered, absorbed energy errors can lead directly to overlay errors, especially for narrow features (50). Undersizing of these features causes considerable line-end pullback, where generally the line ends are designed to connect to features on another layer (Fig. 6). Additionally, control of the substrate reflectivity is important for the alignment system to determine accurately the position of alignment features. Chemical control of the substrate is also important. Resist/substrate chemical interactions can prevent adequate resist/substrate adhesion or, alternatively, cause incomplete resist development at the substrate, or resist scumming” (51).

Simulation

Lithography simulation has proven to be a useful tool for understanding, developing, improving, and explaining optical li-

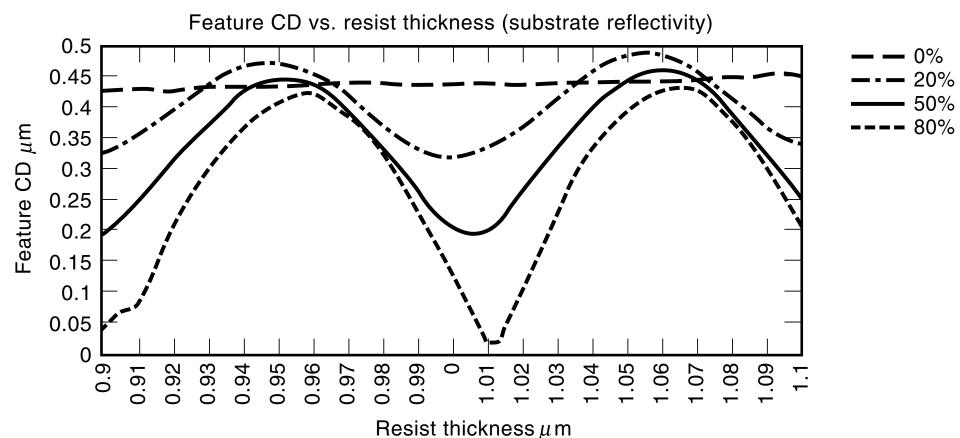


Figure 22. Plot of swing effect for a nominal 0.4 μm photoresist feature showing CD versus photoresist film thickness as a function of reflectivity at the photoresist/substrate interface.

thography processes (52). Many of the examples in this article were generated using lithography simulation. Performing optical lithography experiments via simulation replaces experiments in the fab or research lab, saving time, effort, and money. Many varied models and simulators incorporating these models exist for a large number of applications. These applications include optical element design and manufacture; stepper illumination and projection lens filtering optimization; reticle patterning and manufacture; design optimization; material thickness and property optimization; resist thickness and performance optimization; yield prediction; defectivity analysis; metrology optimization; process throughput analysis; ARC optimization; process cost; and process latitude analysis. The application will vary with the simulation tool, as will accuracy, range of model validity, number of dimensions modeled, speed, scale, cost, software robustness, and ease of use. Simulation is not universally accepted in fabs, mainly because of limitations in resist modeling. However, shorter product development cycles, more complicated processes, and larger equipment costs are increasing the need for simulated experiments. The most common uses of simulation are in optimizations of design features and ARCs and in analysis of focus and exposure latitudes. Current research in simulation (53–57) centers upon the speed of design optimization, the accuracy of resist photochemistry models, new data presentation methods, linkage to models for other semiconductor processes, and development of models for nonoptical lithography methods.

Cost of Ownership

As each of the many layers in a device requires patterning, the optical lithography process is a major part of the cost of manufacturing integrated circuits. It is estimated that optical lithography will soon comprise nearly 50% of the entire cost of semiconductor manufacturing (58). The goal of cost of ownership (COO) analysis is to understand the cost components of lithography processing to maximize manufacturing profitability. Gaining an understanding of the costs in this complex process is not easy. Many parameters outside lithography must be included. However, the effort is worthwhile, as large savings can be realized by even minor reductions in processing cost. The cost of a process is typically measured in dollars/wafer, dollars/layer, dollars/die, or dollars/working circuit. Much of the cost of lithography, or any process, comes from rapidly escalating equipment costs (3). Other components important to COO and potential profitability include cleanroom space, facilities, materials, and payroll (sadly, for engineers, this component is typically minor). Process performance tradeoffs can also be analyzed in terms of cost. Factors include tool capability, resist capability, tool throughput, tool size, tool utilization, field size, wafer size, process development time, product volume, number of manufacturing steps, device size, device performance, yield, defectivity, engineering resources, intellectual property, and extendibility of processes to future device generations.

Additional, somewhat abstract, components are needed for the financially successful production of semiconductor devices. These include adequate supplier support, design capability, marketing expertise, work force technical experience, work force motivation, organizational structure, and management effectiveness. Customer, product, and supplier road-maps are also needed to provide long-term cost analysis. By acknowledging the need for these abstract factors and building a model to analyze and optimize the more defined components, accurate COO comparisons can be made for different business scenarios (3,59). Lithography technology (e.g., DUV versus I-line), tool, material, and process choices can be effectively guided by COO analysis. The importance of accurate planning would be difficult to overestimate. Improvements in optical lithography planning using detailed COO analysis methods can be shown to save a new semiconductor factory hundreds of millions of dollars per year (59).

OPTICAL LITHOGRAPHY EXTENSIONS

The previous sections have explained the basics of optical lithography tools, materials, cost, and processing and examined many of the current capabilities and problems. This section discusses some of the new technologies being implemented and investigated to help push optical lithography resolution further. Current 248 nm optical lithography processes are being used for the 0.25 μm and 0.18 μm device generations. However, improvements are needed to allow optical lithography to meet the requirements of future device generations.

Tool and Process Control

Manufacturing of a circuit for a given design rule generation requires the ability to pattern the designed features within specified tolerances despite process variations. Therefore, reducing the process variability allows smaller and denser features to be patterned manufacturably (Fig. 11). Improving process control requires reducing focus variability, dose variability, or defectivity. Process control can be improved by decreasing tool, material, resist, or environmental variability or by improving the integration of these factors into the patterning process. Tool improvements include the optimization of mechanical precision, optical lens aberrations, thermal control, and fluid handling. Material improvements include optimization of optical properties, thickness, chemical content, and defectivity. Resist improvements include optimization of photochemical properties, thickness, chemical stability, and thermal stability. Environmental improvements include air temperature control, air humidity stability, particle removal, and chemical filtering. Many of the aforementioned improvements will require advances in metrology and problem analysis in order to identify the dominant sources of patterning variation.

Additional control can be gained by improving the integration of the parts in the fabrication process. New control software can analyze metrology data better, determine optimum process settings, ensure uniform tool-to-tool performance, and optimize each individual tool's performance with output data feedback (60). Control software can work in tandem with fast and accurate metrology designed into the tools. Better use of lithography modeling software will improve process development decisions and create processes less sensitive to variations (61). Modeling software can also improve yield by speeding problem identification. Finally, higher productivity and lower-cost processes make low-yielding, leading-edge processes more profitable to manufacture.

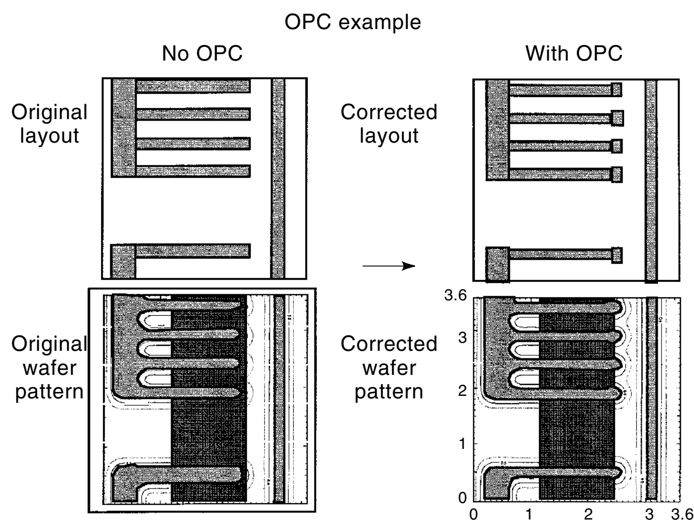


Figure 23. Top-down view of layout design versus wafer pattern with and without OPC. Original layout prints on wafer with significant line-end pullback and CD difference (bias) between densely packed and isolated features. OPC alters the design to compensate for the pullback and CD bias in the final corrected pattern.

Optical Proximity Correction

Due to the nature of lithographic pattern transfer, the final resist and etched features will not match the designed features exactly (Fig. 23). Often a systematic mismatch in pattern size, shape or spacing occurs (62). The original design data can be modified to reduce these systematic errors and allow the final wafer features to resemble the desired shape more closely. The reduction of these systematic errors improves CD and overlay control. The modification of a design to correct for systematic pattern transfer effects has come to be known as optical proximity correction (OPC) (63). However, these effects are not confined to optical limitations. Other sources of error include reticle, substrate, resist, and etch/implant properties. The correction of a design to improve its manufacturability is equivalent to expanding the lithographic design rules. Additional requirements for printability are added, causing the modified design to be more specific to a given patterning process.

The goals of design correction are often to reduce proximity effects (i.e., printing differences between isolated and dense features), line-end pullback, nonlinear pattern transfer, pattern density loading effects, and interactions with features of underlying layers (64) (Fig. 23). CD control is gained by improving the circuit design, without having to purchase expensive new lithography tools, resists, or materials. To these ends, the original design may be modified by adding and/or subtracting small (below the optical lithography resolution limit) features and/or moving the edges of existing features (63). The software used to make the alterations will apply specific rules or pattern transfer models to determine the optimum corrections (63,64). The rules or models are developed based on metrology of specialized test structures patterned by the same process or on simulations of the patterning process. The software may perform the alterations to the design database or the fractured data. Similar software tools have been developed expressly for optimizing the reticle patterning process (65).

Many challenges exist for successful design correction (66). Ensuring that the alterations are performed quickly and correctly is difficult on modern designs, which contain hundreds of millions of features, multiple feature patterns, and multiple design styles. Subresolution features and small jogs in altered features create enormous difficulties for reticle manufacture and inspection (62). Additionally, the substantial increase in design file size can overload the capabilities of reticle patterning and inspection tools. The usefulness of the rules and models may be limited by metrology accuracy, simulation accuracy, and inherent process variability, both in reticle and wafer patterning. Finally, traditionally separate roles of design, reticle, fracture, and process groups can make design correction projects difficult to organize.

Phase Shifting Masks

A new class of reticles known as phase shifting masks (PSM) has shown improvements in imaging performance over traditional chrome on glass, or binary, reticles. The largest improvement is provided by the strong or alternating PSM (alt. PSM) (67) (Fig. 24). During exposure, alt. PSMs create low light intensity areas in the image by varying the phase of the transmitted light between 0° and 180°. During coherent illumination of a PSM, this phase transition causes the light amplitude to transition from a positive to a negative value. As the amplitude must cross zero during the transition, the light intensity (being the square of the amplitude) must also reach zero. This phase shifting effect increases the contrast of the image. For a given patterning process, alt. PSMs can theoretically image features dimensions and spacings one-half of those imaged with a binary reticle. Actual production factors limit the improvement somewhat, but aerial images from alt. PSMs are still substantially better than from binary reticles for small features and dense patterns (68).

The phase shift effect is typically created by selectively etching into the quartz reticle substrate to provide a 180° optical path difference between shifted and unshifted regions (69). Alt. PSMs have many issues to solve before they can be used effectively. In the manufacture of alt. PSMs, additional challenging reticle patterning steps are performed, phase control is difficult, and defectivity is increased (69). Design difficulties also exist (70). Upon exposure, narrow low-intensity areas appear at the edges of every phase region. In a positive resist process, these areas will appear as resist lines (Fig. 25). Many design patterns exist that cannot be implemented with alt. PSMs without creating undesired lines. Techniques have been developed to remove these unwanted phase transition effects, known as phase conflicts. The 0° to 180° phase junction can be performed in 0°, 60°, 120°, and 180° steps to smooth the transition and prevent unwanted lines from printing. However, defocus effects require considerable space in the design for this solution to be effective (71). Unwanted lines can also be prevented in a positive resist process by using a second exposure of the phase conflict areas (72). This method has issues with the design and overlay of a double exposure process.

Other PSM types have been developed to reduce the difficulties encountered with alt. PSMs. The most accepted is the attenuating PSM (att. PSM) (73) (Fig. 24). In an att. PSM the

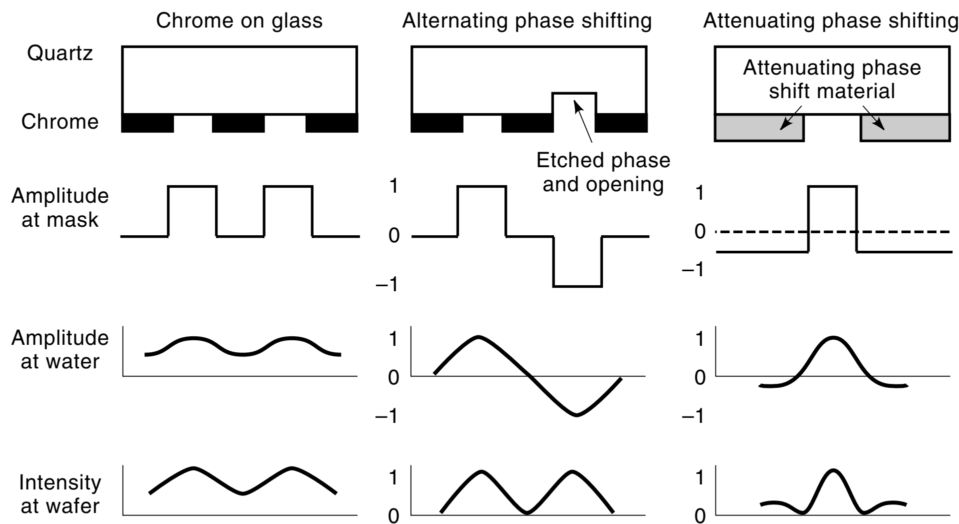


Figure 24. Cross-section views of standard chrome on glass, alternating phase shift, and attenuated phase shift mask performance. Comparisons of light electric field amplitude at the mask and at the wafer are made for each mask type. Light intensities at the wafer show the improvement in image contrast with the phase shift mask types over the chrome on glass mask type.

chrome layer on a binary reticle is replaced with an attenuating phase shifting layer. The attenuating layer allows light to be transmitted with an intensity of 4 to 17% and a phase shift of 180° relative to the clear reticle area light transmission. Att. PSMs have found considerable use improving the image contrast of dark field patterns. The imaging benefits of the att. PSM are less than those of the alt. PSM, but phase conflicts are eliminated. However, att. PSM technology also has challenges. Development and process control of attenuating materials for deep ultraviolet illumination has proven difficult (74). Light diffraction effects at the edges of features can cause secondary features, or sidelobes, to resolve in the resist (75). The light transmitted through the attenuating material can also cause problems at the edges or corners of fields, where double or quadruple exposure can occur. Additional reticle manufacturing and wafer processing improvements are required to eliminate these undesirable effects.

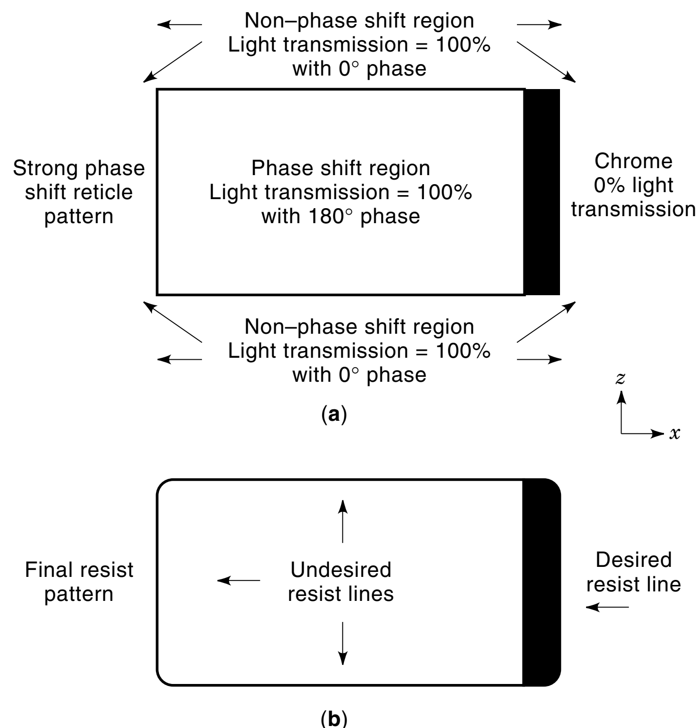


Figure 25. Top-down view of strong phase shift design and subsequent printed wafer resist pattern. Undesired small resist lines appear on the wafer from the junction of phase shifted and non–phase shifted regions. The large resist line below the chrome is the only desired line.

Photoresist Improvements

Improvements to resist chemistries and the development of new resist processing schemes have been and will continue to be a key ingredient in the success and extension of current optical lithography technologies (6). For example, increased contrast and surface inhibition improvements to I-line resist chemistries, in conjunction with the development of high-NA I-line exposure tools, have allowed I-line lithography to be extended into the 0.30 μm generation (76). Further improvements to resist technology are under development. Resists with higher surface inhibition are useful for att. phase shift exposure to help eliminate the common problem of sidelobe formation. Improvements in photospeed and etch resistance will help extend the capability and economic advantages of current optical technologies. For CARs, developing resists with lower sensitivity to environmental contamination will also be of great benefit. Advanced resists often perform better at imaging either lines or spaces, and either dense or isolated features. Resist properties are specifically tailored to the needs of particular patterning layers. This specialization enables improved patterning capability but adds to the complexity of the overall lithographic process.

In addition to improving the resists used for typical single-layer resist (SLR) processes, the possibility of using hardmask, bilayer or top-surface imaging (TSI) processes offers the potential to extend the capability of current optical technologies (6). Figure 26 shows examples of the bilayer and TSI resist processing schemes. In the hardmask and bilayer approaches, a thin resist imaging layer is coated upon a transfer layer. In the hardmask approach, this transfer layer is an inorganic film designed for etch selectivity to the underlying film(s) to be etched and for good ARL properties. In the bilayer approach, the transfer layer is a thick organic planariz-

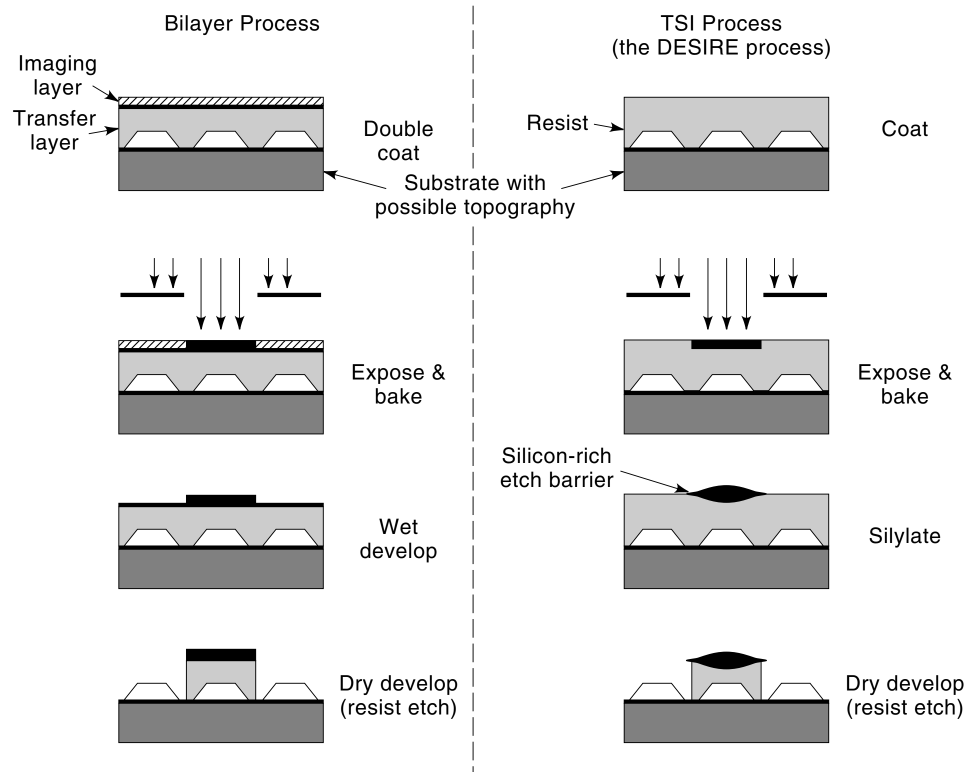


Figure 26. Examples of two alternative photoresist processing schemes, bilayer and top surface imaging.

ing layer (77). The initial pattern formation is performed in this top imaging layer using conventional lithographic techniques, and then the pattern is replicated in the transfer layer using an anisotropic etch process. In TSI, the exposure process creates a chemical change in the top surface layers of the thick resist, which then prevents or allows silylation of this thin exposed region using a subsequent chemical treatment (78). The resulting silated areas of the resist are resistant to an oxygen plasma etch and, thus, the pattern is again transferred through the entire thickness of the resist using an anisotropic etch process. The advantage of all these processing schemes is that the imaging takes place in a very thin layer at the top surface of the resist or patterning layer, thus increasing focus latitude and reducing substrate reflections. The drawbacks for these processes are the added complexity and additional steps required to complete the patterning process. Nonetheless, these advanced processing schemes offer the opportunity to image smaller features with existing optical lithography technologies.

193 nm Lithography

The next optical lithography generation will use 193 nm exposure light. There are a number of very difficult challenges in developing exposure tools at this shorter wavelength (3,79–81). The absorption coefficient of most materials increases as the wavelength of the radiation decreases. At 193 nm, the quartz material used for making the lens elements and mask blanks begins to absorb at levels that can cause imaging problems and damage to the optical system. High fluences of 193 nm radiation through quartz lens elements in experimental exposure tools have shown that the lens elements can be damaged by the formation of color centers within the material and by induced compaction of the material. As the lens elements absorb energy, lens heating also becomes a larger problem, and compensation for its effect on imaging performance becomes more crucial. The end result is that lens lifetimes in these new exposure tools may be significantly shorter than those of past tool sets. One potential solution to some of these problems is the use of calcium fluorite (CaF) lens elements at critical locations. CaF shows lower absorbence than similar quartz elements but is still an immature technology (3,82). To reduce lens manufacturing difficulties, only scanning exposure tools are being considered for the 193 nm generation. The exposure source for these 193 nm exposure tools will be ArF excimer lasers.

The 193 nm technology will also require the development of entirely new resist chemistries for this shorter wavelength (51,83–86). The main problem for resist designers is the lack of a transparent matrix polymer. The polyhydroxystyrene polymers used in 248 nm resists absorb too strongly to make them useful for 193 nm resists. There have been a number of polymer families proposed as possible materials for 193 nm resist design: acrylates, maleic anhydride copolymers, and cyclic olefin polymers. The key problem in development of these new resists is to satisfy the etch, imaging, and photospeed requirements in a single material. High-photospeed resists will help reduce problems due to lens energy absorption. Along with the development of new resists, new ARC materials will also be required to make these resist systems successful. A complicating factor in this development work is the difficulty of optical metrology at the 193 nm wavelength.

Higher NA Imaging

The current maximum NA of stepper projection optics is approximately 0.6 NA for both 365 nm and 248 nm illumination wavelengths. To increase imaging resolution beyond current

capabilities, projection NAs of approximately 0.7 are being considered for 248 nm illumination step-and-scan systems (87). If the resist capabilities are assumed equal, the initial 193 nm 0.6 NA scanners offer moderately better performance than 248 nm 0.7 NA scanners. However, 0.7 NA 248 nm projection systems would increase patterning capability without the high costs and infrastructure changes required to switch to 193 nm wavelength lithography (88,89). For patterning of small features, especially with dense pitches and darkfield patterns, 0.7 NA 248 nm illumination offers improved process latitude over 0.6 NA 248 nm illumination. Exposure latitude is especially improved. However, improved tool and process focus control will be required. The major challenge for this extension is in the manufacture of wide-field, low-aberration 0.7 NA projection lenses. However, stepper companies are already working on plans to manufacture both 248 nm and 193 nm tools with projection NAs of 0.75 to 0.8 NA.

SUCCESSORS TO OPTICAL LITHOGRAPHY

The extensions mentioned above will enable optical lithography to meet the needs of the 0.18 μm, 0.15 μm, and 0.13 μm generation of device/circuit requirements. However, a successor is possibly required for the 0.13 μm and definitely required for the 0.07 μm generation. Due to the reduced ability of fused silica lenses to work below the 193 nm wavelength, the successor will not be a traditional quartz refractive optics technique. The use of 157 nm wavelength optical lithography with entirely CaF refractive optics is a possibility. However, the immaturity of CaF technology and a number of technical challenges makes this likelihood small. Additionally, there are several nonoptical technologies competing to replace optical lithography. All of them are immature with respect to the capabilities that optical lithography now performs for circuit patterning. In particular, nearly all the possible replacements appear considerably more expensive than optical lithography. The following technologies are the main candidates for future advanced semiconductor patterning. A description of each technology is given along with an analysis of their strengths and weaknesses.

X-Ray

X-ray lithography is a proximity patterning method with an approximately 10 μm to 30 μm gap between the reticle and the wafer required for good imaging performance (90). Figure 2 is an accurate representation of X-ray lithography if the exposing radiation is assumed to be X-rays instead of light. The X-ray illumination source is synchrotron radiation with a wavelength of approximately 0.8 nm to 1.5 nm and photon energy of 1 keV to 2 keV. The exposure beam is a long, narrow strip that is scanned across the reticle to complete the image transfer, similar to optical scanning methods. The reticle features are at the same scale as the wafer features (1× reduction). The reticle is composed of a patterned metallic absorber on a silicon carbide substrate membrane. The main benefits of X-ray lithography are the ability to use current chemically amplified resists, the fine resolution capability (<75 nm features can be resolved), the reuse of optical scanning technology, and the considerable industry research experience. X-ray lithography is the only nonoptical lithography contender that has, thus far, succeeded in producing complex functioning circuits. The major drawbacks of this technology are the difficulty of manufacturing 1× reticles with adequate CD control, the risk of wafer particles larger than the gap distance damaging the fragile reticle, and the manufacturing redundancy requirement of installing at least two large synchrotron radiation sources into an IC factory (91).

Masked Projection E-Beam

SCALPEL (scattering with angular limitation projection electron-beam lithography) is an E-beam projection printing method with reticle feature dimensions 4× those of wafer features (21) (Fig. 27). A scanning illumination method is used wherein a long, narrow beam of approximately 100 keV electrons is scanned across the reticle. Electrons unscattered by the reticle pass through an aperture and are electromagnetically imaged onto the wafer. Scattered electrons are blocked by the aperture from reaching the wafer. The reticle is composed of a patterned metallic scattering material on a silicon nitride substrate membrane similar to an X-ray lithography reticle. The reticle requires periodic silicon struts for physical support (92). These struts impact imaging; therefore, no reticle features are placed above them. Design patterns bisecting a strut must be stitched together during exposure. The SCALPEL technology has many benefits. These include patterning resolution, 4× reduction reticles, use of current resists, manufacturing of reticles from standard silicon wafers, reuse of some E-beam reticle write tool technology, and the reuse of optical 4× reduction scanning technology. The main drawbacks of this technology are the requirement for reticle field exposure stitching, the limited throughput, and the potential for device damage from high-energy electron impact.

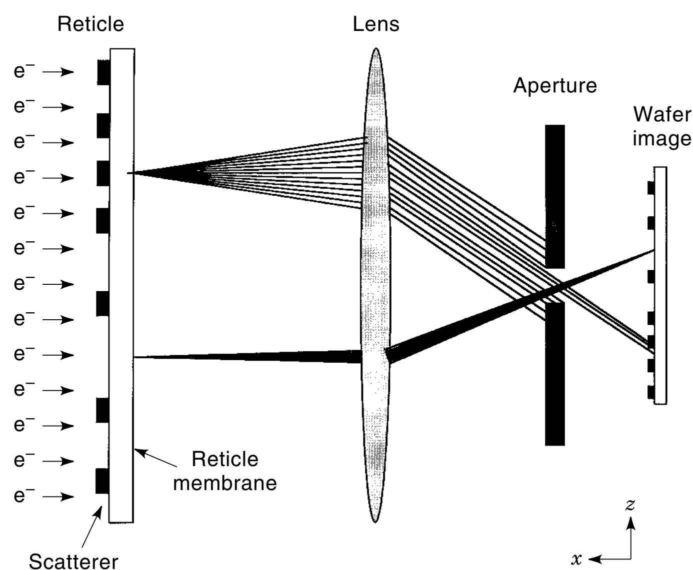


Figure 27. Diagram of SCALPEL wafer exposure. High-energy electrons incident upon a reticle are scattered by an absorber pattern but unscattered by a reticle membrane. The electromagnetic lens focuses electrons onto wafer. The majority of the scattered electrons are blocked from reaching the wafer by an aperture, while the unscattered electrons remain unblocked and reach the wafer to create a high-contrast resist image.

EUV Lithography

EUVL (extreme ultraviolet lithography) is a projection imaging method (93) (Fig. 28). The method uses multilayer reflective optics (mirrors) with NAs of approximately 0.1 to 0.25 in a 4× reduction system. The illumination is ~13 nm wavelength radiation (soft X-ray), which has photon energies of ~0.1 keV. The illuminating radiation is generated by a laser-induced plasma. The superheated plasma emits blackbody radiation, which is then wavelength narrowed and focused by a series of reflective optics. The 4× reticle is itself a multilayer reflector coated with a thin EUV absorbing metal layer for the pattern. The advantages of this technology are the fine resolution capability (allowing extendibility to multiple circuit generations), the 4× reduction reticles, and the research experience at US national labs. The disadvantages of this technology are many. The production of damage-resistant and high-thickness-accuracy (~0.15 nm) multilayer mirrors is a considerable challenge. The production of a high-output radiation source, metrology at wavelengths near 13 nm, and vacuum exposure of wafers are all difficult. Creation of reticles free of even minute imperfections or defects is perhaps the greatest challenge. Also, an entirely new resist technology will need to be developed, most likely utilizing TSI techniques.

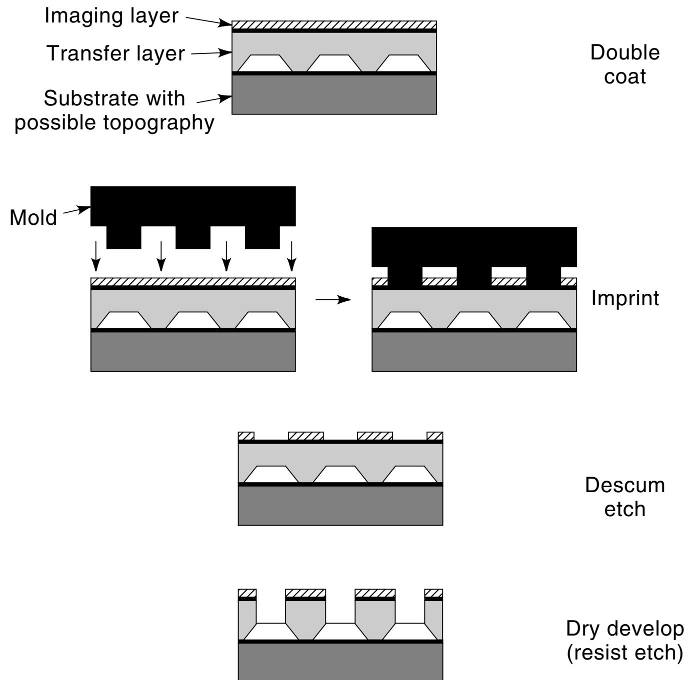


Figure 29. Overview of imprint lithography process.

Imprint Lithography

Imprint lithography, or step and squish, is a high-volume, low-cost contact printing (1×) method borrowed from the CD-ROM production industry (94–96). A master mold is used as an imprint mask to compression mold a pattern into a polymeric coating on a wafer. The technique can utilize a bilayer polymer imprint-resist scheme (Fig. 29). A thick bottom resist layer is covered by a thin top layer of easily imprinted resist with high etch selectivity to the bottom resist. The mold is used to imprint the pattern onto the top resist layer. After a descum step, the pattern is transferred via plasma etch through the thick bottom resist, which is used as an etch hardmask for further implant or substrate etch processes. Early work has demonstrated 25 nm features reproduced over areas up to 30 mm by 30 mm (94). The benefits of this technology are readily apparent. It is low cost, requiring no radiation source or optics. There is some reuse of current resist technology, and the method has very high potential throughput, especially if entire wafers can be imprinted at once. The drawbacks of this technique are the production of 1× master mold patterns; mold lifetime and stability; defectivity during the release of the mold from the resist; and the need for highly accurate mechanical alignment and contact.

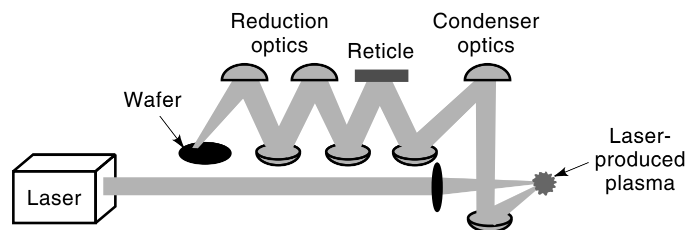


Figure 28. Extreme ultraviolet lithography configuration. A high-power laser heats a small object into a blackbody radiator. Approximately 13 nm radiation is focused by a series of reflective condenser mirrors onto a reflective reticle and by a series of reflective projection mirrors onto the wafer.

CONCLUSION

Optical lithography has been successful at continually improving the functionality and cost of integrated circuits. This success extended for 30 years over many circuit generations. Optical lithography improvements have played a major part in the development of the current information age. The end is now in sight for optical lithography due to some hard physical limits. This article has discussed how optical lithography works, how it can be extended, how far it may go, and what the main candidates are. Within a few years optical lithography will likely be replaced as the leading-edge patterning process at least in process development. However, the tremendous technical and economic advantages of optical lithography will continue to keep this technology in widespread use for many years to come.

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