J. Webster (ed.), *Wiley Encyclopedia of Electrical and Electronics Engineering*

MIS, MIM, AND MSM STRUCTURES

Today, plasma processing is extensively used in integrated-circuit manufacturing for materials deposition and for anisotropic etching to define deep submicron structures. A glow-discharge plasma of a partially ionized gas, formed from an RF discharge, is composed of ions, electrons, and a variety of neutral species that exists in the pressure range of interest. A potential that develops at various points in this RF discharge is important in determining the energies of ions and electrons incident on the wafer surface submerged in the plasma. The energy of charged particles and the reactive gas can initiate either a deposition process or an etching process. This process can induce damage or contamination effects in exposed materials that may modify the potential device characteristics.

In semiconductor manufacturing, plasma-processing-induced charging damage (1,2,3,4,5) to the gate oxide has been a serious reliability issue for submicron complementary metal oxide–semiconductor (*CMOS*) devices. Continued scaling into the deep submicron regime requires very thin gate oxides for the metal oxide–semiconductor (*MOS*) devices. During plasma processing when the MOS device is exposed to plasma ambient, the imbalance in the positive-ion and electron currents on the wafer surface creates an increase in potential across the gate oxide (6). A higher potential is developed on the wafer surface with respect to the electrode, where the wafer is placed, when ion current is larger than the average electron current. In the reverse situation, the potential at the wafer surface decreases. Once a steady-state potential develops on the gate electrode, a current flows through the thin gate oxide as if it were under high-electric-field stress. As a result, the device gate oxide becomes worn out or prematurely broken down because of charge trapping in the oxide and generation of interface states at the Si–SiO_2 interface, which degrades the insulating properties of oxide. An electric field of the order of 9 MV/cm or greater is required for an appreciable amount of current to flow through a good-quality thin gate oxide in uniform plasma. For such a high field across the gate oxide to exist, the substrate potential has to be substantially different from the gate potential (7). Therefore, depending on the plasma potential distribution relative to the electrode on which the wafer is placed, the floating potential on wafer surface could be higher than the substrate potential. Once the gate potential is higher than the substrate potential, electrons are injected from the substrate (substrate injection) and when the substrate potential is higher, electrons are injected from the gate (gate injection). The effect of this polarity difference on plasma-charging damage is seldom addressed because in the high-density plasma gate potential that follows the plasma potential is normally higher than the substrate potential.

In this article, we have explored the effect of polarity difference of injection on plasma-charging damage to CMOS devices. By properly designing a specific plasma-charging experiment, it is shown that both the gate and the substrate potential do change during plasma processing and the behavior is rather complex. This plasma-processing condition follows a unique process in a plasma system in which both polarities coexist. The value of the substrate potential with respect to the gate potential determines the direction of current flow through the thin gate oxide. A comprehensive investigation of plasma-charging damage dependence on the polarity of current flow is presented here. By measuring transistor parameters, we have observed that there are two seriously damaged regions in a wafer. Excessive damage was observed at the center of the wafer and at the perimeter all around the wafer. It was demonstrated that damage at the center region is due to

substrate injection and damage in the perimeter region is due to gate injection. The experimental results further show that the degradation of the hot-carrier lifetime in the *n*-channel metal oxide–semiconductor field-effect transistor (*n-MOSFET*) depends on the polarity of current flow through the gate oxide during plasma-charging damage. Since enhanced charge trapping is noticed due to plasma charging, some correlation is expected between plasma damage and hot-carrier reliability. Many contradicting observations (8,9,10,11) of the dependence of hot-carrier lifetime degradation on plasma damage are reported in the literature. We believe the discrepancy is due to the polarity dependence of plasma charging. If the current flow is due to gate injection, no correlation exists, whereas if the current flow is due to substrate injection, an exponential correlation is present between plasma damage and hot-carrier reliability.

Typically MOSFET subthreshold current characteristics provide an estimate of the interface trap density distribution and it is known that interface state density increases with intensity of damage in plasma-damaged devices (12). The impact of polarity of electron injection on subthreshold swing (*S*) of a plasma-damaged MOSFET was studied for both substrate injection and gate injection. In addition, low-frequency noise in a plasma-damaged device is closely related to the interface traps at the Si/SiO_2 interface because the drain noise arises from charging and discharging of traps through modulation of the channel electrons (13). It is obvious from this point that plasma-charging damage increases the low-frequency noise in a MOSFET. However, it is observed that the MOSFET low-frequency noise is strongly dependent on the polarity of the plasma-charging damage. When the plasma-charging damage is of the gate-injection type, the MOSFET low-frequency noise is insensitive to damage whereas when the polarity is of the substrate-injection type, the MOSFET low-frequency noise is very sensitive to damage.

Device Characterization

To effectively measure the intensity of plasma-charging damage in the gate oxide, initial electron trapping slope (14) measurements were employed. In this method, a voltage-versus-time curve (*V-t* curve) is measured. Specifically, a constant current is injected into the gate oxide from the gate of a MOS transistor under an electric field that is sufficiently high to create traps in the oxide as well as in the Si/SiO_2 interface. The injection lasts only a few seconds, whereas the voltage required to sustain the current is recorded as a function of time. This voltage variation relates directly to the net charges trapped under the current stress. Since the oxide is damaged by current stress during plasma processing, a damaged oxide is expected to have a much higher density of electron traps. An increase in the oxide's charge trapping rate at a given stress field is an indication of damage. From the *V-T* curve the initial portion corresponds to the net electron trapping, which is initially dominated by the filling of existing empty electron traps and thus affected by plasma damage. The slope of the initial portion of the curve represents the net charge-trapping slope per injected electron under the stress condition and is defined as the initial electron-trapping slope (*IETS*). During this part of the *V-t* curve, the hole trapping rate should be saturated and remain constant. The electron trap creation rate should be approximately constant. The different IETSs thus are measures of the rate of filling existing electron traps, and thus is related to the degree of damage experienced by the oxide. IETS is, therefore, directly proportional to the preexisting electron-trap density in the gate oxide. This method is believed to be superior to conventional methods where MOS capacitors are used for high frequency and quasi-static capacitance-voltage (*C-V*) measurements (15). The *C-V* measurement is time consuming and good statistics is difficult to obtain. In addition, breakdown yield and charge to breakdown, two often used methods to detect damage, are not sensitive enough to detect lower level of damage that only causes device degradation in submicron devices. Other devices, such as electrically erasable programmable read only memory (EEPROM) and metal-nitride-oxide-silicon (MNOS) (16), used to measure the voltage developed across the dielectric during plasma processing, do not measure the actual damage sustained (latent damage).

In IETS measurements, completed MOSFETs are employed. Wafers are annealed after plasma processing and before measurement to empty out the traps so that they can be filled during measurement. Gate voltage is monitored when a constant current is injected for a few seconds into the gate oxide from the gate under an electric field sufficiently high to allow electrons to be trapped in the oxide as well as the SiO_2/Si interface. The voltage variation relates directly to the net charges trapped under the Fowler-Nordheim (*FN*) current stress. Because the oxide is damaged by current stress during plasma processing, a damaged oxide is expected to have a much higher density of charge traps. An increase in the oxide's charge trapping rate at a given stress field is an indication of damage. Thus, instead of stressing and measuring separately, the voltage–time method simultaneously stresses and measures the electron traps in the oxide. Depending on injection level (17), hole traps are saturated rapidly lowering the gate voltage and once electron trapping dominates gate voltage increases (18) (rather slowly). The IETS is shown in Fig. 1(a) for the gate-injection case and Fig. 1(b) for the substrate-injection case. IETS represents the net electron trapping, which is initially dominated by the filling of existing empty electron traps per injected electron under either stress conditions. As we continue to stress the oxide, the IETS will decrease and eventually the oxide becomes saturated (19). Immediately after the current stress, trapped holes and trapped electrons near the interfaces start to detrap rapidly. It is therefore essential to measure the transistor characteristics such as threshold voltage and transconductance immediately after the current stress, maintaining the delay between stress and measurement to monitor the difference between a damaged device and a nondamaged device. The difference between damaged and nondamaged devices is more clearly detected with a higher stress level because the difference comes from the product of current density and electron-trap density.

Device Fabrication

Wafers were processed up to metal 1 using a 0.35 μm CMOS technology that uses a twin-tub process on a p-type silicon wafer. The transistors had a physical gate length of 0.40 μm and a width of 6.2 μm. The gate oxide was 80 Å thick. Plasma charging damage to wafers was accomplished by subjecting the wafer to the "power lift" step of a plasma-enhanced deposition, plasma enhanced tetraethylorthosilicate (*PETEOS*). The "power lift" is an oxygen plasma treatment designed to neutralize residual charges in the wafer after a dielectric deposition step. No deposition was involved in the power lift step. The wafers were annealed in forming gas (400°C, 30 min) before electrical measurement. Initial transistor parameters such as threshold voltage (V_t) and transconductance (g_m) before stress were very uniform across the wafer. Only n-MOS transistors with an antenna ratio of 2250:1 (probe pad to gate area ratio) were used in this study. Identical transistor pairs located within 100 μm of each other are used for comparing hot-carrier stress and constant current stress. At such close proximity, the plasma charging can be considered identical for each pair. Initial electron-trapping slopes (14) were extracted from the voltage curve of constant 400 mA/cm^2 stress, which lasted 1.5 s for each transistor using the gate-injection mode. ΔV_t is the difference between the V_t shift obtained from the before and after the current stress was applied. Poststress transistor measurements were carried out at fixed delay in an automated setup. The parameter g_m was defined at a drain voltage $V_D = 0.05$ V. Hot-carrier aging was done at the peak substrate current condition, namely, 5.5 V on the drain and 2.2 V on the gate for n-channel transistors. The value of 10% peak linear g_m degradation is the criteria for the lifetime. Subthreshold slopes were measured before and immediately after the constant current stress was applied. The poststress measurement of drain-current noise was, on the other hand, done with at least 24 h delay to allow sufficient relaxation of the trapped charges. The saturated drain-current noise was measured instead of the linear drain current noise to reduce the influence of V_t variation due to hole detrapping after FN stress. Approximately 40 devices were measured around the wafer.

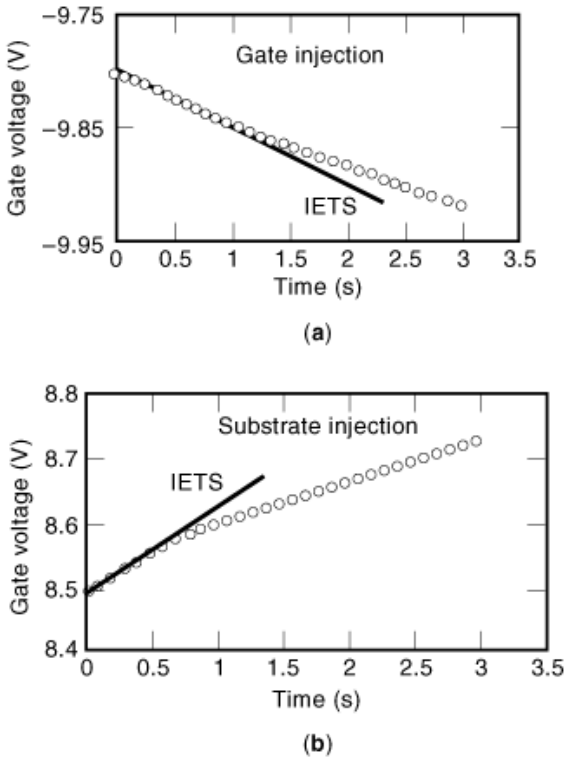

Fig. 1. The slope of initial portion of the curve of gate voltage as a function of time shows the initial electron-trapping slope (IETS). (a) Gate-injection mode. (b) Substrate-injection mode.

Polarity Dependence

Figure 2 shows the map of measured IETS of n-channel devices in a wafer. There are two badly damaged regions (areas with high IETSs). One is in the middle (slightly off center) of the wafer and the other at the perimeter around the wafer. Between the two regions there is a ring of minimum damage. Since the charging plasma is a parallel-plate discharge, it is unlikely that the plasma would have a ring-shaped potential minimum in the middle. This nature of the plasma-damage distribution, therefore, can be explained by evaluating the behavior of a floating conductor in the plasma. Upon exposure to plasma, both the wafer surface and the substrate acquire a dc floating potential with respect to the plasma potential because of the vast mobility difference between ions and electrons that are streaming to the surface (7). This floating potential is determined by the charge-balance requirement and tracks the plasma potential. The normal attribute of a parallel-plate discharge is a high-density plasma at the center with a continuous decay toward the edge. The plasma potential, therefore, is highest at the center, and monotonically decays toward the edge of the wafer. Because the substrate is isolated from the plasma, it is floating at some potential between the maximum and the minimum of the gate potential (7).

The curve in Fig. 3 represents the IETS along the solid line in Fig. 2. Where the IETS turns around (circles in Fig. 3), the gate potential goes below the substrate potential. Right at the turning point, the IETS is at minimum, and the device is damage-free or has minimum damage as shown in Fig. 4, which is an enlargement of the circles in Fig. 3. As can be seen, the surface floating potential (gate potential) follows the

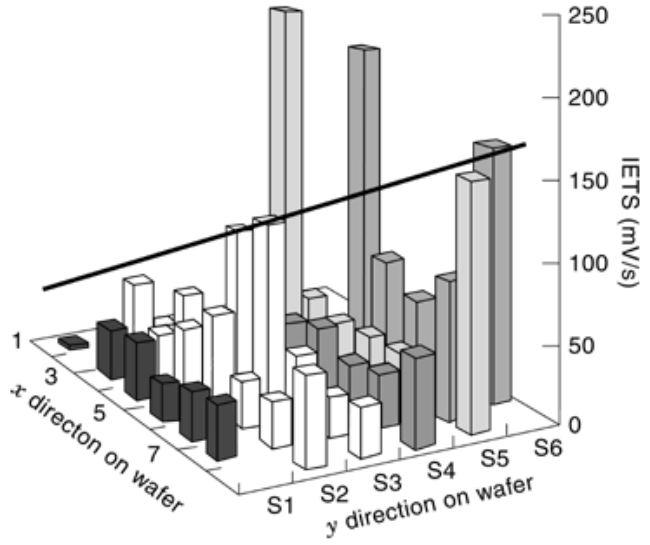

Fig. 2. Map of the IETS at 400 mA/cm^2 in mV/s for an entire wafer showing two regions of the higher-damage area separated by an area of low-damage sites for *n*-channel transistors. The center region is the wafer center and the outer region is the perimeter of wafer.

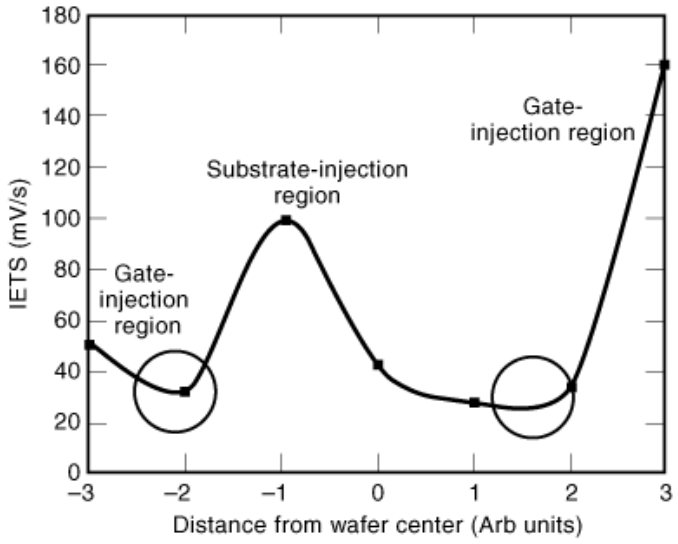

Fig. 3. The distribution of the IETS along the solid line in Fig. 2 showing the turnaround of the IETS. The circles show the area of minimum damage.

plasma potential. The substrate potential (floating) is, therefore, the midpoint of the gate potential as shown in the left-hand side of Fig. 4. From this picture, it is clear that damage in the center region is due to substrate injection and damage in the perimeter region is due to gate injection. When the potential difference between the gate and the substrate is high, tunneling starts. In the center region (right-hand side of Fig. 4), once tunneling

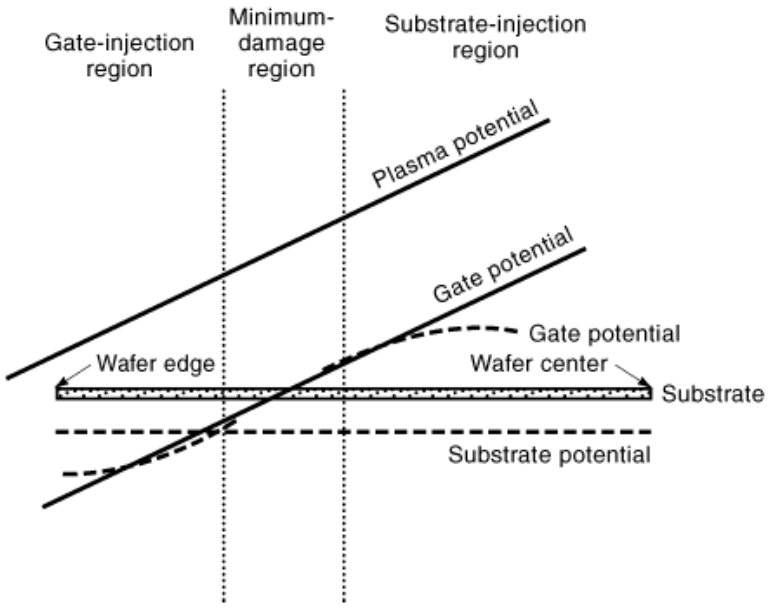

Fig. 4. The potential distribution of gate and substrate across the wafer at the turnaround point (circles in Fig. 3).

is initiated in substrate injection region the gate potential is lowered due to a disturbance in the charge balance at the gate (dotted line). On the left-hand side (Fig. 4), because of gate injection, the gate potential increases. The asymmetry of the electron current from the plasma limits the increase of the gate potential while allowing it to decrease significantly. To keep everything balanced, the substrate potential shifts more negative. Note that the minimum-damage region between the center and the perimeter region of the wafer suffers from less or no injection.

When the gate oxide is stressed by high-field injection, traps are created inside the bulk of the oxide as well as at the interface. Both positive charges and negative charges are trapped in the oxide. The distribution for negative charges inside the oxide is thought to be either uniform (20) or as a sheet near the cathode (the electrode from where electrons are injected) (21) (Fig. 5). As charge distribution is measured by determining the centroid, the electron trap distribution will form the centroid near the cathode as shown in Fig. 5. It is believed that the sheet of the negative-charge model at the cathode/oxide interface is more appropriate to results obtained in this study. The peak of the trap distribution is, therefore, near the substrate for substrate injection and near the gate for gate injection. The dotted line (Fig. 5) is the distribution during current injection while the solid line is the distribution after the current injection is stopped and after some charges have detrapped. The electron trap distribution should be the same as the negative-charge distribution during current injection.

Another expression of IETS is dV_g/dt of the voltage curve during current stress, and V_g is affected only by initial charges trapped within the oxide. Therefore, ΔV_g is given by

$$\Delta V_g = \frac{q(t_{ox} - x)}{\epsilon_{ox}},$$

where q is the electron charge, x is the location of the charge centroid in the oxide measured from the gate, ϵ_{ox} is the oxide permitivity, and t_{ox} is the oxide thickness. The IETS is more sensitive to charge traps that are

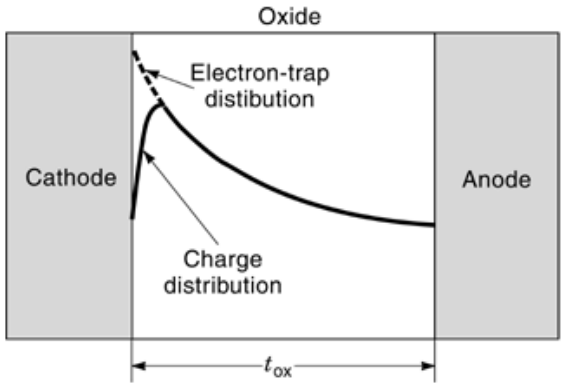

Fig. 5. Electron-trap distribution in the oxide after high-field stress peaks near the cathode.

located near the gate. The n-channel transistor threshold voltage shift ΔV_t, however, is given by

$$\Delta V_t = \frac{qx}{\epsilon_{ox}},$$

ΔV_t is therefore more sensitive to charges trapped near the SiO_2/Si interface. Figure 6 shows the relationship between the IETS and ΔV_t for both regions. For n-channel transistors as shown in Fig. 6, the ΔV_t at the center region clearly decreases more quickly with increasing IETS than the ΔV_t in the perimeter region (dotted line). Note that it is normal for the n-channel ΔV_t to decrease with increasing damage (8). The mechanism responsible for this behavior is, in low-damage devices, a negative threshold voltage shift, indicating positive charge buildup due to hole trapping, making ΔV_t a maximum. In damaged devices, assuming negligible hole trap generation, the positive charge is compensated due to electron trapping and thus ΔV_t decreases with increasing damage. Since we expect the center region to have substrate injection during plasma charging, the damage-induced electron traps must concentrate near the SiO_2/Si interface (the cathode). Electron traps near that interface have a small effect on the IETS but a maximum impact on ΔV_t, consistent with the observed relation. For the perimeter region, it is exactly the opposite. Here, gate injection during plasma charging induces electron traps near the gate (the cathode in this case). The result is a much smaller ΔV_t decrease for the same IETS increase. These results lend further support to the argument that the current-injection direction during plasma charging changed sign from the center to the edge of the wafer. It confirmed the assignment of injection direction. It further supports the electron-trap distribution model shown in Fig. 5. From the slopes of the two linear fits in Fig. 6, the location of the charge centroid can be obtained. For the gate-injection case (outer region), the charge centroid is located at 17.6 Å$\pm$3.5 Å from the gate. For the substrate-injection case (center), the charge centroid is located at 22.5 Å$\pm$3.5 Å from the substrate. The polarity dependence is symmetric to within experimental uncertainty. Note that this is the charge centroid of trapped electrons only. Hole and interface-state contributions are automatically excluded by this measurement method.

Figure 7 shows the shift in the subthreshold swing (ΔS) as a function of the IETS. In the substrate-injection region damage increases more rapidly than in the gate-injection region. An identical IETS dependence is observed of the threshold voltage shift and shift in subthreshold swing. As the MOSFET parameters correlate with each other through interface states and oxide traps near the interface, the shift in the subthreshold swing also confirms the direction of current injection and larger influence of substrate injection on plasma charging damage as the charge centroid is near the Si/SiO_2 interface.

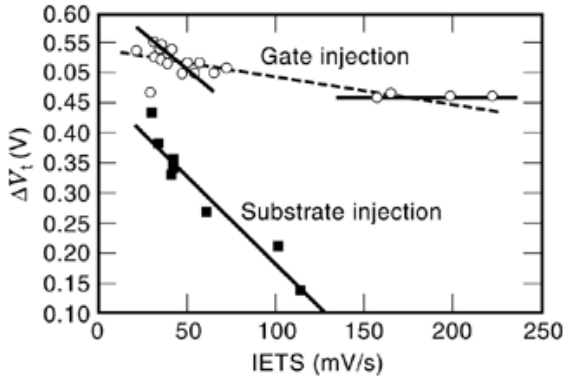

Fig. 6. V_t shift after current stress versus the IETS. Solid squares are for the center region while open circles are for the perimeter sites for *n*-channel transistors.

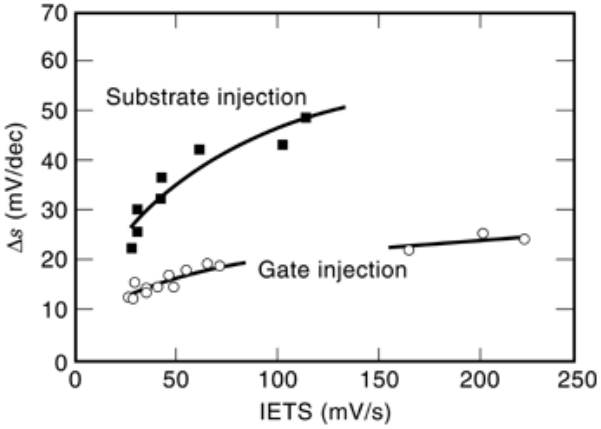

Fig. 7. Shift in the subthreshold swing after the constant current stress versus the IETS in substrate-injection (solid rectangles) and gate-injection (open circles) regions.

It was reported earlier (8) that the hot-carrier lifetime decreases exponentially with increasing amount of damage or increasing pre-existing electron-trap density in the gate oxide. This can be interpreted as, given a hot-carrier injection rate, more carriers are trapped per unit time when the pre-existing electron-trap density is higher. Such interpretation implies that the hot-carrier-induced degradation mechanism for a plasma-damaged gate oxide differs from the nominally good gate oxide, which is degraded by interface trap generation. This is reasonable because filling of pre-existing traps are more efficient or requires lower activation energy than creating interface traps. Figure 8 shows the relationships between the hot-carrier lifetime and the IETS for transistors with a single antenna ratio value for both gate-injection and substrate injection regions. For the center region (substrate injection), an exponential decay of hot-carrier lifetime with increasing IETS is evident, confirming the behavior above for different antenna ratios. For the perimeter region, other than the initial decay at low damage, the hot-carrier lifetime remains constant as damage increases. We believe the polarity dependence of plasma charging is the reason for finding varying correlations (10, 11). If the current flow is due to gate injection, there is no correlation, whereas if the current flow is due to substrate injection, there is an exponential correlation. The result in Fig. 8 also supports our interpretation that if many pre-existing electron

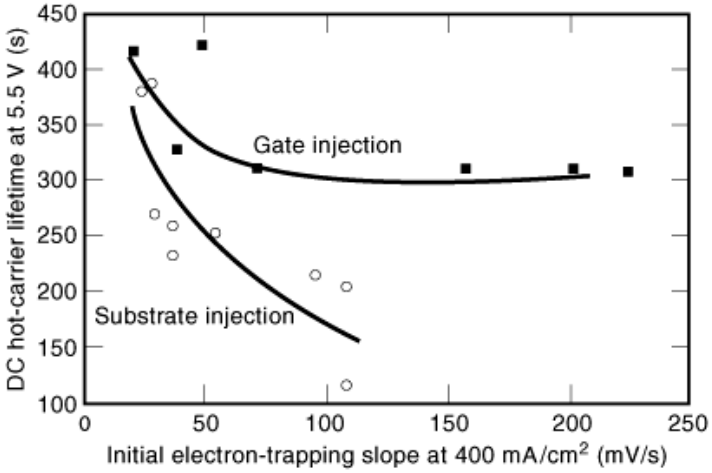

Fig. 8. Direct-current hot-carrier lifetime versus the IETS of n-channel transistors for the two higher-damage regions of the wafer (one antenna ratio). Solid squares are for the perimeter and open circles are for the center.

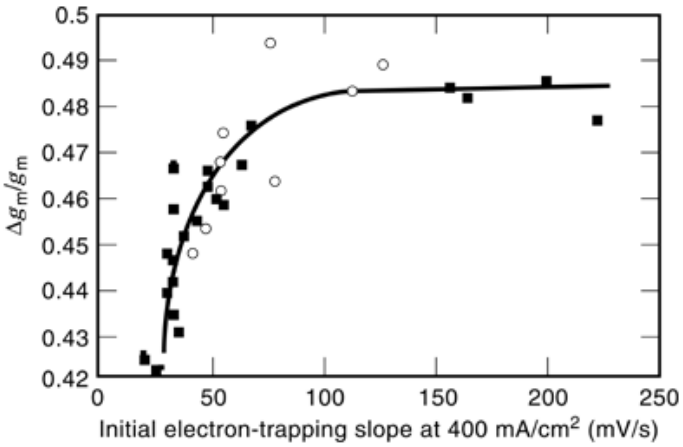

Fig. 9. Degradation of g_m due to current stress versus the IETS for both regions. Solid squares are for the perimeter region. Open circles are for center region. The curve is just a visual guide.

traps exist near the SiO_2/Si interface, then it is easier to fill these traps with the injected hot carriers than to depassivate interface states. It is interesting that the perimeter region initially shows a rapid drop in lifetime with damage and then saturates. It is believed that this initial drop is due to the effect of source and drain junction bias, which will be discussed later.

The $\Delta g_m/g_m$ after current stress, for n-MOSFETs saturate at about the same IETS (Fig. 9) as the hot-carrier lifetime in the perimeter region. The solid squares in Fig. 9 are for the perimeter region, whereas open circles represent the center region. For gate-injection IETS is mostly insensitive to the trap states at the Si–SiO_2 interface. Therefore, Δg_m does not distinguish the two regions for n-MOSFETs. Therefore, all the data fit the same trend.

Figure 10 shows the prestress integrated spectral density S_{tot} (from 10 Hz to 100 kHz) for the output current noise (representing $1/f$ noise) normalized to drain current I_D (referred to as noise from now on) behavior

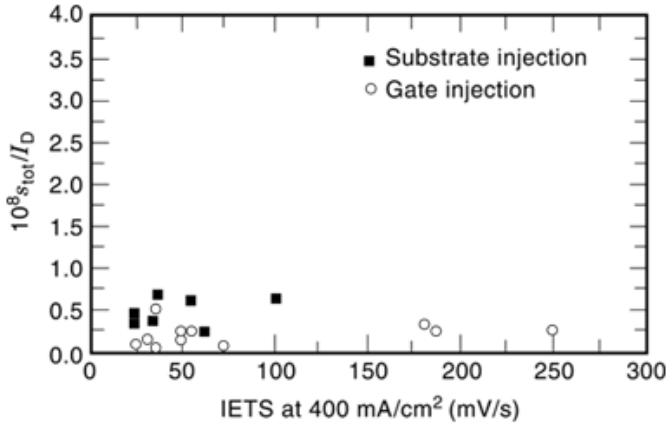

Fig. 10. Prestress integrated spectral density S_{tot} (from 10 Hz to 100 kHz) for the output current noise normalized to drain current I_D versus the IETS for both injection types.

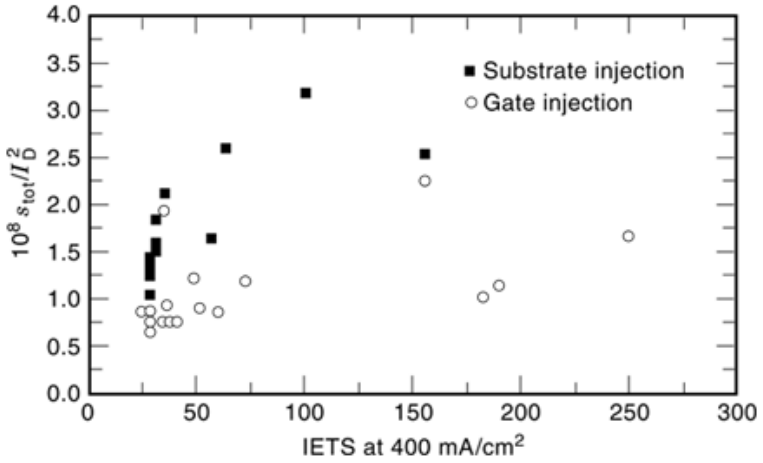

Fig. 11. Poststress integrated spectral density S_{tot} (from 10 Hz to 100 kHz) for the output current noise normalized to drain current I_D versus the IETS for both injection types.

for both injection groups as a function of damage. No damage dependency is evident. This apparent contradiction with previous studies can be resolved by realizing that most previous studies were done without forming-gas anneal after charging damage (22, 23). Since forming-gas anneal is standard in processing, degradations that can be removed by it are not a concern. It is well known that damage can be hidden by forming-gas anneal and can be revealed by stressing the damaged devices. Figure 11 shows the poststress noise behavior of the two injection groups. For both groups, the integrated noise spectral density increases linearly with damage. The slope of increase (i.e., sensitivity), however, is more than an order of magnitude higher for the substrate-injection case than the gate-injection case.

One of the mechanisms causing low-frequency output noise in MOSFETs is carrier-number fluctuation in the channel due to trapping and detrapping of electrons at or near the SiO_2/channel interface. Only traps near quasi-Fermi-level can contribute to the drain-current noise. The much higher noise sensitivity observed for the substrate-injection group is consistent with the picture of the electron-trap density peaking at or near

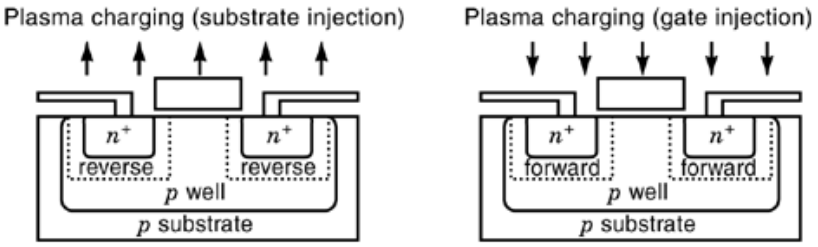

Fig. 12. Cross sections of an n-MOSFET with source and drain junctions reverse-biased during substrate injection and forward-biased during gate injection.

the cathode. Traps too close to the interface fluctuate too frequently to be detected, whereas traps located far from the Si/SiO_2 interface fluctuate too slowly. Because the deviation for the substrate-injection case is much higher, it is possible that a higher trap density exists near the SiO_2/channel interface than the gate-injection case. Interestingly, the deviation for the gate-injection case is not zero. This suggests that although the trap density is higher near the cathode, it does extend all the way to the anode.

From noise measurements and transistor subthreshold swing observations, the question whether all interface states are the same still remains controversial. Radiation-damage studies have long proposed a model of interface states with silicon dangling bonds at the SiO_2/Si interface (P_b centers). There is a maximum density of dangling bonds due to the lattice mismatch between SiO_2 and silicon. The change in interface state density is merely passivation and depassivation of these P_b centers by hydrogen (24). Because only one type of interface state exists and because it can be passivated by annealing in forming gas, there cannot be any damage effect on the interface-state density after anneal.

Shin and Hu (5), however, reported that charging damage does create interface states that more readily reappear under stress. Our result suggests that the damage-related interface states are responsible for the increase in $\Delta g_m/g_m$. Cartier, Stathis, and Buchanan (25) showed that P_b centers cannot account for all the interface states. Stathis and Cartier (26) showed that the two centers P_{b0} and P_{b1}, found in the $Si(100)/SiO_2$ interface do not behave the same, both in terms of depassivation and annealing. The normally observed interface states are predominantly P_{b0} centers. The damage-related interface states are probably P_{b1} centers. This behavior will be investigated later when deuterium incorporation is discussed.

Effect of Source and Drain Junctions. In this section the impact of source and drain (S/D) junctions of a MOSFET on plasma damage due to polarity is discussed. We now know that during plasma processing the injection process can proceed via either substrate or gate depending on the potential distribution at the wafer surface. Protection diodes, typically connected to the gate of the transistor, are used to limit this current through the thin oxide (5, 27). A very small forward-biased diode can shunt a significant amount of current and is effective. The effectiveness of the reverse-biased protection diode, on the other hand, is questionable even if reverse-leakage current and light-enhanced current due to plasma illumination are taken into account (5), as it depends on the magnitude of plasma current relative to that of the diode current. Use of protection diodes is possible after source and drain junctions are formed. The potential developed at the source and drain junctions of such a transistor during plasma etching of metal 1 (*M1*) can have significant impact on device damage. A wafer-charging experiment shows that the gate oxide could encounter greater damage if the source and drain junctions are reverse-biased compared with the damage encountered if they are forward-biased. Along the solid line shown in Fig. 3 the source and drain junctions are reverse-biased in the substrate-injection region and are forward-biased in the gate-injection region (Fig. 12). Devices close to the minimum-damage area (Fig. 2) in the gate-injection region could have their source and drain junctions remain reverse-biased until the potential is sufficiently negative, depending on the antenna to junction-area ratio.

Figure 6 shows the decrease of ΔV_t for the substrate-injection region with an increase in IETS. This occurs because the source and junctions remain reverse-biased during substrate-injection mode and the reverse leakage current (or photoenhanced reverse leakage current) does not reduce the oxide damage. The ΔV_t value in the perimeter region (two solid lines), however, initially starts to decrease and later becomes independent of the IETS. Once the source and drain junctions are forward-biased during gate injection, the substrate potential increases, reducing the potential across the gate oxide (7) rather than shunting the FN current. This mechanism confirms the injection type in the center region as well as in the perimeter region and makes the device independent of damage during gate injection in an n-MOS transistor due to forward-biased S/D junctions.

In Fig. 8 for the perimeter region, the initial decay of the hot-carrier lifetime at low damage confirms the earlier prediction of reverse-biased source and drain junctions close to the minimum damage ring. The hot-carrier lifetime remains constant as the drain and source junctions become forward-biased, reducing damage in the gate oxide.

In the actual process, with the use of advanced reactors and careful selection of process conditions both gate injection and substrate injection may not exist at the same time. However, substrate injection will continue to be the major contributor to charging damage. It is, therefore, important to consider the conductor lines (antenna) connected to source and drain terminals in addition to the gate terminal, which is being reviewed extensively in the literature.

Plasma Damage Due to Reverse-Biased Voltage by Source and Drain Antennas. It is known that plasma-charge-damage effects can be enhanced or exacerbated depending upon the relative direction (from center to edge of the wafer), distance from the gate, and size of antennas connected to the gate, source, drain, and substrate (28, 29). The floating potentials generated due to circuit elements (antennas) at these terminals can induce significant damage even with minimal nonuniformity in the plasma. It is of utmost importance to study the interaction of source and drain (S/D) junctions of a transistor with the charging source to further understand charging damage caused during the metal etching and subsequent dielectric deposition. This section discusses the possible effect of the floating potential at the S/D junctions of a transistor during high-field electron injection. To estimate the effect of antennas connected to S/D terminals during the plasma-processing condition, a reverse-biased potential was applied at the S/D junctions during electrical stress.

Particular n-MOS transistors with a physical gate length of 0.35 μm and a gate oxide thickness of 60 Å were used for this study. In a typical injection case, when a transistor is used to evaluate the gate oxide integrity, the source, drain, and substrate are connected together to ground [Fig. 13(a)]. In this work, 0 V, 2 V, and 4 V were applied at source and drain terminals [Fig. 13(b)] with the substrate grounded where the 0 V case is a typical injection mode [Fig. 13(a)]. The IETSs were obtained from the voltage curve.

Figure 14 shows the variation of the threshold voltage shift (ΔV_t) with IETS for both gate injection and substrate injection. For gate injection the variation of ΔV_t is minimal (tight distribution). For substrate injection as the reverse-biased voltage at source and drain increases, ΔV_t increases with IETS. It is known that for a given oxide, hole trapping depends on level of current stress while electron trapping increases with damage. As can be seen from Fig. 14, devices subjected to gate injection have lower IETS and lower ΔV_t, which indicate decreased damage (electron traps) and a reduced number of trapped holes. A higher threshold voltage prior to stress (not shown) than the threshold voltage after stress for the gate-injection case was also observed. This indicates that hole trapping is dominant and charge buildup from electron trapping is negligible (30). When source and drain junctions are at reverse-biased floating voltages of 0 V, 2 V, and 4 V, the high-field zones of gate-to-drain and gate-to-source regions in localized overlap areas dominate the stress. Therefore, a significant portion of stress current is drained through the high-field zones at source and drain junctions, resulting in a small current density in the oxide–semiconductor region. This small current density results in almost constant hole trapping and constant threshold voltage shifts.

On the other hand, for substrate injection, the experimentally observed threshold voltage prior to stress is lower than threshold voltage after stress, indicating dominant electron trapping. Moreover, the electron

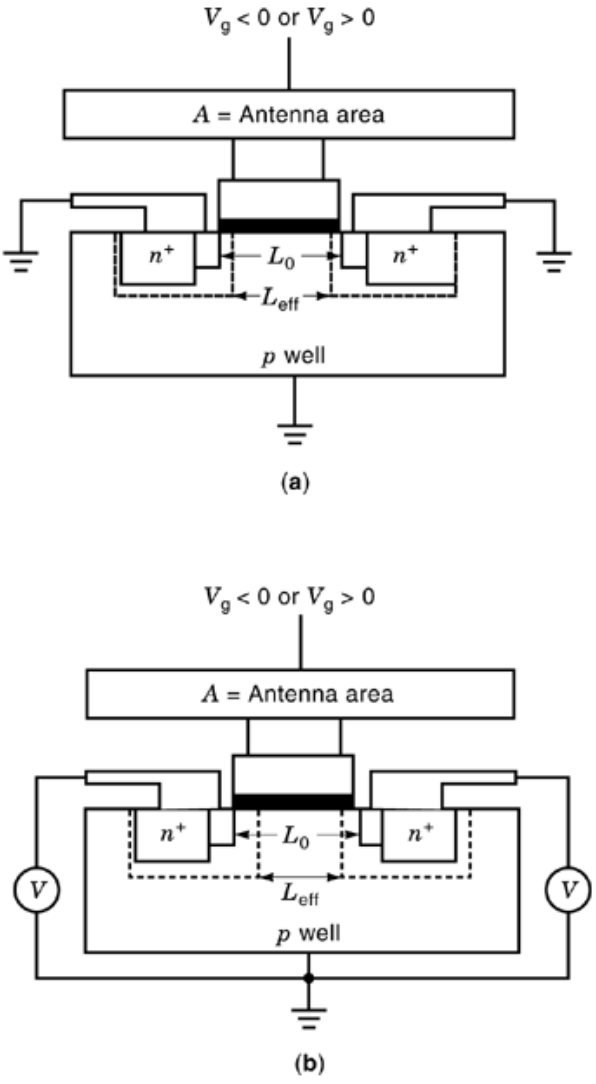

Fig. 13. Cross section of an n-MOSFET (a) in a typical stressing condition and (b) with source and drain terminals at reverse-biased floating voltage.

trapping depends upon oxide damage and the electron-trapping cross section. As the reverse-biased voltage is increased, depletion regions are formed on the source and drain junctions, thereby reducing the effective channel length and increasing the effective current density through the oxide. The scaling of stress current density effectively increases the electron-capture probability, and therefore the electron-capture cross section increases with reverse-biased voltage, which results in higher threshold voltage degradation. A significant difference in plasma damage due to the stress polarity difference has already been discussed. The intensity of damage can increase in the substrate-injection case when the source and drain junctions have a significant floating potential depending on plasma potential distribution on the wafer, which makes the junctions reverse-biased.

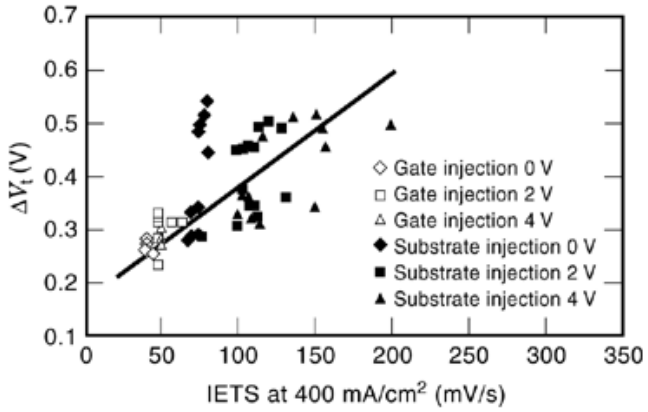

Fig. 14. Threshold voltage shift due to current stress as a function of the IETS for both gate-injection and substrate-injection modes at different source/drain floating potentials.

During plasma processing, the capacitive coupling to devices (wafer surface) and substrate is such that the capacitance of the substrate is higher than the device capacitances. Therefore, the substrate potential lags the gate and source/drain potentials. In the case of substrate injection, therefore, even if gate, source, and drain antennas are located at the same potential, damage can still exist for n-MOS transistors if the source/drain junctions are reverse-biased and the floating gate potential is above the substrate potential. Aum *et al.* (29) found no damage even if the gate, source, and drain antennas are at the same potential because the substrate potential was strongly influenced by source and drain potentials. This is possible when the junctions are forward-biased during gate injection for n-MOS transistors and during substrate injection for p-MOS transistors. Our results suggest that when the high-field injection process is initiated, a reverse-biased source/drain junction will worsen the charge damage by enhancing both electron and hole trap creation in the oxide.

It is known that the oxide charging current produced by plasma processing increases with the "antenna" size of the device structure. The antenna ratio is defined as the ratio of the area of various structures connected to the gate of the transistor (antenna) to the area of the gate. Figure 15 shows the effective antenna ratio as a function of reverse-biased voltage at source and drain junctions on n-MOS transistors with gate lengths of 0.18 μm, 0.25 μm, 0.30 μm, and 0.35 μm, with initial antenna ratios of 20,000:1, 8000:1, 5500:1, and 4000:1, respectively. If L_0 is the as-drawn length of a transistor (Fig. 13), then with depletion regions formed due to reverse-biased voltages at source and drain junctions the effective channel length L_{eff} is given by $L_{\text{eff}} = L_0 - (W_S + W_D)$ where W_S and W_D are the drain and source depletion lengths given by

$$W_S = W_D = \sqrt{\frac{2\epsilon_s(V_{bi} + V_{D,S} - 2kT/q)}{qN_B}} = L_D\sqrt{2[q/kT(V_{bi} + V_{D,S}) - 2]}$$

where

$$L_D = \sqrt{\frac{\epsilon_s kT}{q^2 N_B}}$$

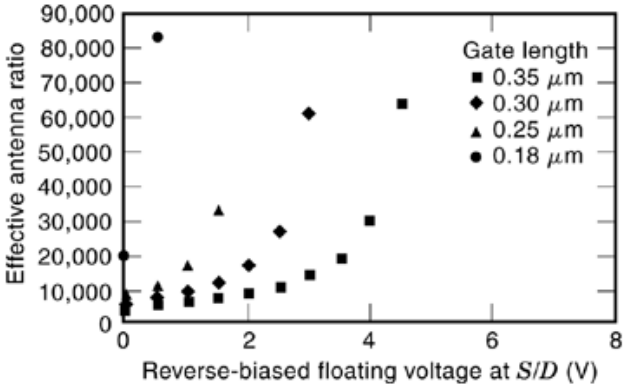

Fig. 15. Effective antenna ratio as a function of reverse-biased floating potentials at source and drain terminals of transistors with two different gate lengths.

is the Debye length. For a channel doping of 2.5×10^{17} cm^{-3} with a Debye length of 80 Å and a lightly doped drain (*LDD*) doping of 1.5×10^{18} cm^{-3}, the effective channel length was calculated. It can be seen that the effective antenna ratio increases with reverse-biased source/drain potential. This is in accord with the expected behavior in threshold voltage degradation for the substrate-injection case. In addition, the increase in effective antenna ratio will also prevail for scaled CMOS devices.

Figure 16 shows the variation of $\Delta g_m/g_m$ as a function of IETS for different reverse-biased voltages. For the gate-injection mode $\Delta g_m/g_m$ is independent of reverse-biased voltage and for the substrate-injection mode it decreases with reverse-biased voltage. Note that $\Delta g_m/g_m$ for the gate-injection mode is higher than that for the substrate-injection mode. If this is dominated by a damage-related interface, then these interface states must be directly proportional to damage-related bulk electron traps or near-interface electron traps. The basic difference between gate injection and substrate injection is that the impact-ionization-generated electron-hole pairs for the gate-injection mode occur at the Si/SiO_2 interface and play an important role in the interface-state generation. For the substrate-injection mode the electron-hole pairs occur in the heavily doped polysilicon interface and quickly recombine (30, 31). For the gate-injection mode, as the reverse-biased voltage is increased, the number of interface states or near-interface electron-trap generation at Si/SiO_2 interface is almost constant. For the substrate-injection mode, as the reverse-biased voltage is increased, the decrease in $\Delta g_m/g_m$ indicates suppression of the interface trap or near-interface trap generation at Si/SiO_2. This explains the mechanism of the reduction in channel length because of the formation of depletion regions on the source and drain junctions. The effective reduction in gate length reduces the interface-state density or near-interface electron traps during high-field injection.

The variation of oxide field at breakdown and charge to breakdown as a function of reverse-biased voltage is shown in Figs. 17 and 18, respectively. It can be seen that the oxide field at breakdown is independent of the reverse-biased voltage for both gate injection and substrate injection. Moreover, the value of the oxide field at breakdown for gate injection is higher than that for substrate injection. This can be attributed to the fact that for gate injection, hole trapping occurs and results in lower damage (electron traps); therefore a higher value of the oxide field is required to cause breakdown. For substrate injection electron trapping occurs and results in higher damages; therefore a lower value of the oxide field is required to cause breakdown.

The charge to breakdown (Fig. 18) decreases with reverse-biased voltage for gate injection and increases for substrate injection. The breakdown mechanism can be explained with the help of an energy-band diagram. The energy-band diagrams of *n*-MOSFETs for gate injection and substrate injection are shown in Figs. 19 and 20, respectively. For gate injection the electrons tunnel from the gate into the conduction band of the oxide and

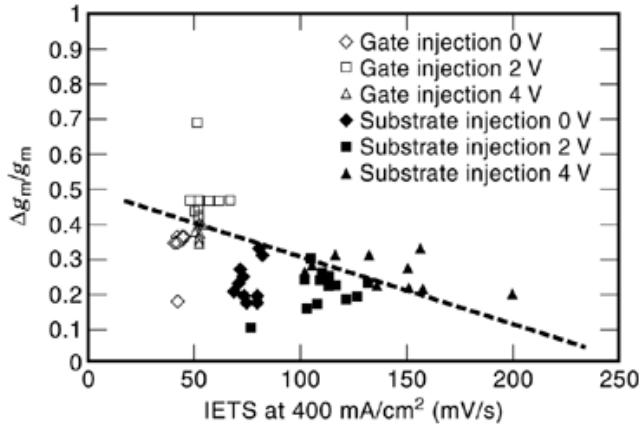

Fig. 16. Values of $\Delta g_m/g_m$ due to current stress as a function of the IETS for both gate-injection and substrate-injection modes at different source/drain floating potentials.

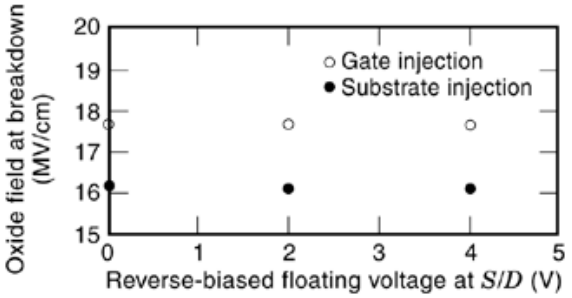

Fig. 17. Oxide breakdown electric field as a function of reverse-biased voltage at source and drain terminals for both gate-injection and substrate injection modes.

gain energy from the electric field. High-field zones at source and drain junctions due to reverse-biased voltage further accelerate a significant portion of these electrons. The acceleration factor increases with reverse-biased voltages at source and drain junctions. All these electrons can cause electron-hole pair production. In other words, the electron-hole pair production in the oxide is directly proportional to the reverse-biased voltage at source and drain junctions. Electrons move toward the substrate and holes move toward the gate. There is a great chance for these holes to be trapped at the defect sites near the gate. The band diagram is altered by the trapped holes as shown by dotted lines in Fig. 19. This trapping of holes increases the internal electric field between the hole-trapping center and gate. As a result, the barrier for electrons tunneling from gate into oxide is reduced and more and more electrons tunnel into the oxide. This process ultimately leads to breakdown due to positive feedback. The band-edge distortion depends on the degree of hole trapping. The degree of hole trapping in turn depends upon the stress current density and the electron acceleration factor in the oxide. Therefore, as the reverse-biased voltage at source and drain junctions increases, the electron acceleration factor and hence the hole trapping increase. The increase in hole trapping with reverse-biased voltage reduces the barrier height for electrons and more and more electrons tunnel into the oxide. Therefore, the charge to breakdown must decrease with reverse-biased voltage in order to keep the stress current constant.

On the other hand, for the substrate-injection mode electrons tunnel into the oxide conduction band from the substrate and gain energy from the electric field. It is to be noted that the acceleration factor for substrate

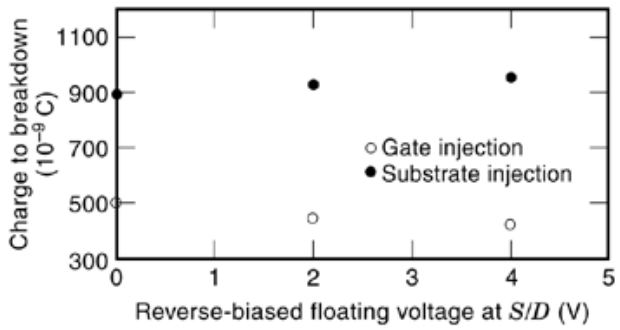

Fig. 18. Charge to breakdown as a function of reverse-biased voltage at source and drain terminals for both gate-injection and substrate-injection modes.

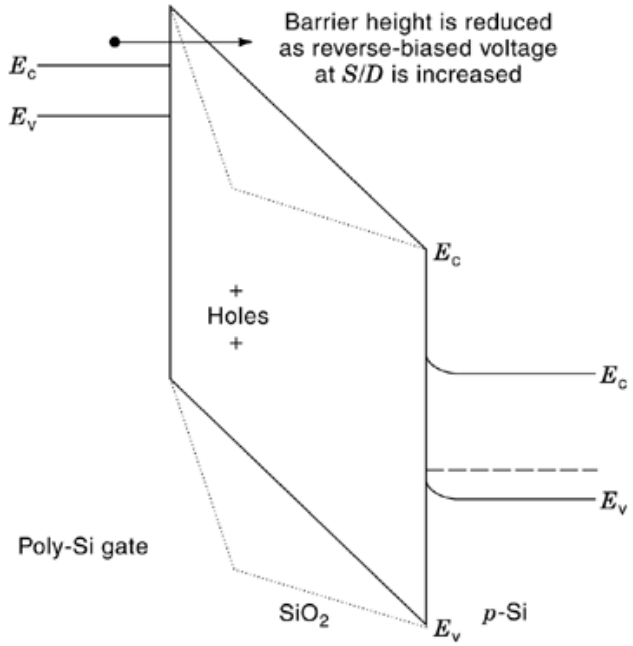

Fig. 19. Energy-band diagram for the gate-injection mode, the barrier height for tunneling electrons is reduced as the reverse-biased voltage is increased.

injection is smaller than the acceleration factor for gate injection because high-field zones at source and drain junctions do not accelerate these electrons. These electrons can produce electron-hole pairs. It is to be noted that in substrate injection the electron-hole pair production is less than that in the gate-injection case. The electrons move toward the gate and holes move toward the substrate. In this case the electrons are trapped in the oxide. The band diagram is altered by the trapped electrons as shown by dotted lines in Fig. 20. This trapping of electrons decreases the internal electric field between the electron-trapping center and substrate. As a result, the barrier for electrons tunneling from the substrate into the oxide is increased and less and less electrons tunnel into the oxide. In order to sustain a constant current, the gate voltage must increase sufficiently to overcome the potential barrier. Once the gate voltage is increased, the critical oxide electric field

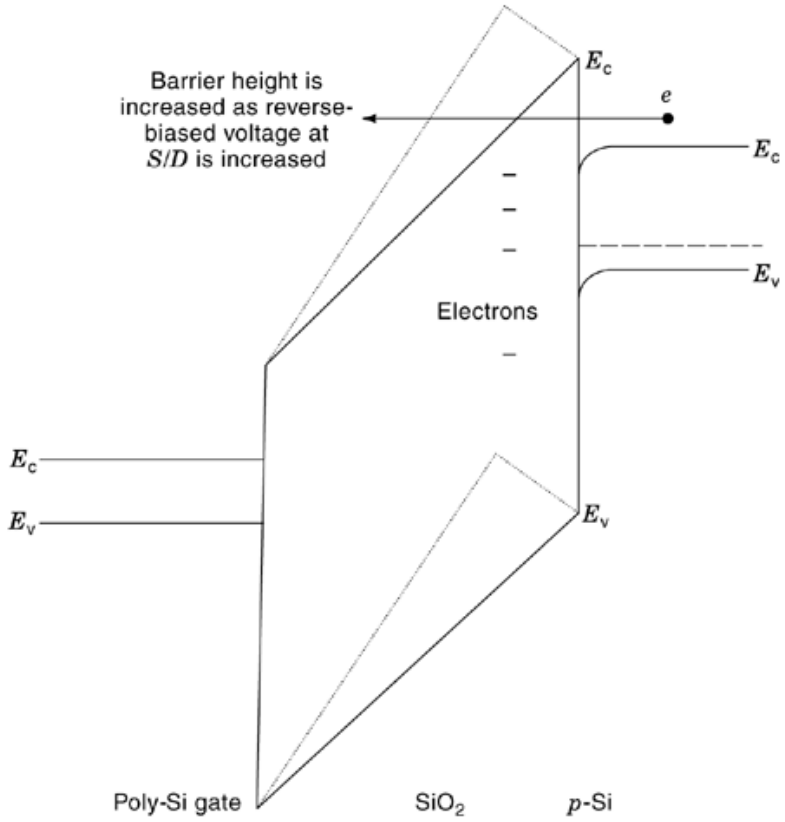

Fig. 20. Energy-band diagram for the substrate-injection mode, the barrier height for tunneling electrons is increased as the reverse-biased voltage is increased.

for breakdown is achieved by positive feedback. The band-edge distortion depends on the degree of electron trapping. The degree of electron trapping in turn depends upon the stress current density. Therefore, as the reverse-biased voltage at source and drain junctions increases, the effective current density increases, and hence the electron trapping increases. The increase in electron trapping with reverse-biased voltage increases the barrier height for electrons and fewer and fewer electrons tunnel into oxide. Therefore, the charge to breakdown must increase with reverse-biased voltage to keep the stress current constant. It is therefore clear that during an actual plasma-processing condition if a potential is developed at the antenna-connected source and drain terminals, then the device will encounter enhanced adverse effects from the antenna connected to the gate.

Immunity from Plasma Damage

Continued scaling of MOS devices into the deep submicron regime requires very thin gate oxides. Thin gate oxide reliability is therefore very important since plasma damage does not scale with oxide thickness. Improving the gate oxide's immunity to plasma-charging damage is becoming a high-priority issue. Much work has centered on the effect of incorporated nitrogen (32) and deuterium (33) to improve gate oxide reliability.

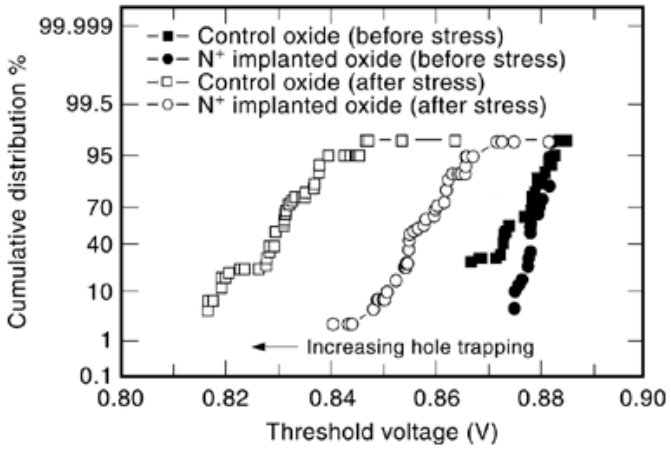

Fig. 21. Cumulative plot of threshold voltage in n-MOS devices with control and nitrogen-implanted oxides before and after FN stress. The shift in threshold voltage shows that the nitrogen-implanted oxide suffers from less hole trapping compared to the control oxide.

Gate Oxide Grown on a Nitrogen-Implanted Substrate. A recently introduced method of incorporating nitrogen into the gate oxide is implanting N into the substrate before gate oxide growth (34). In this section, a study of improvement of plasma-damage immunity using this method of nitrogen incorporation is described (35). In order to gauge the sensitivity of the improvement on a N implant, this work reports the very light dose of $2\times10^{13}/\text{cm}^2$ case only. At this dose level, the gate oxide growth rate was not affected (within the 3% measurement uncertainty) by the nitrogen (34) and thus allows very close comparison.

This work used fully processed n-MOS transistors up to metal-1 using 0.25 μm CMOS technology. First N^+ was implanted into the (100) Si substrates at 25 keV through a 200 Å sacrificial oxide. After the sacrificial oxide was etched the gate oxide was grown in dry O_2 at 800°C. Approximately 3 at.% to 4 at.% of nitrogen was incorporated into the oxide. The oxide thickness for 25 min oxidation was 52 Å for (a) no N^+ ion implant (control oxide) and (b) with $2\times10^{13}/\text{cm}^2$ N^+ ion implant. The gate oxide thickness was measured by multiangle ellipsometry ($\lambda = 632.8$ nm). The transistors had a physical gate length of 0.35 μm. The wafers were annealed in forming gas (400°C, 30 min) before measurement started. Initial transistor parameters such as threshold voltage (V_t) and transconductance (g_m) before stress were very uniform across the wafer. As before, V_t shift and g_m degradation were obtained from before and after current stress measurements.

Figure 21 gives the cumulative percentage distribution of devices before and after FN stress as a function of threshold voltage for both the control and nitrogen-implanted oxides. Before stress, both the oxides show a similar distribution without much of difference. After the devices were subjected to negative FN injection (electron injection from the gate), it was observed from the distribution that the devices with the control oxide suffer from a larger V_t shift (Fig. 21) compared to devices with oxides grown on a nitrogen-implanted substrate. It can be clearly seen that the V_t shift for both types of devices is negative after stress, indicating A larger positive effective charge in the oxide due to hole trapping. However, devices with the control oxide show a larger positive charge buildup (larger negative V_t shift) compared to the nitrogen-implanted oxide. With a smaller V_t shift and a smaller slope during electron trapping, devices with nitrogen-implanted oxide have a lower than expected density of trapped holes similar to most of the nitrogen-incorporated gate oxides. Therefore, nitrogen-implanted devices are less prone to plasma damage compared to devices with standard gate oxides.

Figure 22 shows the average $\Delta g_m/g_m$ value of 41 devices with the control oxide and nitrogen-implanted oxide. As expected, $\Delta g_m/g_m$ for the nitrogen-implanted oxide is lower than the control oxide after the same

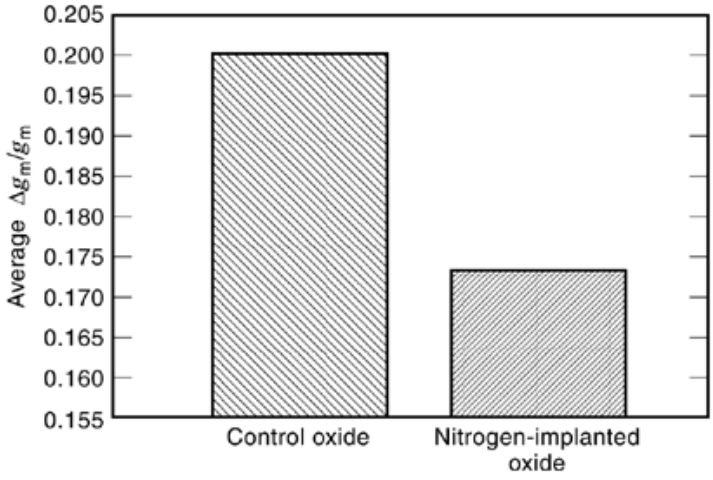

Fig. 22. The average $\Delta g_m/g_m$ values of devices with control and nitrogen-implanted oxide. Δg_m is the difference of g_m measurements taken on 41 devices, in each case before and after the FN stress.

stress. Since $\Delta g_m/g_m$ is quite sensitive to the interface-state density it is clear that nitrogen-implanted oxide has a superior Si/SiO_2 interface. A detrapping kinetic study (36) suggests that the observed $\Delta g_m/g_m$ change could be due to electron traps near interface. In addition, it is believed that the presence of nitrogen at the interface seems to reduce the acceptorlike interface states produced by weak Si–O bonds. The reduction in g_m degradation is further evidence that electron-trap generation near the interface in the nitrogen-implanted oxide is suppressed. Therefore it is confirmed that a low dose of nitrogen implant before gate oxide growth can improve the gate oxide's resistance to plasma-charging damage. Both electron trapping and hole trapping are suppressed effectively in the nitrogen-implanted oxide.

Gate Oxide Grown on a Deuterium-Implanted Substrate. It was reported that a plasma-exposed $Si–SiO_2$ interface showed improved device characteristics when subjected to deuterium sintering (33). It is known that during plasma processing silicon dioxide is exposed to electrical stress and the stress enhances the native electron-trap density in the oxide. In this report, the $Si–SiO_2$ interface was exposed to an electrical stress during the patterning of the polysilicon using reactive ion etching. Incorporating deuterium through implantation prior to gate oxide growth could enhance the resistance to plasma damage. To estimate the electron traps introduced during the above-noted plasma-processing step, MOS capacitors with 40 Å of gate oxide were subjected to a constant current stress of 200 mA/cm^2 (gate injection). The average values of the IETSs for 25 keV deuterium-implanted devices are shown in Fig. 23. There is about an order of magnitude reduction over the control wafer in electron-trap density with deuterium implantation and annealing (37). However, wafers with only deuterium implantation without any annealing also show improvement over the control sample.

To confirm the assumptions from IETS measurements, conductance method was employed to measure the interface trap (*IT*) density D_{IT}. Figure 24 shows the peak D_{IT} values for various deuterium-implanted devices measured by a conductance method at 1 MHz as a function of gate voltage. As can be seen in Fig. 24, D_{IT} decreases with deuterium-implanted samples. The 25 keV deuterium-implanted and annealed sample shows the lowest density of interface states. The improvement in D_{IT} for the 25 keV implanted and annealed sample indicates a completely different behavior of deuterium if the oxide is grown on the implanted substrate compared to annealing of bare silicon. It seems that if the implantation dose is appropriate, deuterium implantation can also enhance the gate oxide's resistance to plasma damage (38).

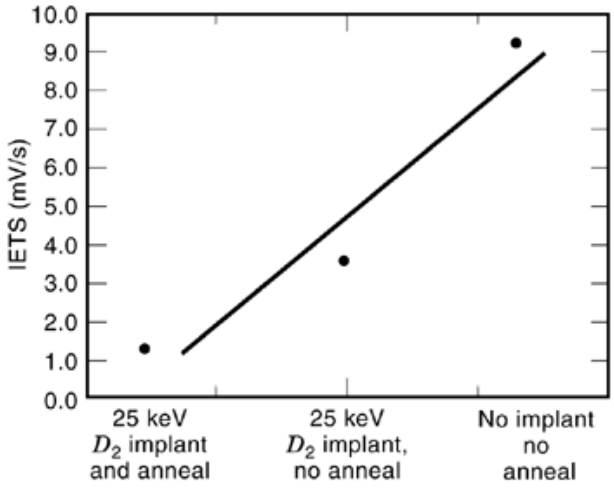

Fig. 23. The average values of the IETS for the 25 keV deuterium-implanted samples compared to the control device.

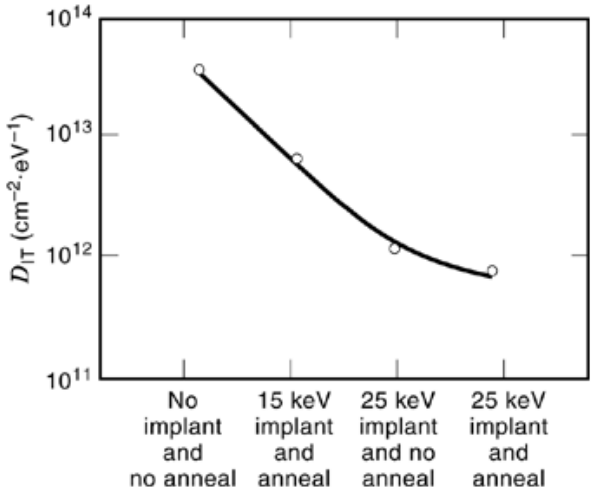

Fig. 24. Peak D_{IT} values measured by the conductance method at 1 MHz as a function of gate voltage for various devices.

Summary

It was demonstrated that the IETS, which is a measure of the preexisting electron-trap density in the gate oxide, is a good indicator of transistor reliability degradation due to plasma damage. Polarity-dependent plasma-charging damage in submicron *n*-MOSFETs was demonstrated considering significant threshold voltage and subthreshold swing variations across the wafer. Experimental observations were used to demonstrate that *n*-channel hot-carrier lifetime degradation by charging damage depends on the difference in the direction of current flow during charging damage. It was found that the MOSFET noise increase due to plasma damage is strongly dependent on the damage polarity. Data were also provided to support the notion that, after high-field stress, the distribution of electron traps is not uniform. It peaks near the cathode and thus looks like a sheet

of negative charge. The damage-induced interface states are different from normal interface states and more readily reappear under stress.

It was also shown that the gate oxide could encounter damage if the source and drain junctions are reverse-biased compared with the damage encountered if they are forward-biased. In addition, during plasma processing if a potential is developed at the antenna-connected source and drain terminals then the device will encounter an enhanced adverse effect from the antenna connected to the gate due to increase in the effective antenna ratio.

Incorporating nitrogen or deuterium through implantation prior to gate oxide growth could enhance the resistance to plasma damage. The reduction in V_t and g_m degradation is evidence that electron-trap generation near the interface in the nitrogen-implanted oxide is suppressed. Therefore, it is confirmed that a low dose of nitrogen implant before gate oxide growth can improve the gate oxide's resistance to plasma-charging damage. In the case of deuterium if the implantation dose is appropriate, deuterium implantation can also enhance gate oxide's resistance to plasma damage.

Acknowledgment

The author would like to acknowledge the help of Dr. K.P. Cheung, Dr. C.T. Liu, Dr. S. Martin, Dr. Paul Layman, and Dr. John McMacken of Bell Laboratories, Lucent Technologies for their help and providing devices and technical discussions for this work. The technical assistance of Dr. R.K. Jarwal of NJIT is also acknowledged.

BIBLIOGRAPHY

1. C. Gabriel J. McVittie How plasma etching damages thin gate oxides, *Solid State Technol.*, **35**: 81–87, 1992.
2. H. Shin *et al.* Plasma etching charge-up damage to thin oxides, *Solid State Technol.*, **36**: 29–30, 1993.
3. W. Greene J. Kruger G. Kooi Magnetron etching of polysilicon: Electrical damage *J. Vac. Sci. Technol. B*, **9**: 366–369, 1991.
4. S. Krishnan *et al.* Inductively coupled plasma (ICP) metal etch damage to 35–60 Å gate oxide, *IEDM Tech Dig.*, 731–734, 1996.
5. H. C. Shin C. Hu Thin gate oxide damage due to plasma processing, *Semicond. Sci. Technol.*, **11**: 463–473, 1996.
6. S. Fang J. McVittie Thin-oxide damage from gate charging during plasma processing, *IEEE Electron Device Lett.*, **13**: 288–290, 1992.
7. K. P. Cheung C -P. Chang Plasma-charging damage: A physical model, *J. Appl. Phys.*, **75** (9): 4415–4426, 1994.
8. K. P. Cheung A new method to monitor gate-oxide reliability degradation, 1995, *Tech. Digest, IEEE Symp. VLSI Technol.*, pp. 83–84, 1995.
9. T. B. Hook *et al.* A comparison of hot-electron and Fowler-Nordheim characterization of charging events in a 0.5 μm CMOS technology, *Proc. IEEE 1st Int. Symp. Plasma Process-Induced Damage, 1996*, pp. 164–167, 1996, North California Chapter of American Vacuum Society, Sunnyvale, CA.
10. K. R. Mistry B. J. Fishbein B. S. Doyle Effect of plasma-induced charging damage on n-channel and p-channel MOSFET hot carrier reliability, *1994 IEEE/IRPS*, pp. 42–47, 1994.
11. K. Noguchi K. Okumura The effect of plasma-induced oxide and interface degradation on hot carrier reliability, *1994 IEEE/IRPS*, pp. 232–237, 1994.
12. D. Park C. Hu Plasma charging damage on ultrathin gate oxides, *IEEE Electron Device Lett.*, **19** (1): 1–3, 1998.
13. K. K. Hung *et al.* A physics-based MOSFET noise model for for circuit simulators, *IEEE Trans. Electron Devices*, **37**: 1323–1333, 1990.
14. K. P. Cheung An efficient method for plasma-charging damage measurement, *IEEE Electron Dev. Lett.*, **15** (11): 460–462, 1994.
15. H. Shin *et al.* Plasma etching charge-up damage to thin oxides, *Solid State Technol.*, 29–30, August 1993.

16. Y. Kawamoto MOS gate insulator breakdown caused by exposure to plasma, *Proceedings of the Dry Process Symposium*, pp. 132–xxx, 1985.
17. Y. Nissan-Cohen *et al.* High field current induced-positive charge transients in SiO_2, *J. Appl. Phys.*, **54**: 5793–5800, 1983.
18. D. A. Buchanan D. J. DiMaria Interface and bulk trap generation in metal-oxide-semiconductor capacitors, *J. Appl. Phys.*, **67** (12): 7439–7452, 1990.
19. D. J. DiMaria D. Arnold E. Cartier Degradation and breakdown of silicon dioxide films on silicon, *Appl. Phys. Lett.*, **61** (19): 2329–2331, 1992.
20. D. J. Dumin *et al.* High field emission related thin oxide wearout and breakdown, *1994 IEEE/IRPS*, pp.143–153, 1994.
21. W. K. Meyer D. L. Cook Model for oxide wear out due to charge trapping, *1983 IEEE/IRPS*, pp. 242–247, 1983.
22. J. T. Hsu X. Li C. R. Viswanathan *Microelectron. Eng.*, **22**: 285, 1993.
23. Z. J. Ma H. Shin P. K. Ko C. Hu Effects of plasma charging damage on the noise performance of thin-oxide MOSFET's, *IEEE Electron Dev. Lett.*, **15**: 224–226, 1994.
24. P. M. Lenahan P. V. Dressendorfer An electron spin resonance study of radiation-induced electrically active paramagnetic centers at the Si/SiO_2 interface, *J. Appl. Phys.*, **54**: 1457–1460, 1983.
25. E. Cartier J. H. Stathis A. A. Buchanan Passivation and depassivation of silicon dangling bonds at the Si/SiO_2 interface by atomic hydrogen, *Appl. Phys. Lett.*, **63** (11): 1510–1512, 1993.
26. J. H. Stathis E. Cartier Atomic hydrogen reactions with Pb centers at the (100) Si/SiO_2 interface, *Phys. Rev. Lett.*, **72** (17): 2745–2748, 1994.
27. F. Shone *et al.* Gate oxide charging and its elimination for metal antenna capacitor and transistor in VLSI CMOS double layer metal technology, *Tech. Digest, IEEE Symposium on VLSI Technology*, pp. 73–74, 1989.
28. W. Lukaszek M. J. Rendon D. E. Dyer Device effects and charging damage: Correlations between SPIDER-MEM and CHARM-2 *Proceedings of the 4th International Symposium on Plasma Process-Induced Damage* (Northern California Chapter of the American Vacuum Society), Monterey, CA, 1999, pp. 200–203.
29. P. K. Aum *et al.* Controlling plasma charge damage in advanced semiconductor manufacturing: Challenge of small feature size device, large chip size, and large wafer size, *IEEE Trans. Electron Devices*, **45**: 722–730, 1998.
30. Y. Lu C. T. Sah Two pathways of positive oxide-charge buildup during electron tunneling into silicon dioxide film, *J. Appl. Phys.*, **76**: 4724–4727, 1994.
31. J. H. Shiue J. Y. Lee T. S. Chao A study of interface trap generation by Fowler-Nordheim and substrate-hot-carrier for 4-nm thick gate oxides *IEEE Trans. Electron Devices*, **46**: 1705–1710, 1999.
32. For a review see L. K. Han et al., Recent developments in ultra thin oxynitride gate dielectric, *Microelectron. Eng.*, **28**: 89–96, 1995.
33. S. Krishnan *et al.* Assessment of charge-induced damage to ultra-thin gate MOSFETs, *IEDM Tech. Dig.*, 445–448, 1997.
34. C. T. Liu *et al.* Light nitrogen implant for preparing thin-gate oxides, *IEEE Electron Device Lett.*, **18** (3): 105–107, 1997.
35. D. Misra Charge-trapping properties of gate oxide grown on nitrogen-implanted silicon substrate, *Appl. Phys. Lett.*, **75** (15): 2283–2285, 1999.
36. T. Hori Inversion layer mobility under high normal field in nitrided-oxide MOSFETs, *IEEE Trans. Electron Devices*, **ED-37**: 2058–2069, 1990.
37. D. Misra S. Kishore Gate oxides grown on deuterium implanted silicon substrate, *IEEE/ECS Electrochem. Solid-State Lett.*, **2**: 637–639, 1999.
38. D. Misra R. K. Jarwal Metal-oxides-semiconductor diodes on deuterium-implanted silicon substrate, *Appl. Phys. Lett.*, **76** (21): 3076–3078, 2000.

DURGAMADHAB MISRA
New Jersey Institute of Technology