ISOLATION TECHNOLOGY

Increased packing density of active and passive devices is essential in integrated circuit technology in order to provide expanded circuit functions at improved performance levels and reduced costs. Tight packing of devices requires good isolation technology in order to keep the activity of one device from affecting the operation of adjacent devices. Isolation technology must meet requirements for low leakage, low complexity, good planarity, low defect generation, low parasitic capacitance, and good reliability in addition to tight packing density.

BASIC ISOLATION REQUIREMENTS

Integrated circuit technologies use various types of active and passive devices that require different isolation techniques. Active devices include bipolar junction transistors (BJTs)and metal-oxide-semiconductor field-effect transistors (MOSFETs). Passive devices include resistors, capacitors, and diodes. The isolation techniques used for these devices can generally be categorized as either junction isolation or as dielectric isolation.

Junction isolation is utilized in both MOSFET and BJT devices. Source-drain regions in MOSFETs are isolated from the substrate using junction isolation. Emitter, base, and collector regions in BJTs are isolated from each other using junction isolation. The junction between a diffused region of opposite impurity type to that of the substrate is referred to as a p–n junction. The p–n junction provides good isolation between the diffused region and the substrate due to the formation of a depletion region around the junction thereby terminating the applied electric field (see Fig. 1). For junction isolation to be effective, the junction must be operated under reverse bias (n-type region held positive relative to p-type region), the reverse bias across the junction must not exceed the junction breakdown voltage (BVJ), and there must be no dislocations or mid-gap impurities in the silicon crystal in the depletion region to cause excess leakage. Most junctions in integrated circuits are made of two different impurity regions where the dopant concentration of one region is much higher than the opposite region. This type of junction is referred to as an abrupt one-sided junction. The breakdown voltage of abrupt one-sided junctions is determined primarily by the dopant concentration (N) of the more lightly doped side, which is typically the substrate doping, and can be ex-

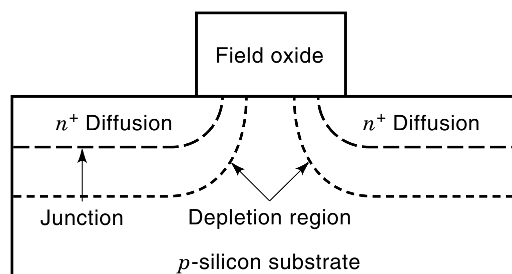

Figure 1. Thick field oxide isolation between two adjacent $n+$ diffusions showing extension of depletion regions into the more lightly doped $p-$ substrate.

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pressed as

$$\text{BVJ} \propto \frac{1}{N} \quad (1)$$

For source-drain junctions on MOSFETs and base-collector junctions BJTs, N is chosen to provide junction breakdown voltages that are higher than the circuit operating voltage, typically twice as high.

Dielectric isolation uses the electrical insulating properties of dielectrics such as silicon dioxide (SiO_2) or silicon nitride (Si_3N_4) to isolate devices from each other while in close proximity on a silicon wafer. The simplest form of dielectric isolation is the thermally grown silicon dioxide layer used to passivate the silicon wafer surface to prevent excessive leakage across p–n junctions terminated at the surface. Diodes, BJTs, and MOSFETs all depend on this surface passivation to avoid excess leakage. Another form of dielectric isolation is the use of a thick field oxide to physically separate diffused junctions and MOSFET channel regions. Figure 1 shows how a thick field oxide made of silicon dioxide is used as the masking layer to separate two $n+$ diffused regions in a $p-$ substrate. The field oxide is first grown on the wafer surface using high temperature oxidation, then patterned and etched to open regions in which active devices can be made. Diffused junctions can be formed in the openings using the field oxide as a diffusion mask. The field oxide region needs to be wide enough to prevent the applied electric field of one junction (and its depletion region) from extending laterally to an adjacent junction and causing excessive current flow. The depletion region width (W) in an abrupt one-sided junction is primarily a function of the reverse bias across the junction (V_R) and the substrate doping concentration (N), although other parameters also have an effect. The relationship between W, V_R, and N can be simplified to

$$W \propto \sqrt{\frac{V_R}{N}} \quad (2)$$

V_R is set by the application and design specifications of the technology and generally is not adjusted to meet isolation requirements. Increasing N will decrease depletion region widths and improve isolation, but reduced depletion region widths also mean increased junction capacitance. The choice of an optimal N is often a trade off between isolation and junction capacitance requirements.

Figure 2 shows how a thick field oxide is used to isolate two MOSFET channel inversion regions. When the gate electrode is under bias, the silicon surface electric field is high enough under thin gate oxide regions to form a conducting inversion layer. The surface electric field is significantly lower under the thick field oxide and no inversion layer is formed, thus keeping the two adjacent inversion layers isolated from each other. The gate electrode bias required to form an inversion layer in a MOSFET structure is referred to as the threshold voltage (V_T). V_T is primarily a function of gate oxide thickness (T_{OX}) and substrate doping, although other parameters contribute as well. The relationship between V_T, T_{OX}, and N can be simplified to

$$V_T \propto T_{OX}\sqrt{N} \quad (3)$$

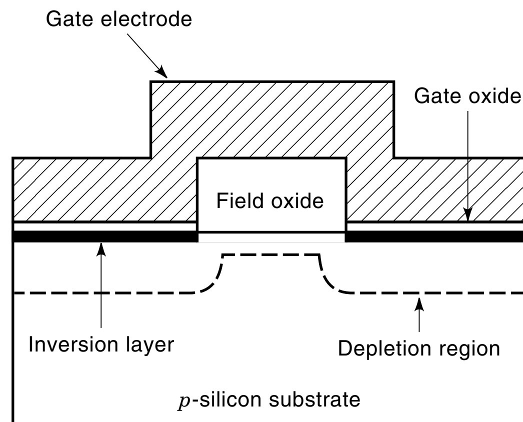

Figure 2. Thick field oxide isolation between two adjacent MOSFET inversion layers.

The V_T of the parasitic field oxide MOSFET should be at least twice as high as the operating voltage of the circuit to ensure good isolation. Increasing field oxide thickness or increasing substrate doping are two ways of accomplishing this. Field oxide thickness is limited by patterning considerations and substrate doping is constrained by the need to target the right V_T for the normal MOSFETs and to keep junction capacitance low. The use of a masked field implant, or channel stop implant, done before field oxidation is a technique used to increase substrate doping only near the field oxide interface and only in field oxide regions. Boron would be used as the field implant in the case of $p-$ substrates, phosphorous or arsenic would be used in the case of $n-$ substrates. The field implant helps to improve isolation characteristics while maintaining low substrate doping in active device regions.

LOCOS ISOLATION

The grow-and-etch field oxide isolation structure illustrated in Figs. 1 and 2 was adequate for early integrated circuit applications, but it had significant limitations that prevented scaling to newer generation technologies with smaller feature sizes. One limitation was the vertical step created by the field oxide that made it difficult to deposit and pattern subsequent layers, such as the polysilicon gate electrode. Another limitation was the inability to self-align the field implant to the edge of the field oxide, resulting in increased junction capacitance and increased MOSFET threshold voltage near field edges when the field implant encroached into active areas. An ideal isolation structure would be planar with the silicon wafer surface and have a field implant that was self-aligned to the field edge.

A new isolation technology was developed in the early 1970s that had improved planarity and provided a self-aligned field implant. This technology is referred to as LOCOS (for LOCal Oxidation of Silicon). The LOCOS process flow is as follows: grow a thin silicon dioxide pad oxide (5 to 50 nm), deposit 50 nm to 200 nm of silicon nitride using chemical vapor deposition (CVD), form the isolation pattern in a photoresist layer on top of the silicon nitride using photolithography, etch the silicon nitride layer, implant a boron field implant in open isolation regions. The field implant is masked

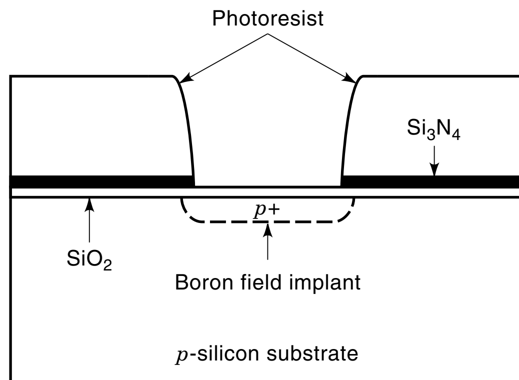

Figure 3. LOCOS isolation structure shown at the point in the process flow where the CVD silicon nitride layer has been patterned and etched and the boron field implant has been implanted into the substrate.

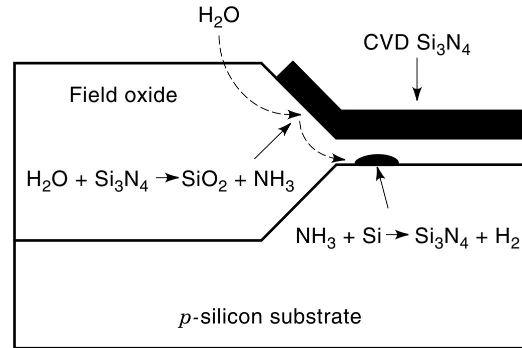

Figure 5. *Kooi* or *white ribbon* affect associated with the use of steam oxidation to form thick field oxides in LOCOS isolation (1). An unintentional silicon nitride layer is formed on the silicon substrate surface near the edge of isolation structures as a result of the chemical reaction between high temperature steam and the CVD silicon nitride layer.

by the photoresist layer used to pattern the silicon nitride and thus is self-aligned to the nitride edge as shown in Fig. 3. Next, the photoresist layer is removed and a thick field oxide (30 nm to 100 nm) is grown in open isolation regions using high temperature steam oxidation (900 to 1000 °C). Silicon nitride is an effective barrier against steam diffusion and prevents oxidation in regions covered by nitride. 0.45 nanometers of silicon is consumed for every nanometer of silicon dioxide grown and the result is a field oxide that is partially recessed into the silicon substrate as shown in Fig. 4. Following field oxidation, the silicon nitride and pad oxide layers are removed and further process steps are done to form the active and passive devices.

One obvious drawback of the LOCOS isolation scheme is the lateral growth of oxide under edges of the silicon nitride layer. This tapered oxide region is referred to as the bird's beak and is undesirable in that it encroaches into active regions and reduces their area. The bird's beak can be reduced by reducing field oxide thickness, reducing pad oxide thickness or increasing silicon nitride thickness, but thinner pad oxide and thicker nitride layers tend to cause higher stress levels in the silicon after field oxidation that can create silicon dislocations that cause junction and gate oxide leakage problems. For practical LOCOS technologies, the length of the bird's beak is about the same as the thickness of the field oxide.

A unique problem encountered early in LOCOS development was the thinning of gate oxides near LOCOS field edges resulting in lower gate oxide breakdown voltages on MOSFETs. The problem is caused by formation of a thin silicon nitride layer on the substrate surface during the steam field oxidation step as shown in Fig. 5. The thin silicon nitride layer retards the growth of the subsequent gate oxide resulting in thin regions. This effect is referred to as the Kooi effect (after the discoverer) (1) or the white ribbon effect (after its visual appearance). The solution to the problem is to grow a thin sacrificial silicon dioxide layer after removing the CVD silicon nitride and pad oxide layers and to strip the sacrificial oxide layer off before growing the final gate oxide. This helps to break up and remove the thin silicon nitride layer and avoid gate oxide thinning.

ENHANCEMENTS TO LOCOS

LOCOS isolation provides improved planarity over the prior grow-and-etch isolation technology, but it is still not completely planar. About half of the LOCOS field oxide thickness extends above the wafer surface. One technique for improving LOCOS planarity is to initially grow more field oxide than needed, and then etch back the field oxide to bring it planar with the wafer surface as shown in Fig. 6. The isotropic etch used not only thins the field oxide, but also pulls back the bird's beak to reduce encroachment. There is a limit to how useful this approach is because the extra field oxidation consumes more of the boron field implant and the etch back step

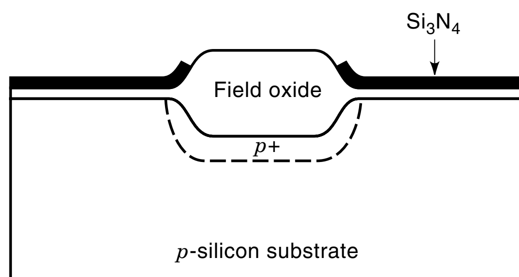

Figure 4. LOCOS isolation structure shown after a thick field oxide has been grown in open regions in the CVD silicon nitride layer.

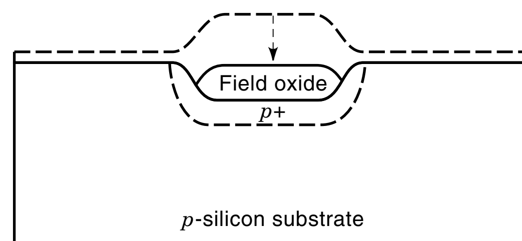

Figure 6. Etchback LOCOS showing a reduction in bird's beak length and improvement in isolation planarity.

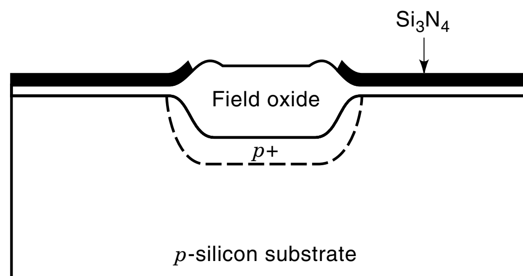

Figure 7. Recessed LOCOS showing an improvement in isolation planarity by adding a silicon recess etch step prior to growing a thick field oxide.

exposes more of the $p+$ doped region along field edges which may be too heavily doped to form active devices.

Another approach to improve LOCOS planarity is to add an additional silicon substrate etch step to the LOCOS process flow right after etching the CVD silicon nitride layer and before the boron field implant. The silicon is recessed by 100 nm to 200 nm in isolation openings using an anisotropic etch. Figure 7 shows how the field oxide is more planar with the substrate surface with this approach, which is referred to as recessed LOCOS.

Numerous other versions of LOCOS have been developed to improve planarity and reduce the size of the bird's beak. SILO (Sealed-Interface Local Oxidation) (2) is a variation of LOCOS where an additional thin CVD silicon nitride layer is deposited on the bare wafer surface before the pad oxide and thicker CVD silicon nitride layers are deposited. The extra silicon nitride layer helps to reduce the length of the bird's beak. Polybuffered LOCOS (3,4) uses a thinner pad oxide layer and thicker CVD silicon nitride layer than standard LOCOS and adds a thin polycrystalline silicon layer between the pad oxide and silicon nitride. This approach also results in a smaller bird's beak and the polycrystalline silicon layer reduces stress that would otherwise create silicon dislocations near the isolation structure. SWAMI (Side WAll-Masked Isolation) (5) follows process steps similar to recessed LOCOS and then adds steps to seal the edges of the etched nitride and silicon before growing the field oxide. The silicon recessing improves isolation planarity while the side wall sealing reduces the size of the bird's beak. Although these technologies improve planarity or reduce beak size, they are considerably more complex than standard LOCOS and introduce increased mechanical stress at field oxide edges that can lead to silicon dislocations resulting in increased junction leakage or degraded gate oxide reliability. However, improvements to LOCOS have allowed this isolation technique to be successfully scaled at least down to 0.35 μm and 0.25 μm generation technologies.

Reference 6 is an excellent source of information on LOCOS isolation and enhanced forms of LOCOS.

SHALLOW TRENCH ISOLATION

Shallow trench isolation (STI), or buried oxide (BOX) isolation, is a new isolation technology that has started to replace LOCOS on advanced integrated circuit technologies as the demands on isolation technology increased and the complexity of the LOCOS solutions grew. Shallow trench isolation has no bird's beak to encroach into active areas and is planar with the wafer surface. The process flow is as follows: grow a thin silicon dioxide pad oxide (5 nm to 20 nm), deposit 100 nm to 300 nm of CVD silicon nitride, form the isolation pattern in a photoresist layer on top of the silicon nitride using photolithography, etch the silicon nitride and pad oxide layers, etch into the silicon substrate for a depth of 300 nm to 500 nm using an anisotropic etch, grow a thin silicon dioxide layer to coat the trench side walls (5 to 40 nm), deposit a conformal CVD silicon dioxide layer that fills the trench and covers the wafer surface (0.5 to 1.0 μm), and polish the CVD silicon dioxide layer back down to the silicon nitride surface using chemical-mechanical polishing (CMP). Silicon nitride typically polishes much more slowly than silicon dioxide in the CMP step and thus acts as polish stop. The shallow trench isolation structure at this point in the process flow is illustrated in Fig. 8. The silicon nitride layer and pad oxide layer are removed next with chemical etchants and the process steps for forming active and passive devices then follow.

Shallow trench isolation is an ideal isolation technology not only because it is planar and has no bird's beak, but also because there is no field implant to encroach into active areas and effect MOSFET threshold voltage or increase junction peripheral capacitance. The trench depth is typically chosen to be deep enough to provide good isolation and avoid the need for an extra field implant. One problem with shallow trench isolation is the tendency to form a parasitic MOSFET along the top corner of the trench that increases off-state leakage in narrow channel MOSFETs. This problem can generally be fixed by adding process steps to round the top corner of the trench or by increasing the silicon nitride thickness to ensure that the CVD oxide surface remains higher than the silicon substrate surface at the end of the process.

References 6 to 8 are good sources of information on shallow trench isolation.

TWIN WELL CMOS

Complementary MOSFET (CMOS) technology incorporates both n-channel (NMOS) and p-channel (PMOS) transistors as a means to improve circuit performance and reduce power consumption. CMOS technology replaced NMOS technology to become mainstream in the industry in the 1980s. Isolation

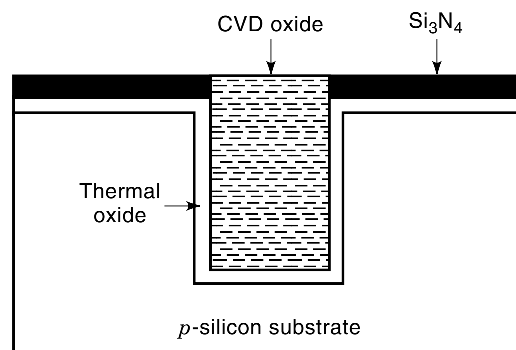

Figure 8. Shallow trench isolation showing excellent planarity and no bird's beak. Trenches are filled with a CVD silicon dioxide layer and planarized with chemical-mechanical polishing.

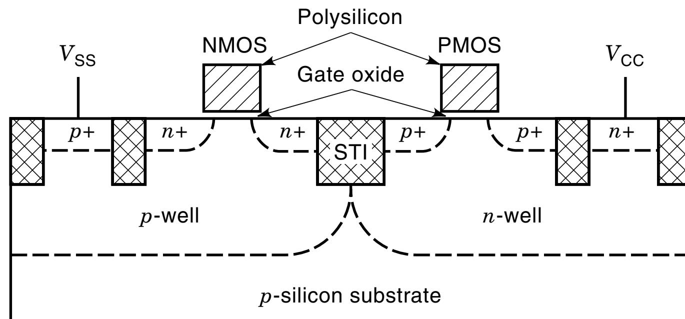

Figure 9. A twin well CMOS technology using shallow trench isolation between devices. Separate $n+$ and $p+$ taps are used to connect V_{CC} and V_{SS} to n-wells and p-wells, respectively.

technology became much more challenging with two types of MOSFETs in the same process flow. Silicon substrates were still p-type for most applications and additional n-well regions had to be formed in which to make the PMOS devices. The boron field implant used to improve isolation characteristics for NMOS technologies could now be done only in NMOS regions, otherwise PMOS isolation would be degraded by the boron implant. This could be accomplished by patterning and etching the LOCOS CVD silicon nitride layer in two separate masking steps: once to open isolation areas and implant boron in NMOS regions, and a second time to open isolation areas in PMOS regions. An additional n-type field implant is typically not needed in PMOS areas because the phosphorous impurity used to form n-wells piles up in the silicon under the field oxide during its growth and provides good PMOS isolation, whereas NMOS regions need the additional field implant due to the tendency of boron to segregate into the oxide during field oxidation.

Newer generations of CMOS technology use thinner gate oxides and require higher substrate or well dopings to achieve the desired transistor threshold voltages. To achieve the right doping levels, modern CMOS technologies use both p-wells and n-wells, or twin wells, in which to form NMOS and PMOS devices as shown in Fig. 9. Substrate dopant concentrations are in the range of 10^{15} cm^{-3} and well dopant concentrations are in the range of 10^{17} cm^{-3}. The boron field implant used on older NMOS technologies can be eliminated on twin well technologies if the p-well is formed after field oxidation or after shallow trench formation using high energy implantation because the p-well dopant concentration is usually high enough to achieve good NMOS isolation.

A new isolation requirement exists in CMOS, namely the need to isolate NMOS and PMOS devices from each other when in close proximity. Figure 8 shows the cross section of a twin well CMOS technology; this example uses shallow trench isolation. NMOS and PMOS devices need to be placed as close together as possible to improve overall circuit density. The isolation between $n+$ diffusions and adjacent n-wells, and between $p+$ diffusions and adjacent p-wells is what generally limits the spacing between NMOS and PMOS devices. Higher well concentrations or deeper trenches are two ways to reduce this spacing, but this interwell isolation spacing tends to be larger than the minimum intrawell isolation spacings.

References 6 and 9 are excellent sources of information on twin well CMOS.

BIPOLAR JUNCTION TRANSISTOR ISOLATION

Modern BJT technologies focus primarily on forming high performance NPN transistors, sometimes in combination with CMOS devices in technologies referred to as BiCMOS. The n-type collector regions have dopant concentrations around 10^{16} cm^{-3} and are formed by relatively deep diffusions in the substrate (1 to 2 μm). The p-type base regions have dopant concentrations $\sim 10^{18}$ cm^{-3} and are formed with relatively shallow implants or diffusions (<0.2 μm). The n-type emitter regions have dopant concentrations $>10^{20}$ cm^{-3} and are formed by shallow arsenic or phosphorous outdiffusion from a separate polysilicon layer. Figure 10 illustrates a typical *npn* BJT structure in a BiCMOS technology.

BJT collector regions differ from MOSFET well regions in that collectors are typically operated in circuits with varying signal voltages, while wells are usually operated under dc bias. Collector resistance and collector capacitance both need to be low to achieve good BJT performance. Collector to base isolation is provided by keeping the collector dopant concentration low to give a high collector–base BVJ. Extra $n+$ buried layers with dopant concentrations $>10^{19}$ cm^{-3} are often added at the bottom of collectors to reduce lateral collector resistance while maintaining high collector–base BVJ. Buried layers are made with a high dose implant into the substrate followed by a lightly doped silicon epitaxial deposition done before the standard well and collector regions are formed. A deep $n+$ diffusion, or collector tap, is added to reduce vertical collector resistance.

BJT collectors need to be isolated from each other in close proximity and with low parasitic collector capacitance. One of the most effective ways of doing this is to insert a deep trench isolation between wells and collectors as illustrated in Fig. 10. The process flow for forming deep trench isolations is as follows: pattern and etch trenches into the silicon substrate (1 to 3 μm deep), grow a thin thermal oxide layer on trench

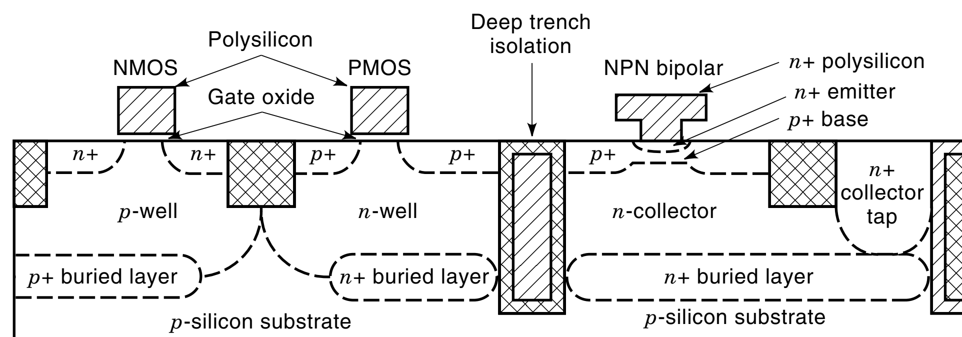

Figure 10. A BiCMOS technology incorporating twin well CMOS and *npn* bipolar transistors. Shallow trench isolation is used between CMOS devices. Deep trench isolation is used to isolate bipolar devices. Added $n+$ and $p+$ buried layers are used to reduce well resistance to improve bipolar performance and to reduce the risk of latchup.

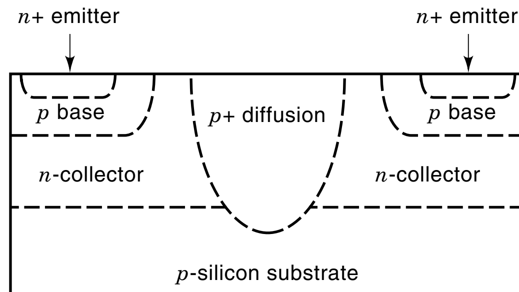

Figure 11. Diffusion isolation between two adjacent *npn* bipolar devices. Relatively wide isolation area and high $p+$ to collector capacitance are drawbacks compared to modern dielectric isolation schemes.

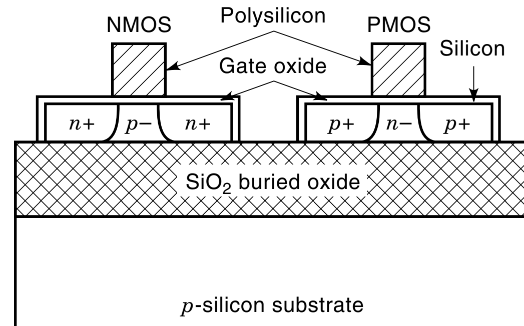

Figure 12. Silicon-on-insulator CMOS devices using a buried oxide layer and MESA isolation for complete isolation.

side walls, fill trenches with a conformal CVD polysilicon layer, and etch the polysilicon layer off the substrate surface leaving polysilicon in the trenches (6, 9). The alternative to deep trench isolation between wells and collectors is the use of junction isolation (see Fig. 11), which is typically not as dense and can have higher collector side wall capacitance and restrict collector operating voltage due to junction breakdown limitations.

The emitter-base BVJ is relatively low due to the high dopant concentrations of emitter and base regions. This low BVJ value is generally tolerable in BJT circuit operation. The polysilicon emitter layer overlaps the base region beyond the region of contact to the silicon substrate to account for alignment variation between the polysilicon emitter and the emitter opening. The polysilicon in this overlap region is isolated from the base with a silicon dioxide layer to reduce parasitic emitter-base capacitance (see Fig. 10).

SILICON-ON-INSULATOR ISOLATION

The use of Silicon-On-Insulator (SOI) substrates serve to isolate MOSFETs from the silicon substrate and can provide enhanced device performance by reducing source and drain capacitance. SOI is used in high voltage circuits, very low power circuits, in applications requiring radiation immunity and lately in smart power technology requiring full dielectric isolation (10). Several techniques are used to form SOI structures including: Separation by IMplanted OXygen (SIMOX), wafer bonding, and epitaxial lateral overgrowth (6). In all cases the goal is to form a 200 nm to 1 μm silicon dioxide layer under a 100 nm to 1 μm crystalline silicon layer. Devices formed in the crystalline silicon layer are isolated from the substrate by the buried oxide layer as shown in Fig. 12.

In principle, a simpler process can be employed to realize CMOS devices once the SOI structure is built. Depending upon the silicon film thickness (t_{Si}) and doping level, a SOI MOSFET may be either partially depleted or fully depleted during operation. SOI MOSFETs targeted for fully depleted operation have t_{Si} around 100 nm, while partially depleted devices have t_{Si} of 200 nm or thicker. A typical process flow closely mimics that of the bulk silicon technology where the lateral isolation is formed using LOCOS, STI or a MESA process. Figure 12 illustrates SOI MOSFETs using simple MESA isolation, which gets its name from the mesa-like shape of the silicon active regions. Such a structure requires fewer process steps to make than standard twin well bulk CMOS (11). The key difference with a bulk process is that the source and drain diffusions on SOI extend all the way to the buried oxide and are completely isolated from the substrate and adjacent devices. Key issues to contend with with MESA isolation are source to drain side wall leakage, poor oxide quality and short carrier lifetime.

LATCHUP

Inherent in the basic CMOS inverter are two parasitic bipolar devices that under appropriate stimuli provide a regenerative low resistance feedback path for current to flow from the supply (V_{CC}) to ground (V_{SS}) (12,13). This feedback state is referred to as latchup and can render circuits nonfunctional. If the current levels are high enough latchup can cause permanent damage to circuits. Referring to Fig. 9, the parasitic lateral *npn* bipolar device is formed with the $n+$ diffusion as the emitter, *p*-well as the base, and *n*-well as the collector. The parasitic *pnp* bipolar device is formed with the $p+$ diffusion as the emitter, *n*-well as the base, and adjacent *p*-well or *p*-substrate as the collector. The parasitic *npn* and *pnp* devices form the intrinsic latchup circuit illustrated in Fig. 13. Lat-

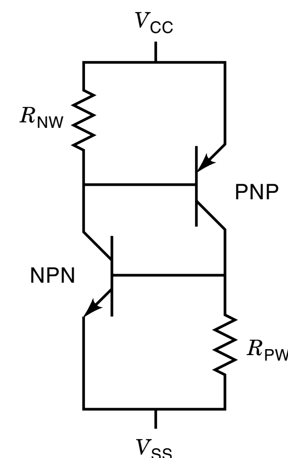

Figure 13. Circuit schematic for parasitic *npn* and *pnp* transistors leading to latchup in CMOS technologies. R_{NW} and R_{PW} are *n*-well and *p*-well resistances, respectively.

eral n-well and p-well resistances (R_{NW} and R_{PW}) complete the circuit.

A typical supply trace of the current I_{CC} versus V_{CC} is illustrated in Fig. 14 for the circuit shown in Fig. 13. For voltages up to the latchup trigger voltage (V_{TRIG}) or injected current up to the trigger current (I_{TRIG}), the *pnp* and *npn* emitters are weakly forward biased with most of the applied voltage applied across the reverse biased n-well/p-well junction. Further increase in voltage or increase in injected current cause the parasitic BJTs to turn on and I_{CC} to rise sharply in a latchup mode. The circuit will not get out of latchup until V_{CC} is reduced below the holding voltage (V_{HOLD}) or I_{CC} is reduced below the holding current (I_{HOLD}). There can be many sources of trigger current that can initiate latchup. As an example consider a noise that pulls the n-well tap below V_{CC}, injects current into the n-well resistor and forward biases the *pnp* emitter causing current to appear in the p-well collector. As this current flows out across the p-well resistor, the *npn* emitter can itself be forward biased providing a positive feedback which under appropriate conditions can continue to draw current from the *pnp*, resulting in a low resistance latched path from V_{CC} to V_{SS}. There can be many sources that initiate latchup, some of which are: I/O voltage overshoot or undershoot, avalanche of the well/substrate junction caused by overvoltage at some node, photo-generation, capacitively coupled transient current injection, impact ionization induced substrate current, and loss of isolation across the well. The objective in any technology is to maximize V_{TRIG} and V_{HOLD}. Circuits are described as being latchup free if they never latch or latchup immune if $V_{HOLD} > V_{CC}$. Typically, a circuit is considered to be latchup immune if it can withstand more than 500 mA at the I/O pins. The loop gain of the circuit in Fig. 13 is given by

$$G = \beta_{NPN} \frac{R_{NW}}{r_{PNP} + R_{NW}} \beta_{PNP} \frac{R_{PW}}{r_{NPN} + R_{PW}} \quad (4)$$

where r_{NPN} and r_{PNP} are the small signal input resistances of the parasitic BJTs, and β_{NPN} and β_{PNP} are the bipolar gains of

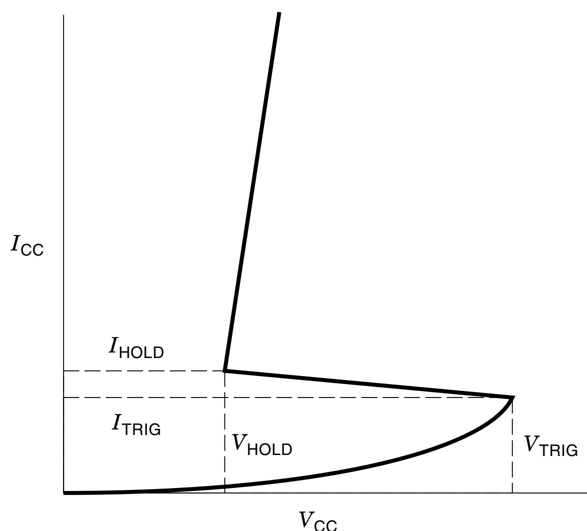

Figure 14. Current-voltage characteristics of a CMOS technology showing trigger (*VTRIG*, I_{TRIG}) and hold (V_{HOLD}, I_{HOLD}) points for latchup. Technologies should design trigger and hold points as high as possible to avoid susceptibility to latchup.

the parasitic BJTs. A latched condition is maintained when $G > 1$.

There are several ways that a CMOS technology can be modified to reduce or eliminate susceptibility to latchup. The primary means to improve margin against latchup are to reduce β of the parasitic BJTs and to reduce lateral well resistances. β can be reduced by increasing well concentrations and by increasing spacings between emitter and collector regions. Increased well dopings or the use of heavily doped buried layers will reduce well resistances. Higher substrate doping has a benefit similar to reducing p-well resistance in the case of the parasitic *pnp* device. Using wafers with a lightly doped silicon epitaxy layer formed on a heavily doped $p+$ substrate (10^{19} cm^{-3}) is one effective means of reducing the *pnp* collector resistance and improving margin against latchup (14). Frequent tapping of wells with low resistance diffusions or surrounding wells with low resistance diffused guard rings are other effective techniques for improving margin against latchup, but come at the cost of additional layout area (15). The use of deep trench isolation at the boundaries between wells is an especially effective means of reducing parasitic β. Lastly, the use of SOI wafers eliminates the parasitic bipolar devices altogether and eliminates latchup.

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ISOLATION TECHNOLOGY. See PASSIVATION.
ISOLATORS, MICROWAVE. See MICROWAVE ISOLATORS.