ION IMPLANTATION

For the fabrication of structures and devices in a semiconductor material, it is often necessary to alter the surface properties locally. Ion implantation is a technique by which impurity atoms or molecules are ionized, accelerated, and shot into the surface of a target material (1,2). In semiconductor manufacturing, this technique has found widespread application in silicon technology (3), where the most commonly implanted impurities are those which dope the silicon such as boron, phosphorus, arsenic, and antimony. Often neutral species are also implanted for surface modification purposes. In principle, any element can be implanted in any target (4), making ion implantation a much more versatile technique than chemical diffusion techniques by which high-temperature treatments are used to drive impurities into the substrate (5).

The basic elements of a typical ion implantation system are shown in Fig. 1. Ions are created in an ion source in which collisions of electrons and neutral atoms result in a plasma of numerous different ions. A direct current (dc) voltage, the extraction potential, attracts the positively charged ions from

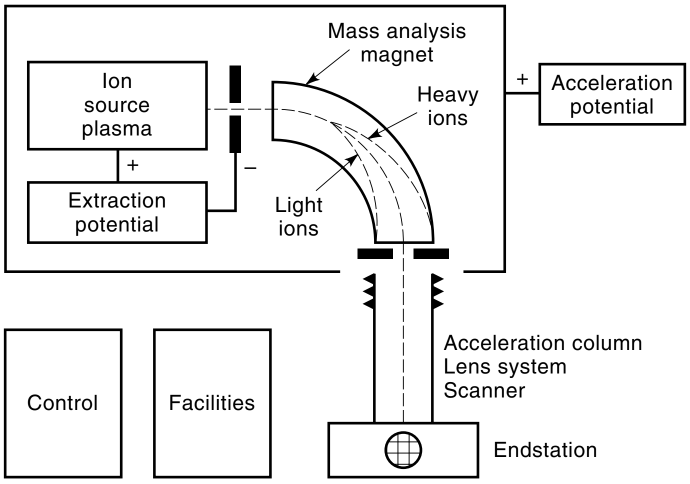

Figure 1. An ion-implantation system.

this plasma, and the required species is selected in an analyzing magnet. The energy required to enable the ions to penetrate beneath the surface of the target is supplied by the acceleration column. After final focusing in the lens system, the beam is usually scanned by electrostatic plates and/or the wafer is moved to achieve uniformity.

An important feature of ion implantation is the ability to accurately determine the number of impurities that are implanted. The target is mounted in a Faraday cup which enables the number of ions impinging on the target to be determined by directly measuring the beam current and integrating with time. By regulating the incident ion dose and energy, a wide range of impurity profiles can be realized, with depths ranging from 0.1 μm to 5 μm and impurity concentrations varying from 10^{14} atoms/cm^3 to 10^{21} atoms/cm^3. The reproducibility is extremely high, and the mass separation of the beam ensures a high level of dopant purity. These features are essential for many important properties of integrated circuits (ICs); among these essential features is the consistency of electrical device characteristics typical of today's IC processes.

The ion-implantation process itself has the great advantage of being a low-temperature technique that is compatible with photolithographical techniques. Therefore, a photoresist is among the many thin film materials which may be used as a mask so that ions can be implanted in selected areas. Moreover, the ability to dope the silicon by implanting through a very thin dielectric surface layer is a unique feature of this technique.

The exact distribution of the implanted impurities will depend on the ion species and energy as well as the structure of the target. When the ions enter the target, they lose their energy through random collisions with target electrons and nuclei, and then they finally come to rest. During this process the crystalline lattice of the semiconductor is deranged, and an annealing step is usually necessary to repair the damage as well as to electrically activate the dopants. This is one of the drawbacks of ion implantation that has been overcome in many silicon applications, but has limited its use in less robust semiconductors such as gallium arsenide.

APPLICATIONS OF ION IMPLANTATION

In the course of the 1970s and 1980s, ion implantation became the preferred technique for doping silicon (6,7). The use of implantations to adjust the metal–oxide semiconductor (MOS) gate threshold was a breakthrough for MOS processing. The dopants were implanted through the thin gate oxide into the channel region, a procedure that is difficult to realize by any other technique. For the first time, threshold voltages less than 1.5 V could be produced in a routine and controlled manner. The self-aligned implantation of the source and drain with respect to a polysilicon gate has contributed to making the aggressive down-scaling of complementary MOS (CMOS) dimensions possible. The device performance was improved because via implantation the drain could be divided into (1) a lightly doped region near the gate and (2) a heavily doped contact. All in all, a typical very large scale integration (VLSI) CMOS process contains about a dozen ion-implantation steps to form the active transistor as well as the isolation wells, channel-stops, and punch-through stoppers. The energies used range from a few kiloelectronvolts for source/drain implantations to several megaelectronvolts for the wells, and doses range from 10^{10} ions/cm^2 for threshold adjustment to 10^{16} ions/cm^2 for channel-stops.

In silicon bipolar technology, ion implantation has been instrumental in achieving high doping concentrations with abrupt doping gradients. This has enabled the vertical downscaling of the devices with overall improvements in device performance, in particular the speed. The emitter, the base, and the buried collector are often formed by implantation of As, B, and either As or Sb, respectively, while deep phosphorus implants are used for collector plugs and pedestal collectors. In high-speed devices, the doping of polysilicon by ion implantation is often used to form arsenic implanted polysilicon emitters and boron implanted polysilicon base contacts. Implanted resistors are important elements in these processes. High ohmic resistors are formed by implantation in the silicon substrate, while in the low/medium resistance range implanted polysilicon resistors are applied.

In some special applications the chemical composition of the substrate is altered by implantation. For example, buried insulator layers are produced by implanting very high doses, about 10^{18} ions/cm^2, of oxygen or nitrogen deep below the surface. By choosing suitable anneal conditions, a recrystallized monosilicon layer about 0.2 μm thick can be formed on top of the oxide or nitride isolating layer. This process is called separation by implanted oxygen (SIMOX). Surface or buried silicide layers are similarly produced by implanting cobalt, for example. In photolithography, implantation of a photoresist is applied for hardening the resist and improving its resistance to dry etching.

The damage created by implantations finds application in the gettering of metallic impurities. For this purpose a damage layer is created under the device region by implanting the backside of the wafer, for example, or by using high-energy implantations to form a buried damage layer far under the surface. Implantation-induced damage of silicon oxide and silicon nitride layers is also used to (locally) enhance the etching of these layers.

In most compound semiconductor processes, the active device areas are epitaxially grown layered structures. In some cases (e.g., GaAs heterojunction bipolar transistors), ion implantation is used to change the doping type of the surface so that a deeper layer can be contacted. Some regions can also be rendered intrinsic by suitable implants. The damage created by an ion implantation is sometimes used in the regions between the devices to make epitaxial regions semi-isolating. In GaAs metal semiconductor field-effect transistors (MESFETs), not only the source/drain contacts are implanted but also the channel may be created by implantation. However, these devices do not exhibit the same reproducibility and reliability that is typical of silicon-based field-effect transistors (FETs).

IMPLANTED IMPURITY DISTRIBUTIONS

On its path through the target material, an implanted ion will lose energy by interactions with the target atoms in the form of nuclear scattering and electronic stopping (8–10). The latter slows down the impinging ion, while nuclear scattering results in a change of velocity and direction as well as a transfer of energy from the ion to the target atom. Thus ions having the same mass and the same initial energy will come to rest at different positions. The average of the total distance thus traveled by a large number of ions is called the range R. The projection of this distance along the axis of incidence is called the projected range R_p. The depth distribution of the ions around the projected range is described by the projected straggle ΔR_p. Likewise, the distribution of ions along an axis perpendicular to the axis of incidence is described by the lateral straggle $\Delta R_\perp$.

In an amorphous substrate, the implanted impurity profile along the axis of incidence can be approximated by a Gaussian distribution function:

$$N(x) = \frac{D}{\sqrt{2\pi}\,\Delta R_p} \exp\left[-\frac{(x - R_p)^2}{2R_p^2}\right] \tag{1}$$

where D is the ion dose per unit area. This ion distribution is shown in Fig. 2.

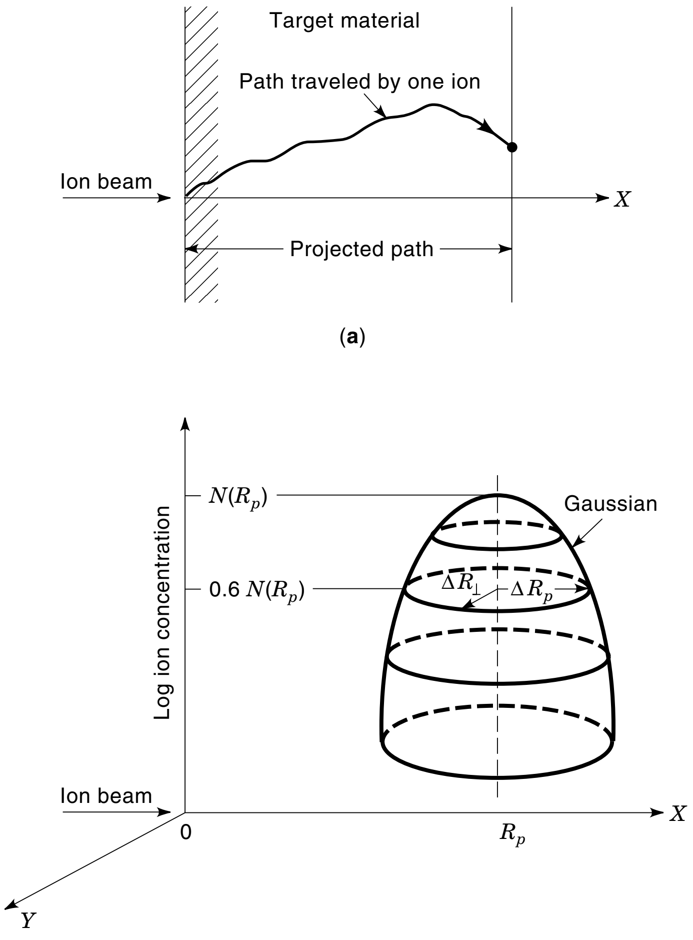

Figure 2. In (a) the projection of the path traveled by a single implanted ion is illustrated, and (b) shows the corresponding Gaussian distribution of a large number of implanted ions. The maximum concentration is at the projected range R_p, and the ion concentration is reduced by 40% from its peak value at a distance of ΔR_p (in the x-direction) or $\Delta R_\perp$ (in the y-direction) from R_p.

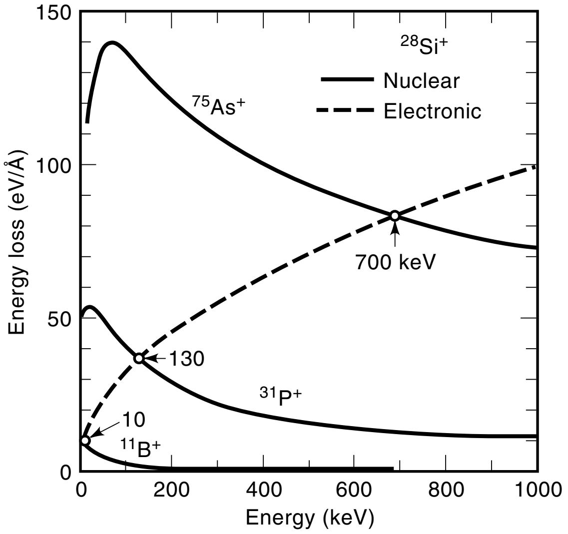

Figure 3. The nuclear and electronic stopping powers for As, P, and B in amorphous Si. The electronic stopping power increases with implantation energy but is only a weak function of atomic mass and number. The heavier the atom and the lower the implantation energy, the higher the nuclear stopping power. The points of intersection of the curves correspond to the energy at which nuclear and electronic stopping powers are equal (11). Reprinted from Ref. 1.

The process by which the incident ion loses energy to the target is characterized by the nuclear stopping power $S_n(E) \equiv (dE/dx)_n$ and the electronic stopping power $S_e(E) \equiv (dE/dX)_e$, where E is the energy of the ion at any point x along its path. The average rate of energy loss with distance is given by a superposition of the two stopping mechanisms:

$$\frac{dE}{dx} = S_n(E) + S_e(E) \tag{2}$$

The range of the implanted ions is then

$$R = \int_0^R dx = \int_0^{E_0} \frac{dE}{S_n(E) + S_e(E)} \tag{3}$$

where E_0 is the initial ion energy. The stopping powers for As, P, and B are given in Fig. 3. The heavier atoms such as As have greater nuclear stopping power—that is, large energy loss per unit distance and thus a short range. For the much lighter boron ions with energies above 10 keV, the main energy loss mechanism is due to electronic stopping because the interaction time with the nuclei is limited, and they are implanted much deeper. Examples of the projected range and straggle in silicon are given in Fig. 4. They can be approximated by the following equations:

$$R_p \cong \frac{R}{1 + \left(\dfrac{M_2}{3M_1}\right)} \tag{4}$$

$$\Delta R_p \cong \frac{2}{3}\left(\frac{\sqrt{M_1 M_2}}{M_1 + M_2}\right) R_p \tag{5}$$

where M_1 and M_2 are the atomic masses of the implanted ion and the target atom, respectively.

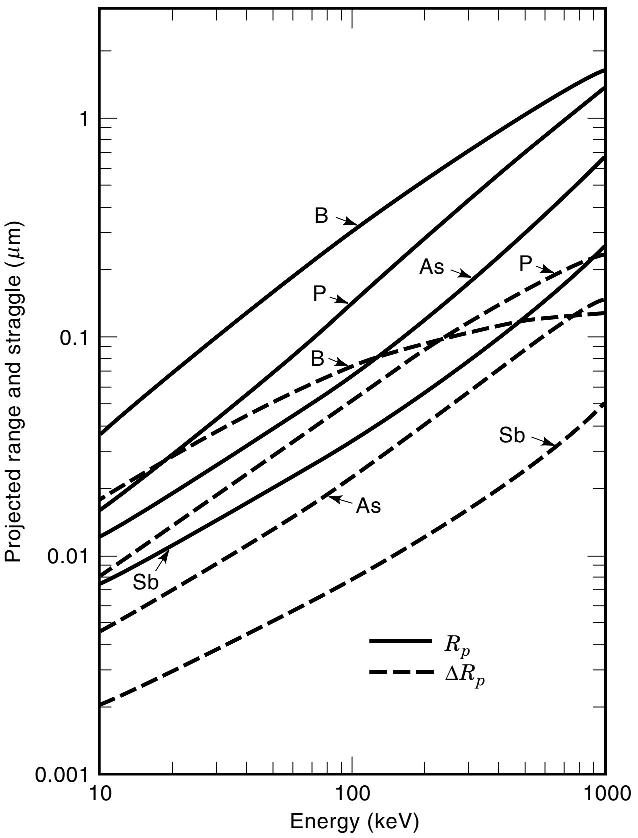

Figure 4. Projected range R_p and straggle ΔR_p for B, P, As, and Sb implanted at various energies into an amorphous silicon target. For a given element at a given incident energy, the lateral straggle $\Delta R_\perp$ (not shown) and the ΔR_p are comparable and usually within 20% of each other. The values are calculated using the SUPREM-3 simulation program (12).

Channeling

In a single-crystalline substrate the organization of the lattice atoms can lead to open channels and planes along which an implanted ion may be guided by electron scattering. Along such directions the ions are protected from nuclear collisions and they can penetrate deep into the crystal, up to 10 times deeper than the Gaussian peak distribution. This effect, illustrated in Fig. 5, is known as channeling. Practical application of channeling is limited because the orientation of the crystal with respect to the ion flight path is very critical. Channeled profiles cannot be maintained at high dose levels, since energetic ions striking the surface of a crystal will displace the crystal atoms, resulting in a near-amorphous condition close to the surface. This is illustrated in the example shown in Fig. 6.

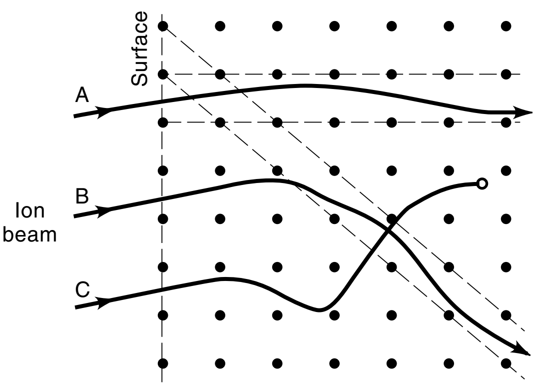

Figure 5. Schematic of ion paths in a single crystal for ions incident in a channeling direction. Ion A is channeled, while ion B is dechanneled into another channeling direction. Ion C is dechanneled and stopped by a nuclear scattering event.

Generally, channeling is avoided as much as possible. The wafer is often tilted a few degrees off the main crystal axis, typically 7° for silicon, or the implantation is performed through an amorphous layer to randomize the directions of the ions as they enter the lattice. Silicon dioxide is often used as a dechanneling layer and can also function as a means of preventing contamination of the underlying substrate. Such a thin layer is called a "screen oxide." Dechanneling is also achieved by amorphizing a thin surface layer of the crystal itself by an inert gas implantation. However, even when atoms enter the lattice in an apparently random direction, they can be diverted into one of the open channels or planes after entering the lattice. This effect leads to the tails in the profiles of ions implanted into single-crystal lattices.

IMPLANTATION DAMAGE IN SILICON

The implanted ions will in many cases derange the target host atoms by nuclear scattering, thus creating a tree of disorder around the path of the impinging ion. The amount of damage created in the host lattice increases with increasing nuclear stopping power and dose, as is illustrated in Fig. 7. Heavy ions such as P, As, and Sb will enter the surface and immediately undergo nuclear scattering, thus creating damage over the whole range. On the other hand, light ions such as boron initially undergo electronic scattering, and nuclear scattering will not dominate before the end of their range. The bulk of the disorder will therefore be found at the peak concentration.

When a sufficient number of ions are implanted into a crystalline system, the individual damage regions may over-

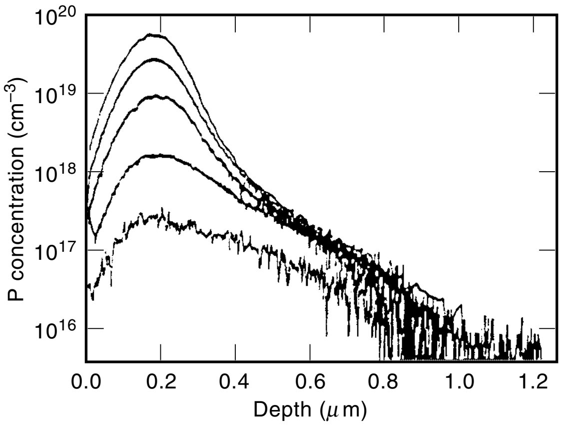

Figure 6. Phosphorus depth profiles for implantations in crystalline silicon at 100 keV in the <100> direction. For the lowest implantation dose of 10^{13} ions/cm^2 a channeling tail dominates the profile, but with increasing dose the relative significance of this tail decreases and the implanted distribution more closely approximates a Gaussian profile. The maximum dose shown is 10^{15} ions/cm^2. Reprinted from Ref. 13, Copyright, 1991, with permission from Elsevier Science—NL, Sara Burgerhartstraat 25, 1055 KV Amsterdam, The Netherlands.

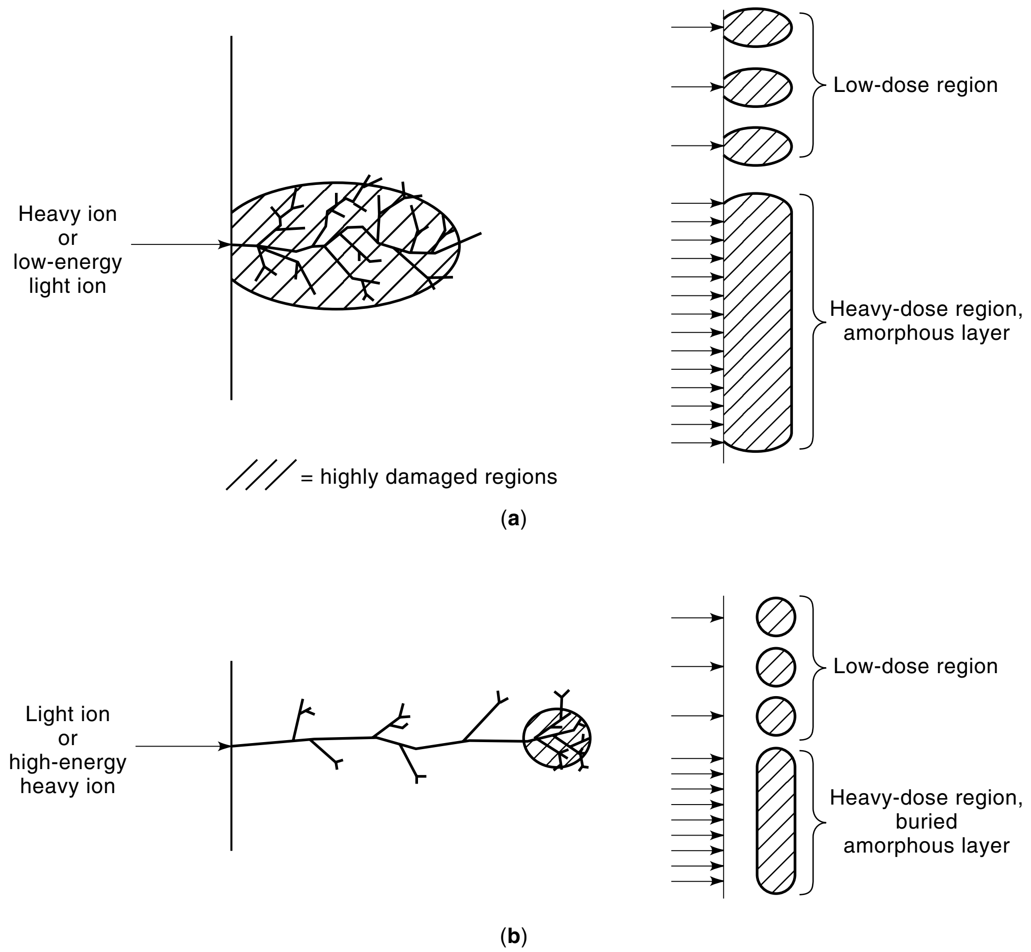

Figure 7. (a) The implantation disorder due to a heavy ion or low-energy light ion extends to the silicon surface and creates a continuous amorphous layer for high dose implantations. (b) For a light ion or high-energy heavy ion, the highly disordered region is located at the projected range and a buried amorphous layer can be formed for high-dose implantations.

lap, and damage to the lattice can become so extensive that it relaxes into an amorphous state. The implantation dose necessary to convert the crystalline surface to an amorphous state is dependent on a number of factors: the mass of the implanted species, the dose rate, and the implant energy, along with the wafer temperature and orientation during implantation. For room temperature implantations in silicon, the amorphization threshold for the heavy ions As and Sb is approximately 10^{14} ions/cm^2, while for P a dose of 10^{15} ions/cm^2 is necessary. For the much lighter B ions, at least a dose of 10^{16} ions/cm^2 is needed; but in general room temperature B implants do not amorphize.

Damage Annealing

When dopant ions are implanted into a semiconductor lattice, only a small percentage will initially occupy substitutional sites, and as a result they are mainly electrically inactive. An annealing treatment is necessary to both activate dopants in the implanted region and to remove the associated implantation damage. Movement of the dopants may then also occur as a result of diffusion. The annealing process is very complex, and the exact temperature and time intervals of the total anneal cycle will have a strong influence on resulting dopant and defect distributions (14).

Generally, temperatures of 400°C to 600°C for several minutes are sufficient for bringing about electrical activity. The as-implanted doping profile is then preserved, but higher temperatures and/or longer anneal times are usually required for sufficient recovery of the carrier mobility and lifetime. For conventional furnace anneals at temperatures exceeding 1000°C for 30 min or longer, the depth of the resulting doping profile will be determined by normal thermal diffusion, which is quite high at these temperatures. The depth profiles can then be broadened by a few tenths of a micrometer, but at these temperatures the implantation damage is effectively removed. For high doping concentrations the solid solubility of the dopant will limit the dopant activation.

In the temperature range 600°C to 900°C, the activation and diffusion of the dopants will be very strongly influenced by the nature of the implantation disorder and the associated anneal mechanisms. Some annealing of the damage can already occur during the implantation, depending on the corresponding (self-) heating of the wafer. In regions where the implanted dose is sufficiently low, isolated point defects or point-defect clusters are created. Vacancy-type (V-type) defects are created where target atoms are removed from lattice positions, and interstitial type (I-type) defects typically occur in the region where the implanted ions come to rest. Vacancies and silicon self-interstitials recombine during implantation and annealing; but because the implantation introduces extra atoms into the lattice, a resulting supersaturation of self-interstials, comparable in number to the implantation dose, can often be identified in the defect configurations. If the implant dose is high, but not high enough to bring about amorphization, extended defects such as dislocation loops may form, usually at the projected range. These may be difficult to remove because they can be stable at temperatures up to 1100°C. Moreover, precipitation of the implanted species can result if the solid solubility at the annealing temperature is exceeded. The solid solubility decreases with decreasing anneal temperature. Therefore any slow ramp-down of the anneal temperature or post-anneal processing at lower temperatures may lead to further precipitation and clustering of the dopants, thus decreasing the dopant activation.

For high-dose implantations which generate an amorphous layer, the defect types related to lower dose implants will appear in the tail of the implantation. In the amorphous region itself, the underlying single-crystal semiconductor material will serve as a seeding area for recrystallization. In this process, called solid-phase epitaxy (SPE), the dopant atoms are built into substitutional sites along with the host atoms at a relatively low activation energy. A high electrical activation and mobility can therefore be obtained at temperatures as low as 600°C. The disorder created just beyond the amorphous–crystalline interface in the heavily damaged, but still crystalline substrate, is difficult to remove. It is always associated with amorphizing implants and is called the end-of-range (EOR) damage. Some of the different defect types associated with implantation and annealing are illustrated in Fig. 8.

JUNCTION FORMATION IN SILICON

When implantations are used for either contacting or forming *p–n* junction diodes in a silicon integration process, a large number of factors must be considered before the most suitable implantation and anneal conditions can be determined. Generally speaking, the junctions must have low reverse-bias leakage and near ideal forward characteristics. Any process-induced damage in the space-charge region of the junction may become a source of leakage currents. Defects in the neutral region of the junction will not contribute to leakage, but can reduce the carrier mobility and thus increase series resistance. In contact windows, a high doping level at the silicon surface is usually necessary for forming a low ohmic contact to metal electrodes (15). The degree to which such defect-free junctions with high carrier mobility and dopant activation can be realized will depend on the junction depth that can be tolerated and on the compatibility with the total process flow. Pure manufacturability issues such as process complexity, controllability, and reproducibility also place restrictions on the implantation conditions and thermal budget for annealing.

Amorphizing implants are often preferred for junction formation, because the recrystallization process by SPE gives better control of defect during annealing. Problems with the EOR damage are then avoided by diffusing the implanted dopants past this region during annealing. Alternatively, by using an inert species to amorphize a region deeper than the implanted dopant profile, the EOR damage can be moved deeper than the junction.

A wide range of doping profiles can be achieved by using a series of implants with varying energies and doses. Serial implantations of different species are also performed to create multiple junctions, such as the emitter and base of the bipolar transistor shown in Fig. 9. Here it is important that no extended defects intersect the base from emitter to collector, since even one dislocation can cause an emitter–collector short. This is particularly a problem in high-speed bipolar transistors where the base is very narrow.

Deep junctions are formed by two methods. Conventionally, a relatively shallow implant is performed and followed

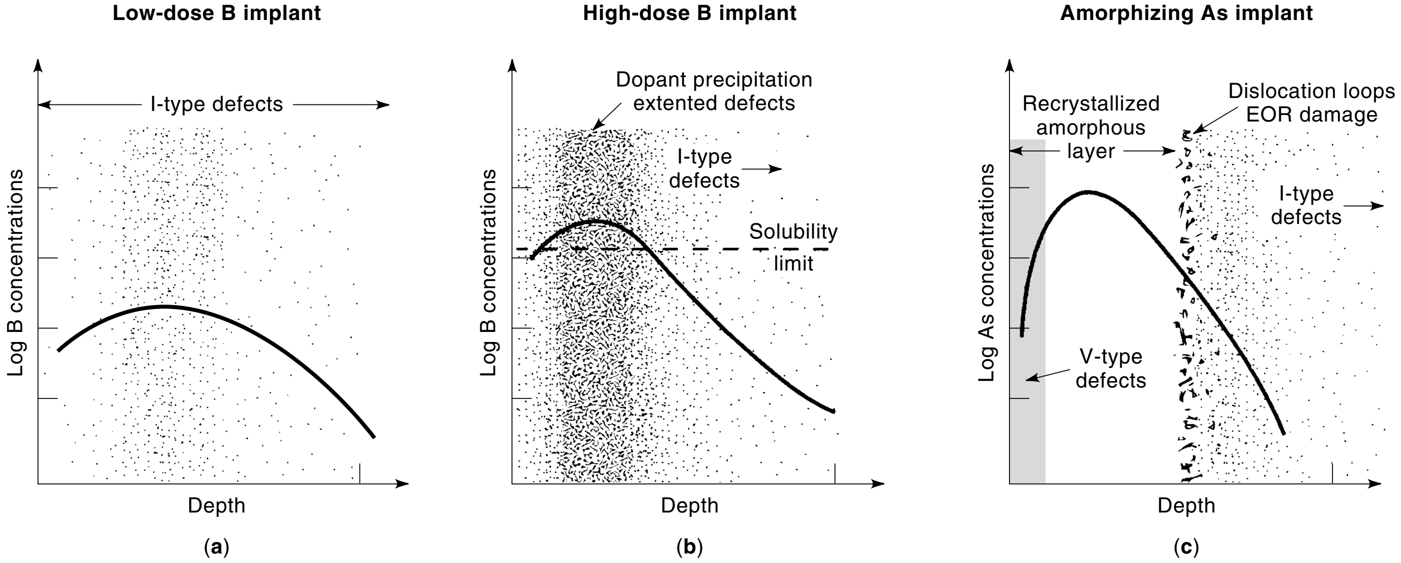

Figure 8. A visualization of defect types that may occur as a result of implantation and annealing. The three as-implanted profiles are associated with increasing levels of implantation damage: (a) a light-dose boron implantation, (b) a high-dose nonamorphizing boron implantation, and (c) an amorphizing arsenic implantation.

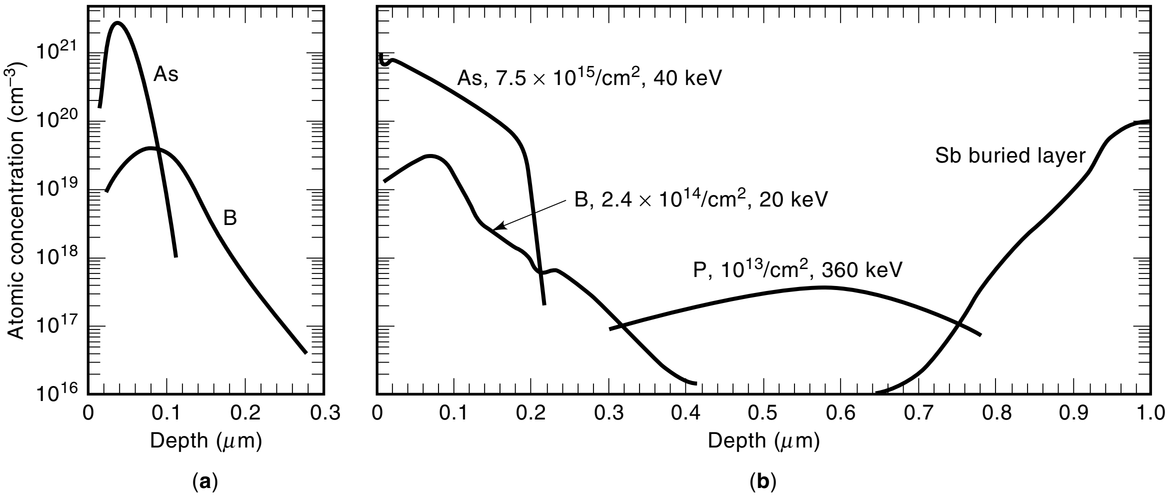

Figure 9. The as-implanted (a) and fully processed (b) dopant profiles of a fully implanted bipolar *NPN* transistor, where emitter, base, pedestal collector, and buried collector are formed by implantation of As, B, P, and Sb, respectively (16). The diffusion of the boron ions during the 950°C 30 min anneal is strongly influenced by the electrical gradient created by the arsenic profile. A 0.85 μm *n*-type epitaxial layer is grown after the Sb implantation and drive-in anneal.

by a high-temperature furnace anneal to drive the dopants into the substrate and remove the implantation damage. Alternatively, high-energy implants can be used in combination with a more moderate thermal anneal. This is, for example, used to simplify the processing of deep retrograde wells and triple wells in CMOS processes (17).

When silicon epitaxy is to be performed on implanted wafers to form buried doping layers, the type of implantation-induced damage created at the surface becomes important. Generally, amorphization of the surface combined with SPE during a pre-epitaxy anneal is necessary for avoiding defects in the epitaxial layer. Another problem is an effect called auto-doping whereby the epitaxial layer is unintentionally doped from the implanted regions. All in all, realizing the desired buried layer can be problematic. High-energy implantations, which can place dopants up to 5 μm from the silicon surface, can be a cost-efficient substitution for epitaxy/buried layer processes.

Shallow Junctions

Shallow junctions with depths less than 0.2 μm are important elements in modern VLSI and ultra-large scale integration (ULSI) CMOS and high-speed bipolar processes, where lateral dimensions have been scaled-down to well below the micron (18). The depth of implanted junctions is reduced by using heavy ions, by reducing implantation energy, and by reducing anneal temperature and/or time. Shallow, heavily doped, *n*-type junctions can be readily obtained at thermal anneal temperatures above 900°C by using As or Sb, which both are heavy mass ions with low diffusivity. Shallow, heavily doped *p*-type junctions, which are important for forming the source and drain of *p*-channel MOS (PMOS) transistors and the base in *NPN* bipolar transistors, are, however, normally doped with boron. This light atom penetrates much deeper and also creates a significant channeling tail. Its diffusivity is high; and upon annealing, the boron profile will in most cases be significantly broadened for all temperatures above 600°C. Above 900°C, normal thermal diffusion accounts for this broadening; below this temperature, defect-assisted diffusion dominates. The latter occurs as long as defect annealing is in progress and is called transient enhanced diffusion (TED). Not only will the implanted dopants themselves experience TED, but other dopants in the vicinity of the implant can also be affected. Implantation-induced TED has been connected to the dissolution of I-type defects or clusters during annealing, whereby interstitials are released. These have a strong interaction with dopants such as B and P that diffuse predominantly by an interstitial mechanism. Point defect dissolution is often very fast, and the bulk of the dopant movement may take place in a matter of seconds. On the other hand, extended defects can keep on emitting interstitials, resulting in very prolonged TED effects.

Preamorphization with a neutral species is an important technique for improving the properties of shallow boron implanted junctions. The EOR damage, which contains the I-type defects, can then be placed deeper than the dopant profile, giving some reduction in TED. Boron channeling is also suppressed, and recrystallization by SPE means that a much lower sheet resistance can be achieved. Such an amorphizing effect will also be achieved by implanting the much heavier ion BF_2^+ instead of B^+. The effective implantation energy of the B atoms is then 11/49 the energy of the BF_2^+ molecule, and very shallow as-implanted profiles are achieved at commonly available implanter energies.

The removal of defects is important for controlling the position of the junction and for suppressing leakage currents. However, the high temperatures necessary for dissolving defects will lead to undesirable broadening of the dopant profiles. Rapid thermal annealing (RTA)—with lamps, for example—offers a means of reducing the thermal anneal cycle to as low as the tens of seconds range, thus limiting the junction depth while still supplying the high anneal temperatures necessary for dopant activation and defect annealing (19). RTA is considered indispensable for shallow junction processing.

Nevertheless, problems related to thermal stresses and deficient control of wafer temperature and corresponding dopant diffusion have made this technique much less accessible for production purposes than conventional furnace annealing.

For the CMOS generations with less than 0.2 μm channel lengths, ultra-shallow junction depths of less than 0.1 μm are required. Due to the inherent advantages, in particular the accuracy with which the dopants are introduced, ion implantation is also playing a major role in this area. Ion-implantation energies below 1 keV are necessary. Wafer charging is then a problem, and damage-induced leakage currents must be reduced by introducing ultra-clean processing to eliminate wafer contamination. TED effects are still a major problem, although they are markedly reduced because the proximity of the Si surface to the EOR damage provides a sink for point defects.

The undesirable effects of implantation damage and enhanced diffusion can be avoided by implantation into a thin film deposited on the Si surface, such as polysilicon or silicides, and diffusing the dopant from this film into the semiconductor. In this manner, shallow junction emitters in bipolar technology are formed by implanting As into a polysilicon film. Other low-temperature techniques which are being studied for the realization of (ultra-) shallow junctions are plasma-immersion ion implantation (20), doping from a gas, doped silicon epitaxy, and gas immersion laser doping (GILD) (21). Excimer laser annealing of implanted regions is also interesting as a means of achieving 100% activation of the implanted dopants, but the method has not yet been found production worthy.

MASKING AND PATTERNING

Normally the ions to be implanted are scanned over the whole wafer. Thus regions on the wafer surface which should not be implanted must be masked in some way. This is generally done by applying a suitable masking layer on the wafer surface. This layer must be compatible with photolithographic techniques and the total IC process. Therefore in silicon IC fabrication such materials as photoresist, silicon oxide, silicon nitride, and polysilicon are often applied. The quality of these materials as masking for implantations can be evaluated from knowledge of the range of the implanted ions in the materials. In Fig. 10, the mask thickness required to achieve a masking effectiveness of 99.99% is calculated.

Masking layers such as silicon oxide and silicon nitride are not always removed after the implantation steps. During subsequent thermal steps, the implanted ions may diffuse from the masking layers into underlying substrate if the masking layer is too thin. Knowledge of such effects is important if adequate masking materials and thickness are to be selected.

The lateral spread of the implantation under the mask edge window will determine the size of the as-implanted region. As the device dimensions decrease and further dopant out-diffusion is limited, this lateral spread and any ions implanted through the mask edges become important for the properties of the junctions, as is illustrated in Fig. 11. A significant number of surface layer atoms are recoil-implanted or "knocked-on." This effect increases with implant ion mass, and thus it is much greater for As than for B. For As implants in SiO_2 the number of knock-on oxygen atoms is comparable to the As dose. When the oxide thickness approaches the projected range of the implanted ions, a large number of oxygen atoms are knocked-on into the Si substrate. This can have a significant effect on the residual defects after annealing and may cause degradation of the junctions.

It is possible to modify the properties of a material with respect to a specific processing step by ion implantation. For example, oxide and nitride mask layers can become so damaged by low-dose argon implantations that they etch much faster than unimplanted layers if the damage is not annealed out first. Another example is the oxidation rate of implanted silicon. Upon thermal oxidation, the SiO_2 thickness will be enhanced in a region implanted with, for example, Si, P, or As and will be retarded in a region implanted with nitrogen. To avoid problems in a given process flow, such effects must be considered carefully. Sometimes they are used with profit for performing resistless pattern generation, often in self-aligned structures.

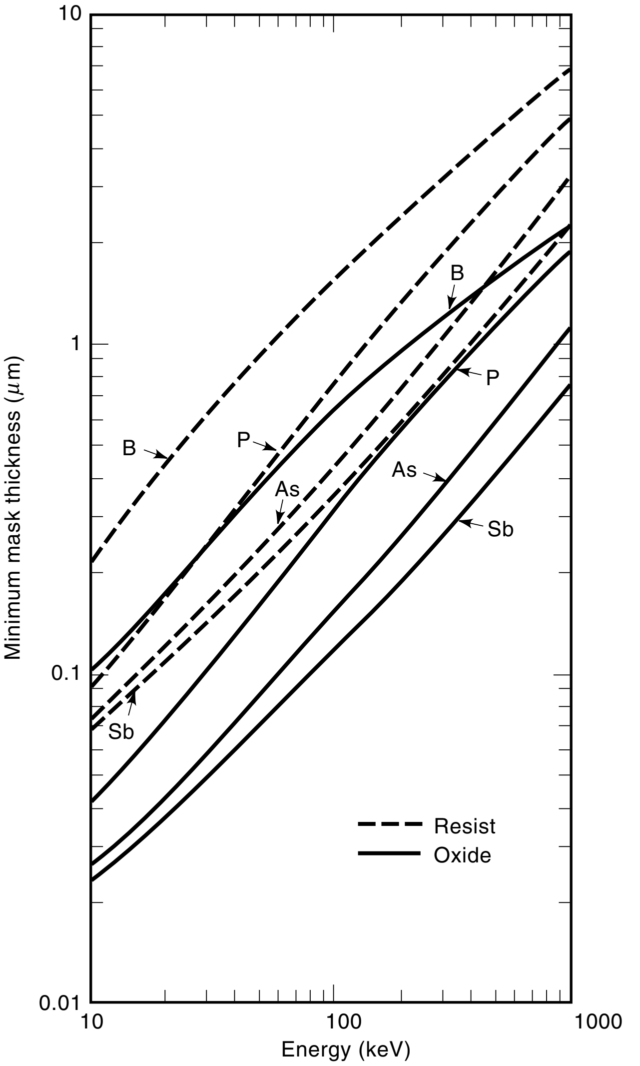

Figure 10. From a knowledge of the projected range and straggle of the dopants B, P, As, and Sb in SiO_2 and AZ-111 photoresist, the minimum mask thickness needed to stop 0.9999 of the incident ions can be well approximated as (R_p + 3.96ΔR_p) (1). The R_p and ΔR_p are calculated using the SUPREM-3 simulation program (12).

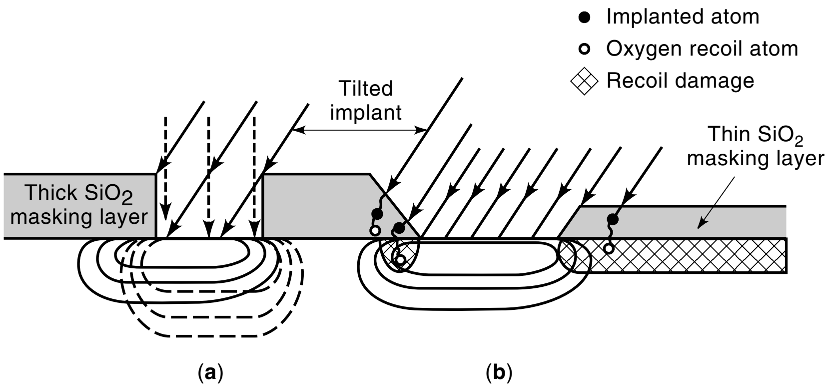

Figure 11. An illustration of three mask-related problems: shadowing and asymmetries due to tilting, and recoil implantation of masking atoms. In (a) the influence of tilting the wafer during implantation is shown. With no tilt the profile is deeper due to channeling, but symmetrical. With a tilt, channeling is reduced, but a shadow is cast at one side of the mask window. For a 7° tilt the shadow is 12% of the mask height. As shown in (b), shadowing is eliminated by tapering the mask edge, but an asymmetry in the implanted profile remains. This effect can be reduced by rotating the wafer a number of times during implantation. In (b) the damage created by recoil implantation of masking atoms is also indicated.

MEASUREMENT TECHNIQUES FOR CHARACTERIZATION OF ION IMPLANTATIONS

The accuracy, reproducibility, and versatility of the ion-implantation technique rely on an intensive application of numerous characterization tools. In production the dose and dose uniformity are routinely controlled, but also the implantation depth profiles are determined regularly. Particularly in process development, the implantation damage before and after annealing are also characterized by various methods.

Four-point probe sheet resistance measurements and optical dosimetry are widely used as routine methods by which an immediate feedback on the functioning of the implantation equipment can be achieved. Commercially available equipment can supply contour and/or three-dimensional maps, which are very useful for monitoring the uniformity of the implanter and diagnosing possible problems. The four-point sheet resistance measurements are usually performed on separate monitor wafers, which are given a standard anneal before they can be measured. Doses from 10^{11} ions/cm^2 can be directly measured. By using a special double-implant technique, where two implantations are superposed, the sheet resistance measurements can be performed accurately down to the 10^{10} ions/cm^2 range. The optical dosimetry technique is based on measurements of the darkening of a photoresist layer as a result of exposure to ion beams. Doses down to the 10^{10} ions/cm^2 range can also be monitored with this method.

The chemical concentration of the implanted species as a function of depth, as well as the fraction that is electrically activated after annealing, must be determined. Secondary ion mass spectroscopy (SIMS) is the most popular technique for determining the depth profile of both the selected impurity and any co-implanted contaminants. Rutherford backscattering spectroscopy is often used as a means to calibrate these measurements. The profiles of electrically active dopants are characterized with speading resistance techniques. For profiles deeper than 0.1 μm, these methods can be routinely applied; but for those shallower than 0.1 μm, many extra precautions must be taken to guarantee measurement accuracy. For implantation depths greater than 1 μm, lapping and staining offers a rapid method of determining the junction depth. Capacitance–voltage measurements for profiling the active dopant concentration are applied both in-line and as a part of the final electrical characterization (22,23).

Both the as-implanted damage and the damage that remains after various annealing cycles, are studied by techniques that are typically used to study defects in semiconductors. A variety of chemical etchants can be used to make defects and amorphous layers visible, thus allowing inspection with optical microscopy or scanning electron microscopy (SEM). Direct imaging of the surface is also possible with transmission electron microscopy (TEM), and cross-sectional TEM gives information on the location in depth of the damage. Rutherford backscattering, X-ray topography, and infrared absorption techniques can give information on the degree of crystallinity. The electrical device characterization is, however, always indispensable, since it will often reveal damage-related leakage currents that cannot be predicted by analytical methods.

MODELING AND SIMULATION OF IMPLANTATIONS

The simulation of implanted doping profiles plays an important role in the development of today's IC processes. A large number of both physical and phenomenological models have been developed to predict the doping profiles which result when implantation processes are included in a complete process sequence. Many of these models are included in commercially available process simulation programs such as SUPREM-3 and SUPREM-4.

The as-implanted impurity profiles can be well described by a number of models with increasing degrees of applicability and accuracy. One set of extensively used analytical models is based on the Lindhard, Scharff, and Schiott (LSS) theory for implantation into amorphous material (24). In the simplest form a Gaussian distribution is assumed. This gives a quite accurate determination of the range and the projected range and straggles. The experimental doping profiles will, however, in most cases deviate from the Gaussian profile. In amorphous material some degree of asymmetry or skewness is usually observed in the profiles. For boron in silicon a significant amount of backscattering of these light atoms will occur when they collide with target atoms, resulting in a higher doping concentration at the surface. On the other hand, for heavier ions such as arsenic, deeper junctions than predicted will be produced. Such effects can be described by using probability distributions with higher order moments. The skewness is well described by a Pearson IV distribution function which uses four moments. For implantations directly into crystalline silicon, the channeling tail is described by adding an exponential tail to the Pearson IV distribution.

For implantations in multilayer substrates (e.g., implantations through oxide layers on the silicon surface), the assumptions of the LSS theory are no longer valid. Models based on numerical solutions rather than analytical techniques are then employed. These include the solution of the Boltzmann transport equation (BTE), which is valid for layers on amorphous substrates. The most general method uses the Monte Carlo simulation technique, which is also applicable to complex two-dimensional structures on crystalline substrates. In this approach, ion implantation is simulated by following the history of an energetic ion through successive collisions with target atoms, using the binary collision assumption. To predict the profile, a large number of trajectories must be calculated, and the main concern is to reduce calculation time without sacrificing accuracy.

The simulation of doping profiles after annealing can be performed with reasonable accuracy if the main diffusion mechanism is normal thermal diffusion. However, for the simulation of, for example, transient diffusion phenomena, low-temperature diffusion, and co-diffusion of dopants, it becomes important to couple the diffusion model to implantation damage models. Many such models have been developed and include such effects as point defect generation during implantation, clustering at high dopant concentrations, and coupling between point defects and individual dopants. Many coordinated efforts from research institutes and universities in cooperation with industry led to quick commercialization of new data and model improvements. Among other things, databases of one- and two-dimensional doping profiles are gathered, and the resulting phenomenological models are adequate for solving many process problems.

ION IMPLANTATION SYSTEMS

Ion implanters are quite complicated machines where high demands are placed on the process control and productivity (25). The use of high voltages and toxic gases has also made safety a prominent consideration in the equipment development. The wide spectrum of implantation doses and energies required in IC production have meant that no single machine strategy has been considered profitable in terms of cost of ownership and overall equipment effectivensss. Dedicated equipment has therefore been developed and can basically be classified as follows:

1. High-energy implanters with an ion beam energy up to 10 MeV
2. Low-energy implanters with an ion beam energy down to 200 eV
3. Medium-current implanters with ion beam currents up to 2 mA
4. High-current implanters with ion beam currents up to 35 mA

Ion-implantation systems are large: Typical dimensions are $5 \times 3 \times 3$ m^3, with weights ranging from 900 kg to 1600 kg. The main parts, illustrated in Fig. 1, are the ion source, the beam-line, and the end station.

Ion Source

Figure 12 shows the design of an ion source. Most commonly, gas molecules are fed into the ion source from a gas cylinder, in which the species to be implanted is diluted in a carrier gas such as H_2. Alternatively, the desired species is produced by evaporating from a solid inside the ion source itself. A plasma is then generated at low pressure by means of one or two filaments and the arc-voltage, whereby the gas molecules are ionized. If, for example, the source gas is BF_3, a variety of ions such as BF_2^+, BF^+, $^{10}B^+$, $^{11}B^+$, and $^{11}B^{2+}$, are created. A negative extraction voltage at the outlet of the source will accelerate the positive ions into the beamline. The efficiency of the source determines the size of the ion beam current. Obtaining a high efficiency is particularly important for high-current implanters and for enabling the implantation of doubly or triply charged species, which are normally generated in much lower concentrations than the corresponding singly charged ions. Lowering of the operating pressure and optimization of the ion source design have led to enhanced beam plasma confinement and higher discharges of the source gas. Consequently, noteworthy production of multicharged ions such as P^{2+} and P^{3+} has been achieved.

Beamline

In the beamline a uniform ion beam of the desired species, energy, and charge must be produced from the multitude of ions created in the ion source. The construction of the individual beamline parts and the sequence in which the necessary operations are performed will depend on the implanter type and application, but the following main parts can be identified:

1. *The Mass Separator.* The positive ions from the ion source go through a magnet analyzer and are separated according to mass and charge. By adjusting the magnetic field strength, the path of the ions of interest can be given a specified radius of curvature and they will pass through a resolving slit. To increase the ion beam current and thus decrease the implantation time, a wide slit can be set. The trade-off is that a larger num-

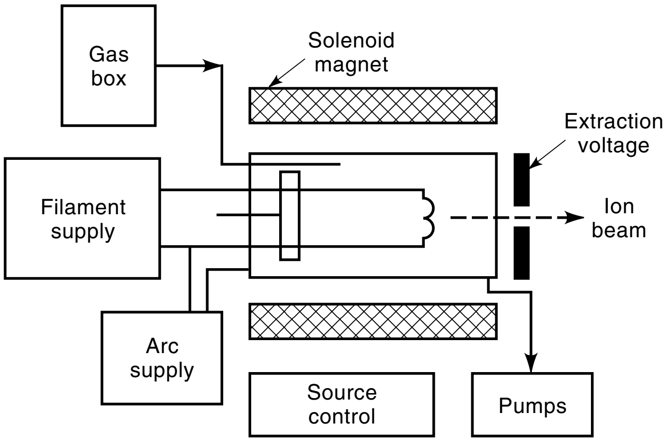

Figure 12. Schematic of an ion source. The source itself is immersed in a magnet field that is oriented parallel to the axis and a spiral trajectory of electrons is created, thus increasing the ionizing efficiency of the source.

ber of isotopes and mass interference contaminants may pass the slit as well.

2. *The Lens and Scanner.* In the lens section, the ion beam is focused to give either a round spot-sized beam or an elongated ribbon-shaped beam that extends over the width of the wafer. The shape of the beam that is chosen depends on the equipment design. The spot-sized beams are scanned across the wafer in both the X and Y directions. On the other hand, the ribbon-shaped beam needs only to be scanned in one direction. This reduces the complexity of the wafer scanning system, which can be either electrostatic, magnetic, or mechanical.
3. *The Accelerator and Decelerator.* In the extraction of the ions from the source, the ions receive their initial acceleration energy. After mass separation and focusing, the ions can be further accelerated (or decelerated) in the acceleration column; the final energy is the sum of both accelerations. To increase the energy capability of the implanter, doubly or even triply ionized species can be implanted. For an acceleration voltage V, the ion energy E is then

$$E = mqV \qquad (6)$$

   where m is the number of ion charges (1, 2, . . .) and q is the charge of an electron. Normally, doubly ionized species are produced less abundantly in the ion source, so beam currents are typically smaller and implantation times are longer. The beam purity is also compromised by ions that have lost a charge, and a significant number of atoms with much lower energy may also be implanted.
4. *The Neutralizer.* Before entering the endstation the ion beam is purified by using electrostatic plates to deflect the ions and filter out neutral atoms and other contaminants.

Endstation

Wafers in cassettes are loaded into the implanter via a vacuum load-lock, and a robot handler transports them to the endstation. Implanters have either a batch-type or serial-type endstation. In a batch-type implanter, for example, about seventeen 200 mm wafers can be clamped to a disk spinning at up to 1200 rpm through the ion beam. Serial processing, however, can become more economical for wafer diameters of 200 mm and above. The individual wafer is then clamped electrostatically to a chuck by using alternating current (ac) voltages of several hundred volts, as shown in Fig. 13. A ring of holes in the chuck near the backside of the wafer are used for gas cooling with, for example, nitrogen. The wafer temperature can then be kept below 100°C, even when it is coated with a patterned photoresist layer. Particularly for high-current or high-dose implants the wafer temperature may otherwise rise to several hundred degrees Celsius, which endangers the integrity of the photoresist masking layer. The chuck is designed to eliminate sputtering contamination from the disk, clamps, or other exposed metals near the wafer. Serial processing is also more flexible with respect to the control of channeling and mask shadowing effects. The wafers can be tilted from 0° to ±60° and rotated during implantation by steps of 0° to 360°.

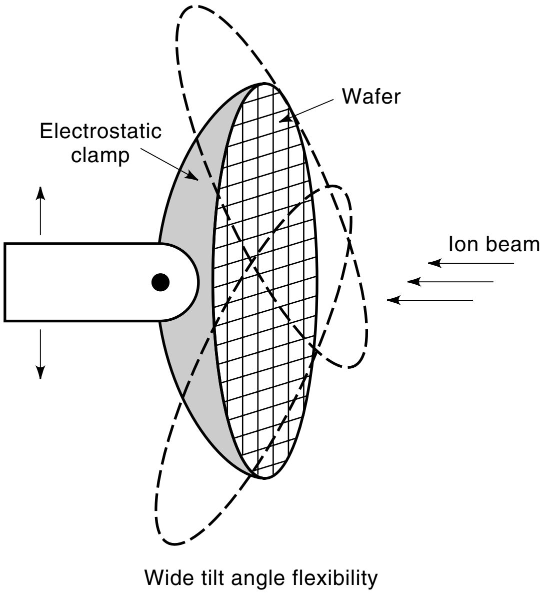

Figure 13. Example of an electrostatic chuck used in a serial implanters.

Ion doses are measured in a Faraday cup construction, where the actual beam current is sampled every millisecond and integrated over the implantation time. The total dose Q is calculated as

$$Q = \frac{It}{Amq} \qquad (7)$$

where I is the beam current, t the implantation time, and A the implanted area. Modern Faraday systems also monitor the beam profile, the overall ion dose, and the stability of the beam during implantation, thus enhancing the uniformity, accuracy, and reproducibility of the implantations. Typical specifications for the nonuniformity of the implanted ion dose are $\leq 0.5\%$ ($1\ \sigma$) over the wafer as well as from wafer to wafer.

Wafer Contamination

Historically, ion implantation is considered an inherently clean process compared to other IC-manufacturing techniques. The increasing demands for ultra-clean processing have, however, made the elimination of wafer contamination an issue of major importance in the design of implanters. The purity of the ion beam itself must be safeguarded at all stages of the implanter. The ions selected in the analyzer travel through the rest of the beamline and the endstation before hitting the wafer surface. Collisions with critical areas in the beamline and endstation or with any residual gases can lead to discharging of the ions as well as a change of the implantation energy. At the same time, species from previous implants (e.g., B) can be sputtered and may receive enough energy to penetrate the target surface. Improvements in the beamline and endstation constructions to prevent collisions have resulted in high levels of beam purity. Typically, modern implanters do not add more than 0.1 particle/cm^2 silicon surface (particle size $\geq 0.16\ \mu$m), and beam impurity contamination is less than 1%.

The main source of particle contamination is mechanically generated particles. To minimize this in the wafer handling, for example, only backside wafer contact is made with the robot arm. Particles are also generated during implantation, particularly at high ion beam currents. Erosion of beamline components, typically those made of graphite, and micro-discharging are common causes of the elevated defect levels. Optimization of the beamline design, including the coating of metal parts with Si and SiC, has dramatically reduced the number of Al, Fe, and Cr atoms found on the wafer surface.

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Lis K. Nanver
Egbert J. G. Goudena
Delft University of Technology

ION IMPLANTATION. See Plasma implantation.

IONIZATION. See Field ionization.