GATE AND TUNNEL DIELECTRICS, MANUFACTURING ASPECTS

The scaling of the gate oxide thickness of high-performance complementary metal-oxide semiconductor (CMOS) devices is nearly linear with the channel length. The limitation on how thin the gate oxide can be is determined by many factors. Whether these factors are based on device optimization for high performance, low power or reliability, it is obvious that the state-of-art devices will be using oxides with thicknesses below 100 Å. Thicknesses below 40 Å or less for future CMOS devices have been projected, with corresponding reductions in supply voltage and power.

The thin oxide layers play a critical role in the memory cell of nonvolatile memories. These oxides, called *tunnel oxides,* pose especially difficult problems because of their double role:

- The oxide needs to be an insulator with low leakage current during reading and data storage.
- The oxide needs to be a conductive medium with very high breakdown voltage during the programming and erasing mode.

The minimal thickness of tunnel oxide, unlike gate oxide, is limited to approximately 60 Å to 70 Å due to direct tunneling through the thinner oxide. Direct tunneling may increase the leakage current to a level that is incompatible with the data-retention characteristics of the memory cell. Because of the demand for 10^5 to 10^6 programming/erasing cycles, the tunnel oxide is exposed to bipolar stress with the electric field very near the intrinsic oxide breakdown limit. The requirements on the oxide quality are extreme.

For MOS devices the scaling has led to high electric fields, giving rise to hot-carrier injection close to the drain region. Hot carriers injected into the oxide gradually degrade the device performance. For nonvolatile devices, the oxide is stressed by tunneling. In addition, the high concentration of the drain region may induce band-to-band tunneling. Tunneling and hot-carrier injection have a different oxide degradation mechanism.

Scaling and integration require not only thinner oxides but also relatively low-temperature processing in order to minimize the thermal budget. The oxide manufacturing process needs to be carefully optimized to satisfy various conflicting requirements. To cope with these challenges, the control of complex process parameters is mandatory. Recently, the capabilities of manufacturing equipment to control the process have improved significantly. However, the control of oxide properties such as thickness, growth rate, charge, and density of interface traps, which are of technological importance, still remains largely empirical.

A word needs to be said about the published data. Most of the results of oxide investigation are reported only in terms of the breakdown voltage or the charge or time to breakdown. The conventional breakdown voltage test, time to zero breakdown (TZDB), when performing voltage ramps, is not a reliable parameter if the measured oxides exhibit trapping behavior dependent on the stressing voltage, as it is in the case of tunnel oxides. The time-dependent dielectric breakdown (TDDB) test is a more sensitive breakdown characterization technique. However, it cannot detect the phenomena related to the low electrical field, such as stress-induced oxide leakage, because the measurement and breakdown voltage concentrate on the high-current and high-electrical-field region.

It is also well documented that the electrical parameters of oxide depend strongly on the properties of the silicon substrate itself, the preoxidation clean, the delay between the preclean and oxidation, and the loading and ramp-up cycle before oxidation (Fig. 1). These dependencies are different for thick and thin (<100 Å) oxides. As a consequence, if the oxide history is not known, it is almost impossible to compare experimental data done under different conditions and the benefit of such published data is debatable. The reason for the apparently conflicting results obtained by different workers is primarily due to the difficulties of characterization of thin oxides, and secondarily due to the fact that the final property of oxide depends on the complete sequence: preclean–loading–oxidation–unloading. As already mentioned, such data are very seldom described completely.

For thick oxides (thicker than 200 Å) a wealth of knowledge of the phenomenological behavior of these oxides has been accumulated. A good summary of the topics can be found in the classical works (1,2). Certain caution needs to be exercised in the interpretation of the conclusions formulated in the early works because the state-of-the-art silicon substrates have very different properties from those used two decades ago.

The properties of thin oxides are different from those for thick oxides. The tacit assumption underlying the scaling of oxide thickness is the invariance of the oxide charge and the interface traps density on the oxide thickness. However, when the oxide thickness is reduced to a thickness less than 100 Å, the assumption of the invariance of oxide charge, interface trap density on the oxide thickness, and the dependence on

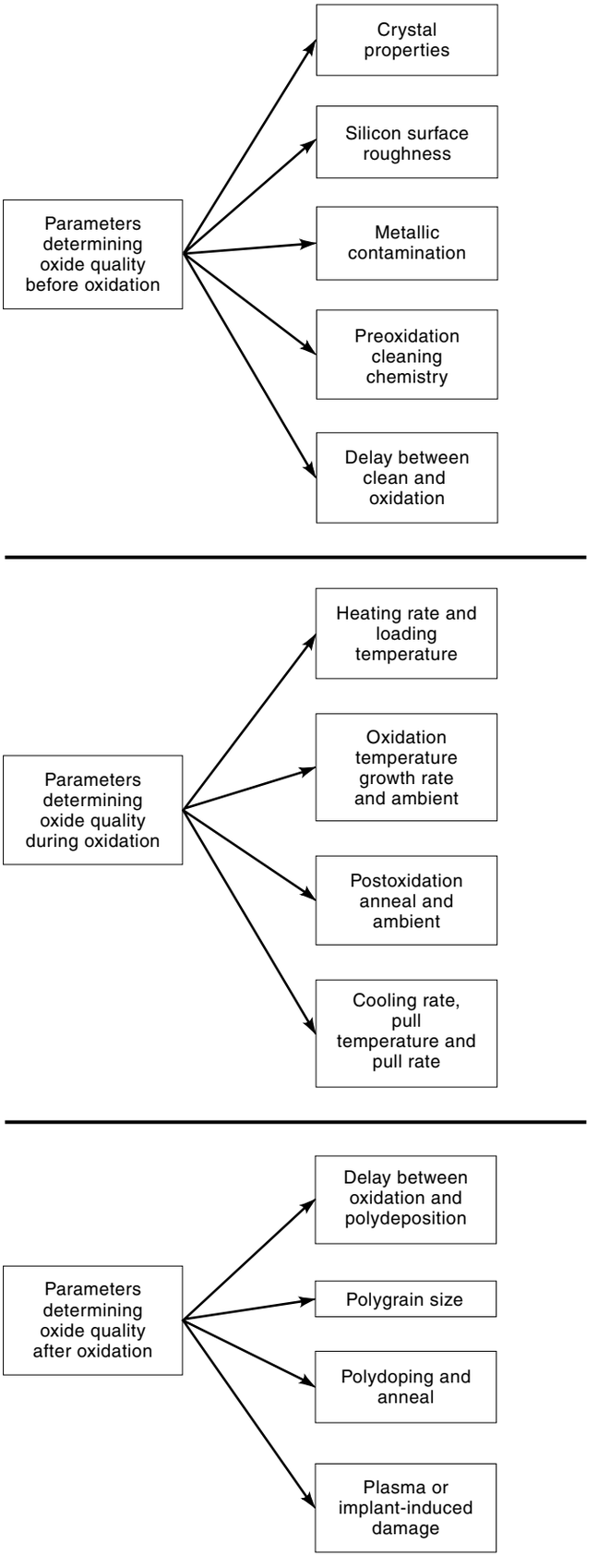

Figure 1. Processing conditions defining the oxide quality.

the processing as described for the thick oxide are no longer valid. Results of Hung and Cheng (3) show that postoxidation anneal of thin oxides, even with optimal conditions, cannot reduce the fixed oxide charge to a value comparable to that of thick oxides. Additionally, very interesting properties unique to the thin oxides have been reported. These include the higher dielectric breakdown field, an increased polarity dependence of dielectric breakdown in thin oxides (4) with degraded Q_{BD} behavior under negative bias (5,6), a sharp increase in the interface state density D_{it} (7), and fixed oxide charge density (8) with decreasing oxide thickness.

The reason thin oxides behave differently may be explained by the thickness dependence on the stress at the Si/SiO_2 interface. As the wafer is cooled from the oxidation temperature, the difference in the thermal expansion coefficient of Si and SiO_2 causes the oxide to be under compression stress. Stress in the oxide is approximately uniform through its thickness. This will result in a linear increase of the stress with increasing thickness of oxide. The thickness dependence would appear to imply some process involving the bulk of the oxide. However, no conclusive data are available, and the origin of the thickness dependence remains a mystery.

The different aspects related to the manufacturing of thin oxides are reviewed here. The first section focuses on the properties of the transition structural region at the interface between Si and SiO_2. The second section discusses the impact of the imperfection of the manufacturing equipment on thin oxides. Finally, the last section summarizes the results and provides the conclusions.

THIN OXIDE STRUCTURE

The electrical behavior of oxides is strongly dependent on the conditions of the oxide growth process. It is well established that before destructive breakdown of the oxide layer occurs, several degradation phenomena such as trap creation, charge accumulation, interface state generation, and leakage current enhancement have been observed. Ning et al. (10), Naboru (11) and others demonstrated that oxide charge in an as-grown oxide is correlated with the rate of generation of traps created during oxide stressing. Devine (12) reported that some types of defects in oxide cannot be created during oxide stressing. The defects or traps must be present in the oxide as precursors as a result of the oxide-processing step.

For a thin SiO_2 film, a large number of properties will be affected, or even controlled, by the microscopic structure of the Si/SiO_2 interface. A distinction needs to be made between two factors:

1. The roughness of the silicon surface and its evaluation during oxidation
2. The structural transition region between the crystalline silicon and amorphous SiO_2

The surface roughness is determined by the processing before oxidation. The structural transition region is due to the mismatch in the atomic structure of the Si/SiO_2 interface. This mismatch results in the presence of strained layers on both sides of the interface relaxing the stress produced by oxide formation (13).

Both factors are strongly correlated. Koga et al. (14) reported that the local stress at the Si/SiO_2 interface controls the "smoothing" of interface roughness. Hasegawa (15) showed that a decrease in the thickness of the structural transition region at the Si/SiO_2 interface results in a better oxide performance. Based on these results it is clear that from the device point of view, minimization of the thickness of the transition region and the Si/SiO_2 interface is preferable.

The structural transition region in the silicon substrate takes place with displacement of not more than two silicon layers, while the structural transition region in oxide consists of several sub-regions as illustrated in Fig. 2:

- The layer at the interface is known to consist of a mixture of Si suboxides denoted as Si^{+1}, Si^{+2}, and Si^{+3}, where the Si atoms have one, two, and three first-nearest-neighbor oxygen atoms.
- In the bulk oxide, the network consists of silicon mostly in six-tetrahedra rings with the 144° silicon–oxygen–silicon bond angle. There may be also some numbers of four- and eight-member rings with 120° and 180° bond angles.
- To accommodate the structural deviation between the bulk and suboxides, there is a layer with three-, five-, and seven-member rings. The bonds are strained and their density increases towards the Si/SiO_2 interface. This transition layer has a lower density than the immediate bulk SiO_2 layer.

Yasuda and Toriumi (16) demonstrated that based on the measurement of the peak wave number of the oxide absorption band, the amount of strain caused by stress as a result of lattice mismatch between the silicon and oxide gradually decrease with increasing distance from the Si/SiO_2 interface.

Some authors observe that the interface roughness of wet oxides is different from dry oxides and they suggest that the type of the oxidizing ambient is critical. Satake et al. (17) report that the strain gradient of the peak wave number at the Si/SiO_2 interface is lower for wet oxides. Fang et al. (18) concluded that the amount of stress at the Si/SiO_2 interface is associated with the reaction between diffused oxygen and silicon at the interface.

If we consider the diffusivity and solubility of H_2O and O_2 in SiO_2 as published in Ref. 19, we can easily calculate the initial oxide thickness that must be present on the silicon surface in order to proceed with reaction-controlled oxidation.

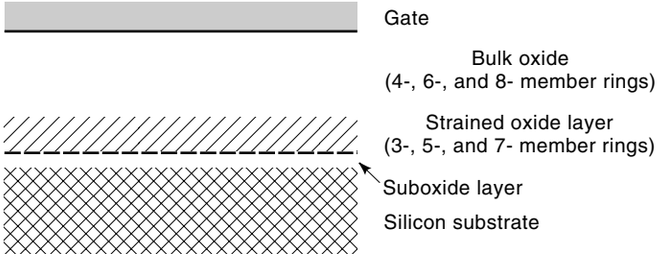

Figure 2. Schematic illustration of thin thermal oxide structure.

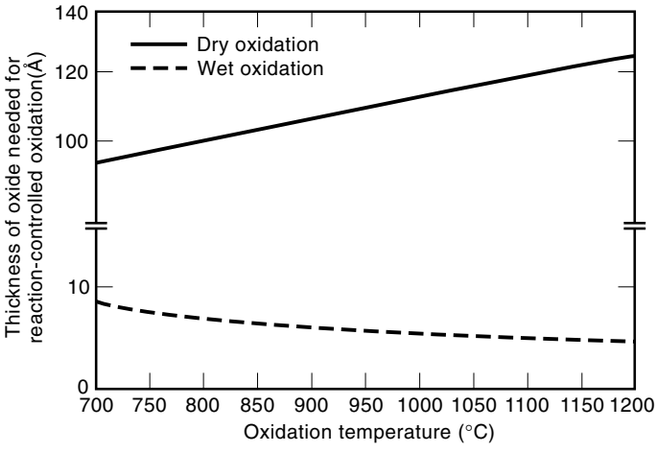

Figure 3. Calculated thickness of the oxide needed for reaction-controlled oxide growth. (The calculation is based on the Grove-Deal oxidation model.)

Results of such calculations are plotted in Fig. 3. Reaction-controlled oxidation will be dominated for all oxidation temperatures in wet ambient if the initial oxide is thicker than approximately 8 Å to 10 Å. For oxides thinner than 100 Å, the dry oxide will be grown only by the initial rapid oxidation mechanism. The diffusivity of H_2O in SiO_2 is lower than the diffusivity of O_2. Therefore it is plausible to expect that the diffusion-controlled mechanism will occur during the later phase of wet oxidation. Under the diffusion-controlled oxidation mechanism, the oxidant diffuses more "uniformly" towards the Si/SiO_2 interface. Niwa et al. (20) suggest that under such conditions the Si/SiO_2 interface will form smooth morphology so that large undulations localized at the interface release the stress introduced during oxide growth.

When the surface is cleaned before oxidation by conventional wet cleaning, the interface initially tends to become rough and gradually smoothes as the oxide thickness grown in the dry oxidizing ambient increases. This is demonstrated in Fig. 4, where the evaluation of the surface roughness as measured by atomic force microscopy (AFM) is shown. The virgin *p*-type ⟨100⟩ substrates were conventionally cleaned in SC-1 and immediately loaded into the oxidation furnace. The oxidation was performed in dry oxidizing ambient at 900°C.

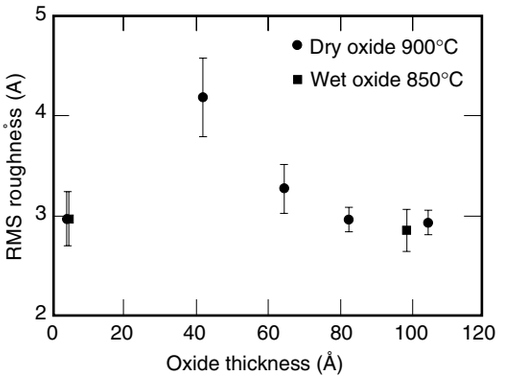

Figure 4. Silicon surface roughness evaluation as measured in 1 mm^2 area for dry and wet oxidation.

A similar experiment was performed at the same oxidation temperature by diluted wet oxidation with a H_2/O_2 flow ratio of 0.5. Due to the fast wet oxide growth rate, only one oxide thickness was verified. No difference in the surface roughness of silicon substrate after wet oxidation was found for the oxide thickness of approximately 100 Å.

Data in Fig. 4 are consistent with previous observations (18). The variation of interface roughness among samples grown in different oxidizing ambient and different temperatures seems to be very small as long as the thickness of oxide is the same. This implies that the dominating factor determining the Si/SiO_2 roughness is the oxide thickness.

From the preceding discussion we can draw an important conclusion. The properties of the thin oxides are significantly affected by the structure of the transition region.

If manufacturing equipment is not well characterized and is not operating under controlled conditions, the "initial oxide" in the structural transition region may originate as an extraneous oxide produced during the push-in, purge, or temperature ramp-up phase due to the residual oxygen in the processing chamber. This may result in significant variation and uncertainty of the oxide performance with uncontrollable reproducibility of processing. Therefore, the processing ambient needs to be under control not only during oxidation at high temperature, but also during the complete processing sequence regardless of temperature.

THIN OXIDE MANUFACTURING EQUIPMENT

Currently, most high-temperature oxidation processes are conducted in either horizontal or vertical batch furnaces. Up to the mid-1980s, horizontal furnaces were used almost exclusively for all processes requiring thermal treatment. As the geometric features of the scaling device were reduced and wafer size was increased, the industry shifted to vertical furnaces. In addition to better temperature control, the main advantage of vertical furnaces in comparison with conventional horizontal furnaces is superior control of the processing ambient. Most modern vertical furnaces are equipped with load lock and nitrogen purge of the loading and unloading area.

Recently, single-wafer thermal processing (RTP) has emerged as a viable technology for thermal processing of semiconductors with excellent capabilities of controlling the temperature and processing ambient. Unfortunately, the time required to transport wafers to the load lock, process chamber, and cooling station has seriously limited the throughput of the single-wafer processing systems. Hence economical rules dictate the use of the batch system, where the processing of 100 to 200 wafers is common.

It is obvious that due to the increasing thermal mass of silicon substrates and due to increasing process complexity, it is increasingly difficult to maintain semiconductor thermal processing in large batch systems. There is an urgent need to reduce the cost of manufacturing by developing new approaches such as single-wafer processing, tool clustering, and in situ process control.

MANUFACTURING ISSUES RELATED TO THIN OXIDE PROCESSES

In the oxide thickness range below 100 Å, the Si/SiO_2 interface becomes a substantial fraction of the oxide thickness, and

good control of the interface becomes mandatory during the manufacturing process. In addition, unwanted oxide growth during the loading and unloading phase and during the purge and temperature ramp-up need to be well controlled. Even a small change in the thickness of the oxide or a variation of its uniformity may be significant if the thickness of the oxide needs to be controlled within the range of a few angstroms.

Here we are not considering oxide variations due to the poorly profiled furnace. A properly profiled temperature is the fundamental assumption for thin oxide processes. There is always some temperature offset between spike and profile temperature. This offset is the function of the processing gas flow. If the temperature profiling is completed under different processing conditions, significant differences in the temperature distribution may occur.

From the manufacturing point of view, the main concerns are as follows:

1. Si/SiO_2 interface control and minimization of the surface roughness
2. Control and minimization of the as-grown trap sites contained in oxide film
3. Minimization of unwanted (and not well controlled) oxidation during loading, unloading, and purging due to the residual oxygen in the processing tube.

The impact of the interface on the performance of the device depends on two factors. First, as reported by Ohmi et al. (21), the dielectric breakdown of thin oxides degrade rapidly with increasing interface roughness. Second, to suppress the short channel effects, the channel concentration needs to be increased. This will result in a high electrical field along the channel length with minority-carrier mobility dominated by surface roughness scattering. A decrease in the mobility will degrade the drain saturation current (driving current), which has the strongest impact on the circuit speed.

As-grown oxide traps are related to metal contamination on the Si surface, contamination during processing, or due to the residual moisture in the processing atmosphere. If the oxide preclean processes and equipment itself are not the source of metallic contamination, metal-related as-grown traps can be neglected. The most important of these are traps generated during oxidation or postoxidation annealing.

Traditionally gate tunnel oxides have been prepared by the dry oxidation method at relatively high temperatures. Conventional high-temperature (~1000°C) dry oxidation inevitably generates weak and/or dangling bonds. In addition, the high oxide growth rate is inapplicable to thin oxides from the manufacturing standpoint because the oxidation time is shorter than the processing time, which can be reproducibly controlled in batch systems. The pyrogenic oxidation was in the past unsuitable for the gate oxide application. It is common knowledge that hydrogen atoms form centers that act as traps. For this reason thicker wet oxides (>200 Å) exhibit enhanced charge trapping. Since charge trapping decreases with the oxide thickness reduction, this issue is less important for thin oxides, even with the use of wet oxidation.

Equivalent performance results have been reported for thin dry and wet oxides. From the reliability point of view thin wet oxides are marginally better, while dry oxides present a lower charge to breakdown, especially for structures involving the field oxide periphery. Presence of the field oxide periphery causes an enhancement of the charge trapping (22).

Robust manufacturing must result in excellent thin oxide thickness reproducibility, thickness uniformity, and high dielectric breakdown field. In order to achieve these goals, ultra-thin gate and tunnel oxides are formed currently by one of the following methods:

- Lowering the processing temperature
- Diluting the oxidant gas and/or reducing the oxidant pressure
- Low-temperature pyrogenic oxidation

Numerous experimental observations indicate that the dielectric properties and manufacturing stability of the oxides are often degraded under these oxidation conditions. One of the most significant factors causing this degradation is the residual oxygen and moisture included in the processing ambient during the wafer loading and unloading. On the other hand, it is well understood that if the silicon surface with native oxide is exposed at high temperature in ambient deficient of oxygen, the volatile component SiO can degrade the Si/SiO_2 interface and increase the surface roughness.

The impact of residual oxygen and moisture in the processing gases on the dielectric properties of oxides is determined by the following equipment parameters:

- Processing tube door closure and seal
- Purge rate and purge time
- Wafer loading and unloading procedure
- Position of the wafer inside the processing tube
- Quality and purity of used processing gases

In the next section it is shown that the suppression of the residual oxidizing ambient is critical for thin oxides.

RESIDUAL OXIDE GROWN DUE TO THE AIR BACK-DIFFUSION

There is significant difference in the control of the air back-diffusion between horizontal and vertical furnaces. Vertical furnaces, unlike horizontal furnaces, use the load lock or nitrogen purge of the loading space to prevent air diffusion into the processing tube.

Figure 5 shows the typical oxygen concentration at the center of the quartz tube in the conventional horizontal fur-

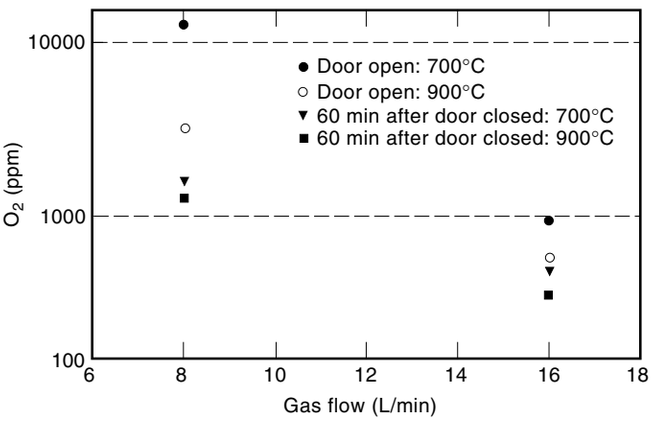

Figure 5. Residual oxygen concentration as a function of the nitrogen purge flow for a 150 mm atmospheric horizontal furnace.

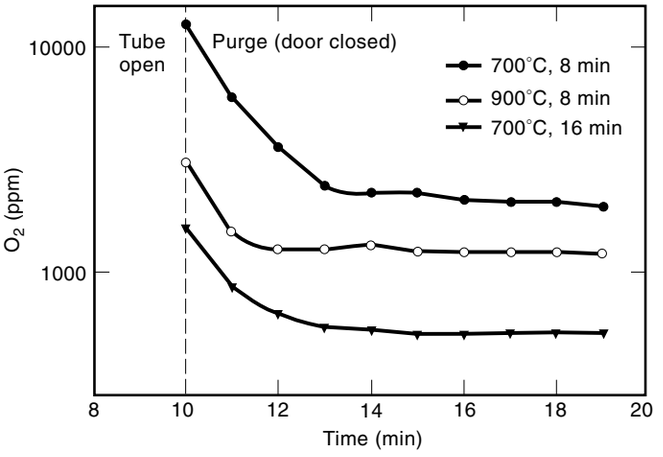

Figure 6. Residual oxygen concentration as a function of the nitrogen purge time for a 150 mm atmospheric horizontal furnace.

nace. The volume of the tube is approximately 84 liters and the oxygen concentration has been measured by a zirconia cell gas analyzer as a function of the different gas-flow rate. In this experiment a full load of wafers was inserted into the processing tube under the following conditions:

1. Load at an idle temperature of 900°C.
2. Load at an idle temperature of 700°C and then ramp up to 900°C.

In both experiments two types of gases were used:

1. House-gas-purity nitrogen with less than 500 ppb of O_2 and less than 450 ppb of H_2O and house-purity oxygen with less than 3000 ppb of H_2O
2. High-purity gases from a liquid source with 100 ppb of O_2 and less than 50 ppb of H_2O and house-purity oxygen with less than 500 ppb of H_2O

Oxygen concentration was measured at the center of the tube immediately after wafer load insertion was completed and 60 min after the door was closed. No major difference was found in the oxygen concentration for loading to 700° or 900°C. The decrease in oxygen concentration for high-purity gases was also insignificant. Clearly the equipment itself, the conventional horizontal furnace, was responsible for this result. The gas flow has the biggest impact on oxygen concentration, and therefore the flow rate during loading and purging needs to be very high. A twofold increase in the flow rate reduces the oxygen concentration by a factor of 100.

The decrease of the oxygen concentration during the purge (after the tube door closed) is shown in Fig. 6. The dramatic decrease of the oxygen was observed during the first 5 min of purging. However, even after 60 min of purging the oxygen concentration did not fall to a point where it could be ignored.

Surprisingly, no significant difference in residual oxygen concentration was found for high-purity gases if used in an atmospheric horizontal furnace.

A similar experiment was executed for the 200 mm vertical furnace with load lock. The oxygen concentration in the center of the tube after a 10 min purge was lower than 1.8 ppm for both processing temperatures.

Initial oxide growth cannot be disregarded for reasons described previously. In order to verify the impact of the residual oxidizing ambient on the oxide thickness the full load of wafers, shielded on both ends by 10 dummy wafers, was inserted into the conventional horizontal furnace. The loading temperature was maintained at 700°C. Loading was followed by purge and temperature ramp-up to 1000°C. During the processing, nitrogen was the only gas present in the processing tube. After unloading, the oxide thickness was measured on all wafers. Figure 7 shows the results for the two nitrogen flow rates. In this plot, wafer number 1 was the first wafer following the 10 dummy wafers at the source (tube gas inlet) side. The thickness of oxide was measured at the center of the wafer and at the position corresponding to the top position when the wafers were in the processing tube. In this experiment the wafer flat was oriented towards the top of the processing tube, and the crown of the wafers was on the bottom of the processing tube. Results indicated that for low nitrogen flow, the first 30 wafers (40 wafers including dummies) exhibit oxide thickness variation. Thickness of the oxide was marginally lower at the center of the wafer. This could be explained by the fact that in the atmospheric horizontal furnace used in this experiment, the profile and spike thermocouples were placed on the bottom of the tube. The heaters symmetrically surround the quartz tube. Due to natural thermal convection, the top of the tube may be hotter.

Although this experiment is somewhat the extreme, it clearly indicates how important the impact of the residual oxygen can be on the oxide nonuniformity. However, the main problem remains: the "initial oxide growth" during loading and purging begins when the wafers are at a low temperature and not in thermal equilibrium. As a consequence, the structural transition region that has the biggest impact on the performance of thin oxides is not formed by the reproducible process with the same stress between the Si/SiO_2 interface.

The oxide thickness nonuniformity can be reduced by the higher wafer loading speed. Increasing the boat speed can decrease oxide thickness because the actual oxidation time at the phase when the door of the tube is open decreases. The

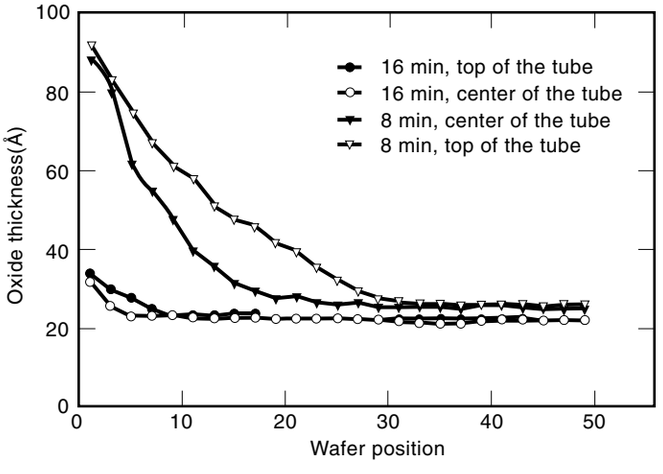

Figure 7. Oxide thickness grown due the residual oxygen concentration in a 150 mm atmospheric horizontal furnace.

lattice crystalline defects limit the loading speed. The only reasonable way to minimize the residual oxygen concentration is to increase the flow rate during loading and purging.

The experimental results described here do not allow the separation of the grown oxide thicknesses between the loading and unloading phases. However, for the range of oxide thicknesses 80 Å to 100 Å, the loading phase dominates. As the thickness will continue to decrease, it is reasonable to expect that even the unloading phase will become critical.

CONCLUSION

The physical properties and electrical performance of thin oxides are determined by the properties of the interface and by the structural transition region on both sides of Si/SiO_2 interface. Thick oxide performance is determined mostly by properties of the bulk oxide; however, for thin oxides the structural transition region is a significant part of the final oxide thickness. Therefore, in addition to all processing parameters that are important for thick oxide processes, control of the Si/SiO_2 interface and the condition of the initial oxide growth need to be precise.

The loading of wafers into the processing tube and the purge phase are critical. It has been demonstrated that the significant oxide thickness may increase if the equipment and/or processing recipe is not well characterized. The flow rate of nitrogen gas has been identified as a critical factor. Even if high-purity gases are used in conventional atmospheric horizontal furnaces, the level of the residual oxygen in the processing tube is unacceptably high.

It has been shown that the batch size needs to be reduced as long as thin oxide performance is concerned. Although vertical furnaces are capable of controlling the thin oxide growth by nitrogen purge during loading, load lock, and loading at low temperatures, thickness of the oxide grown in the "initial uncontrollable oxidation regime" is in the range 3 Å to 6 Å. There may be unacceptable variations for oxide thicknesses of 60 Å or less.

The rule of thumb for thin oxidation in furnaces could be summarized as follows:

- Process batches with the same loading pattern (i.e., the same number of products and dummy wafers in load).
- Control the delay between preclean and loading.
- The temperature of the loading should be as low as the system allows.
- The nitrogen flow during loading and purging should be as high as the system allows.
- Do not ramp up the temperature during loading.
- Start the temperature ramp up after the purging cycle is completed and the wafer temperature is in equilibrium with the loading idle temperature of the processing tube.
- During the temperature ramp up, scale down the flow of purging gas.
- After oxidation, during ramp down, gradually increase the flow of purging gas.
- Pull out the wafers at high purging gas flow.
- Control the delay between oxidation and polysilicon deposition.

Each manufacturing facility and each type of manufacturing equipment has its own footprint. Critical processing steps such as the tunnel or gate oxides cannot be "just transferred." Processing recipes performing well in one manufacturing facility may fail in another manufacturing environment. The complete characterization and recipe optimization need to be performed each time if robust processing is expected.

The optimization of the batch type of processing is usually more expensive and more time-consuming than single-wafer process optimization. Batch thermal processing technology served the industry well for many years. However, with an increasing level of integration and increasing wafer diameter, it is increasingly difficult to optimize the numerous conflicting requirements.

Mainly economical issues are preventing wider application of single-wafer thermal processing, which remains for this reason a challenge with considerable potential benefits.

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