RADIO-FREQUENCY MULTIPLIERS

Frequency multipliers are harmonic generators that produce various frequency multiples of an input (fundamental) frequency. These devices are employed in such diverse applications as electronic instruments, designing radar, communications, and electronic warfare systems. High-frequency signals are generated from lower-frequency signals by harmonic multiplication, as demonstrated in the simple representation depicted below in Fig. 1. In the development of such a device, the circuit designer seeks to maximize the power delivered to the output load at the Nth harmonic.

The capability of optimization of multiplier performance, in and of itself, can improve the overall performance of a system. Such potential for enhanced performance leads to the optimization process becoming a crucial consideration in the development of the system. Multiplier performance is dependent upon the nonlinear device producing the required frequency harmonics and the design technique employed. The most important design considerations in frequency multipliers are conversion gain, harmonic suppression, output power, efficiency, dc bias requirements, and bandwidth. Frequency multipliers exhibiting high conversion gain, good harmonic suppression, wide bandwidth when required, and high efficiency are achieved from optimum designs. As will be discussed in this article, many authors give various, contradictory means of optimizing the performance of frequency multipliers.

One of the dominant operating parameters of a frequency multiplier is its conversion gain or conversion loss. The conversion gain is the ratio of the output power at the desired harmonic frequency to the input power at the fundamental frequency. It has been demonstrated that various parameters affecting the conversion gain include the bias level, the input power, the harmonic terminations, and the nonlinear device producing the frequency harmonics (1–7). Techniques that maximize the conversion gain are necessary for the development of frequency multipliers.

With the advent of new active devices, such as the high electron mobility transistor (HEMT), the pseudomorphic high electron mobility transistor (PHEMT), and the heterojunction bipolar transistor (HBT), new multiplier designs incorporating these devices are desired. This has led to the emergence of new research areas where relatively little information has been reported in the literature. This presentation will address some of these areas. Some areas considered are the development of accurate nonlinear circuit models, identifying pertinent properties of the transistor, optimizing multiplier designs, and improving some of the existing design techniques.

APPLICATIONS OF FREQUENCY MULTIPLIERS

The extension of system operating frequencies into higher frequency bands has led to considerable interest in generating RF power at lower frequencies and using a nonlinear device to achieve RF power at a higher harmonic frequency. Harmonic generators provide a convenient source of signals at higher frequencies, where direct generation from an oscillator is difficult or inconvenient. The frequency multiplier produces an output signal at a harmonic frequency multiple of the fundamental input frequency and eliminates the requirement for a high-frequency oscillator. The ability to design frequency multipliers generating the higher harmonic frequencies has made frequency multipliers important circuits in RF and microwave components, and thus they find a wide range of use in the electronics arena. Applications include instrument design, radar systems, communications systems, subscriber radio systems, and low-phase-noise EW applications.

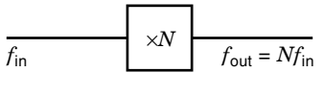

Figure 1. Simple harmonic multiplier.

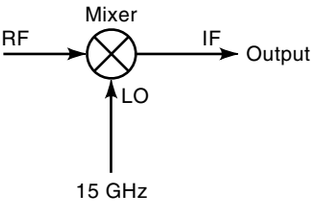

Figure 2. Configuration without frequency multiplier.

Communication Systems

As an illustration demonstrating the convenience of a frequency multiplier, consider a communication system requiring a 15 GHz local oscillator (LO) source as shown in Fig. 2. The configuration shows a 15 GHz source driving the LO chain of the mixer. Alternatively, the 15 GHz source can be replaced by a 5 GHz local oscillator and frequency tripler to obtain the required 15 GHz signal. Advantages in using the 5 GHz source over the 15 GHz source lie in the cost associated with the two sources, because high-frequency components usually are more expensive than lower-frequency ones. Additionally, the 5 GHz source could possibly pose less of a design challenge than the 15 GHz source. With this change in the configuration, the final circuit is represented by Fig. 3.

Frequency multiplier applications have been extended to monolithic microwave integrated circuit (MMIC) receivers in communication systems (8–11). One such application is shown in Fig. 4 (9). In this configuration, two doublers are used in series to supply the LO chain of the mixer. Using these doublers in the topology allows a 6.5 GHz voltage controlled oscillation (VCO) to be implemented. The 6.5 GHz signal is led into the two frequency doubler circuits, which produce an output signal at 26 GHz. Without the use of the two

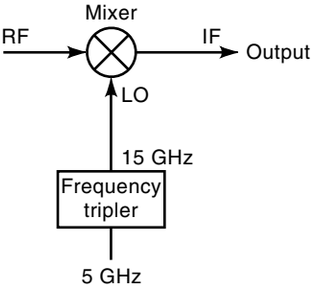

Figure 3. Configuration with frequency multiplier.

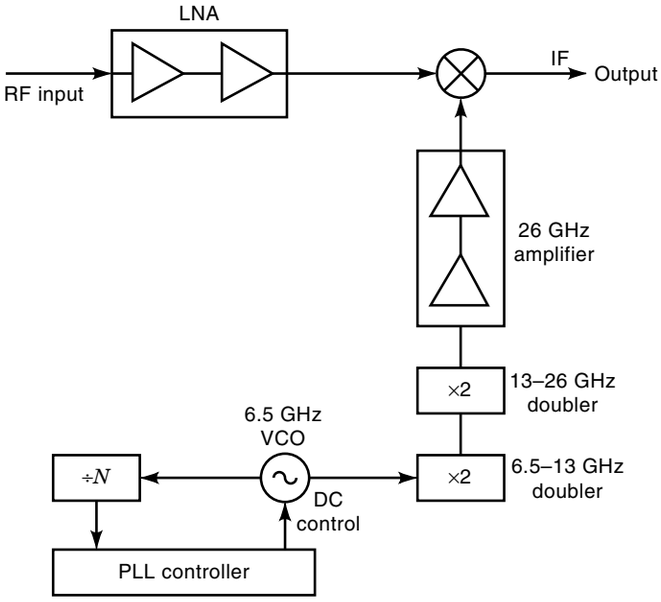

Figure 4. Block diagram of 26 GHz MMIC receiver model.

doubler circuits in the block diagram, a 26 GHz VCO would have been required.

Cellular Applications

Wireless applications operating in the 900 MHz to 2500 MHz range frequently use frequency multipliers in their design topologies. The systems include synthesizers, transmitters, receivers, and transceivers (12). A transmitter topology demonstrating the use of frequency multipliers is shown in Fig. 5. The modulated signal at 450 MHz is multiplied by the doubler to produce a signal at 900 MHz for transmission.

The receiver topology using a frequency doubler is shown in Fig. 6. The doubler is placed in the LO chain of the downconverter. The downconverter produces an intermediate frequency, (IF) which is signal-processed to obtain the desired information from the signal.

As a final example, a block diagram of a transceiver employing the use of a frequency doubler is shown in Fig. 7 (12). This topology uses a single LO source. The doubler is used in the LO chain of the receiver and to produce the transmitting frequency in the transmitter.

PASSIVE FREQUENCY MULTIPLIERS

As previously mentioned, frequency multipliers are harmonic generators that produce frequency multiples of an input (fundamental) frequency. At radio and microwave frequencies, frequency multipliers typically employ a nonlinear device to generate the desired harmonic spectrum. The choice of this nonlinear device divides multipliers into two categories: passive multipliers and active multipliers. In the case of the active multipliers, the nonlinear device includes any of the devices in the transistor classes (BJT, FET, MESFET, etc.), as will be discussed in the following section. This section will discuss the development of passive multipliers. The discussion will include the basic theory and operation of passive multipliers, various devices that are typically used in the development of passive multipliers with their various advantages and disadvantages, the nonlinear mechanism responsible for harmonic production, power considerations, optimization of efficiency, realizations, and design topologies.

Background and Theory

As mentioned, frequency multipliers at radio frequencies typically require a nonlinear element to produce the desired harmonic spectrum. For passive multipliers, this requirement is fulfilled by the exploitation of the nonlinear characteristics of nonlinear resistors, nonlinear inductors, or nonlinear capacitors. The excitation of these devices by an input fundamental frequency produces an output spectrum possessing the desired harmonic output of interest. Typical nonlinear devices providing the aforementioned properties in the development of passive frequency multipliers include rectifying metal–semiconductor junctions with their nonlinear current–voltage characteristics, reverse-biased metal–semiconductor or *pn* junctions with their nonlinear capacitance, and nonlinear transmission lines having distributed nonlinear capacitance (13).

As mentioned, harmonic generation is produced in a passive frequency multiplier whenever a sinusoidal input signal drives a nonlinear impedance. A variable resistance, inductance, or capacitance whose magnitude varies instantaneously with the applied voltage or current characterizes this nonlinear impedance. Semiconductor diodes have been reported throughout the literature as an efficient means of providing the necessary nonlinear characteristics for passive multiplier design (9,11,13–41). The diodes have various characteristics, which produce, as expected, different performance.

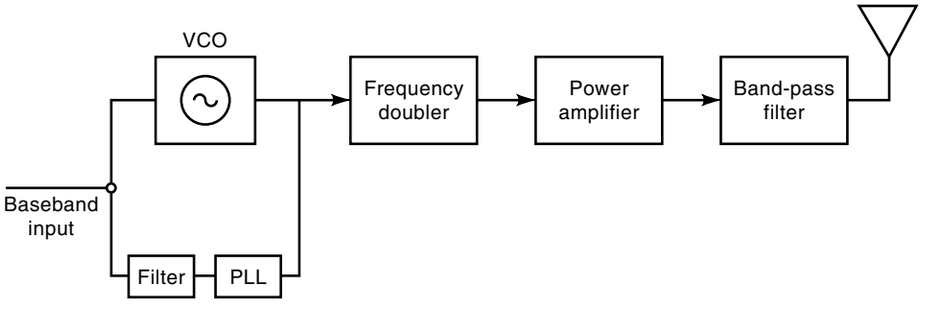

Figure 5. Transmitter with direct VCO modulator.

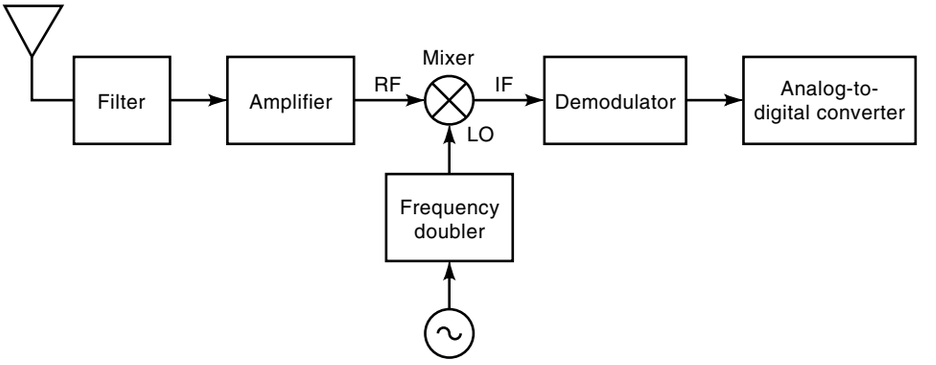

Figure 6. Receiver employing frequency multiplier.

Varactor diodes are commonly used by microwave designers in the development of passive multipliers with great success (14–17). The varactor diode is a variable-reactance element where the diode junction capacitance changes nonlinearly as a function of the applied voltage, as will be discussed in the following section. Varactors are classified into two major categories: (1) p–n junction varactors, which are widely used at microwave frequencies, and (2) Schottky junction devices, typically used for millimeter-wavelength applications. It has been shown by Manley and Rowe (42) as will be discussed later, and it has been mentioned by other authors (19,43,44) that a nonlinear capacitance (reactance) harmonic generator, such as that developed with a junction varactor, can theoretically generate harmonics with efficiencies ($\eta = P_{out}/P_{in}$) approaching 100%. On the other hand, passive frequency multipliers utilizing passive nonlinear resistors for harmonic generation have at most an efficiency of $1/N^2$, where N is the order of the harmonic, as shown by Page (45) and referenced by other authors (15,16,19). Therefore, in the case of a frequency doubler, theoretically, the highest efficiency achievable is 25% ($N = 2$).

The step recovery diode is also used in passive frequency multiplier design for lower frequencies (≤30 GHz) (17). The step recovery diode is another variable-reactance element, which is a variation of the varactor diode. Archer (26) states that the step recovery diode is a pn-junction diode explicitly designed to enhance the charge storage capacitance associated with minority carrier injection during forward conduction and that the charge storage capacitance supplies the nonlinearity necessary for harmonic generation. Based on the available literature, step recovery diodes are not as popular as varactor diodes in the design of passive frequency multipliers because of the complexity in reproducible control of the forward injection of minority carriers. Therefore, the ensuing discussions will not focus on step recovery diodes.

Diode Model. As will be mentioned in the following section, one of the most important tools of microwave circuit designers is the availability of device circuit models, which allows the performance of the device to be predicted before and after embedding with external networks. Since a diode model is essential in the understanding and development of passive frequency multipliers utilizing these devices as the source of nonlinearity, the following discussion will be devoted to the circuit model of the diode.

An equivalent circuit model for the varactor model is shown in Fig. 8. This simple circuit model contains a frequency-dependent series resistance R_s and a voltage-dependent nonlinear conductance $g(v)$ in parallel with the voltage-dependent junction nonlinear capacitance $C_j(v)$, where v is the voltage over the junction (17,36). The nonlinear conductance, which can produce resistive multiplication, is defined as (36)

$$g(v) = \frac{\partial i_g}{\partial v} \tag{1}$$

$$i_g = I_{sat}\left[\exp\left(\frac{qv}{\eta kT}\right) - 1\right] \tag{2}$$

where I_{sat} is the diode saturation current, q is the magnitude of the electron charge, η is the ideality factor of the diode, k

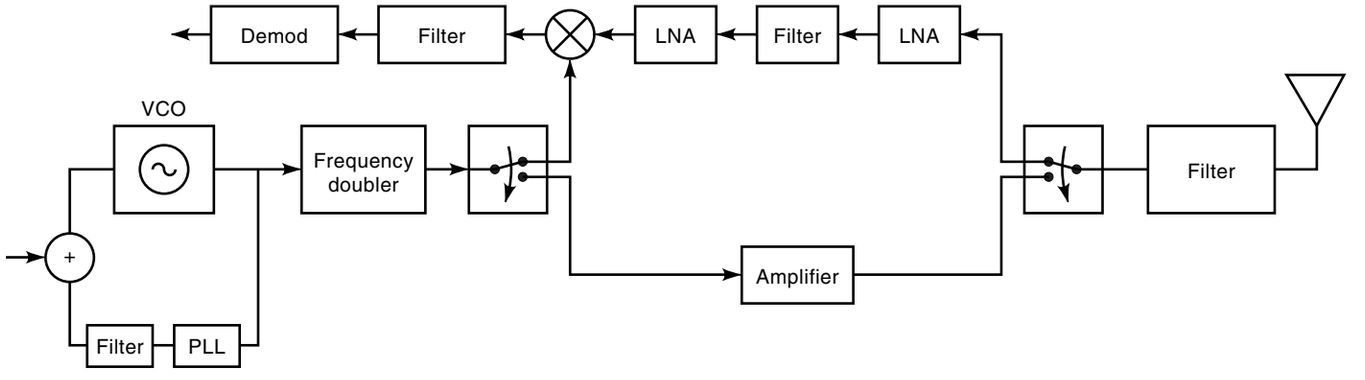

Figure 7. Transceiver employing frequency multiplier.

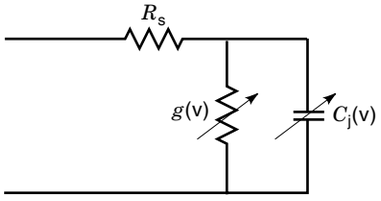

Figure 8. Varactor diode circuit model.

is the Boltzmann constant, and T is the diode temperature. The nonlinear capacitance $C_j(v)$, which is responsible for supplying the nonlinear reactance, is defined as (36)

$$C_j(v) = \frac{C_{j0}}{(1 - v/\phi_{bi})^{\gamma}} \tag{3}$$

where C_{j0} is the zero-bias junction capacitance, ϕ_{bi} is the built-in voltage potential, and γ is related to the doping profile in the epitaxial layer. Raisanen (36) indicates that typical values of these parameters for a varactor diode with radius of 1 μm to 5 μm are as follows: the zero-bias junction capacitance C_{j0} ranges from 3 fF to 20 fF, the series resistance R_s ranges from 5 Ω to 20 Ω, the built-in potential ϕ_{bi} ranges from 0.6 V to 1.0 V, and γ ranges from 0.4 to 0.5. The series resistance R_s arises from the undepleted materials in the diode and the contact resistance (14).

As shown in this model, suitable nonlinear elements exist for harmonic generation, namely, the nonlinear resistor $1/g(v)$ and the nonlinear capacitance $C_j(v)$. As was previously mentioned and will be discussed in a following subsection, harmonic generation due to the nonlinear reactance produced by $C_j(v)$ is, theoretically, more effective because it is possible to convert all of the available power applied to a lossless nonlinear reactive element to output power at any higher harmonic frequency. An ideal resistive multiplier utilizing the nonlinear resistor $1/g(v)$ theoretically has a maximum efficiency of only $1/N^2$, where N is the harmonic frequency.

Nonlinear Mechanism. As previously mentioned, high-frequency signals can be generated from lower-frequency signals by harmonic multiplication. Frequency multipliers provide an efficient means of exploiting the nonlinear characteristics of various devices to provide the desired harmonic multiplication. The circuit designer of frequency multipliers seeks to accentuate the device nonlinearity in a particular way such that exciting the nonlinear device by a sinusoidal input signal at a fundamental frequency produces an output spectrum at harmonic frequencies of the input fundamental, which obviously includes the desired harmonic of interest. This section will identify and discuss the general nonlinear mechanisms responsible for harmonic production in passive frequency multipliers.

It was noted in the previous section that nonlinear resistors, nonlinear capacitors, and nonlinear inductors could be exploited for their nonlinear characteristics. Typical nonlinear devices providing these nonlinear characteristics essential for harmonic production include rectifying metal–semiconductor junctions with the nonlinear current–voltage characteristics, reverse-biased metal–semiconductor or p–n junctions with their nonlinear capacitance, and nonlinear transmission lines having distributed nonlinear capacitance (13). As a simple example demonstrating harmonic generation, consider a nonlinear device whose nonlinear transfer function can be represented as a polynomial of the form

$$V_{out} = a_1 V_{in} + a_2 V_{in}^3 \tag{4}$$

where a_1 and a_2 are constants. Inserting a sinusoidal input ($V_{in} = \cos \omega t$) into Eq. (4) gives

$$\begin{aligned} V_{out} &= a_1 \cos \omega t + a_2 (\cos \omega t)^3 \\ &= a_1 \cos \omega t + a_2 (\tfrac{1}{4} \cos 3\omega t + \tfrac{3}{4} \cos \omega t) \\ &= \left(a_1 + \frac{3a_2}{4}\right) \cos \omega t + \frac{a_2}{4} \cos 3\omega t \end{aligned} \tag{5}$$

Equation (5) shows that an output harmonic is generated at the fundamental frequency (ω) and the third-harmonic frequency (3ω). Therefore, for the specific application of a frequency tripler, this nonlinear device, as represented by the transfer function given in Eq. (4), theoretically provides the nonlinear characteristics for the design of a frequency tripler.

Throughout the literature, researchers and designers have developed passive multipliers, typically with nonlinear diodes. For this reason, the ensuing discussion focuses on the nonlinear mechanism associated with semiconductor diodes, which are used throughout the microwave industry.

As mentioned, semiconductor diodes have been reported throughout the literature as an efficient means of harmonic production. To demonstrate the nonlinear mechanism of the diode, consider an abrupt p–n-junction diode, shown in Fig. 9, excited by an applied voltage V_a (46). Muller and Kamins (46) show that

$$X_d = X_p + X_n = \left[\frac{2\epsilon}{q}(\phi - V_a)\left(\frac{1}{N_a} + \frac{1}{N_d}\right)\right]^{1/2} \tag{6}$$

$$X_p = \left(\frac{2\epsilon(\phi - V_a)}{qN_a(1 + N_a/N_d)}\right)^{1/2} \tag{7}$$

$$X_n = \left(\frac{2\epsilon(\phi - V_a)}{qN_d(1 + N_d/N_a)}\right)^{1/2} \tag{8}$$

where

X_p = reactance of the depletion region extending into the p-type semiconductor

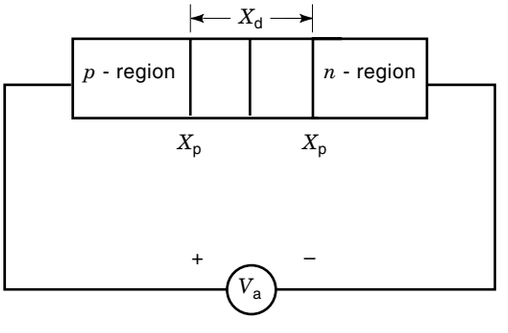

Figure 9. p–n-junction diode structure.

X_n = reactance of the depletion region extending into the n-type semiconductor
X_d = reactance of the total depletion region
ϕ = built-in potential
V_a = applied voltage
N_a, N_d = semiconductor dopant concentrations
ϵ = permittivity

By charge neutrality,

$$N_a X_p = N_d X_n \tag{9}$$

$$Q = qN_d X_n = qN_a X_p \tag{10}$$

$$dQ = qN_d\, dX_n = qN_a\, dX_p \tag{11}$$

$$C_j(V_a) = \frac{dQ}{dV_a} = \frac{dQ}{dX_p}\frac{dX_p}{dV_a} \tag{12}$$

$$= qN_a\left(\frac{\epsilon}{2qN_a(1+N_a/N_d)(\phi - V_a)}\right)^{1/2} \tag{13}$$

$$= \left(\frac{q\epsilon N_a N_d}{2(N_a+N_d)}\right)^{1/2}\frac{1}{\sqrt{\phi - V_a}} \tag{14}$$

$$= \frac{C_{j0}}{\sqrt{1 - V_a/\phi}} \tag{15}$$

where

$$C_{j0} = \left(\frac{q\epsilon N_a N_d}{2(N_a+N_d)}\right)^{1/2} \tag{16}$$

Equation (15) shows that the magnitude of the junction capacitance varies nonlinearly as a function of applied voltage V_a, which is essential for generating frequency harmonics when a sinusoidal voltage is added to V_a. Using a binomial series expansion on Eq. (15) yields

$$C_j(V_a) = C_{j0}(1 - V_a/\phi)^{-1/2}$$

$$= C_{j0}\left[1 + \frac{1}{2}\left(\frac{V_a}{\phi}\right) + \frac{3}{8}\left(\frac{V_a}{\phi}\right)^2 - \frac{5}{16}\left(\frac{V_a}{\phi}\right)^3 + \cdots\right] \tag{17}$$

$$= \alpha_0 + \alpha_1 V_a + \alpha_2 V_a^2 + \alpha_3 V_a^3 + \cdots \tag{18}$$

$$= \sum_{i=0} \alpha_i V_a^i \tag{19}$$

where

$$\alpha_0 = C_{j0}$$
$$\alpha_1 = \frac{C_{j0}}{2\phi}$$
$$\alpha_3 = -\frac{5C_{j0}}{16\phi^3}$$
$$\vdots$$

From Eqs. (12) and (18),

$$dQ(V_a) = C_j(V_a)\, dV_a \tag{20}$$

$$Q(V_a) = \int C_j(V_a)\, dV_a \tag{21}$$

$$= \int (\alpha_0 + \alpha_1 V_a + \alpha_2 V_a^2 + \cdots)\, dV_a \tag{22}$$

$$= \alpha_0 V_a + \tfrac{1}{2}\alpha_1 V_a^2 + \tfrac{1}{3}\alpha_2 V_a^3 + \tfrac{1}{4}\alpha_3 V_a^4 + \cdots \tag{23}$$

$$= \sum_{i=0} \alpha_i' V_a^{i+1} \tag{24}$$

where

$$\alpha_0' = \alpha_0$$
$$\alpha_1' = \tfrac{1}{2}\alpha_1$$
$$\alpha_2' = \tfrac{1}{3}\alpha_2$$
$$\vdots$$

Demonstrating the effect of applying a sinusoidal signal across the p–n junction, the current across the diode can be calculated from

$$I(t) = \frac{dQ}{dt} \tag{25}$$

Inserting Eq. (23) into Eq. (25) with the p–n junction excited by the sinusoidal signal $V_a = \cos \omega t$ gives

$$Q = \alpha_0 V_a + \tfrac{1}{2}\alpha_1 V_a^2 + \tfrac{1}{3}\alpha_2 V_a^3 + \cdots$$

$$= C_{j0}(\cos \omega t) + \frac{C_{j0}}{4\phi}\cos^2 \omega t + \frac{C_{j0}}{8\phi^2}\cos^3 \omega t + \cdots \tag{26}$$

$$= \frac{C_{j0}}{8\phi} + \left(C_{j0} + \frac{3C_{j0}}{32\phi^2}\right)\cos \omega t + \frac{C_{j0}}{8\phi}\cos 2\omega t + \frac{C_{j0}}{32\phi^2}\cos 3\omega t + \cdots \tag{27}$$

and inserting Eq. (27) and differentiating gives

$$I(t) = \frac{dQ}{dt}$$

$$= -\omega\left(C_{j0} + \frac{3C_{j0}}{32\phi^2}\right)\sin \omega t - \frac{2\omega C_{j0}}{8\phi}\sin 2\omega t - \frac{3\omega C_{j0}}{32\phi^2}\sin 3\omega t + \cdots \tag{28}$$

This result illustrates the various frequency harmonics produced by the p–n junction when excited by a sinusoidal source and demonstrates the nonlinear mechanism by which the semiconductor diode produces harmonic generation. This variable capacitance has led semiconductor diodes, varactors, and the like to be vital components aiding microwave engineers in nonlinear circuit development.

Voltage–Capacitance and Charge–Capacitance Characteristics. As previously stated, harmonic generators utilizing the nonlinear capacitance characteristics of varactors are often employed throughout the microwave industry by researchers and designers. The voltage– and charge–capacitance characteristics of the varactor diode are important in analyzing and studying the behavior of diodes. This section will discuss the relationships between the voltage and the capacitance and between the charge and the capacitance, since they are often utilized in studying the performance and the design of passive frequency multipliers.

We refer to the diode example in the preceding sub-subsection along with Eqs. (12) and (15), which are restated below (18):

$$C_j(v) = \frac{dQ}{dv} = \frac{C_{j0}}{(1 - v/\phi)^m} \tag{29}$$

where

v = voltage across the junction in the absence of any applied bias
ϕ = built-in potential
C_{j0} = zero-bias junction capacitance
m = index number ($\frac{1}{2}$ for abrupt junctions, and $\frac{1}{3}$ for linearly graded junctions)

Scanlan (18) indicates that the minimum capacitance ($C_{\min}$) occurs at the reverse breakdown voltage ($v = -V_R$) and the junction capacitance at this bias is

$$C_{\min} = C_j(-V_R) = \frac{C_{j0}}{(1 + V_R/\phi)^m} \tag{30}$$

Letting $V_0 = V_R + \phi$ and rewriting Eq. (30) gives

$$\begin{aligned} C_{j0} &= C_{\min}\left(1 + \frac{V_R}{\phi}\right)^m \\ &= C_{\min}\left(1 + \frac{V_0 - \phi}{\phi}\right)^m \end{aligned} \tag{31}$$

and inserting Eq. (31) in Eq. (29) gives

$$\begin{aligned} C_j(v) &= \frac{C_{\min}\left(1 + \dfrac{V_0 - \phi}{\phi}\right)^m}{\left(1 - \dfrac{v}{\phi}\right)^m} \\ &= C_{\min}\left(\frac{V_0}{\phi - v}\right)^m \end{aligned} \tag{32}$$

From Eq. (29),

$$dQ = C_j(v)\,dv \tag{33}$$

and inserting Eq. (32),

$$\begin{aligned} Q(v) &= \int C_j(v)\,dv \\ &= -\frac{C_{\min}V_0^m}{1-m}(\phi - v)^{1-m} + k \end{aligned} \tag{34}$$

where k is the constant of integration. When $v = \phi$, the voltage across the junction is zero and the charge is zero, which indicates that $k = 0$ as well. This allows Eq. (34) to be rewritten as follows, where the charge is represented as a function of the voltage:

$$Q(v) = -\frac{C_{\min}V_0^m}{1-m}(\phi - v)^{1-m} \tag{35}$$

The depletion-region reactances X_p, X_n and the electric field across p–n junctions increase as the reverse bias increases (46). Intuitively, there are physical limitations to these increases, as governed by the structure of the junction and the dopant concentrations. As the reverse bias increases, eventually a voltage is encountered where the barrier to current flow is broken, and current flow increases substantially. The voltage at which this occurs is defined as the breakdown voltage ($v = -V_R$). At the breakdown voltage, Eq. (35) gives

$$Q(-V_R) = Q_R = -\frac{C_{\min}V_0^m}{1-m}(\phi + V_R)^{1-m} \tag{36}$$

and recalling that $V_0 = V_R + \phi$ gives

$$Q(-V_R) = Q_R = -\frac{C_{\min}V_0}{1-m} \tag{37}$$

Now, dividing Eq. (35) by Eq. (37) gives

$$\begin{aligned} \frac{Q(v)}{Q_R} &= \frac{-\dfrac{C_{\min}}{1-m}V_0^m(\phi - V_R)^{1-m}}{-\dfrac{C_{\min}V_0}{1-m}} \\ &= \left(\frac{\phi - v}{V_0}\right)^{1-m} \end{aligned} \tag{38}$$

This expression relates the charge across the junction in terms of breakdown characteristics (V_R, Q_R) and the minimum capacitance ($C_{\min}$).

Historically, in the literature, the capacitance is used in defining the elastance (18,19):

$$S(v) = \frac{1}{C(v)} \quad \text{and} \quad S_{\max} = \frac{1}{C_{\min}} \tag{39}$$

This allows Eq. (32) to be rewritten in terms of the elastance as shown below, where the elastance is written as a function of voltage:

$$\frac{C(v)}{C_{\min}} = \left(\frac{V_0}{\phi - v}\right)^m = \frac{S_{\max}}{S(v)} \tag{40}$$

or

$$\frac{S(v)}{S_{\max}} = \left(\frac{\phi - v}{V_0}\right)^m \tag{41}$$

Referring back to Eq. (38), the charge $Q(v)$ is expressed as a function of v. Alternatively, Eq. (38) can be rearranged to give the voltage as a function of the charge:

$$\begin{aligned} v(Q) &= \phi - V_0\left(\frac{Q}{Q_R}\right)^{1/(1-m)} \\ &= V_0 - \phi - V_0\left(\frac{Q}{Q_R}\right)^{1/(1-m)} \end{aligned} \tag{42}$$

and therefore,

$$\begin{aligned} v + V_R &= V_0\left[1 - \left(\frac{Q}{Q_R}\right)^{1/(1-m)}\right] \\ &= V_0\left[1 - \left(\frac{Q}{Q_R}\right)^{\gamma}\right] \end{aligned} \tag{43}$$

where

$$\gamma = \frac{1}{1-m}$$

Equations (29)–(43) are mathematical expressions for the characteristics between the voltage, charge, capacitance, and elastance of p–n-junction semiconductor diodes. Researchers and designers often use these expressions, amongst others, in analyzing diodes and incorporating diodes into multiplier designs.

Power Considerations. A discussion on power flow into and out of the nonlinear device is very useful in understanding the behavior of passive nonlinear devices and their usefulness in designing passive frequency multipliers, as it can be used to predict optimum power and conversion efficiency. This subsubsection will discuss the power flow at the various harmonics and their relation to the performance of frequency multiplier designs, which leads to a fundamental understanding of the limitations imposed by diodes.

Manley and Rowe (42) have provided a general relation, which is commonly used throughout the microwave industry, for discussing the power flow of a particular class of nonlinear elements. They derive general power relations that govern single-valued nonlinear elements such as nonlinear inductors and capacitors. Their final derivations, independent of input power, give two independent equations characterizing the power content at various harmonics.

Manley and Rowe perform their derivation on an ideal nonlinear capacitor, but state that a similar analysis can be performed on a nonlinear inductor. Their analysis begins by evaluating the voltage across the nonlinear capacitor, which is defined as some arbitrary function of the charge. Then, they write an equation for the charge across the capacitor represented in a Fourier series. From the charge, they are able to calculate the current in Fourier series form. Next, the voltage across the nonlinear capacitor is given in a Fourier series, from which the Fourier coefficients for the voltage are calculated using orthogonality. After further substitutions and integrations, they conclude with the following equations:

$$\sum_n \sum_m \frac{mP_{mn}}{mf_1 + nf_2} = 0 \tag{44}$$

$$\sum_n \sum_m \frac{nP_{mn}}{mf_1 + nf_2} = 0 \tag{45}$$

where m and n are integers representing various harmonics and P_{mn} is the average power flowing into the nonlinear reactances at the frequencies mf_1 and nf_2. These equations are significant in that they indicate that for an ideal, lossless capacitance (with $R_s = 0$ in Fig. 8), the sum of all inward power flows at the different frequencies must be zero. This indicates, theoretically, that on exciting the nonlinear capacitor at a fundamental frequency, the output power at the desired harmonic has the same magnitude as the input power of the fundamental. This is achieved *provided* that all power at the undesirable harmonics has been reactively terminated, which ensures that no power is dissipated at these undesirable harmonics.

As an example demonstrating this procedure, consider exciting a nonlinear capacitor at the fundamental frequency $f_1(m = 1, n = 0)$. Then Eq. (44) gives

$$\frac{P_{10}}{f_1} + \frac{mP_{m0}}{mf_1} = 0 \tag{46}$$

or

$$P_{10} = -\sum_{m=2}^{\infty} P_{m0} \tag{47}$$

or in general, the sum of all powers flowing at the various harmonic frequencies must be zero. Equation (47) indicates that the input power P_{10} at the fundamental is the sum of the output powers at all harmonics combined. Therefore if external embedding circuitry to which the nonlinear capacitor is connected is developed such that the power at all undesirable harmonics is reactively terminated, then the power delivered to the load at the desired harmonic can, theoretically, represent conversion efficiencies of 100% (17). Practical diodes, however, exhibit nonzero series resistance ($R_s \neq 0$), so that practical conversion efficiencies are less than 100%.

Optimization of Efficiency. Achieving optimum efficiency is an essential goal in the design of any component. In the case of passive multipliers, proper techniques should be employed in efforts to maximize the conversion efficiency of the multiplier and maximize the power delivered to the load at the desired harmonic.

The Manley–Rowe equations given above indicate that, theoretically, an ideal nonlinear capacitor can achieve 100% conversion efficiency. In practical applications, nonlinear capacitors (varactors) are not ideal components but have some loss. Therefore, as a general example, the varactor utilized in passive multiplier design should exhibit low series resistance (R_s) at the frequency and power level of operation (18,36). Impedance matching at the input of the nonlinear device is also required, to ensure that the input power is efficiently coupled to the diode. Similarly, output impedance matching at the desired harmonic of interest should be implemented so that power generated in the nonlinear device at the output harmonic is efficiently transferred to the load. Significant real power should exist in the diode at the fundamental and the output harmonic of interest and low-loss resonators should be utilized as idler circuits (13,42–44,47), which will be discussed in a following subsection.

Archer and Batchelor (12) note that an equivalent-circuit model of a varactor diode embedded in external circuitry can be utilized to predict and optimize the performance of a passive multiplier. They give an equivalent circuit for a varactor multiplier, showing the connection between the varactor and the embedding network, as in Fig. 10. There, the embedding network models the impedance presented to the diode at the fundamental frequency and other harmonics. The two networks (embedding and equivalent diode circuit model) are optimized to obtain maximum power transfer between the embedding network and the reactance of the diode at the input fundamental frequency and the output harmonics. This optimization can be performed manually using the mathematical equations governing the response of the networks or through an optimization routine provided by a commercial circuit simulator.

The conversion efficiency is dependent upon the large-signal diode currents and voltages, which are determined by the impedances presented to the diode at the fundamental and higher harmonic frequencies (17,18). Simulations can be performed to optimize the conversion efficiency, utilizing the im-

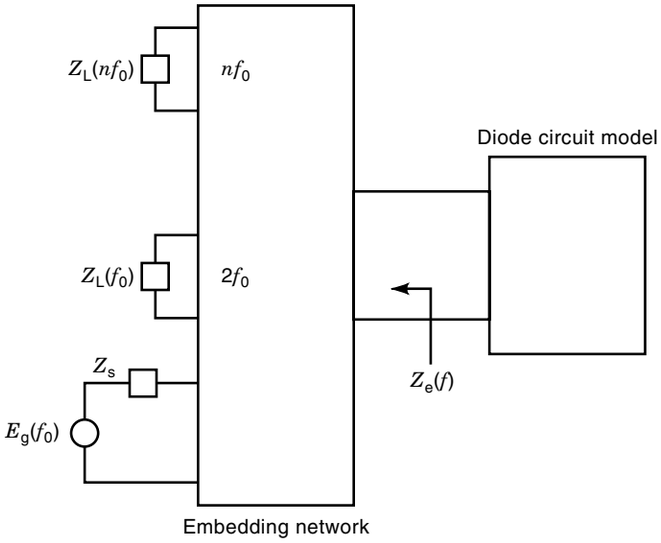

Figure 10. Equivalent network model of passive frequency multiplier.

pedances presented to the diode in conjunction with the diode circuit model.

The steady-state large-signal voltage and current coefficients are V_k and I_k in (17).

$$v_j(t) = \sum_k V_k e^{jk\,2\pi ft} \tag{48}$$

$$i_c(t) = \sum_k I_k e^{jk\,2\pi ft} \tag{49}$$

where f is the fundamental frequency. The predicted performance and thus the optimization of efficiency are determined after solving Eqs. (48) and (49) subject to the boundary conditions imposed by the diode and the embedding network [the embedding impedance $Z_e(f)$]. Such solutions have been calculated and presented by various authors (9,11,14–18,20–41), using idealized models, to obtain the nonlinear large-signal behavior of specific multipliers (doublers, triplers, etc.). They present data on the efficiency, power handling, input and load resistances, and P_{max}/P_{in}, for example, versus frequency for various multipliers. Using such plots and data, theoretical optimization can be achieved for specific multiplier types.

In summary, it is important to optimize the performance of frequency multipliers. Chang et al. (29) state general guidelines for achieving this:

1. Good impedance matching should be provided at the input and output of the nonlinear device over the frequency range of interest, and all idler circuits terminated reactively with low loss.
2. At frequencies other than the fundamental, desired harmonic of interest, and idler harmonics, the nonlinear device should be mismatched to the embedding circuitry to minimize power loss.
3. The input and output networks should be isolated physically and electrically.

Idlers. An important concept in the fundamental development of passive frequency multipliers, as briefly mentioned in prior sections, is that of idler currents and idler circuits. Idler currents are currents flowing at frequencies other than the input fundamental frequency and output harmonic frequency, which are required for a particular class of passive multipliers (47). This section will discuss the property of idlers and demonstrate the requirement of them for particular multiplier designs.

In the section "Voltage–Capacitance and Charge–Capacitance Characteristics," a discussion was presented of the voltage and charge relations of nonlinear varactors. Referring to Eq. (42) it is observed that a square-law characteristic is exhibited by an abrupt junction diode ($m = \frac{1}{2}$): the voltage is proportional to the square of the charge (43). Consider the condition in which the charge across the junction of an abrupt junction diode is sinusoidal at the fundamental frequency ($\omega = 2\pi f$):

$$Q(t) = Q_0 + Q_1 \cos \omega t \tag{50}$$

where Q_0 is the dc biasing component. Inserting Eq. (50) into Eq. (42) and using the trigonometric identities gives

$$v(Q) = \phi - V_0 \left(\frac{Q}{Q_R}\right)^2 \tag{51}$$

$$v(t) = \phi - V_0 \left(\frac{Q_0 + Q_1 \cos \omega t}{Q_R}\right)^2 \tag{52}$$

$$= \phi - \frac{V_0}{Q_R^2}\left(Q_0^2 + \frac{Q_1^2}{2}\right) - \frac{2V_0 Q_0 Q_1}{Q_R^2} \cos \omega t - \frac{V_0 Q_1^2}{2Q_R^2} \cos 2\omega t \tag{53}$$

From Eq. (53) it is observed that the voltage produced by the charge across the abrupt junction diode has a dc component, a component at the fundamental frequency, and a component at the second harmonic frequency, but no component at any harmonic higher than the second, such as required for frequency triplers, quadruplers, and so on. The component at the second harmonic frequency indicates that this diode is suitable for a frequency doubler, however. This example indicates that except for the case of the doubler, if currents flow only at the input and output frequencies, it is impossible to generate harmonics higher than the second with an *abrupt* junction varactor. This is an expected result due to the square law behavior of the varactor. Thus, in order to achieve output harmonics for $n > 2$, it is necessary for intermediate currents (idler currents) to flow in the varactor at specific harmonic frequencies.

The abrupt junction varactor can be thought of as providing a mechanism for frequency doubling (due to the square-law relationship previously mentioned) and for frequency mixing when idler currents are utilized (19). In the case of mixing, currents flowing at specific harmonic frequencies are mixed with the fundamental frequency and with each other (if more than one is introduced) to produce additional currents at various harmonics. Therefore, introducing an idler current into an abrupt junction varactor at the second harmonic causes the second harmonic to mix with the fundamental frequency to produce an output at the third harmonic. This additional idler produces the component necessary for frequency tripler design.

Introducing additional currents into an abrupt junction varactor provides a means for the device to generate higher harmonics. This extends the use of abrupt junction varactors from frequency doublers to higher-order multipliers.

Analysis Techniques

Passive frequency multipliers are nonlinear circuits requiring solutions from large-signal circuit analysis. As stated in preceding subsections, the efficiency of passive multipliers utilizing diodes is affected by the diode parameters: the embedding impedance $Z_e(nf_0)$ at the fundamental and harmonic frequencies, the input power level P_{in}, and the bias voltage. Various techniques are utilized by researchers and designers for analyzing and optimizing nonlinear circuits and, specifically, passive multipliers. In some simple cases, analytic closed-form solutions may be obtained for optimizing the efficiency; however, for most cases the most convenient method is through numerical analysis. Some of these techniques include power series analysis, Volterra series analysis, and harmonic balance techniques where time-domain current and voltage solutions are sought that satisfy the diode boundary conditions and frequency-domain solutions are sought that satisfy the external circuit equations. Using these analysis techniques along with an accurate equivalent circuit model of the passive nonlinear device, the predicted performance of the device embedded in external circuitry can be obtained.

Since the analysis techniques for passive and active frequency multipliers are similar, the author refers further discussion on this topic to a later section, where a detailed discussion is presented on the analysis techniques mentioned above. The final section of this article deals with active frequency multipliers, but the analysis techniques are applicable for passive nonlinear devices as well.

Pertinent Properties of Passive Devices

The RF performance of passive multipliers is governed by, among other things, the pertinent properties of the nonlinear device. These properties can be divided into two categories (41): (1) those affecting the efficiency of the multiplier, and (2) those affecting its power-handling capability. Tolmunen (41) notes that the efficiency of the nonlinear diode is mostly affected by the cutoff frequency, which will be defined below, the strength of the nonlinearity, and the type of multiplication (resistive or reactive, as discussed in the section "Background and Theory" above. The power-handling capability is affected by the device area, the extent of the nonlinearity, and the breakdown voltage, which was discussed in the section "Voltage-Capacitance and Charge-Capacitance Characteristics."

Focusing on varactor frequency multipliers, for efficient varactor operation it is necessary, as expected, for the reactance of the junction capacitance of the varactor to be much larger than the device series resistance (R_s in Fig. 8) (17). Therefore, this necessitates an upper frequency limit (cutoff frequency) on the usefulness of a given varactor (18). The dynamic cutoff frequency is defined as (41).

$$f_{cd} = \frac{1/C_{min} - 1/C_{max}}{2\pi R_s} \tag{54}$$

where C_{min} and C_{max} are the minimum and the maximum capacitance of the varactor, and R_s is the diode series resistance. Therefore, for optimum performance, the cutoff frequency should be greater than the frequency of application.

A sharp nonlinearity in the C–V response of the varactor results in efficient harmonic generation, since the nonlinearity of the device is responsible for harmonic generation. The advantages of a sharp or steep nonlinearity depend on the extent of the voltage swing across the diode generated by the input power. Varactors have high input impedance, thus enabling large voltage swings to be generated across the device. A diode with high nonlinearity, even at low input power levels, produces significant voltage swings, and therefore is capable of achieving optimum performance. Typically, the optimum conditions occur in applications where the nonlinearity extends over voltages comparable to the voltage swing of the input power signal.

Tolmunen (41) states that the power-handling capability is proportional to the average capacitance of the device area. As in the case of other high-power devices, diodes with large surface areas are able to handle larger input power levels and consequently produce larger RF current. In practical diode applications, however, this may result in matching problems, because matching the diode over a broad voltage range is quite challenging and thus tradeoffs have to be made. As will be shown in the discussion of design techniques in the last section, another approach commonly used to improve the power-handling capability is to stack devices in series or parallel. This configuration increases the total area of the diode, thus allowing it to sustain larger voltage swings. Large device arrays are useful in high-power applications.

Classical Realizations

The previous sections highlighted some of the basic properties of passive multipliers and the fundamental characteristics of nonlinear components, which are utilized extensively in passive-multiplier development. As mentioned, the nonlinear component is embedded in external circuitry to accentuate the desired harmonic. As seen throughout the literature, various topologies exist for realizing passive multipliers, revealing the interaction between the embedding circuitry and the nonlinear device. This section will highlight some of the classical realizations utilized extensively by microwave designers and researchers.

Scanlan (18) and Leeson and Weinreb (20) have presented some simple, classical realizations for passive multipliers, as shown in Figs. 11 and 12. Scanlan identifies the passive multiplier topology shown in Fig. 11 as a series model where the varactor diode is series-mounted with the embedding network. The input and output networks F_1 and F_N, respectively, represent ideal filters at the fundamental frequency and the Nth harmonic, which permit voltages to exist at the fundamental frequency and the Nth harmonic, respectively. In

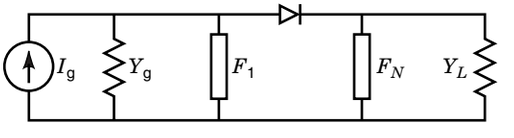

Figure 11. Series-mounted passive diode frequency multiplier.

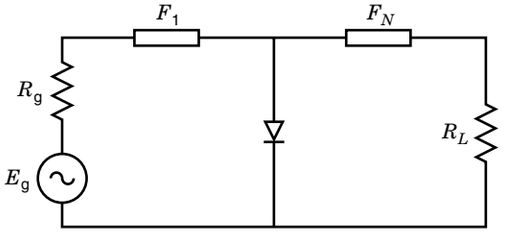

Figure 12. Shunt-mounted passive diode frequency multiplier.

other words, F_1 acts to short-circuit all frequencies other than the fundamental frequency, and F_N acts to short-circuit all frequencies other than the harmonic frequency of interest. Although more sophisticated filters may be required, parallel LC networks can be synthesized for F_11 and F_N at their respective frequencies, as shown by

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{55}$$

Figure 12, on the other hand, is the shunt diode topology for passive frequency-multiplier design using a nonlinear diode. Again, the input and output networks, F_1 and F_N, respectively, represent ideal filters at the fundamental frequency and the Nth harmonic, which permit currents to flow at the fundamental frequency and the Nth harmonic, respectively. This indicates that F_1 acts to open-circuit all frequencies other than the fundamental frequency and F_N acts to open-circuit all frequencies other than the harmonic frequency of interest. Similarly, F_1 and F_N can be synthesized as series LC networks resonant at the fundamental frequency and the output harmonic frequency of interest.

Faber (13) has discussed the realizations presented by Scanlan, with emphasis on achieving optimum efficiency of the multiplier. Block diagrams of the realizations (series-mounted and shunt-mounted) shown by Faber are given in Figs. 13 and 14. Recall from the section "Power Considerations" that the Manley–Rowe power equations imply that it is *theoretically* possible to deliver all input power at the fundamental frequency to the output load at the desired harmonic of interest, thereby achieving 100% efficiency. Achieving optimum efficiency requires that power should not be dissipated at any of the undesired harmonics in either the input network or the output network. This indicates, with regard to Fig. 13, that

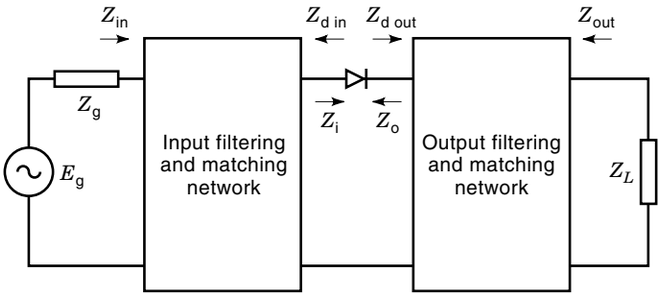

Figure 13. Block diagram of series-mounted diode frequency multiplier.

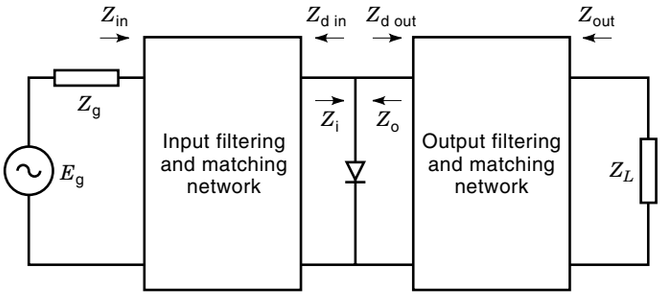

Figure 14. Block diagram of shunt-mounted diode frequency multiplier.

$$\mathrm{Re}\, Z_{d\,out}(f) \approx 0 \tag{56}$$

$$\mathrm{Re}\, Z_{d\,in}(nf) \approx 0 \tag{57}$$

when the input and output networks contribute to the device reactance compensation. If the conditions represented by Eqs. (56) and (57) are met, power is not dissipated at the fundamental frequency in the output network and power is not dissipated at any of the harmonic frequencies in the input network, respectively.

Similarly, for Fig. 14 the following conditions are sought:

$$\mathrm{Re}\, Y_{d\,out}(f) \approx 0 \tag{58}$$

$$\mathrm{Re}\, Y_{d\,in}(nf) \approx 0 \tag{59}$$

Apart from the realizations previously mentioned, several variations of these topologies have been utilized as well. At RF and microwave frequencies several diodes connected in series or parallel have been utilized to handle cases where there was insufficient power, voltage, or current-handling capability of a single device or where the single-device impedance levels were inconvenient. Connecting m diodes in series (stacking) produces a breakdown voltage m times as high, and m diodes in parallel provide m times higher current (13). Therefore, topologies such as those shown in Figs. 15 and 16 are commonly encountered.

The circuit complexity of passive multipliers can be increased even further. Some more complicated topologies are shown in Figs. 17–20 (13,17,18,30). The antiparallel topology of Fig. 17 produces currents containing components at the fundamental frequency and higher odd-order harmonics. This can substantially simplify the design of input and output filters in the development of odd-order multipliers.

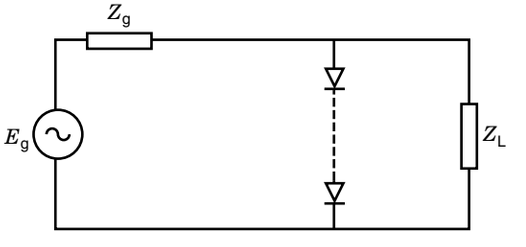

Figure 15. Series-connected diode multiplier topology.

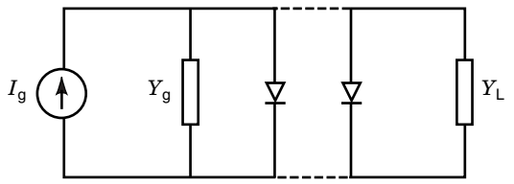

Figure 16. Parallel-connected diode multiplier topology.

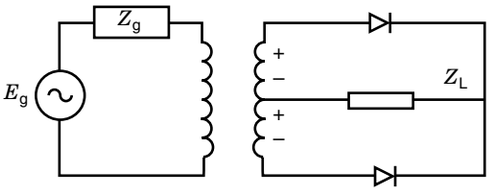

Figure 18. Antiseries diode pair.

Figure 18 shows the antiseries topology utilizing a transformer between the input signal and the diode circuit. The transformer provides a 180° phase shift between the input signal voltages feeding the two diodes. Therefore, the current components cancel in the load, producing no voltage across the load at the fundamental frequency. In contrast to the antiparallel topology, the antiseries topology provides even-order harmonics and therefore leads to less stringent requirements on the input and output filters.

Figure 19 utilizes a transformer in the antiparallel series topology as well. Faber notes that the odd-order components are in phase, so that when the odd-order components flow through the transformer primary winding, they do not excite the load mesh. The even-order components, on the other hand, are of opposite phase, so they cancel in the input signal source branch but excite current in the load mesh. This action causes the antiparallel series topology to produce even-order harmonic multiplication.

Finally, Fig. 20 shows a bridge frequency multiplier. Similarly to full-wave rectifiers, bridge rectifiers can be used to produce even-order harmonic multiplication.

Passive-Multiplier Design Techniques

Existing Design Techniques. Numerous techniques exist for the design of passive multipliers utilizing various topologies, many of which are presented in the previous section. This section presents, in perusal of the available literature, various existing design techniques, and in some cases details their performance.

A fundamental topological representation for realization of passive RF/microwave multiplier circuits is shown in Fig. 21, where networks N_1 and N_2 are on the input and output of the nonlinear device, respectively. As mentioned in a previous section, multiplier performance is governed by the embedding circuitry (networks N_1 and N_2) and the pertinent properties of the nonlinear device. Authors have used various networks in the synthesis of N_1 and N_2. Traditional syntheses have included short-circuited and open-circuited stubs at the fundamental frequency and various harmonics (16,24,25), impedance matching and filter networks (15,26–29), and waveguides and filters (11,14,31–33,36–40).

As shown in Fig. 21, in the synthesis of N_1 and N_2, several authors have utilized short-circuited and open-circuited stubs for low-frequency and high-frequency applications. Gavan and Peled (16), for example, use microstrip stubs in the development of a 1250 MHz to 2500 MHz step recovery diode frequency doubler. They synthesize N_1 with a $\lambda_0/8$ stub (at $2f_0$) on the input network to provide a short circuit for the second-harmonic signal, and synthesize N_2 with a $\lambda_0/4$ microstrip stub (at f_0), which provides a short circuit to ground for the fundamental frequency. Using this design technique, they achieve conversion gain efficiency of 75%, but do not present any data on harmonic suppression. Chen et al. (24,25) perform a 47 GHz to 94 GHz Schottky-barrier varactor diode frequency-doubler design utilizing MMIC technology. They use a $\lambda_0/2$ short-circuited stub (at $2f_0$) on the input network to create an RF short at 94 GHz, and a $\lambda_0/4$ short-circuited stub (at f_0) on the output to create an RF short at the fundamental frequency. This high-frequency MMIC design provided a maximum conversion efficiency of 25% (6 dB conversion loss).

Several authors have developed passive frequency multipliers utilizing impedance-matching networks and filters in the input and output networks (15,26–29). The impedance-matching networks are employed to match the input and output impedances of the nonlinear device, while the filters are used to attenuate specific harmonics. Gavan and Peled (15) designed a 1250 MHz to 2500 MHz varactor frequency doubler utilizing the shunt varactor topology shown in Fig. 14 along with a low-pass filter in the input network and a two-section coupled band-pass filter at 2500 MHz in the output network. This design technique yields a maximum conversion gain efficiency of 71%. Chang et al. (29) developed a varactor 46 GHz to 92 GHz frequency doubler utilizing a topology similar to that shown in Fig. 14. Input and output networks are synthesized with filters and additional matching networks to achieve optimum power transfer at the source and load. This design achieves a conversion loss of 8 dB to 9 dB over a 500 MHz bandwidth.

Furthermore, some authors have chosen to utilize a balanced topology for the design of frequency multipliers (30–33). A block diagram of a balanced design topology is shown in Fig. 22. In typical balanced circuits, a 180° phase difference

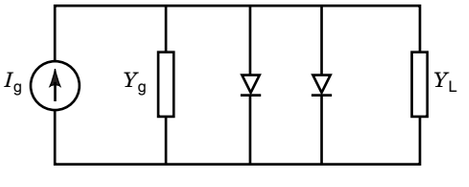

Figure 17. Antiparallel diode pairs.

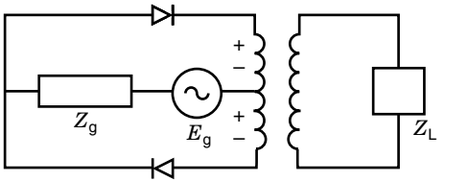

Figure 19. Antiparallel series-connected diodes.

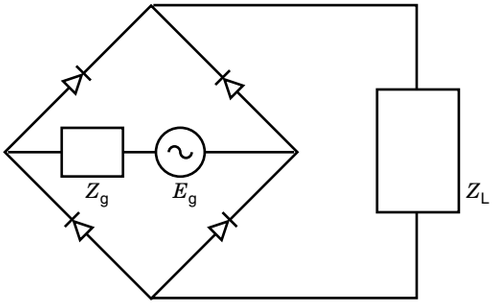

Figure 20. Bridge frequency multiplier.

in the input signals feeding the nonlinear device produces fundamental signals and other odd-harmonic signals with opposite phase. By destructive interference, the fundamental and other odd harmonics cancel, giving good harmonic suppression, while the second-harmonic signals, on the other hand, interfere constructively, thereby enhancing the output signal at the second harmonic. This design technique will be revisited in the discussion of active frequency multipliers.

Bitzer (30) utilized a balanced topology similar to that shown in Fig. 19 and presented again in Fig. 23 to design a broadband Schottky-barrier diode frequency doubler. In this structure, the input signal is fed antiphase to the diodes in order to switch on one diode patch every half cycle. The rectified output signal is coupled to the load via a balun. As mentioned previously, the fundamental signals and other odd-harmonic signals from the diodes have opposite phase and therefore, by destructive interference, cancel, giving good harmonic suppression. The second-harmonic signals interfere constructively, thereby enhancing the output signal at the second harmonic. Bitzer's data show that from 6 GHz to 18 GHz, the conversion loss is 9.5 ± 1 dB and harmonic suppression >15 dBc.

Archer (33) developed a balanced varactor diode 85 GHz to 116 GHz frequency doubler similar to the typical topology shown in Fig. 22. Archer uses a waveguide T junction as a power divider on the input to feed two varactor diodes. On the output, a matched waveguide hybrid T junction combines the power at the output port. Using this design topology, a maximum conversion efficiency of 16.5% was achieved. Unfortunately, Archer does not present any data on harmonic suppression.

Waveguide circuitry provides an efficient means of realizing frequency multipliers (14). Waveguides provide low loss, possess desirable high-pass filter characteristics, and provide a good thermal path for dissipated power. Energy is typically coupled/decoupled from the input and output of the waveguide through a low-pass filter. Various authors have utilized

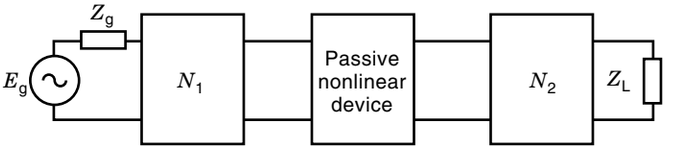

Figure 21. Passive frequency-multiplier realization.

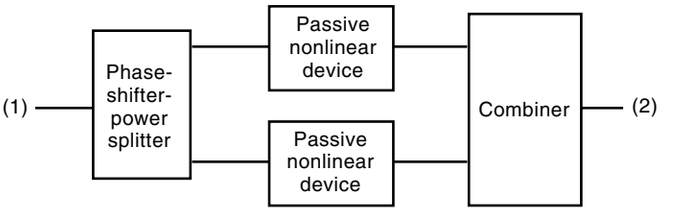

Figure 22. Block diagram of typical passive balanced frequency multiplier.

waveguide circuitry in high-frequency multiplier designs (11,14,31–33,36–40). Raisanen (36) notes that for frequencies from 100 GHz to about 500 GHz, for example, the highest efficiencies and highest output powers have been achieved with waveguide multipliers.

Archer (38) has developed a varactor frequency doubler at 260 GHz utilizing waveguides and filters. The input network consists of a low-pass filter and a waveguide. The low-pass filter is a seven-section design, which passes the fundamental signal while attenuating higher-order harmonics. The output network consists of a $\lambda_0/4$ impedance transformer and a waveguide. Using this design technique, Archer achieves a conversion gain efficiency of 20% for narrowband applications (5% bandwidth) and conversion efficiencies of 10% for wider-band applications (8% bandwidth).

Mott (11) has developed a varactor frequency doubler design at a lower frequency (19 GHz to 38 GHz), utilizing waveguides as well. Mott synthesized the input network with a waveguide, a $\lambda_0/4$ impedance transformer, and a low-pass filter and notes that the characteristic impedance of the filter is synthesized so that it equals the real part of the diode input impedance. The output network consists of an output waveguide impedance transformer synthesized to present the optimum load impedance to the output of the diode. Mott achieves a conversion efficiency of 60% (conversion loss of 2.2 dB) over a 1 dB output bandwidth of 640 MHz.

At higher frequencies, frequency multipliers are capable of achieving high conversion efficiency at low input powers, but the output power tends to saturate at rather low power levels (31). The use of series arrays of diodes provides an attractive approach to overcoming this defect. Cascading multiple-diode junctions increases the beakdown voltage and provides greater power-handling capability (9). A series array of n

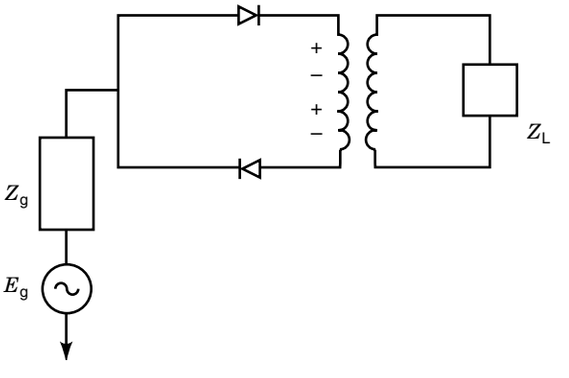

Figure 23. Antiparallel balanced diode configuration.

identical diodes can handle n^2 times as much power as a single diode (31). For these reasons, various authors have utilized series- and parallel-stacked diodes in passive design, as shown in Figs. 15 and 16, to improve the power-handling capability of passive frequency multipliers (9,14,30,31,34,35). Chu (34) developed an 18 GHz to 36 GHz stacked-diode frequency doubler utilizing two series diodes. The input and output matching circuits consist of $\lambda_0/4$ impedance transformer sections with open-circuited stubs resonant at the input and output frequencies. This design produced a maximum output power of 150 mW with a conversion efficiency of 24%, and a peak conversion efficiency of 35% at 95 mW of output power.

State of the Art. In the development of passive frequency multipliers, as well as other technologies, researchers and designers are constantly pushing the leading edge in attempts to achieve better performance. In passive frequency multipliers, designers desire, among other things, greater power-handling capability and greater conversion gain efficiency. This section will highlight state-of-the-art developments in passive frequency designs.

The available literature indicates that the leading edge of technology in passive designs is not focused so much on developing new design topologies as on new methods of fabricating new semiconductor diodes, particularly for millimeter and submillimeter-wavelength applications (25,36,39,41). It has been demonstrated that the performance of passive frequency multipliers is highly dependent on the pertinent properties of the nonlinear device. Therefore, it is reasonable to expect that efforts at improving the performance of passive frequency multipliers would begin with the nonlinear device.

Over the years, the GaAs Schottky varactor diode has served as one of the most important nonlinear elements for frequency multipliers (36,41). Consequently, over the past few years growing interest in novel diodes has brought to light new structures showing excellent theoretical performance comparable to or better than the conventional Schottky varactor. In comparison with the Schottky varactor, these new diodes have potential advantages, such as stronger nonlinearity or a special symmetry, which make them very attractive for millimeter and submillimeter-wave frequency multiplication. Stronger nonlinearities allow more efficient higher-order harmonic generation with smaller input signal levels (36). These novel diodes include single-barrier varactors (SBVs), quantum barrier varactors (QBVs), barrier–intrinsic–n^+ (BIN) diodes, and high-electron-mobility varactors (HEMVs).

The quantum well diode (QWD) has been studied since 1970 (41). The QWD is a heterojunction diode in which a thin undoped layer between two thin barriers forms the quantum well. Its high speed and negative differential resistance make it attractive for millimeter-wave oscillators. Due to its symmetric structure, the highly nonlinear antisymmetric I–V curves and symmetric C–V characteristics result in odd-harmonic generation. Therefore, as expected, QWDs have been utilized in tripler designs, with some designs going up to 200 GHz. Raisanen (36) notes that the resulting output powers from these tripler designs are promising, but are lower than those achieved from the best Schottky multipliers. Replacing the quantum well with a single thicker barrier produces a QBV or a SBV, where the nonlinear current is suppressed but the nonlinear C–V characteristic remains. Due to the symmetric C–V characteristic, this diode is also attractive for tripler and quintupler design. SBV triplers have been developed up to 280 GHz, producing output powers of 2.5 mW (36).

The BIN diode has been proposed as an improved diode for harmonic generation (41). Unlike QWDs or SBVs, which consist of a heterostructure and two ohmic contacts as terminals, the BIN diode is essentially a Schottky varactor with an unique doping profile that yields a sharper C–V characteristic than the Schottky varactor. The BIN diode consists of a Schottky contact, a barrier layer, and an intrinsic layer. Tulmunen (41) notes that connecting two BIN diodes back to back produces a symmetric C–V characteristic.

The HEMV is a modification of the planar Schottky varactor where a heterostructure is used. The electrons in this device have higher mobility, as in HEMTs (which are modeled and used in active multiplier designs in the final section), thus making it attractive for high-frequency applications. In a varactor, this structure produces a strongly nonlinear capacitance, but with an undesirable high parasitic capacitance associated with its structure.

Tolmunen (41) has designed several multipliers utilizing the above-mentioned novel devices at 200 GHz. The conclusions from his study reveal that the sharp C–V characteristic of the BIN diodes improves the performance at low input powers ($\leq$10 mW) and makes them the most effective of all the devices. The SBV yields excellent theoretical performance, but is less efficient due to its high resistive losses. It does, however, provide the best performance at high input power levels.

As researchers and designers continue to push the envelope of technology for higher-performance devices, these novel devices will be utilized extensively, particularly at submillimeter and millimeter frequencies.

ACTIVE FREQUENCY MULTIPLIERS

Another class of frequency multipliers encompasses those that are designed and constructed utilizing active nonlinear devices. As previously discussed, multipliers require a nonlinear element for harmonic production. Active frequency multipliers, as shown in the block diagram in Fig. 24, utilize the nonlinear characteristics of an active element to produce an output spectrum rich in harmonics when excited by a sinusoidal source. Typically, the active element consists of any of the transistor classes, which include the BJT, HBT, field-effect transistor (FET), MESFET, HEMT, and PHEMT.

Active multipliers offer various advantages over their passive counterparts. An example, which will be discussed in the following section, is in the conversion gain. Active multipliers are capable of producing conversion gains greater than 0 dB, whereas passive multipliers are not. This section will also dis-

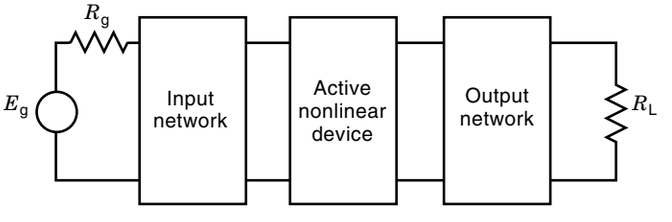

Figure 24. Block diagram of active frequency multiplier.

cuss the development of active-frequency-multiplier technology, including the fundamental performance descriptions, pertinent properties of the active device (which include modeling and quantification of the nonlinear properties), and design techniques of active frequency multipliers.

Numerous authors have presented discussions of active frequency multipliers, which are referenced throughout this section. In the development of active frequency multipliers, one of the primary concerns is the ability to accurately predict the linear and nonlinear performance of the active device before embedding it into other networks, which is typical in the development and design of frequency multipliers. Several authors (48–86) have presented details and techniques for modeling the active devices. Each author delineates the various advantages and disadvantage of their study. Techniques for modeling HBMTs are presented as an example in this discussion, since they are employed in the illustrative multiplier designs in later sections.

Fundamental Performance Descriptions

As discussed previously, frequency multipliers are nonlinear circuits that convert signals at an input fundamental frequency (f_0) into signals at a harmonic frequency multiple of the input frequency (nf_0). Several performance descriptions and parameters represent the effectiveness of frequency multipliers for frequency conversion. The objective of this section is to identify and discuss the prominent fundamental performance descriptions of active frequency multipliers.

Active frequency multipliers utilize the nonlinear characteristics possessed by any of the several transistor classes (BJT, FET, etc.). Exciting the nonlinear device with a fundamental frequency provides an output spectrum rich in frequency harmonics. One of the main advantages of active multipliers is their capability of producing positive conversion gains (conversion gains greater than 0 dB). The conversion gain of a frequency multiplier is defined as the ratio of the output power for a particular harmonic delivered to the load to the fundamental input power. Maximizing the conversion gain is crucial in the development and design of frequency multipliers. In the specific case of frequency doublers, an input signal at the fundamental frequency (f_0) is converted into a signal at the second harmonic ($2f_0$). Mathematically, the conversion gain can be expressed as (87)

$$\text{conversion gain} = \frac{P_{\text{out}}(2f_0)}{P_{\text{in}}(f_0)} \tag{60}$$

or

$$\text{conversion gain(dB)} = P_{\text{out},2f_0}(\text{dBm}) - P_{\text{in},f_0}(\text{dBm}) \tag{61}$$

Frequency doublers, which will be presented in the next section, have been designed and developed exhibiting conversion gains approaching 9 dB. Alternatively, the conversion gain can be expressed as a percentage (88). This percentage is defined as the ratio of the input power at the fundamental to the output power delivered to the load at the desired harmonic. Using the example of the frequency doubler, this can be represented as

$$\eta = \frac{P_{\text{in}}(f_0)}{P_{\text{out}}(2f_0)} \times 100\% \tag{62}$$

Similarly, as in the consideration of RF amplifiers, the effectiveness of the conversion of dc power into ac power is also a meaningful parameter in discussing frequency multipliers. In the case of frequency doublers, the consideration is focused on the effectiveness of converting dc power into ac power at the second harmonic. A general expression for the dc-to-RF efficiency can be represented as (88)

$$\text{dc-to-RF} = \left(\frac{P_{\text{out}}(\text{harmonic})}{P_{\text{dc}}}\right) \times 100\% \tag{63}$$

From this equation, it is observed that optimum dc-to-RF efficiency performance is achieved when maximum RF power is produced from minimum dc power. For the class of frequency multipliers presented in the next subsection, dc-to-RF efficiencies of up to 24% have been obtained.

The transfer of power from the fundamental frequency at the generator to the desired harmonic at the load is dependent, amongst other things, upon the return loss or voltage standing-wave ration (VSWR) of the input port and the output port of the multiplier circuitry. The return loss is a measure of the impedance match of the input and output ports of the frequency multiplier to the source impedance and the load impedance. Computer simulations for HEMT frequency doublers are performed in the section "Optimum Bias Selection Referencing Harmonic Terminations" (Tables 3 and 4) delineating the advantages of good impedance matching. In these simulations significant improvements in the conversion gain are achieved in the cases where the input and output ports are impedance-matched.

As previously discussed, frequency multipliers are harmonic generators that produce an output harmonic (nf_0) when excited by a fundamental frequency (f_0). In the generation of the desired harmonic, undesired harmonics are generated as well. As an example, in the case of a frequency doubler, the desired output harmonic is $2f_0$, but other harmonics at f_0, $3f_0$, $4f_0$, are generated. The ability of the multiplier to suppress the undesired harmonics is another key performance factor. This property of the frequency multiplier is called *harmonic suppression.* It is defined mathematically as

$$\text{suppression}_{(mf_0)}(\text{dBc}) = P_{0(nf_0)}(\text{dBm}) - P_{0(mf_0)}(\text{dBm}) \tag{64}$$

where nf_0 is the desired frequency harmonic and mf_0 is an undesired harmonic. In the case of the frequency doubler, $n = 2$ and $m = 1, 3, 4, \ldots$, which indicates that the desired harmonic is $2f_0$ and harmonic suppression is calculated for the fundamental frequency (f_0), third harmonic frequency ($3f_0$), and so on.

An application of frequency multipliers previously discussed is their use in communication systems in receivers and transmitters. A performance description of receivers in communication systems, and therefore of frequency multipliers used in receivers, is their *dynamic range,* defined as the range of input or output power levels where signals can be processed with high quality without signal distortion. At low power levels, the dynamic range is limited by the sensitivity to the noise floor or the minimum detectable signal as governed by the noise floor. At higher powers, the dynamic range is limited by the acceptable level of signal distortion or, specifically, by the power level where the small-signal gain has been compressed by 1 dB (89,90).

Using these definitions for the dynamic range, the optimum dynamic range for frequency multipliers is achieved when the power range between the noise floor and signal distortion is maximized. It involves tradeoffs between the input signal drive level, the noise floor level, and the output signal distortion.

Another important multiplier performance parameter is the operational bandwidth. Bandwidth is defined as the frequency band where specific performance specifications are met, typically, one uses the conversion gain. Specifying a -3 dB bandwidth indicates the frequency band where the conversion gain decreases by 3 dB from its peak. Optimizing multiplier bandwidth is an important task to the designer. Typically, tradeoffs have to be made in the performance of the devices to achieve high bandwidths. As an example, higher conversion gains are achieved for narrow bandwidth designs, and usually wide bandwidth designs are accomplished at the expense of the conversion gain. One explanation for this is the difficulty of achieving impedance matching over broad ranges. Consequently, the conversion gain is reduced over the band to compensate for the extended bandwidth. Over narrow frequency bands impedance matching is less of a challenge and thus readily facilitates optimization of conversion gain.

Pertinent Properties of the Active Device

Nonlinear Modeling. As pointed out previously, accurate device models are an essential ingredient for the efficient design of active microwave multipliers. This section presents typical information on active devices necessary in active multiplier design. Since most of the effort on active multipliers employs FET type devices, the remaining portions of this presentation will stress this class of active elements. Some multiplier realizations utilizing BIPOLAR devices are addressed in Ref. 95.

Classification of Device Models. Active device circuit models are developed and categorized according to their specific applications. Depending on this, a specific model is typically employed, such as small signal models and S parameter data for small signal amplifier applications.

Alternatively, for frequency multiplier applications, excellent nonlinear models are required to predict both the linear and nonlinear device performances.

The development of such models is a challenging undertaking which requires more depth in its exposition than space permits. The interested reader is referred to (49–78) for in-depth treatment of this topic.

Development of Precision Models. Based on the necessity of requiring precision nonlinear models for illustration of accurate multiplier designs, we will utilize a high electron mobility transistor manufactured by Fujitsu (FHX35LG) for that purpose.

Additionally, the frequency multiplier examples illustrated below are doublers, and thus, the highest frequency harmonic which will be modeled is the third harmonic. Furthermore, it has been pointed out in these applications, that the first three harmonics are of the greatest significance (99).

A number of authors (48–78) have developed nonlinear active device models which are typically employed in active multiplier development. The interested reader is referred to References 49 and 56 for in-depth discussion of most of these models.

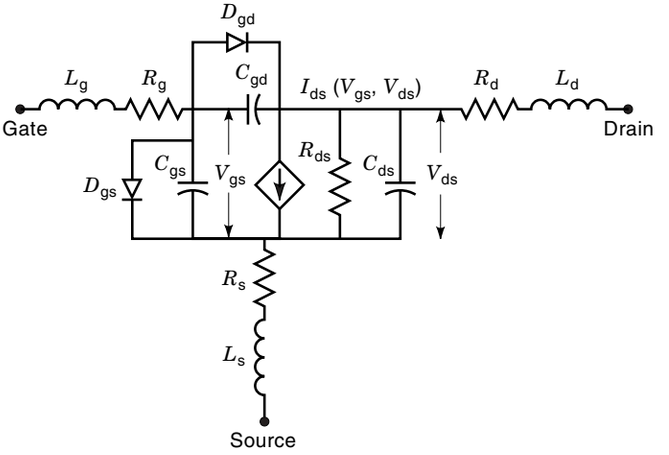

Figure 25. Nonlinear device equivalent circuit model.

For the purposes of our discussion, a general nonlinear FET/HEMT model is shown in Fig. 25. In this model, the nonlinear parameters include the following (49):

D_{gs} = gate-to-source diode
D_{gd} = gate-to-drain diode
C_{gs} = gate-to-source capacitance
C_{gd} = gate-to-drain capacitance
C_{ds} = drain-to-source capacitance
I_{ds} = drain-to-source current
R_{ds} = output resistance
g_m = transconductance (not shown in model but is represented by the equation: $g_m = i\partial I_{ds}/\partial V_{gs}$)

For an in-depth discussion of these parameters and their device design implications refer to Refs. (49) and (56).

Device Nonlinearities. It was discussed above that while the class of active devices available for multiplier applications includes BJT, MESFET, HEMT, etc., this work will employ HEMT transistors as a vehicle for design illustrations.

The equivalent circuit for this device was shown in Fig. 25 with the nonlinear elements displayed which are exploited in the generation of frequency harmonics.

Analysis of Nonlinearities. In analyzing FET/HEMT performance, several authors have addressed the issue of identifying the elements that contribute to the nonlinear behavior of FET transistors (49,75,76,79,86,93,97,98,101). Maas (86) has analyzed the nonlinear behavior of MESFET transistors. In his study, Maas provided the magnitude of all parasitic components (L_s, L_g, L_d, R_g, and R_d) and intrinsic components (R_i, R_{ds}, C_{gs}, C_{gd}, and g_m) in tabular form for various bias voltages. This provides insight into the nonlinear behavior of these component* for a typical transistor. Maas' data for the parasitic inductors (L_s, L_g, and L_d) show that the magnitudes of these inductors are very small and are on the order of hundredths of nH. Their values vary from 0.03 to 0.08 nH for L_s,

* R_i (not shown in Fig. 25) is the charging resistance in series with C_{gs}.

from 0.09 to 0.12 for L_g, and 0.06 to 0.07 nH for L_d or, in the worst case, their magnitudes vary by only 0.05 nH over the bias ranges. This indicates that at an arbitrary frequency of 1 GHz, the impedance of this inductance variation is approximately 0.25 Ω. This implies that the parasitic inductors can be approximated with fixed, constant values for all bias regions and, therefore, do not contribute as a source of nonlinearity to the MESFET. The magnitude of the parasitic resistors (R_g, R_s, and R_d) vary by only a few tenths of an ohm as functions of applied voltage. Therefore, similar to the parasitic inductors, their magnitudes can be fixed as constants in the device models.

Maas' data show that the output resistance of the MESFET varies nonlinearly over bias from approximately 10 Ω to 283 Ω (86). This variation is significant and indicates that due to this nonlinear characteristic, the output resistance of the transistors is one of the contributors to the nonlinear effects observed in the MESFET transistor. The gate-to-source and gate-to-drain capacitors (C_{gs} and C_{gd}) also vary nonlinearly as functions of applied voltage. C_{gs} is shown to vary from 0.415 pF to 0.636 pF, and C_{gd} varies from 0.049 pF to 0.266 pF. This nonlinear variation in C_{gs} and C_{gd} indicates that they are viable contributors to the harmonic production of the MESFET as well. The final element considered by Maas is the transconductance. The transconductance shows significant nonlinear variation over bias, particularly in the saturation region as it varies nonlinearly from 61.3 mS to 89.2 mS. This nonlinear variation indicates that it also contributes to the nonlinear behavior of the MESFET. In summary, Maas' study reveals that the elements significantly contributing to the nonlinear behavior of the MESFET are R_{ds}, C_{gs}, C_{gd}, and g_m. The remaining elements (L_s, L_g, L_d, R_i, R_g, R_s, and R_d) do not vary nonlinearly and can be considered to be constants in the models. Maas' study was performed on a MESFET, however, his results can be employed in identifying the nonlinear contributors to HEMT performance as well.

Gopinath and Rankin (79,119) have performed a study identifying the relative contributions of the various nonlinear elements of MESFETs valuable for harmonic generation. Their work emphasizes harmonic generation at the second harmonic using computer simulations and identifies the major contributors to the nonlinear behavior of the MEFSET as (1) C_{gs} and C_{gd}, (2) drain current nonlinearity, which results from the drain current clipping when V_{gs} swings below pinch-off or into forward conduction, (3) the nonlinearity of the drain current equation representing I_{ds}, and (4) output resistance nonlinearity.

Based on computer analysis, Gopinath and Rankin conclude that, in the absence of other nonlinear contributions, the second harmonic power level due to C_{gs} is on the order of 18 to 11 dB below the output power at the fundamental. In evaluating the effect of I_{ds} clipping, they neglect the transfer characteristic of I_{ds} and perform a Fourier analysis of the half-wave rectified waveform with $V_{gs} = 0$ V. They find that the second harmonic output power level is 7.4 dB below the output power level at the fundamental. Gopinath and Rankin analyze the nonlinear contributions from the I_{ds} current equation nonlinearity and the output resistance by simulating the harmonic response of the FET with the drain current represented by Eqs. (65) and (66), respectively. The simulations show that the second harmonic output power level is 16 dB below the output power level at the fundamental using Eq. (65) to represent I_{ds}, and that the second harmonic output power level is 15 dB below the output power level at the fundamental when using Eq. (66) to represent I_{ds}.

$$I_{ds} = I_{dss}\left(1 - \frac{V_{gs}}{V_p}\right)^2 \tag{65}$$

$$I_{ds} = I_{dss}\left(1 - \frac{V_{gs}}{V_p}\right)^2\left(1 + \frac{V_{ds}}{R_{do}I_{dss}}\right) \tag{66}$$

The conclusion is that the major contributor to the nonlinearity of the FET is the I_{ds} nonlinear clipping effect which produced second harmonic output power 7.4 dB below the output power at the fundamental. Slight contributions to the nonlinearity of the FET came from the C_{gs} nonlinearity, output conductance nonlinearity, and I_{ds} transfer nonlinearity. It should be noted, however, that the study uses approximations in the computer simulations. The computer model neglects the gate-to-drain branch of the circuit (C_{gd} and D_{gd}), the authors use a predetermined unknown resistive load (R_L), and they indicate that the results are valid only for $R_L \ll R_{do}$ where R_{do} is the output resistance. A final observation of this study is that measured data indicating the accuracy and practicality of the results are not presented.

With reference to the earlier work of Camargo (98), Dow (97) discusses the nonlinear contributions of the MESFET transistor using a graphical approach. He develops an equivalent circuit model from measured *S*-parameters to evaluate the bias dependent nonlinear intrinsic circuit elements, and, afterwards, presents curves representing g_m, C_{gs}, and G_{ds} versus V_{gs} and V_{ds} to show the nonlinear behavior of these parameters. Examining the curves, Dow identifies particular bias regions of V_{gs} and V_{ds}, where the nonlinear variation of g_m and G_{ds} is more prominent and significant for harmonic generation. With regard to the contribution from C_{gs}, Dow references the study performed by Gopinath and Rankin, as previously discussed, in stating that second harmonic generation is weakly dependent upon C_{gs} nonlinearity. In summary, Dow's study concludes that harmonic generation is obtained from three sources of the MESFET: (1) nonlinearity of the intrinsic parameters C_{gs}, g_m, and G_{ds}, (2) current rectification, which occurs when the gate voltage swings into forward conduction, and (3) current clipping occurring when the gate voltage swings below pinch-off.

The previous discussions have stressed the determination of the nonlinear elements responsible for harmonic generation in MESFETs. Focusing on the HEMT transistor, Golio (49) indicates that the major nonlinear elements of the HEMT device are (1) the drain-to-source current I_{ds}, from which the transconductance and output conductance are derived, (2) the gate-to-source and gate-to-drain capacitors (C_{gs} and C_{gd}), and (3) the gate-to-source and gate-to-drain diodes (D_{gs} and D_{gd}).

HEMT Characteristics. Modeled drain-to-source current, transconductance, and output conductance data for a Fujitsu FHX35LG HEMT are shown below to demonstrate the nonlinear characteristics of these types of active devices. Static I–V curves are shown in Figs. 26 and 27 for the transistor using the modeling techniques previously discussed and the equivalent nonlinear model shown in Fig. 28. From the static I–V curves, the transconductance and output conductance are derived and plotted versus the drain-to-source (V_{ds}) and gate-to-source (V_{gs}) voltages as shown in Figs. 29–32. These plots

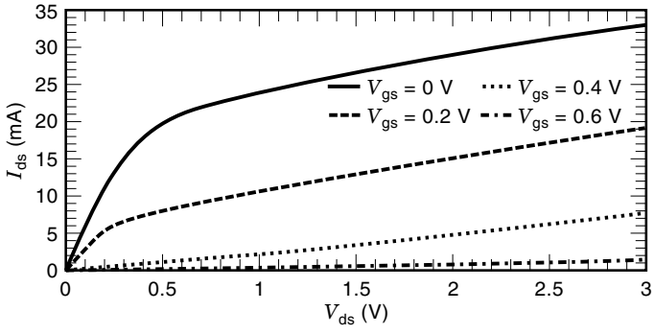

Figure 26. Modeled drain current of HEMT transistor versus drain-to-source voltage.

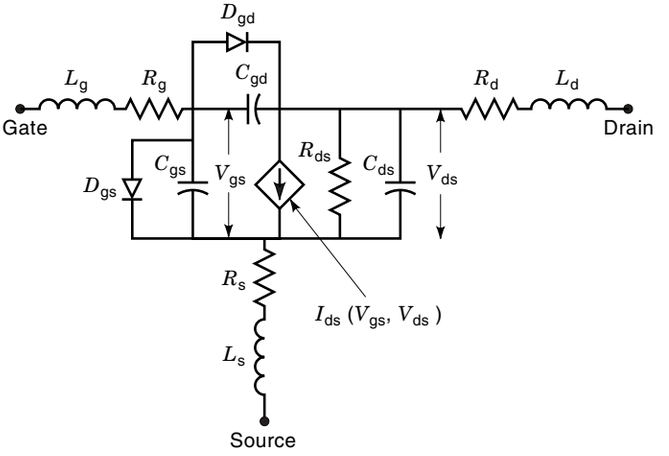

Figure 28. HEMT/PHEMT nonlinear equivalent model.

graphically display the nonlinearity of the transconductance and output conductance of the HEMT transistor as functions of the dc bias voltages. As shown in these plots, these elements show varying degrees of nonlinearity, which are dependent on the drain-to-source (V_{ds}) and gate-to-source (V_{gs}) voltages bias. The exploitation of these nonlinearities with respect to the optimum bias conditions will be discussed in the following section.

Nonlinearities Utilized for Frequency Multiplication. The preceding sections presented a general synopsis of device nonlinearities. This section delineates the nonlinearities of specific importance for frequency multiplication applications, given certain optimum bias conditions. Additionally, the impact of terminating impedances on multiplier performance is detailed.

Optimum Bias Selection. Golio (49) has noted that the drain-to-source current (I_{ds}) contributes to the nonlinear behavior of the HEMT transistor. In this accord, static I–V curves representing the drain-to-source current are utilized to characterize two dominant nonlinear circuit elements previously identified: the transconductance (g_m) and the output conductance (g_{ds}). These parameters plotted versus the drain-to-source (V_{ds}) and gate-to-source (V_{gs}) voltages as shown in Figs. 26–32, show the nonlinearity of the elements displayed as a function of the dc bias voltages.

For the class of multipliers under consideration, the nonlinear behavior of the drain-to-source current (I_{ds}) produces harmonic generation through its clipping effect (79,98). In the case of harmonic generation, the conclusion has been advanced that *optimum* harmonic generation occurs for either $V_{gs} = 0$ or $V_{gs} = V_p$ (97,98,102,127). If the FET is biased at $V_{gs} = 0$, the input voltage waveform appearing across the gate-to-source capacitance (C_{gs}) is clipped and will be half-wave rectified due to the conduction cycles experienced by the gate-to-source diode. This rectified waveform is transferred to I_{ds} through the device's transfer properties as reflected by the analytical relation between I_{ds} and V_{gs} (55). When the device is biased at the pinch-off voltage ($V_{gs} = V_p$), however, the input voltage at the gate causes the FET to turn on during the positive half-cycle of the input voltage and the output voltage again becomes a half-wave rectified waveform. When the gate voltage is biased between 0 V and pinch-off ($0 \geq V_{gs} \geq V_p$), and the input voltage swing is large enough to cause clipping on both ends, the output current at the drain will resemble a square wave. If the square wave is symmetrical, the second harmonic component will be small, but the third harmonic is large allowing frequency tripling (97).

It has been shown that rich harmonic generation will result for Class A and Class B operation of the transistor (97,98). Class A operation occurs for $V_{gs} = 0$ V and causes drain current (I_{ds}) rectification when the gate diode swings into forward conduction. Class B operation occurs for $V_{gs} = V_p$, where V_p is the pinch-off voltage, and causes the drain

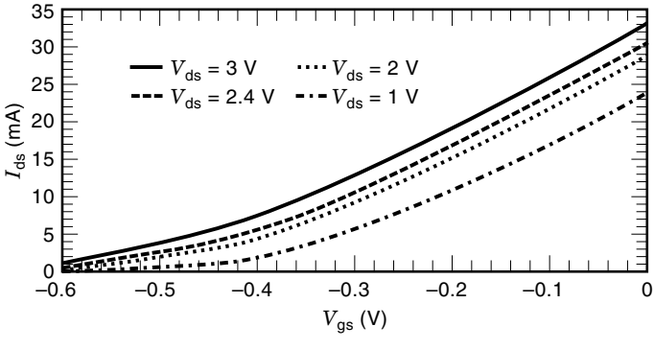

Figure 27. Modeled drain current of HEMT transistor versus gate-to-source voltage.

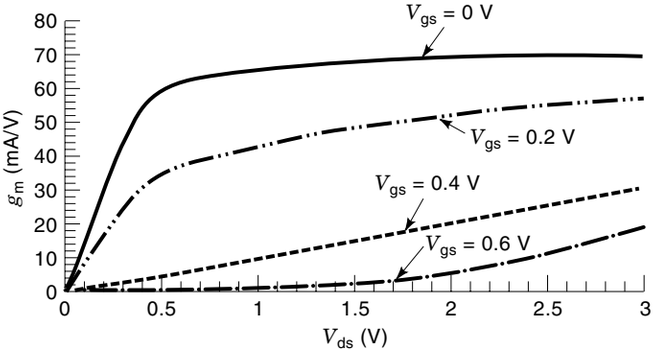

Figure 29. Modeled transconductance of HEMT transistor versus drain-to-source voltage.

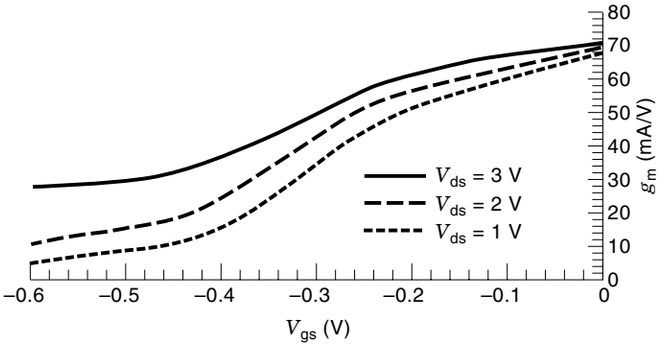

Figure 30. Modeled transconductance of HEMT transistor versus gate-to-source voltage.

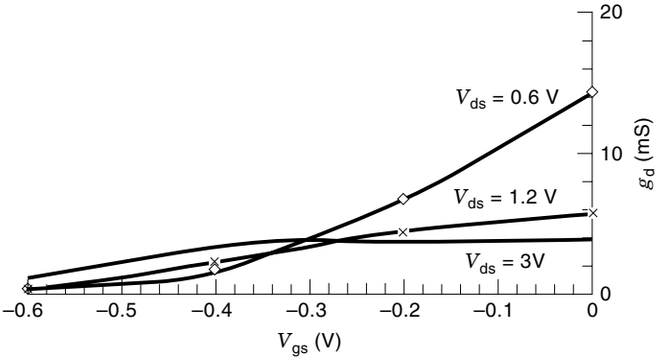

Figure 32. Modeled output conductance of HEMT transistor versus gate-to-source voltage.

current to clip when the gate voltage swings below pinch-off. Dow (97) and Camargo (98) conclude that Class A FET multipliers provide good multiplication gain and poor dc to RF efficiency, while Class B FET multipliers have poor multiplication gain and good dc to RF efficiency.

Using the dc-to-RF efficiency expression, Eq. (63), the efficiency for typical HEMT frequency doublers which was simulated with $V_{gs} = V_p$ and $V_{gs} = 0$ V, respectively, can be computed. As an example, evaluating various simulation data for $V_{gs} = V_p$, the dc-to-RF efficiency is 23.5%, and for typical simulations for $V_{gs} = 0$ V, the dc-to-RF efficiency is 0.03%. In each simulation the dc supply voltage (V_{ds}) was 3 V, which causes the dc power for the simulation with $V_{gs} = 0$ V to be considerably higher and, subsequently, to reduce the dc-to-RF efficiency. Usually, for Class A operation the device is biased at a lower V_{ds} voltage than the case presented here, thus, reducing the dc power and increasing the dc-to-RF efficiency.

Focusing on the Fujitsu FHX35LG HEMT device, measured and modeled measurements provide static I–V curves as shown in Fig. 33. From these data, measured and modeled transconductance and output conductance are derived. Figures 34–37 show the transconductance and output conductances plotted as functions of the gate-to-source (V_{gs}) and drain-to-source (V_{ds}) voltages. Recalling that the optimum bias conditions are either $V_{gs} = 0$ or $V_{gs} = V_p$, the HEMT transconductance and output conductance plots of Figs. 34–37 show the nonlinear behavior of the transconductance and output conductance at the optimum bias regions.

In Figs. 34 and 36, oval circles representing the regions (Region I) of optimum nonlinearity are indicated for $V_{gs} = 0$ V. These regions are identified as areas where the nonlinear variation in the transconductance and output conductance is greatest. In Fig. 34, the variation in the transconductance is actually greatest for $V_{ds} < 0.5$ V, but in this area of operation the transistor does not supply appreciable gain, thus limiting its usefulness at these bias levels for significant conversion gains. For $V_{ds} > 1$ V, the transconductance tends to flatten with no significant variation for $V_{gs} = 0$ V. This behavior is observed again in Fig. 36 with the output conductance.

In Figs. 35 and 37, regions (Region II) for optimum nonlinearity are represented for $V_{gs} = V_p$. Again, areas where the nonlinear variation in the magnitudes of the transconductance and output conductance is greatest are indicated by oval circles. In Fig. 35, significant nonlinear variation in the transconductance is also seen in the vicinity of $V_{gs} = -0.3$ V. Operating in this vicinity is optimum for frequency multipliers, where the third harmonic (frequency tripler) is of interest (97). Biasing in this vicinity with large voltage swings at the gate of the FET causes the I_{ds} waveform to clip at both pinch-off and forward conduction and causes I_{ds} to resemble a square wave, which enhances the third harmonic frequency (97). In Fig. 35 significant variation in the output conductance also occurs for $V_{gs} \approx 0$ to -0.1 V for lower V_{ds} values ($V_{ds} \leq 0.6$ V). As mentioned previously, the gain of the transistor diminishes significantly in these bias areas thus causing the conversion gain of the frequency multiplier to reduce as well.

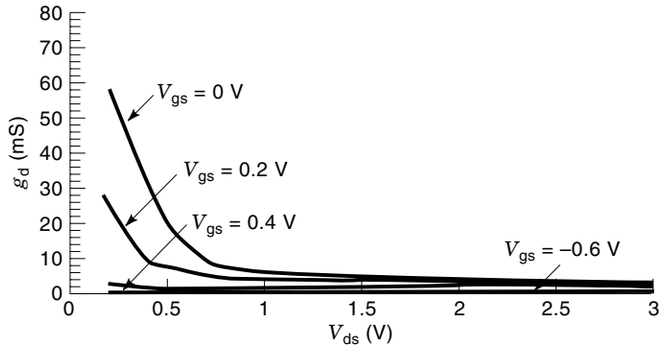

Figure 31. Modeled output conductance of HEMT transistor versus drain-to-source voltage.

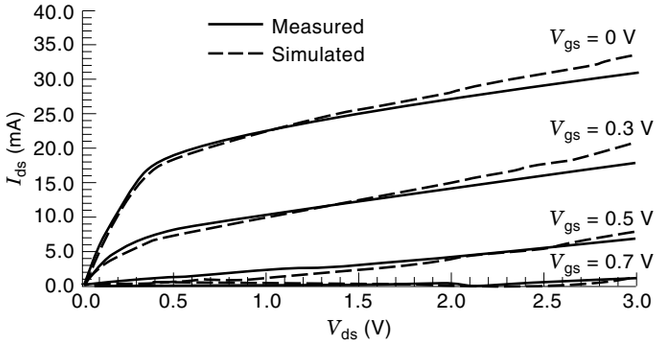

Figure 33. Measured and simulated IV curves of FHX35LG HEMT transistor.

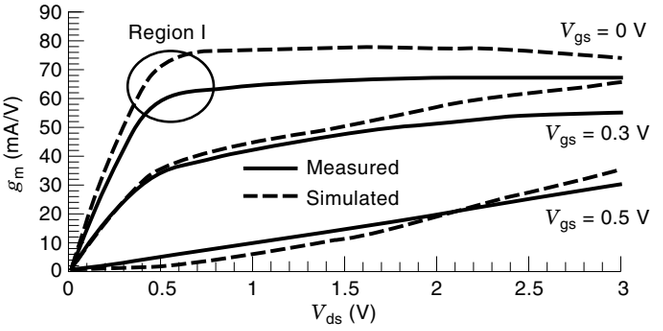

Figure 34. Measured and simulated transconductance of FHX35LG (Region I).

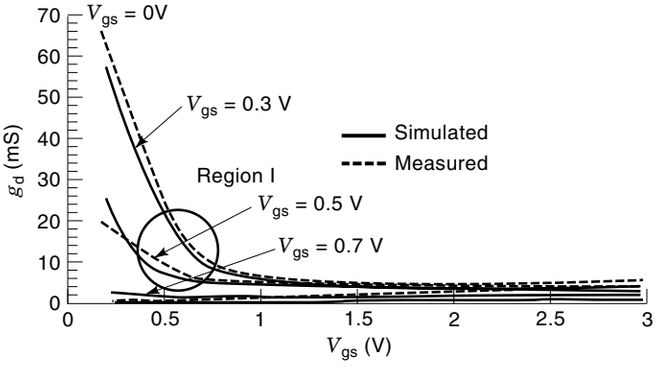

Figure 36. Measured and simulated output conductance of FHX35LG (Region I).

From these curves the prominent nonlinearity regions for $V_{gs} = 0$ is Region I of Fig. 36, where g_{ds} is dominant and for $V_{gs} = V_p$, Region II of Fig. 35, with g_m showing the dominant effect.

Detrimental Parasitics

Definition of the Parasitics. The equivalent circuit topology for the nonlinear FET transistor as given in Fig. 25 includes the parasitic elements (L_s, L_g, L_d, R_s, R_d, and R_g). These parasitics arise from the fabrication process in the development of semiconductor transistors and influence the performance of the transistor and, thus, warrant inclusion into the equivalent circuit model. The parasitic inductors (L_s, L_g, and L_d) primarily represent the inductance associated with the metal contact pads deposited on the active channel layer of the FET. The source and drain parasitic resistors (R_s and R_d) represent the contact resistance of the ohmic contacts underneath the metal contact pads and any bulk resistance leading up to the active channel, and the gate parasitic resistance (R_g) represents the metallization resistance of the gate Schottky contact (49).

Optimum Bias Selection Referencing Harmonic Terminations. A primary factor affecting optimum performance of microwave multipliers employing nonlinear devices is the proper termination of the fundamental and other harmonic frequency components with regard to bias selection. This section presents a *quantitative* analysis leading to the assessment of optimum terminating impedances in the design of active frequency multipliers, with special attention given to harmonics other than those desired. The analysis includes computer modeled HEMT data and supporting measured data for corresponding circuit realizations. Circuit designs are presented utilizing HEMT transistors as the active element to verify modeled results. Based on available literature, the results demonstrate, for the first time, the *quantitative* effects of harmonic termination on active multiplier conversion gain and fundamental and higher harmonic suppression. An experimental design, which will be discussed later, reveals an improvement in multiplier gain of 77% over the conventional approach, and data are presented which *quantitatively* illustrate the advantages of impedance termination considerations under optimal bias conditions.

Background and Motivation. Numerous techniques exist for the realization of frequency multipliers, as will be discussed below. At radio frequencies, these techniques typically employ a nonlinear device to generate the desired frequency multiple. In the design of passive multipliers, the nonlinear element is typically a varactor diode. In the active case, the nonlinear element typically includes any of several transistor classes such as BJT, FET, etc.

In many frequency multiplier design approaches, the operating performance is improved by the proper selection of input and output circuits terminating impedances at the fundamental and harmonic frequencies (91–95,109,145).

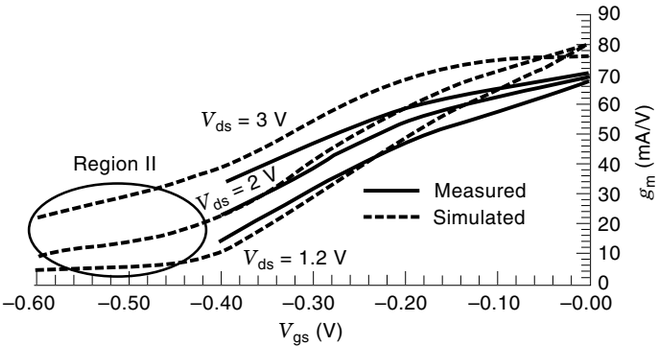

Figure 35. Measured and simulated transconductance of FHX35LG (Region II).

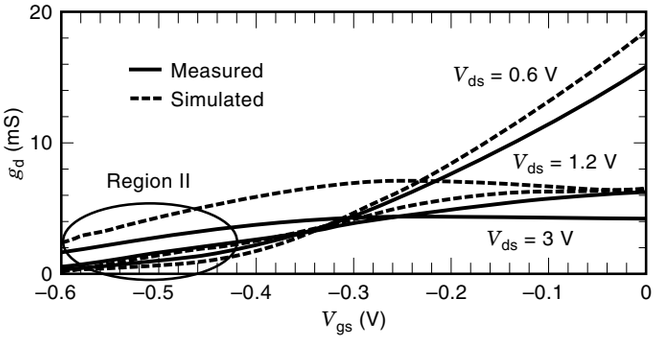

Figure 37. Measured and simulated output conductance of FHX35LG (Region II).

This section presents a *quantitative* analysis of the optimization of active multiplier conversion gain and spectral purity, as governed by fundamental and harmonic terminating impedances and regions of nonlinearity. It is believed that access to this quantitative information will be of use for designers of future circuits. HEMT transistors are employed to represent the class of nonlinear elements to illustrate the approach. The optimum terminating impedances are determined for the input and output ports of the active device, utilizing a recent nonlinear circuit model for HEMT transistors. This is in marked contrast with earlier studies which used approximations in the simulated performance predictions (79,93,98). The results presented in this section incorporate dependences between the input and output harmonic terminating impedances which are not found in previous studies. For the multipliers examined in this section, these impedances include terminations at the fundamental, second harmonic, and third harmonic frequencies. Measured data are presented which validate the practicality of the designs and the accuracy of the simulations.

Nonlinear Model. An accurate nonlinear circuit model is required for the quantitative assessment of optimum terminating impedances in the design of active frequency multipliers. Such an equivalent circuit model permits supporting simulated data to accompany any measured data which further authenticate results. An accurate nonlinear model was presented earlier for the Fujitsu FHX35LG HEMT, which will be employed below for analyzing bias selection with regard to harmonic terminations (case parasitics are included in the model but not shown in the figure).

Static I–V curves for this HEMT, obtained from the model of Fig. 25 and laboratory measurements, are employed to characterize two dominant circuit element nonlinearities: transconductance (g_m) and the output conductance (g_d). These parameters (modeled *and* measured), which were derived from the above sources, are plotted versus the drain-to-source (V_{ds}) and gate-to-source (V_{gs}) voltages shown in Figs. 33–37. These plots graphically display the nonlinearity of the corresponding HEMT elements as a function of the dc bias voltages. The conclusions for the HEMT multiplier are presented quantitatively below.

Utilizing the HMET transconductance and output conductance plots of Figs. 33–37, the prominent nonlinear regions for the optimum dc bias points (either $V_{gs} = 0$ or $V_{gs} = V_p$) were identified in previous sections. Fundamental load line analysis indicates that the optimum impedance for Region I ($V_{gs} = 0$) is an open-circuit impedance which allows a maximum V_{ds} voltage swing, and for Region II ($V_{gs} = V_p$) the optimum impedance is a short-circuit impedance which allows a maximum I_{ds} current swing (145). These qualitative assertions will be substantiated *quantitatively* in the ensuing discussion.

The above analysis provides motivation for development of an optimal design approach. We employ the following multiplier design as an illustration. The basic topology of the frequency multiplier used is illustrated in Fig. 37. In this configuration, SC_i, $i = 1 \ldots n$, and OC_j, $j = 1 \ldots m$, represent short-circuit and open-circuit terminating impedances, respectively, for the multiplier input network at the respective frequencies. Similarly, SC_k, $k = 1 \ldots o$, and OC_l, $l = 1 \ldots p$, represent short- and open-circuit terminating impedances for the multiplier output network. An infinite number of circuit realizations exist which conform to the configuration of Fig. 38. This provides the motivation for development of a matrix of various circuit configurations as illustrated in Table 1, which displays various harmonic terminating impedances on the input and output ports of the multiplier realization depicted in Fig. 38. Tables have been constructed for multiplier operation (up to the third harmonic) utilizing the precision HEMT computer model with case parasitics. Table 1, the left-hand vertical column represents various impedance terminations of the input network at the fundamental, second harmonic, and third harmonic frequencies. The top horizontal row represents various impedances of the output network at the fundamental, second harmonic, and third harmonic frequencies.

To assess performance under various load terminations, several load configurations were analyzed. Based on previous discussions, fundamental and harmonic loads of interest may be short-circuited, open-circuited, matched or 50 Ω.

As a first case, the options shown in Tables 1 and 2 were selected. Since only 50 Ω, short and open loads are used, this choice of terminations would appear to provide a concrete basis for assessing the effects of a variety of other input and output harmonic load conditions. Table 1 illustrates the conversion gains obtained employing the FHX35LG HEMT utilizing a Harmonic Balance program with input and output networks synthesized with lumped elements to realize the indicated harmonic terminations with $f_0 = 3$ GHz. The HEMT in this table is biased at pinch-off $V_{gs} = V_p$ and driven with 0 dBm at the gate terminal (Region II). This table is presented as a basis by which to measure the *quantitative* impact of a variety of terminations on multiplier conversion gain. The numbers to the right of each entry in the table represent the powers obtained at respective harmonics. It is instructive to consider a typical entry of interest in this table. The entry located in the second row and second column, for example, shows that a conversion gain of 1.5 dB is obtained if the input network terminates the fundamental f_0 and third harmonic $3f_0$ in 50 Ω, while the second harmonic $2f_0$ is short-circuited. The output network for this entry terminates the fundamental in a short circuit and all other harmonics in 50 Ω. Several authors (93,98,99,102) have reported that the input network should terminate the second harmonic in a short circuit. For lumped input circuit realizations, however, this table reveals that this provides a 1.5 dB improvement over a 50 Ω or an open circuit termination at $2f_0$ (row 1, column 2 and row 5, column 2, respectively). While the conversion gains represented in *this* table are not large and the dB values do not show great variation, several trends are seen to emerge, and subsequent results will substantiate their implications. In particular, the impact of *input* network terminations from the data in rows 2 and 3 show, that for doubler operation, a short circuit termination at $2f_0$ provides the best conversion gain in all cases considered.

Furthermore, a perusal of output network termination responses shows that a short circuit at f_0 provides the best performance using conversion gain as a basis.

Table 2 shows similar data when the HEMT is biased at $V_{gs} = 0$ (Region I). This V_{gs} value was chosen in accordance with our previous discussion on optimum bias regions. While an important outcome of the $V_{gs} = 0$ table was typically lower conversion gains in comparison with Table 1, where $V_{gs} = V_p$, an even more significant observation is the dramatic im-

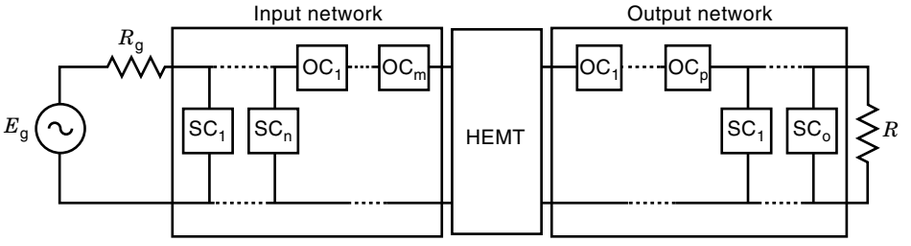

Figure 38. Frequency multiplier realization.

provement (~12 dB) obtained by employing an *open* circuit termination at f_0 in the output network, in contrast with a short circuit, which was the optimum case for Region II. Note that Table 1 predicts only a 1.6 dB improvement for the analogous comparison.

Based on the above, we present results only for the specific case where the input network is short-circuited at $2f_0$ in the ensuing discussion.

Table 3 presents the results obtained for Region II operation ($V_{gs} = V_p$) when the input network was synthesized to provide a matched load at the fundamental frequency, f_0, and a short at $2f_0$. In comparison with its counterpart in row 2 of Table 1 which had a 50 Ω termination at f_0, it is seen that, as expected, significant improvements occur in conversion gains for all output network impedance terminations. A perusal of the values indicates that *significant increases* in conversion gain of over 5 dB are typical in each case. Furthermore, the following quantitative results may be observed for various *output* network terminations: (i) 3.0 dB better conversion gains are obtained due to short circuiting as compared with open circuiting the fundamental (i.e., 8.0 dB vs. 5.0 dB), (ii) 1.5 dB better conversion gain will be obtained for a short circuit at f_0 in comparison with a 50 Ω termination (notwithstanding the fact that the 50 Ω case would require some form of output circuit fundamental suppression), (iii) 1.2 dB of additional conversion gain is obtained if the third harmonic is open circuited in contrast with the frequently used short-circuited third harmonic (8.6 vs. 7.4 dB), and (iv) 3.8 dB additional conversion gain is obtained over the case where an open circuit fundamental and short circuit third harmonic output network are employed (i.e., 8.6 dB vs 4.8 dB).

Table 4 presents the results obtained for Region II operation when the output network is synthesized to provide a matched load at the second harmonic ($2f_0$) versus the previous cases where a simple 50 Ω load was employed. Based on these results, it can be seen that for output network terminations, where the fundamental has been short circuited, an addi-

Table 1. Doubler Simulations with Lumped Components ($V_{gs} = -0.7$ V, $P_{in} = 0$ dBm, $V_{ds} = 3$ V)

		Output Power (dBm)[a]								
Input Network $(\Omega)^{a,b}$	Output Network $(\Omega)^{a,b}$:	$\begin{pmatrix}50\\50\\50\end{pmatrix}$	$\begin{pmatrix}0\\50\\50\end{pmatrix}$	$\begin{pmatrix}\infty\\50\\50\end{pmatrix}$	$\begin{pmatrix}0\\50\\\infty\end{pmatrix}$	$\begin{pmatrix}\infty\\50\\\infty\end{pmatrix}$	$\begin{pmatrix}50\\50\\0\end{pmatrix}$	$\begin{pmatrix}50\\50\\\infty\end{pmatrix}$	$\begin{pmatrix}0\\50\\0\end{pmatrix}$	$\begin{pmatrix}\infty\\50\\0\end{pmatrix}$
$\begin{pmatrix}50\\50\\50\end{pmatrix}$		$\begin{pmatrix}5.96\\-0.9\\-14.7\end{pmatrix}$	$\begin{pmatrix}-73\\0\\-14\end{pmatrix}$	$\begin{pmatrix}-66.5\\-1\\-17.8\end{pmatrix}$	$\begin{pmatrix}-73.2\\0.3\\-72.5\end{pmatrix}$	$\begin{pmatrix}-66.5\\-0.7\\-107\end{pmatrix}$	$\begin{pmatrix}5.9\\-1.3\\-94\end{pmatrix}$	$\begin{pmatrix}5.9\\-0.7\\-104\end{pmatrix}$	$\begin{pmatrix}-73.2\\-0.2\\-94\end{pmatrix}$	$\begin{pmatrix}-66.5\\-1.4\\-97.2\end{pmatrix}$
$\begin{pmatrix}50\\0\\50\end{pmatrix}$		$\begin{pmatrix}6.2\\0.3\\-11.8\end{pmatrix}$	$\begin{pmatrix}-72.9\\1.5\\-10.6\end{pmatrix}$	$\begin{pmatrix}-66.3\\-0.1\\-17.2\end{pmatrix}$	$\begin{pmatrix}-72.8\\1.8\\-68.9\end{pmatrix}$	$\begin{pmatrix}-66.3\\0.2\\-106\end{pmatrix}$	$\begin{pmatrix}6.2\\0\\-92\end{pmatrix}$	$\begin{pmatrix}6.3\\0.7\\-100\end{pmatrix}$	$\begin{pmatrix}-72.9\\1.2\\-91.1\end{pmatrix}$	$\begin{pmatrix}-66.3\\-0.5\\-97.7\end{pmatrix}$
$\begin{pmatrix}50\\0\\0\end{pmatrix}$		$\begin{pmatrix}6\\1.2\\-13.4\end{pmatrix}$	$\begin{pmatrix}-72.9\\1.5\\-10.6\end{pmatrix}$	$\begin{pmatrix}-66.3\\-0.1\\-17.2\end{pmatrix}$	$\begin{pmatrix}-72.8\\1.8\\-99.1\end{pmatrix}$	$\begin{pmatrix}-66.5\\0.9\\-109.6\end{pmatrix}$	$\begin{pmatrix}6.2\\0.3\\-11.8\end{pmatrix}$	$\begin{pmatrix}6.3\\0.7\\-100.6\end{pmatrix}$	$\begin{pmatrix}-72.9\\1.2\\-91.1\end{pmatrix}$	$\begin{pmatrix}-66.3\\-0.5\\-97.7\end{pmatrix}$
$\begin{pmatrix}50\\50\\0\end{pmatrix}$		$\begin{pmatrix}5.9\\-2.2\\-17.1\end{pmatrix}$	$\begin{pmatrix}-73.2\\1.3\\-16.8\end{pmatrix}$	$\begin{pmatrix}-66.5\\-2.3\\-15.8\end{pmatrix}$	$\begin{pmatrix}-73.2\\-1.2\\-108.2\end{pmatrix}$	$\begin{pmatrix}-66.5\\-1.7\\-106.6\end{pmatrix}$	$\begin{pmatrix}5.9\\-1.3\\-94.5\end{pmatrix}$	$\begin{pmatrix}5.9\\-2.1\\-108\end{pmatrix}$	$\begin{pmatrix}-73.2\\-0.1\\-94.1\end{pmatrix}$	$\begin{pmatrix}-66.7\\-2.7\\-90.5\end{pmatrix}$
$\begin{pmatrix}50\\\infty\\50\end{pmatrix}$		$\begin{pmatrix}6.1\\-1\\-15.9\end{pmatrix}$	$\begin{pmatrix}-73\\0\\-15.3\end{pmatrix}$	$\begin{pmatrix}-66.6\\-1.2\\-21.2\end{pmatrix}$	$\begin{pmatrix}-73.1\\0.1\\-104\end{pmatrix}$	$\begin{pmatrix}-66.6\\-1\\-109\end{pmatrix}$	$\begin{pmatrix}6.1\\-1.1\\-96\end{pmatrix}$	$\begin{pmatrix}6.1\\-0.8\\-105\end{pmatrix}$	$\begin{pmatrix}-73\\-0.2\\-96.1\end{pmatrix}$	$\begin{pmatrix}-66.5\\-1.5\\-100.4\end{pmatrix}$
$\begin{pmatrix}50\\\infty\\\infty\end{pmatrix}$		$\begin{pmatrix}6.1\\-0.9\\-15.7\end{pmatrix}$	$\begin{pmatrix}-73\\0\\-15.1\end{pmatrix}$	$\begin{pmatrix}-66.5\\-1.1\\-20\end{pmatrix}$	$\begin{pmatrix}-73\\0.3\\-104\end{pmatrix}$	$\begin{pmatrix}-66.5\\-0.9\\-108\end{pmatrix}$	$\begin{pmatrix}6.1\\-1.2\\-96.2\end{pmatrix}$	$\begin{pmatrix}6.1\\-0.7\\-105\end{pmatrix}$	$\begin{pmatrix}-73\\-0.2\\-96\end{pmatrix}$	$\begin{pmatrix}-66.5\\-1.4\\-99.8\end{pmatrix}$
$\begin{pmatrix}50\\50\\\infty\end{pmatrix}$		$\begin{pmatrix}6\\-0.8\\-14.3\end{pmatrix}$	$\begin{pmatrix}-73.1\\0.1\\-13.6\end{pmatrix}$	$\begin{pmatrix}-66.5\\-0.9\\-17\end{pmatrix}$	$\begin{pmatrix}-73\\0.4\\-102\end{pmatrix}$	$\begin{pmatrix}-66.5\\-0.7\\-105\end{pmatrix}$	$\begin{pmatrix}6\\-1.3\\-94.4\end{pmatrix}$	$\begin{pmatrix}6\\-0.5\\-103\end{pmatrix}$	$\begin{pmatrix}-73\\-0.2\\-93.9\end{pmatrix}$	$\begin{pmatrix}-66.5\\-1.4\\-96.9\end{pmatrix}$

[a] At $\begin{pmatrix}f_0\\2f_0\\3f_0\end{pmatrix}$.

[b] 0 = short circuit; ∞ = open circuit.

Table 2. Doubler Simulations with Lumped Components (V_{gs} = 0 V, P_{in} = 0 dBm, V_{ds} = 3 V)

Input Network $(\Omega)^{a,b}$	Output Network $(\Omega)^{a,b}$:	Output Power (dBm)[a]								
		$\begin{pmatrix}50\\50\\50\end{pmatrix}$	$\begin{pmatrix}0\\50\\50\end{pmatrix}$	$\begin{pmatrix}\infty\\50\\50\end{pmatrix}$	$\begin{pmatrix}0\\50\\\infty\end{pmatrix}$	$\begin{pmatrix}\infty\\50\\\infty\end{pmatrix}$	$\begin{pmatrix}50\\50\\0\end{pmatrix}$	$\begin{pmatrix}50\\50\\\infty\end{pmatrix}$	$\begin{pmatrix}0\\50\\0\end{pmatrix}$	$\begin{pmatrix}\infty\\50\\0\end{pmatrix}$
$\begin{pmatrix}50\\50\\50\end{pmatrix}$		$\begin{pmatrix}12.5\\-10.1\\-13.9\end{pmatrix}$	$\begin{pmatrix}-66.2\\-10.9\\-10.7\end{pmatrix}$	$\begin{pmatrix}-62.1\\-2.4\\-7.1\end{pmatrix}$	$\begin{pmatrix}-66.2\\-10.6\\-98\end{pmatrix}$	$\begin{pmatrix}-62\\-2\\-92\end{pmatrix}$	$\begin{pmatrix}12.5\\-10.2\\-94.8\end{pmatrix}$	$\begin{pmatrix}12.5\\-10\\-101\end{pmatrix}$	$\begin{pmatrix}-66.3\\-11.2\\-91.8\end{pmatrix}$	$\begin{pmatrix}-62.1\\-2.2\\-89.5\end{pmatrix}$
$\begin{pmatrix}50\\0\\50\end{pmatrix}$		$\begin{pmatrix}12.4\\-11.1\\-14.1\end{pmatrix}$	$\begin{pmatrix}-66\\-14.7\\-11.1\end{pmatrix}$	$\begin{pmatrix}-62.2\\-2.6\\-7.3\end{pmatrix}$	$\begin{pmatrix}-66\\-14.1\\-98.4\end{pmatrix}$	$\begin{pmatrix}-62\\-2.1\\-92.7\end{pmatrix}$	$\begin{pmatrix}12.4\\-11.3\\-94.9\end{pmatrix}$	$\begin{pmatrix}12.5\\-10.8\\-101\end{pmatrix}$	$\begin{pmatrix}-66.2\\-15.3\\-92.2\end{pmatrix}$	$\begin{pmatrix}-62\\-2.7\\-89.8\end{pmatrix}$
$\begin{pmatrix}50\\0\\0\end{pmatrix}$		$\begin{pmatrix}12.4\\-11.2\\-18.6\end{pmatrix}$	$\begin{pmatrix}-66\\-15.3\\-14.6\end{pmatrix}$	$\begin{pmatrix}-62\\-3.2\\-5.9\end{pmatrix}$	$\begin{pmatrix}-66\\-15.4\\-105\end{pmatrix}$	$\begin{pmatrix}-62\\-2.2\\-94.2\end{pmatrix}$	$\begin{pmatrix}12.4\\-10.8\\-82.7\end{pmatrix}$	$\begin{pmatrix}12.4\\-11.1\\-109\end{pmatrix}$	$\begin{pmatrix}-66.1\\-13.8\\-81.8\end{pmatrix}$	$\begin{pmatrix}-62.4\\-2.8\\-78\end{pmatrix}$
$\begin{pmatrix}50\\50\\0\end{pmatrix}$		$\begin{pmatrix}12.4\\-10.2\\-18.3\end{pmatrix}$	$\begin{pmatrix}-66.3\\-11.2\\-14.9\end{pmatrix}$	$\begin{pmatrix}-62.1\\-3\\-5.7\end{pmatrix}$	$\begin{pmatrix}-66\\-11.2\\-37.1\end{pmatrix}$	$\begin{pmatrix}-62.1\\-2.1\\-93.9\end{pmatrix}$	$\begin{pmatrix}12.5\\-10.4\\-82.4\end{pmatrix}$	$\begin{pmatrix}12.4\\-10\\-109\end{pmatrix}$	$\begin{pmatrix}-66\\-10.9\\-82.2\end{pmatrix}$	$\begin{pmatrix}-62.3\\-2.4\\-78\end{pmatrix}$
$\begin{pmatrix}50\\\infty\\50\end{pmatrix}$		$\begin{pmatrix}12.6\\-9.3\\-13.7\end{pmatrix}$	$\begin{pmatrix}-66.1\\-10.3\\-10.3\end{pmatrix}$	$\begin{pmatrix}-62.1\\-2.1\\-7.1\end{pmatrix}$	$\begin{pmatrix}-66.1\\-10.1\\-97.8\end{pmatrix}$	$\begin{pmatrix}-62.1\\-1.7\\-92.4\end{pmatrix}$	$\begin{pmatrix}12.6\\-9.3\\-94.6\end{pmatrix}$	$\begin{pmatrix}-12.6\\-9.2\\-101\end{pmatrix}$	$\begin{pmatrix}-66.1\\-10.7\\-91.5\end{pmatrix}$	$\begin{pmatrix}-62.1\\-1.9\\-89.6\end{pmatrix}$
$\begin{pmatrix}50\\\infty\\\infty\end{pmatrix}$		$\begin{pmatrix}12.6\\-9.3\\-13\end{pmatrix}$	$\begin{pmatrix}-66\\-10.3\\-9.7\end{pmatrix}$	$\begin{pmatrix}-62\\-1.9\\-7.3\end{pmatrix}$	$\begin{pmatrix}-66\\-9.9\\-96.5\end{pmatrix}$	$\begin{pmatrix}-62.1\\-1.7\\-91.6\end{pmatrix}$	$\begin{pmatrix}12.6\\-9.3\\-94.8\end{pmatrix}$	$\begin{pmatrix}-12.6\\-9.2\\-100\end{pmatrix}$	$\begin{pmatrix}-66\\-10.7\\-91.5\end{pmatrix}$	$\begin{pmatrix}-62\\-1.8\\-90.7\end{pmatrix}$
$\begin{pmatrix}50\\50\\\infty\end{pmatrix}$		$\begin{pmatrix}12.5\\-10.1\\-13.3\end{pmatrix}$	$\begin{pmatrix}-66.2\\-10.8\\-10.1\end{pmatrix}$	$\begin{pmatrix}-62.1\\-2.2\\-7.3\end{pmatrix}$	$\begin{pmatrix}-66.1\\-10.4\\-96.8\end{pmatrix}$	$\begin{pmatrix}-62.1\\-2\\-91.6\end{pmatrix}$	$\begin{pmatrix}12.5\\-10.2\\-95.1\end{pmatrix}$	$\begin{pmatrix}12.5\\-9.9\\-100\end{pmatrix}$	$\begin{pmatrix}-66.2\\-11.2\\-92\end{pmatrix}$	$\begin{pmatrix}-62.1\\-2.1\\-90.7\end{pmatrix}$

[a] At $\begin{pmatrix}f_0\\2f_0\\3f_0\end{pmatrix}$.

[b] 0 = short circuit; ∞ = open circuit.

tional ≈ 2 dB has been obtained over the results in Table 3 and approximately 9 dB over Table 1 results.

Tables 5 and 6 display the results obtained utilizing microstrip line circuits that were synthesized to provide shorted, open, and 50 Ω terminations at respective fundamental and harmonic frequencies as employed in many traditional designs (79,92,95,97,98,100–110).

With reference to Table 5 (Region II, $V_{gs} = V_p$), a comparison of the effect of the distributed input network (row 2, column 1) with a 50 Ω input network at f_0, $2f_0$, and $3f_0$ (row 1, column 1) shows that 5.2 dB improvement in conversion gain performance may be obtained by employing the distributed structure with a short circuit at $2f_0$. Some additional conclusions obtained from a further perusal of this table are as follows: (i) 8.6 dB conversion gain improvement may be obtained by providing a distributed output network which is short circuited at f_0 and $3f_0$ as compared with 50 Ω input and output terminations (row 1, column 1 vs. row 2, column 4), (ii) with the distributed input network terminated in a short circuit 1.3 dB improvement in conversion gain may be obtained by short circuiting the output network at f_0 and $3f_0$ (column 4) as compared with open circuits at f_0 and $3f_0$ (column 5), (iii) the difference in termination in the output network between open and short circuits at f_0 is on the order of 1 dB, and (iv)

Table 3. Doubler Simulations Matched on Input with Microstrip Transmission Lines (V_{gs} = −0.7 V, P_{in} = 0 dBm, V_{ds} = 3 V)

Input Network $(\Omega)^{a,b}$	Output Network $(\Omega)^{a,b}$:	Output Power (dBm)[a]								
		$\begin{pmatrix}50\\50\\50\end{pmatrix}$	$\begin{pmatrix}0\\50\\50\end{pmatrix}$	$\begin{pmatrix}\infty\\50\\50\end{pmatrix}$	$\begin{pmatrix}0\\50\\\infty\end{pmatrix}$	$\begin{pmatrix}\infty\\50\\\infty\end{pmatrix}$	$\begin{pmatrix}50\\50\\0\end{pmatrix}$	$\begin{pmatrix}50\\50\\\infty\end{pmatrix}$	$\begin{pmatrix}0\\50\\0\end{pmatrix}$	$\begin{pmatrix}\infty\\50\\0\end{pmatrix}$
$\begin{pmatrix}50\\50\\50\end{pmatrix}$		$\begin{pmatrix}5.96\\-0.9\\-14.7\end{pmatrix}$	$\begin{pmatrix}-217\\-0.3\\-221\end{pmatrix}$	$\begin{pmatrix}-210\\-0.7\\-231\end{pmatrix}$	$\begin{pmatrix}-215\\-0.2\\-270\end{pmatrix}$	$\begin{pmatrix}-208\\0.4\\-270\end{pmatrix}$	$\begin{pmatrix}5.5\\-3.9\\-232\end{pmatrix}$	$\begin{pmatrix}4.1\\0.3\\-237\end{pmatrix}$	$\begin{pmatrix}-216\\-3.3\\-270\end{pmatrix}$	$\begin{pmatrix}-209\\-4.2\\-270\end{pmatrix}$
$\begin{pmatrix}M\\0\\54\end{pmatrix}$		$\begin{pmatrix}13\\6.5\\-6.7\end{pmatrix}$	$\begin{pmatrix}-65.7\\8\\-4.1\end{pmatrix}$	$\begin{pmatrix}-62.3\\5\\-7.9\end{pmatrix}$	$\begin{pmatrix}-65.7\\8.6\\-92.1\end{pmatrix}$	$\begin{pmatrix}-62.5\\5.2\\-92.2\end{pmatrix}$	$\begin{pmatrix}13\\6.1\\-87.6\end{pmatrix}$	$\begin{pmatrix}13\\6.9\\-94.9\end{pmatrix}$	$\begin{pmatrix}-65.6\\7.4\\-84.7\end{pmatrix}$	$\begin{pmatrix}-62.2\\4.8\\-92.6\end{pmatrix}$

[a] At $\begin{pmatrix}f_0\\2f_0\\3f_0\end{pmatrix}$.

[b] 0 = short circuit; ∞ = open circuit; M = matched.

Table 4. Doubler Simulations Matched on Input and Output with Microstrip Transmission Lines (V_{gs} = −0.7 V, P_{in} = 0 dBm, V_{ds} = 3 V)

Input Network $(\Omega)^{a,b}$	Output Network $(\Omega)^{a,b}$:	Output Power (dBm)[a]								
		$\begin{pmatrix}50\\50\\50\end{pmatrix}$	$\begin{pmatrix}0\\M\\85\end{pmatrix}$	$\begin{pmatrix}\infty\\M\\85\end{pmatrix}$	$\begin{pmatrix}0\\M\\\infty\end{pmatrix}$	$\begin{pmatrix}\infty\\M\\\infty\end{pmatrix}$	$\begin{pmatrix}36\\M\\0\end{pmatrix}$	$\begin{pmatrix}37\\M\\\infty\end{pmatrix}$	$\begin{pmatrix}0\\M\\0\end{pmatrix}$	$\begin{pmatrix}\infty\\M\\0\end{pmatrix}$
$\begin{pmatrix}M\\0\\54\end{pmatrix}$		$\begin{pmatrix}14.4\\6.4\\-2.9\end{pmatrix}$	$\begin{pmatrix}-70.2\\10.1\\-8.1\end{pmatrix}$	$\begin{pmatrix}-61.9\\-4.7\\-16.2\end{pmatrix}$	$\begin{pmatrix}-70\\10.4\\-89.5\end{pmatrix}$	$\begin{pmatrix}-61.5\\5\\-99.1\end{pmatrix}$	$\begin{pmatrix}12.8\\9.1\\-95.8\end{pmatrix}$	$\begin{pmatrix}12.5\\7.3\\-86.1\end{pmatrix}$	$\begin{pmatrix}-70\\9.5\\-96.7\end{pmatrix}$	$\begin{pmatrix}-60.6\\5.1\\-110.3\end{pmatrix}$

[a] At $\begin{pmatrix}f_0\\2f_0\\3f_0\end{pmatrix}$.

[b] 0 = short circuit; ∞ = open circuit; M = matched.

an additional 2.3 dB of conversion gain is obtained by introducing an additional short-circuited stub at $3f_0$.

Table 6 presents similar results for Region I ($V_{gs} \sim 0$) operation. Several significant conclusions are evident from these results: (i) best performance is considerably less (2.8 dB vs. 7.7 dB) than that for Region II operation, (ii) significant conversion gain improvement is obtained when the output network is open circuited at f_0 in comparison with the short circuited condition (1.8 dB vs. − 13.1 dB ≈ 15 dB, and (iii) 1 dB of conversion gain performance improvement is achieved by introducing an additional open-circuited stub at the third harmonic.

This topic will be revisited in the next section in the discussion of active multiplier design. Specific multiplier designs are illustrated demonstrating the efficacy of harmonic terminations and optimum bias selection.

Active-Multiplier Design Techniques

Existing Design Techniques. Over the last few years, numerous researchers have discussed numerous design approaches leading to various design procedures utilizing various active devices and topologies in different media and frequency ranges. This section presents various existing design techniques and other techniques implemented by the author.

A fundamental topological representation for realization of active microwave multiplier circuits is shown in Fig. 39. While this is not the most generalized topology, it is one of the most frequently used. The physical realization of an efficient frequency multiplier subject to design criteria utilizing this configuration is strongly reliant on the synthesis of networks N_1, N_2, and N_3, which are typically, but not always, passive. The criteria for specification of N_1, N_2, and N_3 rely, heavily as usual, on fundamental active-device parameters. In the case of multipliers, this is heavily dependent upon bias conditions, input power level, and frequency.

Only very seldom have designers intentionally employed feedback (N_3) in multiplier designs in the realization of such circuits. Synthesis of N_3 is typically avoided, due in part to potential stability problems (93,106,147). This network, however, has the potential of providing useful improvement in conversion efficiency by proper combination of harmonics emerging from the active device with the input fundamental, for example, at the correct phase. The feedback network (N_3) combines a harmonic component from the drain (collector) of the transistor with the fundamental component on the gate (base). Theoretically, this produces an enhanced component at the desired output harmonic frequency on the drain (collector), assuming that in the ideal case the phase of the feedback is optimal (106,147).

Some designers have selected a balanced version of the topology given in Fig. 39 for doubler design, with expectations of superior doubler performance (91,109,111–113,148,149).

Table 5. Simulated Doubler Response with Microstrip Elements (Region II; (V_{gs} = −0.7 V, P_{in} = 0 dBm, V_{ds} = 3 V)

Input Network $(\Omega)^{a,b}$	Output Network $(\Omega)^{a,b}$:	Output Power (dBm)[a]					
		$\begin{pmatrix}50\\50\\50\end{pmatrix}$	$\begin{pmatrix}0\\50\\0\end{pmatrix}$	$\begin{pmatrix}\infty\\50\\0\end{pmatrix}$	$\begin{pmatrix}0\\62\\0\end{pmatrix}$	$\begin{pmatrix}\infty\\63\\\infty\end{pmatrix}$	$\begin{pmatrix}27\\49\\\infty\end{pmatrix}$
$\begin{pmatrix}50\\50\\50\end{pmatrix}$		$\begin{pmatrix}5.96\\-0.9\\-14.7\end{pmatrix}$	$\begin{pmatrix}-27.1\\-0.7\\-26.3\end{pmatrix}$	$\begin{pmatrix}-10.4\\-0.9\\-36.2\end{pmatrix}$	$\begin{pmatrix}-25\\0.4\\-52.9\end{pmatrix}$	$\begin{pmatrix}-17.3\\0.8\\-60.1\end{pmatrix}$	$\begin{pmatrix}4\\0.6\\-37.7\end{pmatrix}$
$\begin{pmatrix}50\\0\\50\end{pmatrix}$		$\begin{pmatrix}10.7\\4.3\\-10.2\end{pmatrix}$	$\begin{pmatrix}-27.4\\5.4\\-22.6\end{pmatrix}$	$\begin{pmatrix}-22\\4.5\\-21\end{pmatrix}$	$\begin{pmatrix}-19.9\\7.7\\-46.9\end{pmatrix}$	$\begin{pmatrix}-13.5\\6.4\\-61\end{pmatrix}$	$\begin{pmatrix}9\\7.2\\-32\end{pmatrix}$

[a] At $\begin{pmatrix}f_0\\2f_0\\3f_0\end{pmatrix}$.

[b] 0 = short circuit; ∞ = open circuit.

Table 6. Simulated Doubler Response with Microstrip Elements (Region I; (V_{gs} = 0 V, P_{in} = 0 dBm, V_{ds} = 3 V)

Input Network $(\Omega)^{a,b}$	Output Network $(\Omega)^{a,b}$:	Output Power (dBm)[a]					
		$\begin{pmatrix}50\\50\\50\end{pmatrix}$	$\begin{pmatrix}0\\50\\0\end{pmatrix}$	$\begin{pmatrix}\infty\\50\\\infty\end{pmatrix}$	$\begin{pmatrix}0\\62\\0\end{pmatrix}$	$\begin{pmatrix}\infty\\63\\\infty\end{pmatrix}$	$\begin{pmatrix}27\\49\\\infty\end{pmatrix}$
$\begin{pmatrix}50\\50\\50\end{pmatrix}$		$\begin{pmatrix}12.5\\-10.1\\-13.9\end{pmatrix}$	$\begin{pmatrix}-20.2\\-11.4\\-26.3\end{pmatrix}$	$\begin{pmatrix}-15.1\\-2.5\\-25.4\end{pmatrix}$	$\begin{pmatrix}-22.9\\-10.9\\-49.3\end{pmatrix}$	$\begin{pmatrix}-12.5\\-4\\-55.4\end{pmatrix}$	$\begin{pmatrix}11.1\\-10\\-33.9\end{pmatrix}$
$\begin{pmatrix}50\\0\\50\end{pmatrix}$		$\begin{pmatrix}14.7\\-12.5\\-8.4\end{pmatrix}$	$\begin{pmatrix}-18.4\\-13.1\\-18.4\end{pmatrix}$	$\begin{pmatrix}-14.4\\1.8\\-25.6\end{pmatrix}$	$\begin{pmatrix}-21.3\\-10.4\\-41\end{pmatrix}$	$\begin{pmatrix}-11.1\\2.8\\-52\end{pmatrix}$	$\begin{pmatrix}13.2\\-10.6\\-2.8\end{pmatrix}$

[a] At $\begin{pmatrix}f_0\\2f_0\\3f_0\end{pmatrix}$.

[b] 0 = short circuit; ∞ = open circuit.

These seem to have been inspired by the advantages actually realized in the design of diode doublers (150). Developers of such balanced active multipliers state that these circuits are better due to the natural cancellation of the fundamental and all odd harmonics, thus providing a virtual ground at the output of the active devices and permitting the location of any matching networks closer to the drain (collector) of the devices (99). Furthermore, they indicate that such designs have the advantage of high conversion efficiency, 3 dB better output power, better isolation, good harmonic suppression, and the elimination of the long ($\lambda/4$) stubs that are common in single-ended designs.

One of the classes of designs emphasizes the arrangement of two or more transistors in one of several topological configurations as shown in Figs. 40 and 41. The technique shown in Fig. 40 utilizes two identical fundamental-frequency signals, which are fed 180° out of phase to transistors T_1 and T_2. The circuit functions as a type of active full-wave rectifier in that when the voltage at port 1 is positive, T_1 conducts and T_2 is turned off and current flows through the emitter of T_1 to the load Z_L. When the polarity of the input signal $V(f_1)$ is reversed, T_2 conducts and T_1 is turned off and current flows through the collector of T_2, providing an output to Z_L. This process effectively provides a rectified output at Z_L with the corresponding strong second-harmonic content. This approach has been demonstrated for doubler action over a broad frequency range (1 GHz to 7 GHz) in MMIC topology. Conversion gains range from 0 to 12 dB, utilizing input and output amplification stages. Fundamental rejections of less than 10 dB appear to be realizable.

A block diagram of a typical balanced multiplier design is shown in Fig. 41. At the input, the input signal of the multiplier is fed through a power-divider-phase-shifter, which divides the power between the two transistors with 180° phase difference between the input ports of the transistors. The drains (collectors) of the transistors are connected on the output by a combiner. At the output, the fundamental and harmonic signals have opposite phase, and, by destructive interference, cancel, giving good harmonic suppression. The second-harmonic signals from the transistors have the same phase and thus interfere constructively.

A perusal of the published literature on such balanced designs reveals, however, that they require complex components in their realization. In addition to two "matched" active devices (some designers use more in their "active" matching stages), balanced designs typically require large baluns or power-splitter-phase-shifter combinations, T junctions, and in some cases air bridges. Some realizations also require complex transitions and additional lengths of transmission lines to rotate the active device outputs to achieve a pure reactance output. Finally, only frequency-doubler designs are typically

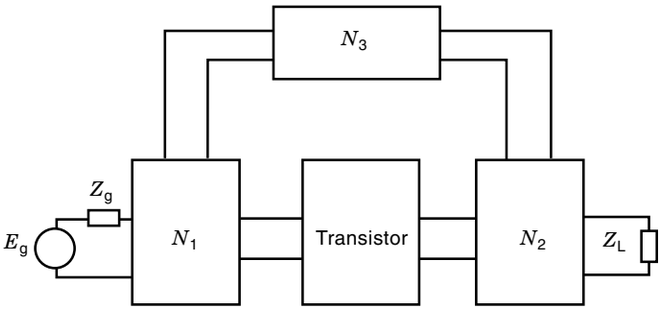

Figure 39. Frequency-multiplier realization.

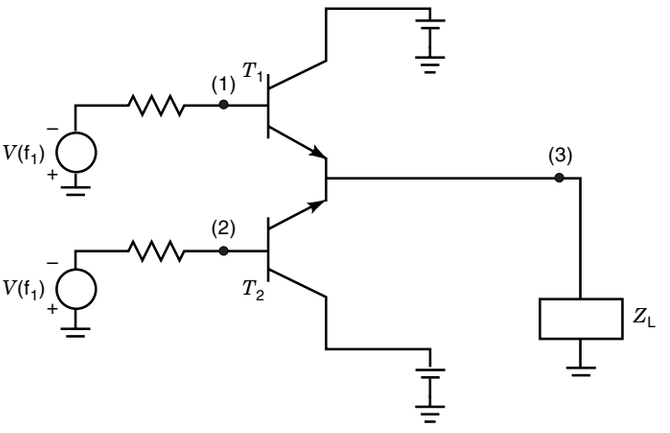

Figure 40. Block diagram of push–push topology of frequency multiplier.

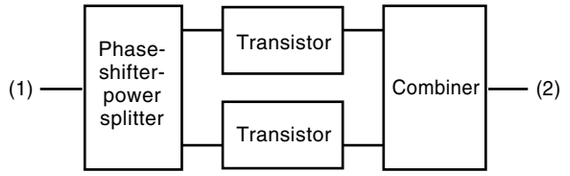

Figure 41. Block diagram of typical balanced frequency multiplier.

reported. It is found that, with due consideration of the importance of the particular active device characteristics and frequency bands, these designs in almost all cases are narrowband (≈10%) (Ref. 112, with −9 dB conversion gains is one exception; it uses an additional active device), have modest conversion gain (−5 dB to +5 dB; 3 dB to 12 dB in one case), and frequently yield sparse data on fundamental suppression (typically between 12 dB and 30 dB).

Hiraoka (148), for example, developed a broadband MMIC balanced frequency doubler with a fundamental frequency of 5 GHz, consisting of a common-gate FET and a common-source FET directly connected in parallel, followed by an output-matching network. A phase-shifter network precedes the common-gate FET to compensate for the phase error between the outputs from the common-gate FET and the common-source FET. A conversion loss of 8 dB to 10 dB was achieved for output frequencies between 6 GHz and 16 GHz. Fundamental-frequency isolation (suppression) better than 17 dB up to output frequencies of 20 GHz was obtained. Unfortunately, the author did not provide any data on the third-harmonic isolation (suppression).

Angelov (113) discusses a 20 GHz to 40 GHz balanced doubler where two common-source PHEMTs are connected in parallel followed by sections of transmission lines on the gates before combining into a 3 dB coupler. The input signal to the doubler is fed to a power divider, which divides the power equally between the two input ports with 180° phase difference between the input ports. Sections of transmission lines connect the power divider to the drain of the PHEMTs. The completed doubler circuit provides approximately −1 dB of conversion gain with a −3 dB bandwidth of approximately 5%. The author notes that the bandwidth is limited mainly by the 180° ratrace coupler. The author does not provide data on the fundamental and the third-harmonic suppression.

Takenaka and Ogawa (111,112) developed a wideband MMIC balanced frequency multiplier utilizing line-unified HEMT configurations. In line-unified HEMT configurations, coplanar lines such as slotlines and coplanar waveguides are used to connect the circuit electrically. A coplanar waveguide precedes a common-gate HEMT followed by slotline series T junction, which acts as an out-of-phase divider to drive two parallel, common-drain HEMTs. The output of the two HEMTs is connected to a coplanar waveguide followed by the load resistance. This topology yields conversion loss of 8 dB to 10 dB in the 4 GHz to 40 GHz output frequency range, and fundamental-frequency signal isolation of better than 21 dB above the input frequency of 7 GHz. The authors do not provide any data on third-harmonic isolation.

One final observation on balanced designs is the almost universal disregard for the deleterious effects of channel imbalances. It has been reported that for Δ-phase imbalances of 10°, the output conversion gain at the second harmonic will decrease by 1 dB in a 4 dB design, while a Δ-amplitude imbalance of 0.3 dB produces the same 1 dB decrease. A combination of imbalances of 10° and 0.3 dB together results in a ≈3 dB decrease in a 4 dB conversion gain design (113,151). For these reasons, balanced realizations are not considered further in this article although obviously some principles presented are directly transferable to balanced circuits.

Numerous investigators have reported designs for single-ended microwave multipliers. Referring to Fig. 25, these designs include networks N_1 and N_2 but exclude an external network N_3. Thus, single-ended designs are based primarily on the realization of N_1 and N_2. Traditional synthesis of N_1 and N_2 have followed the lines of the passive case where N_1 is traditionally composed of a bandpass or lowpass filter or matching network tuned to a fundamental frequency, and N_2 is similarly a matching network or bandpass or highpass filter tuned to the appropriate harmonic frequency of interest. Synthesis of these networks includes the use of cascades of filters and matching networks (87,88,97,99,108,110,124,125, 128,147,152–154) and such methods have been realized utilizing transmission lines and stubs to open-circuit or short-circuit specific harmonics (88,108,110,154), while some authors have additionally considered these networks as a cascade of matching and reflection networks (95,104,110,154). Many of these techniques determine optimal networks by utilizing load-line analysis (91,92), intuitive reasoning based on previous results (92,124), computer optimization of generalized models (106,108), and experimental techniques based on stub tuner measurements (88,154).

The following paragraphs illustrate some specific examples of these classes of realizations. Dow (97) developed an FET frequency doubler with a fundamental frequency of 20 GHz utilizing matching networks and tuners. Network N_1 includes a matching network at the gate designed to match the fundamental frequency and an output matching network N_2 at the drain which was designed to match the second harmonic. In addition to the matching networks, tuners were also included in both N_1 and N_2 to optimize the performance of the frequency doubler. A maximum conversion gain of −1.8 dB was achieved utilizing this topology.

Chen (87) developed a MESFET frequency doubler utilizing filters and matching networks. A low-pass filter was placed on the input of the circuit, which allows the fundamental frequency to pass through to the gate of the device, and a high-pass filter was placed on the output of the device to allow the desired second harmonic to pass. A matching network designed to match the second-harmonic frequency was placed in series with the high-pass filter. Utilizing this topology, Chen achieved 8 dB of conversion gain.

Borg (95) has developed BJT frequency-doubler designs utilizing transmission lines and stubs. In one of these, a 50 Ω transmission line is placed on the input of the circuit, and short-circuited stubs are employed on the output of the device. This design produces 2.5 dB of conversion gain. Rauscher (93) provides an FET frequency doubler utilizing transmission lines and stubs as well. On the input of the device, transmission lines are utilized to form impedance transformations and an open-circuited stub. On the output, they are utilized to provide an open-circuited stub at the fundamental frequency. Rauscher's data show that −0.5 dB of conversion gain was achieved in this design.

Stancliff (91) and Gilmore (92) determine optimal networks utilizing load-line analysis for their FET multiplier designs. Using the I_{ds} versus V_{ds} curves, they employ fundamental load-line analysis to demonstrate the output characteristics for a fundamental-frequency open-circuited load line placed on the output of the FET. Stancliff utilizes this approach in a balanced configuration, whereas Gilmore uses it for the development of a single-ended multiplier.

Various authors have used computer optimization techniques for generalized large-signal device models to develop frequency multipliers (106,108). El-Rabaie (108) uses a harmonic balance analysis technique to optimize a MESFET frequency doubler utilizing a large-signal MESFET device model. This technique determines the terminating impedance value that should be presented to the multiplier for optimum performance, while the approach utilized by Guo (106) determines optimum bias voltages and optimum load impedances.

Le (88) utilizes experimental techniques based on stub tuner measurements to design frequency multipliers. In this approach, load-pull measurements are performed to measure impedances at various harmonics at various bias voltages, and utilizing these data, frequency multipliers are designed optimizing conversion gain and efficiency. Le uses this approach in the development of a frequency tripler, which provided a conversion gain of -2.4 dB.

Single-ended designs using the previously mentioned design techniques have exhibited excellent performance. Conversion gains approaching 9 dB, harmonic suppression exceeding 40 dBc, and bandwidths approaching 35% have been reported (140,142). A significant drawback of some single-ended designs is the potentially large size constraints required by matching networks and harmonic terminating stubs. Long stubs of lengths approaching $\lambda_0/4$ are commonly used. Even though the performance of frequency multipliers using these design techniques is excellent, they are unsuitable for applications where size constraints are specified. In certain cases, however, it has been shown that discrete networks are feasible for significant size reduction.

A Unified Design Technique. Existing frequency multiplier design techniques are presented in the previous sections. While these approaches suffice to produce multipliers that work, they are not necessarily efficient in that proper synthesis of N_1 and N_2 can yield significant improvements in performance as measured by conversion gain. In this section, a consistent design technique is proposed for the design of active frequency multipliers, using the topology shown in Fig. 42 stemming from research on terminating-impedance effects on active devices.

Due to the extraordinary complexity of nonlinear circuit problems, it is proposed that the technique, while heavily reliant on experimental measurements, be based on in-depth computer-aided design. Based on a perusal of the literature, there appears to be little discussion on this topic for active multipliers other than an occasional reference to power limitation in overdriving the drain in MESFET/HEMT realizations. As with any such active design, the first step requires the selection of an active device possessing the appropriate performance characteristics (113), and particularly, in this case, developing accurate nonlinear computer device models. (In the present case, a particular device on hand has been selected for convenience.) Here, for example, we consider the effects of each devices nonlinearity [e.g. C_{gs}, C_{gd}, g_{ds}, I_{ds}, V_{gs}, V_{ds})] on augmenting a particular device harmonic (97). At this point the nonlinear device model should be accurately developed, based on both dc and ac characteristics, to match the measured performance of the transistor (48,109,146).

The next step requires utilizing the device model and/or measured data to determine optimum bias points and input power levels, using both static and P_{in} versus P_{out} data. Examples of this process may be found in previous publications (97,147). At this stage, it is important to develop the requirements on the termination networks N_1 and N_2 of Fig. 39 leading to optimum multiplier performance. This process requires the use of expensive computer analysis to be efficient timewise, although, as has been done by several researchers (88,108), some limited results can be achieved by extensive time-consuming measurements. As mentioned previously, El-Rabaie (108) and Le (88) used computer optimization of generalized nonlinear models to optimize frequency multipliers. The outcome of this process is the prescribed driving-point responses for networks N_1 and N_2 when terminated in R_g and R_L, respectively, where R_g is the source resistance and R_L is the load terminating impedance.

The final step (Fig. 42) involves the synthesis of Z_{N_1} and Z_{N_2} to realize the prescribed impedances, where Z_{N_1} and Z_{N_2} are the respective driving point impedances of N_1 and N_2.

Illustration of Unified Design Technique. Here we describe the design of an experimental frequency doubler based on the above approach, utilizing a Fujitsu FHX35LG HEMT transistor. This transistor was modeled in a previous section where measured and modeled data were presented showing the accuracy of the nonlinear model subsequent to performing step 1 above.

We need to determine the optimum bias points and input power levels from either measured or modeled data. Figures 43–47 show simulated data for various bias conditions and input power levels of the FHX35LG transistor. Figure 43 shows the simulated output power at 3 GHz versus the gate-to-source voltage V_{gs} at the fundamental frequency and the second-harmonic frequency, Fig. 44 shows the simulated output power at the second-harmonic frequency versus the drain-to-source voltage V_{ds}, Figs. 45 and 46 show the conversion gain at the second harmonic versus V_{gs} for various input power levels, and Fig. 47 shows the simulated output power versus input power. Figures 43, 45, and 46 show that good second-harmonic generation occurs for $V_{gs} = 0$ V and $V_{gs} = V_p = -0.7$ V. However, in the present case, the conversion gain is greater by approximately 9 dB (-1 dB versus -10 dB) when operating at $V_{gs} = V_p$ with $P_{in} = 0$ dBm (Fig. 46) then when operating at $V_{gs} = 0$ V. The results indicate that the

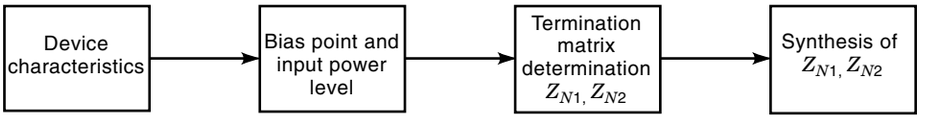

Figure 42. Topology of active microwave multiplier.

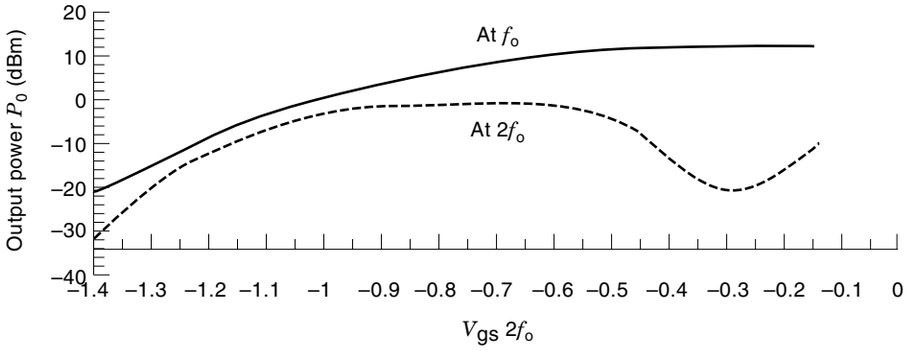

Figure 43. Simulated output power of FHX35LG HEMT versus V_{gs} (P_{in} = 0 dBm, V_{ds} = 3 V, f = 3 GHz).

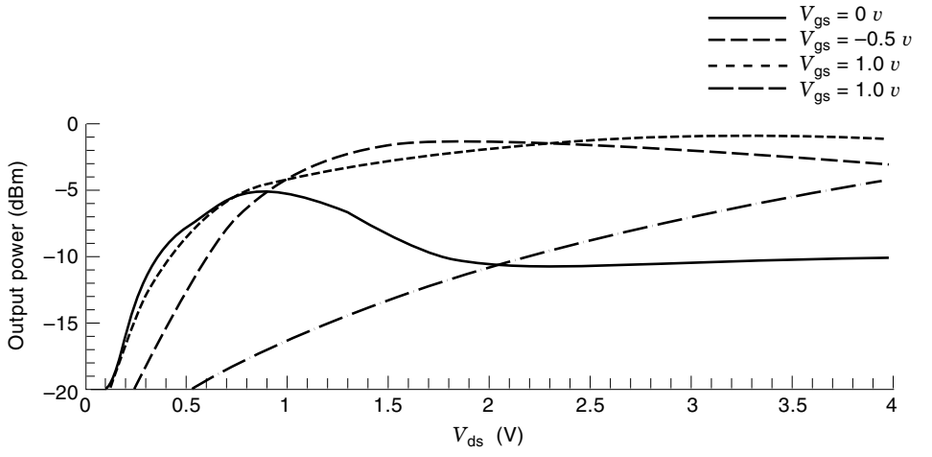

Figure 44. Simulated output of the second harmonic versus V_{ds} for FHX35LG HEMT (P_{in} = 0 dBm, f = 3 GHz).

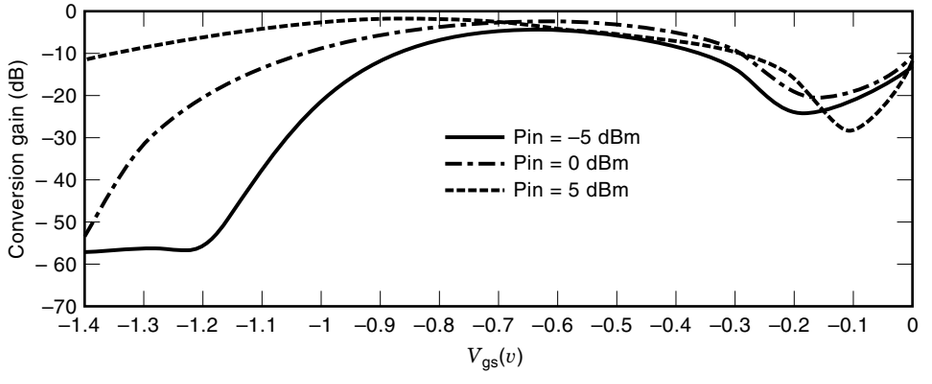

Figure 45. Simulated conversion gain of FHX35LG HEMT versus V_{gs} (V_{ds} = 3 V, f = 3 GHz).

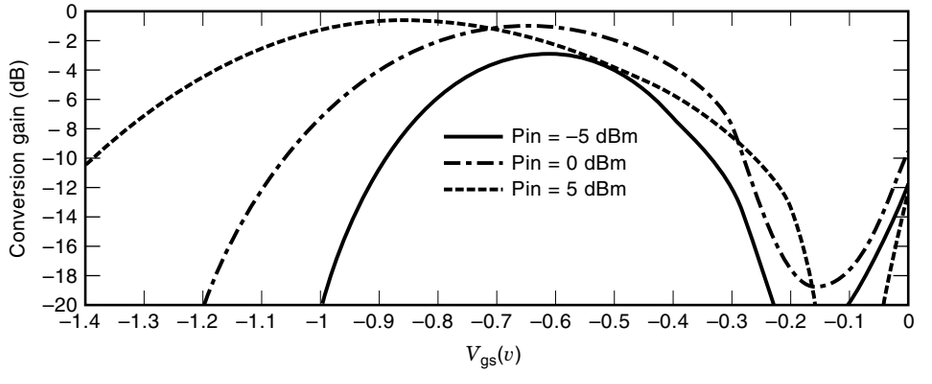

Figure 46. Simulated conversion gain of FHX35LG HEMT versus V_{gs} (V_{ds} = 3 V, f = 3 GHz).

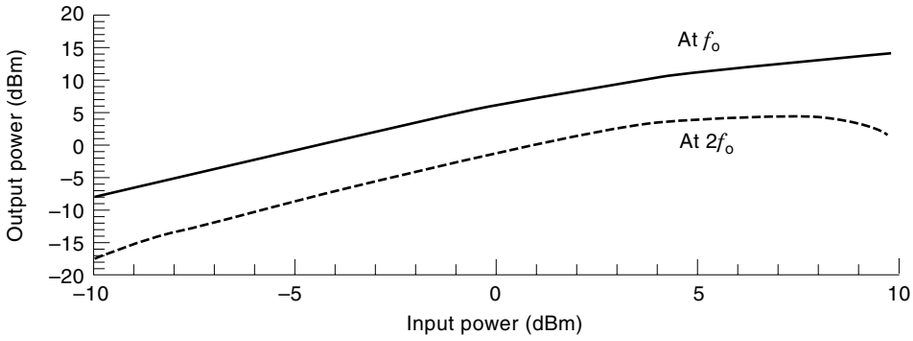

Figure 47. Simulated output power versus input power of FHX35LG ($V_{gs} = V_p = -0.7$ V, $V_{ds} = 3$ V, $f = 3$ GHz).

optimum bias and input power values for the doubler are $V_{gs} = V_p = -0.7$ V and $P_{in} = 0$ dBm.

The next step requires the generation of matrix tables for the design of a frequency doubler operating at 3 GHz input. These matrix tables represent the simulated output powers of the HEMT frequency doubler for various combinations of the input and output impedances (Z_{N_1} and Z_{N_2}) presented to the HEMT. In this case extensive terminating tables were generated for both $V_{gs} = 0$ V and $V_{gs} = V_p = -0.7$ V (79). Several matrix tables are shown in Tables 1–4, 7–12.

Tables 1 and 2 show the output power simulations where lumped elements (not always practical values) were utilized to present the various impedances to the input and output ports of the HEMT for $V_{gs} = 0$ V and $V_{gs} = V_p$. As an example, Table 2 shows an analysis with the HEMT biased at $V_{gs} = 0$ V. The table illustrates the wide variation in the conversion gain based on resistive termination and pole–zero placement for both N_1 (Z_{N_1}) as the input network and N_2 (Z_{N_2}) as the output network. In particular, it is seen that if the device is driven from an N_1 that admits a real 50 Ω impedance presented to the gate and is terminated in a real 50 Ω impedance for N_2 seen from the drain, then the conversion gain will have a value of −10.1 dB for operation as a doubler or −13.9 dB as a tripler, with due consideration of unwanted harmonics. However, if N_1 presents an impedance to the gate of the HEMT of 50 Ω at f_0, a pole at $2f_0$, and 50 Ω at $3f_0$, and N_2 presents a pole f_0, 50 Ω at $2f_0$, and a pole at $3f_0$, then the conversion gain increases 8.4 dB to a value of −1.7 dB.

In efforts to realize impedances with transmission lines, ideal transmission lines were used to present the various ideal impedances to the HEMT, without considering losses, to obtain a best-case scenario before proceeding to practical

Table 7. Doubler Simulations with Ideal Transmission Lines ($V_{gs} = -0.7$ V, $P_{in} = 0$ dBm, $V_{ds} = 3$ V)

		Output Power (dBm)[a]								
Input Network (Ω)[a,b]	Output Network (Ω)[a,b]:	$\begin{pmatrix}50\\50\\50\end{pmatrix}$	$\begin{pmatrix}0\\50\\50\end{pmatrix}$	$\begin{pmatrix}\infty\\50\\50\end{pmatrix}$	$\begin{pmatrix}0\\50\\\infty\end{pmatrix}$	$\begin{pmatrix}\infty\\50\\\infty\end{pmatrix}$	$\begin{pmatrix}50\\50\\0\end{pmatrix}$	$\begin{pmatrix}50\\50\\\infty\end{pmatrix}$	$\begin{pmatrix}0\\50\\0\end{pmatrix}$	$\begin{pmatrix}\infty\\50\\0\end{pmatrix}$
$\begin{pmatrix}50\\50\\50\end{pmatrix}$		$\begin{pmatrix}5.96\\-0.9\\-14.7\end{pmatrix}$	$\begin{pmatrix}-217\\-0.3\\-221\end{pmatrix}$	$\begin{pmatrix}-210\\-0.7\\-231\end{pmatrix}$	$\begin{pmatrix}-215\\0.2\\-270\end{pmatrix}$	$\begin{pmatrix}-208\\0.4\\-270\end{pmatrix}$	$\begin{pmatrix}5.5\\-3.9\\-232\end{pmatrix}$	$\begin{pmatrix}4.1\\0.3\\-237\end{pmatrix}$	$\begin{pmatrix}-216\\-3.3\\-270\end{pmatrix}$	$\begin{pmatrix}-209\\-4.2\\-270\end{pmatrix}$
$\begin{pmatrix}50\\0\\50\end{pmatrix}$		$\begin{pmatrix}10.5\\4.5\\-17.9\end{pmatrix}$	$\begin{pmatrix}-213\\+5.4\\-215\end{pmatrix}$	$\begin{pmatrix}-207\\3.9\\-224\end{pmatrix}$	$\begin{pmatrix}-211\\6\\-270\end{pmatrix}$	$\begin{pmatrix}-204\\5.2\\-270\end{pmatrix}$	$\begin{pmatrix}10.2\\1.8\\-225\end{pmatrix}$	$\begin{pmatrix}8.7\\6.1\\-232\end{pmatrix}$	$\begin{pmatrix}-212\\-2.5\\-270\end{pmatrix}$	$\begin{pmatrix}-206\\0.1\\-270\end{pmatrix}$
$\begin{pmatrix}50\\0\\0\end{pmatrix}$		$\begin{pmatrix}8.7\\2.5\\-12.6\end{pmatrix}$	$\begin{pmatrix}-215\\3.2\\-219\end{pmatrix}$	$\begin{pmatrix}-208\\2\\-232\end{pmatrix}$	$\begin{pmatrix}-213\\4.3\\-270\end{pmatrix}$	$\begin{pmatrix}-205\\2.8\\-270\end{pmatrix}$	$\begin{pmatrix}8.3\\-0.7\\-229\end{pmatrix}$	$\begin{pmatrix}6.9\\4.3\\-235\end{pmatrix}$	$\begin{pmatrix}-213\\0.1\\-270\end{pmatrix}$	$\begin{pmatrix}-207\\-0.9\\-270\end{pmatrix}$
$\begin{pmatrix}50\\50\\0\end{pmatrix}$		$\begin{pmatrix}5.4\\-2\\-18.2\end{pmatrix}$	$\begin{pmatrix}-218\\-1.4\\-213\end{pmatrix}$	$\begin{pmatrix}-211\\-2.5\\-237\end{pmatrix}$	$\begin{pmatrix}-216\\-2.3\\-270\end{pmatrix}$	$\begin{pmatrix}-208\\-2.3\\-270\end{pmatrix}$	$\begin{pmatrix}3.4\\-4.1\\-220\end{pmatrix}$	$\begin{pmatrix}3.4\\-2.1\\-246\end{pmatrix}$	$\begin{pmatrix}-217\\-3.6\\-270\end{pmatrix}$	$\begin{pmatrix}-209\\-5.3\\-270\end{pmatrix}$
$\begin{pmatrix}50\\\infty\\50\end{pmatrix}$		$\begin{pmatrix}2.7\\-4.4\\-19.8\end{pmatrix}$	$\begin{pmatrix}-221\\-3.7\\-227\end{pmatrix}$	$\begin{pmatrix}-213\\-4.1\\-239\end{pmatrix}$	$\begin{pmatrix}-219\\-4.1\\-270\end{pmatrix}$	$\begin{pmatrix}-211\\-3.8\\-270\end{pmatrix}$	$\begin{pmatrix}2.3\\-6.5\\-235\end{pmatrix}$	$\begin{pmatrix}0.6\\-4.2\\-246\end{pmatrix}$	$\begin{pmatrix}-220\\-6\\-270\end{pmatrix}$	$\begin{pmatrix}-212\\-7\\-270\end{pmatrix}$
$\begin{pmatrix}50\\\infty\\\infty\end{pmatrix}$		$\begin{pmatrix}4.7\\-2.7\\-23.4\end{pmatrix}$	$\begin{pmatrix}-219\\-3.2\\-219\end{pmatrix}$	$\begin{pmatrix}-211\\-2.4\\-235\end{pmatrix}$	$\begin{pmatrix}-217\\-5\\-270\end{pmatrix}$	$\begin{pmatrix}-209\\-2.6\\-270\end{pmatrix}$	$\begin{pmatrix}4.3\\-4.9\\-237\end{pmatrix}$	$\begin{pmatrix}2.6\\-2.6\\-238\end{pmatrix}$	$\begin{pmatrix}-217\\-4.8\\-270\end{pmatrix}$	$\begin{pmatrix}-210\\-4.9\\-270\end{pmatrix}$
$\begin{pmatrix}50\\50\\\infty\end{pmatrix}$		$\begin{pmatrix}3\\-4.3\\-15.9\end{pmatrix}$	$\begin{pmatrix}-221\\-4\\-222\end{pmatrix}$	$\begin{pmatrix}-212\\-4.2\\-235\end{pmatrix}$	$\begin{pmatrix}-218\\-1.8\\-270\end{pmatrix}$	$\begin{pmatrix}-210\\-2\\-270\end{pmatrix}$	$\begin{pmatrix}2.2\\-8.8\\-236\end{pmatrix}$	$\begin{pmatrix}1.2\\-1.6\\-232\end{pmatrix}$	$\begin{pmatrix}-220\\-8.2\\-270\end{pmatrix}$	$\begin{pmatrix}-212\\-8.5\\-270\end{pmatrix}$

[a] At $\begin{pmatrix}f_0\\2f_0\\3f_0\end{pmatrix}$.

[b] 0 = short circuit; ∞ = open circuit.

Table 8. Doubler Simulations with Ideal Transmission Lines (V_{gs} = 0 V, P_{in} = 0 dBm, V_{ds} = 3 V)

Input Network $(\Omega)^{a,b}$	Output Network $(\Omega)^{a,b}$:	Output Power (dBm)[a]								
		$\begin{pmatrix}50\\50\\50\end{pmatrix}$	$\begin{pmatrix}0\\50\\50\end{pmatrix}$	$\begin{pmatrix}\infty\\50\\50\end{pmatrix}$	$\begin{pmatrix}0\\50\\\infty\end{pmatrix}$	$\begin{pmatrix}\infty\\50\\\infty\end{pmatrix}$	$\begin{pmatrix}50\\50\\0\end{pmatrix}$	$\begin{pmatrix}50\\50\\\infty\end{pmatrix}$	$\begin{pmatrix}0\\50\\0\end{pmatrix}$	$\begin{pmatrix}\infty\\50\\0\end{pmatrix}$
$\begin{pmatrix}50\\50\\50\end{pmatrix}$		$\begin{pmatrix}12.5\\-10.1\\-13.9\end{pmatrix}$	$\begin{pmatrix}-211\\-11.3\\-219\end{pmatrix}$	$\begin{pmatrix}-206\\-2\\-217\end{pmatrix}$	$\begin{pmatrix}-208\\-11\\-270\end{pmatrix}$	$\begin{pmatrix}-203\\-3.3\\-270\end{pmatrix}$	$\begin{pmatrix}11.9\\-13.2\\-232\end{pmatrix}$	$\begin{pmatrix}11.1\\-10.3\\-235\end{pmatrix}$	$\begin{pmatrix}-209\\-14.2\\-270\end{pmatrix}$	$\begin{pmatrix}-204\\-5\\-270\end{pmatrix}$
$\begin{pmatrix}50\\0\\50\end{pmatrix}$		$\begin{pmatrix}14.8\\-13.8\\-5.6\end{pmatrix}$	$\begin{pmatrix}-209\\-11.8\\-211\end{pmatrix}$	$\begin{pmatrix}-205\\3.2\\-214\end{pmatrix}$	$\begin{pmatrix}-207\\11.2\\-270\end{pmatrix}$	$\begin{pmatrix}-202\\3\\-270\end{pmatrix}$	$\begin{pmatrix}14.2\\-18.7\\-223\end{pmatrix}$	$\begin{pmatrix}13.2\\-13.9\\-226\end{pmatrix}$	$\begin{pmatrix}-208\\-14.7\\-270\end{pmatrix}$	$\begin{pmatrix}-203\\0.2\\-270\end{pmatrix}$
$\begin{pmatrix}50\\0\\0\end{pmatrix}$		$\begin{pmatrix}13.7\\-11.6\\-10.4\end{pmatrix}$	$\begin{pmatrix}-210\\19.8\\-216\end{pmatrix}$	$\begin{pmatrix}-205\\1.3\\-214\end{pmatrix}$	$\begin{pmatrix}-207\\-19.5\\-270\end{pmatrix}$	$\begin{pmatrix}-202\\0.6\\-270\end{pmatrix}$	$\begin{pmatrix}13.2\\-15.7\\-228\end{pmatrix}$	$\begin{pmatrix}12.3\\-13.9\\-231\end{pmatrix}$	$\begin{pmatrix}-208\\-22.4\\-270\end{pmatrix}$	$\begin{pmatrix}-204\\-2\\-270\end{pmatrix}$
$\begin{pmatrix}50\\50\\0\end{pmatrix}$		$\begin{pmatrix}12.4\\-10\\-19.3\end{pmatrix}$	$\begin{pmatrix}-211\\-9.3\\-213\end{pmatrix}$	$\begin{pmatrix}-206\\-2.2\\-222\end{pmatrix}$	$\begin{pmatrix}-208\\-10.3\\-270\end{pmatrix}$	$\begin{pmatrix}-203\\-3.8\\-270\end{pmatrix}$	$\begin{pmatrix}11.9\\-12.6\\-224\end{pmatrix}$	$\begin{pmatrix}10.9\\-10.6\\-243\end{pmatrix}$	$\begin{pmatrix}-210\\-12.8\\-270\end{pmatrix}$	$\begin{pmatrix}-204\\-5\\-270\end{pmatrix}$
$\begin{pmatrix}50\\\infty\\50\end{pmatrix}$		$\begin{pmatrix}10.9\\-11.6\\-19.4\end{pmatrix}$	$\begin{pmatrix}-212\\-11.6\\-226\end{pmatrix}$	$\begin{pmatrix}-206\\-6.1\\-222\end{pmatrix}$	$\begin{pmatrix}-210\\-12.4\\-270\end{pmatrix}$	$\begin{pmatrix}-204\\-8.2\\-270\end{pmatrix}$	$\begin{pmatrix}10.3\\-14.4\\-236\end{pmatrix}$	$\begin{pmatrix}9.4\\-12.6\\-242\end{pmatrix}$	$\begin{pmatrix}-211\\-14.1\\-270\end{pmatrix}$	$\begin{pmatrix}-205\\-8.5\\-270\end{pmatrix}$
$\begin{pmatrix}50\\\infty\\\infty\end{pmatrix}$		$\begin{pmatrix}12.1\\-10.7\\-21.4\end{pmatrix}$	$\begin{pmatrix}-211\\-13\\-215\end{pmatrix}$	$\begin{pmatrix}-205\\-1.3\\-217\end{pmatrix}$	$\begin{pmatrix}-209\\-13.9\\-270\end{pmatrix}$	$\begin{pmatrix}-203\\-3.1\\-270\end{pmatrix}$	$\begin{pmatrix}11.6\\-15.8\\-226\end{pmatrix}$	$\begin{pmatrix}10.6\\-11.7\\-246\end{pmatrix}$	$\begin{pmatrix}-210\\-15.7\\-270\end{pmatrix}$	$\begin{pmatrix}-204\\-4.3\\-270\end{pmatrix}$
$\begin{pmatrix}50\\50\\\infty\end{pmatrix}$		$\begin{pmatrix}10.9\\-13.3\\-19.8\end{pmatrix}$	$\begin{pmatrix}-212\\-10.4\\-228\end{pmatrix}$	$\begin{pmatrix}-206\\-5.5\\-220\end{pmatrix}$	$\begin{pmatrix}-210\\-9.5\\-270\end{pmatrix}$	$\begin{pmatrix}-204\\-6.4\\-270\end{pmatrix}$	$\begin{pmatrix}10.3\\-16.8\\-239\end{pmatrix}$	$\begin{pmatrix}9.5\\-11.6\\-241\end{pmatrix}$	$\begin{pmatrix}-211\\-14.5\\-270\end{pmatrix}$	$\begin{pmatrix}-205\\-9.8\\-270\end{pmatrix}$

[a] At $\begin{pmatrix}f_0\\2f_0\\3f_0\end{pmatrix}$.

[b] 0 = short circuit; ∞ = open circuit.

Table 9. Doubler Simulations with Microstrip Transmission Lines (V_{gs} = −0.7 V, P_{in} = 0 dBm, V_{ds} = 3 V)

Input Network $(\Omega)^{a,b}$	Output Network $(\Omega)^{a,b}$:	Output Power (dBm)[a]								
		$\begin{pmatrix}50\\50\\50\end{pmatrix}$	$\begin{pmatrix}0\\50\\50\end{pmatrix}$	$\begin{pmatrix}\infty\\50\\50\end{pmatrix}$	$\begin{pmatrix}0\\50\\\infty\end{pmatrix}$	$\begin{pmatrix}\infty\\50\\\infty\end{pmatrix}$	$\begin{pmatrix}50\\50\\0\end{pmatrix}$	$\begin{pmatrix}50\\50\\\infty\end{pmatrix}$	$\begin{pmatrix}0\\50\\0\end{pmatrix}$	$\begin{pmatrix}\infty\\50\\0\end{pmatrix}$
$\begin{pmatrix}50\\50\\50\end{pmatrix}$		$\begin{pmatrix}5.96\\-0.9\\-14.7\end{pmatrix}$	$\begin{pmatrix}-27.1\\-0.7\\-26.3\end{pmatrix}$	$\begin{pmatrix}-10.4\\-0.9\\-36.2\end{pmatrix}$	$\begin{pmatrix}-25\\0.4\\-52.9\end{pmatrix}$	$\begin{pmatrix}-17.3\\0.8\\-60.1\end{pmatrix}$	$\begin{pmatrix}5.6\\-5.1\\-26.9\end{pmatrix}$	$\begin{pmatrix}4\\0.6\\-37.7\end{pmatrix}$	$\begin{pmatrix}-26.1\\-4.3\\-41.8\end{pmatrix}$	$\begin{pmatrix}-18.9\\-5.2\\-54.3\end{pmatrix}$
$\begin{pmatrix}50\\0\\50\end{pmatrix}$		$\begin{pmatrix}10.7\\4.3\\-10.2\end{pmatrix}$	$\begin{pmatrix}-27.4\\5.4\\-22.6\end{pmatrix}$	$\begin{pmatrix}-22\\4.5\\-21\end{pmatrix}$	$\begin{pmatrix}-20.5\\8.6\\-42.8\end{pmatrix}$	$\begin{pmatrix}-13.5\\6.4\\-61\end{pmatrix}$	$\begin{pmatrix}10.5\\0.3\\-24\end{pmatrix}$	$\begin{pmatrix}9\\7.2\\-32\end{pmatrix}$	$\begin{pmatrix}-21.2\\1.3\\-37.3\end{pmatrix}$	$\begin{pmatrix}-15.6\\-0.4\\-41.8\end{pmatrix}$
$\begin{pmatrix}50\\0\\0\end{pmatrix}$		$\begin{pmatrix}8.4\\2.8\\-8.7\end{pmatrix}$	$\begin{pmatrix}-24.5\\3.2\\-22\end{pmatrix}$	$\begin{pmatrix}-17.6\\2.1\\-36.8\end{pmatrix}$	$\begin{pmatrix}-22.2\\5.5\\-46\end{pmatrix}$	$\begin{pmatrix}-15\\4.6\\-73.7\end{pmatrix}$	$\begin{pmatrix}8\\-2\\-21.3\end{pmatrix}$	$\begin{pmatrix}6.8\\5.9\\-30.4\end{pmatrix}$	$\begin{pmatrix}-23.6\\-0.9\\-35.6\end{pmatrix}$	$\begin{pmatrix}-17\\-2.2\\-47\end{pmatrix}$
$\begin{pmatrix}50\\50\\0\end{pmatrix}$		$\begin{pmatrix}5.8\\-1.3\\-17\end{pmatrix}$	$\begin{pmatrix}-27.4\\-0.2\\-29.1\end{pmatrix}$	$\begin{pmatrix}-20\\-1.7\\-38.1\end{pmatrix}$	$\begin{pmatrix}-23\\1\\-55.2\end{pmatrix}$	$\begin{pmatrix}-17.7\\-0.2\\-74\end{pmatrix}$	$\begin{pmatrix}5.5\\-5\\-27.6\end{pmatrix}$	$\begin{pmatrix}3.7\\0.2\\-43.1\end{pmatrix}$	$\begin{pmatrix}-18\\-5.6\\-33.5\end{pmatrix}$	$\begin{pmatrix}-19.2\\-5.7\\-47.9\end{pmatrix}$
$\begin{pmatrix}50\\\infty\\50\end{pmatrix}$		$\begin{pmatrix}3.1\\-3.9\\-18.3\end{pmatrix}$	$\begin{pmatrix}-28.4\\-3.6\\-43.8\end{pmatrix}$	$\begin{pmatrix}-28.4\\-3.6\\-43.8\end{pmatrix}$	$\begin{pmatrix}-28.2\\-3\\-64.3\end{pmatrix}$	$\begin{pmatrix}-20.1\\-2.9\\-66.9\end{pmatrix}$	$\begin{pmatrix}2.9\\-7.1\\-28.1\end{pmatrix}$	$\begin{pmatrix}0.9\\-3.3\\-50.6\end{pmatrix}$	$\begin{pmatrix}-30\\-6.4\\-43.2\end{pmatrix}$	$\begin{pmatrix}-21.3\\-7.6\\-53\end{pmatrix}$
$\begin{pmatrix}50\\\infty\\\infty\end{pmatrix}$		$\begin{pmatrix}5.7\\-1.1\\-16.5\end{pmatrix}$	$\begin{pmatrix}-27.6\\-1\\-30.2\end{pmatrix}$	$\begin{pmatrix}-19.9\\-1\\-44.2\end{pmatrix}$	$\begin{pmatrix}-25.7\\-0.5\\-55.4\end{pmatrix}$	$\begin{pmatrix}-17.8\\-0.1\\-60.5\end{pmatrix}$	$\begin{pmatrix}5.5\\-5.1\\-29.2\end{pmatrix}$	$\begin{pmatrix}3.5\\0\\-38.8\end{pmatrix}$	$\begin{pmatrix}-26.4\\-4.5\\-43.8\end{pmatrix}$	$\begin{pmatrix}-19\\-4.9\\-51.8\end{pmatrix}$
$\begin{pmatrix}50\\50\\\infty\end{pmatrix}$		$\begin{pmatrix}2.9\\-5.2\\-16.4\end{pmatrix}$	$\begin{pmatrix}-35.5\\-5\\-29\end{pmatrix}$	$\begin{pmatrix}-28.3\\-4.8\\-37.1\end{pmatrix}$	$\begin{pmatrix}-28.3\\-4.2\\-50.3\end{pmatrix}$	$\begin{pmatrix}-20.2\\-3.8\\-54.5\end{pmatrix}$	$\begin{pmatrix}2.3\\-10.1\\-35.4\end{pmatrix}$	$\begin{pmatrix}0.8\\-4.2\\-31.4\end{pmatrix}$	$\begin{pmatrix}-29.5\\-9.7\\-47.5\end{pmatrix}$	$\begin{pmatrix}-21.6\\-9.7\\-51.9\end{pmatrix}$

[a] At $\begin{pmatrix}f_0\\2f_0\\3f_0\end{pmatrix}$.

[b] 0 = short circuit; ∞ = open circuit.

Table 10. Doubler Simulations with Microstrip Transmission Lines (V_{gs} = 0 V, P_{in} = 0 dBm, V_{ds} = 3 V)

Input Network $(\Omega)^{a,b}$	Output Network $(\Omega)^{a,b}$:	Output Power (dBm)[a]								
		$\begin{pmatrix}50\\50\\50\end{pmatrix}$	$\begin{pmatrix}0\\50\\50\end{pmatrix}$	$\begin{pmatrix}\infty\\50\\50\end{pmatrix}$	$\begin{pmatrix}0\\50\\\infty\end{pmatrix}$	$\begin{pmatrix}\infty\\50\\\infty\end{pmatrix}$	$\begin{pmatrix}50\\50\\0\end{pmatrix}$	$\begin{pmatrix}50\\50\\\infty\end{pmatrix}$	$\begin{pmatrix}0\\50\\0\end{pmatrix}$	$\begin{pmatrix}\infty\\50\\0\end{pmatrix}$
$\begin{pmatrix}50\\50\\50\end{pmatrix}$		$\begin{pmatrix}12.5\\-10.1\\-13.9\end{pmatrix}$	$\begin{pmatrix}-20.2\\-11.4\\-26.3\end{pmatrix}$	$\begin{pmatrix}-15.1\\-2.5\\-25.4\end{pmatrix}$	$\begin{pmatrix}-22.9\\-10.9\\-49.3\end{pmatrix}$	$\begin{pmatrix}-12.5\\-4\\-55.4\end{pmatrix}$	$\begin{pmatrix}12\\-13.9\\-28.9\end{pmatrix}$	$\begin{pmatrix}11.1\\-10\\-33.9\end{pmatrix}$	$\begin{pmatrix}-19.3\\-15.1\\-39.1\end{pmatrix}$	$\begin{pmatrix}-14.3\\-6\\-36.3\end{pmatrix}$
$\begin{pmatrix}50\\0\\50\end{pmatrix}$		$\begin{pmatrix}14.7\\-12.5\\-8.4\end{pmatrix}$	$\begin{pmatrix}-18.4\\-13.1\\-18.4\end{pmatrix}$	$\begin{pmatrix}-14.4\\1.8\\-25.6\end{pmatrix}$	$\begin{pmatrix}-21.3\\-10.4\\-41\end{pmatrix}$	$\begin{pmatrix}-11.1\\2.8\\-52\end{pmatrix}$	$\begin{pmatrix}14.2\\-17.1\\-22\end{pmatrix}$	$\begin{pmatrix}13.2\\-10.6\\-2.8\end{pmatrix}$	$\begin{pmatrix}-17.5\\-17\\-31.8\end{pmatrix}$	$\begin{pmatrix}-13.6\\-2.5\\-34.5\end{pmatrix}$
$\begin{pmatrix}50\\0\\0\end{pmatrix}$		$\begin{pmatrix}13.6\\-11.5\\-9.3\end{pmatrix}$	$\begin{pmatrix}-19.2\\-19\\-22.4\end{pmatrix}$	$\begin{pmatrix}-14.6\\0.5\\-21.8\end{pmatrix}$	$\begin{pmatrix}-21.9\\-15.3\\-45\end{pmatrix}$	$\begin{pmatrix}-11.7\\0.4\\-59.6\end{pmatrix}$	$\begin{pmatrix}13.2\\-17.1\\-24.8\end{pmatrix}$	$\begin{pmatrix}12.3\\-11.2\\-28.8\end{pmatrix}$	$\begin{pmatrix}-18.3\\-22.8\\-35.3\end{pmatrix}$	$\begin{pmatrix}-13.9\\-3\\-32.3\end{pmatrix}$
$\begin{pmatrix}50\\50\\0\end{pmatrix}$		$\begin{pmatrix}12.6\\-10.3\\-17.5\end{pmatrix}$	$\begin{pmatrix}-20.2\\-11.3\\-29.7\end{pmatrix}$	$\begin{pmatrix}-15\\-2.6\\-29.5\end{pmatrix}$	$\begin{pmatrix}-22.9\\-11.1\\-53\end{pmatrix}$	$\begin{pmatrix}-12.3\\-4\\-53.4\end{pmatrix}$	$\begin{pmatrix}12.1\\-13.7\\-33.9\end{pmatrix}$	$\begin{pmatrix}11.1\\-10.4\\-36.5\end{pmatrix}$	$\begin{pmatrix}-19.3\\-14.7\\-42.8\end{pmatrix}$	$\begin{pmatrix}-14.2\\-5.9\\-41\end{pmatrix}$
$\begin{pmatrix}50\\\infty\\50\end{pmatrix}$		$\begin{pmatrix}11.2\\-11.4\\-18.9\end{pmatrix}$	$\begin{pmatrix}-21.6\\-11.6\\-32.4\end{pmatrix}$	$\begin{pmatrix}-15.6\\-6.8\\-32.3\end{pmatrix}$	$\begin{pmatrix}-24.4\\-11.9\\-54.6\end{pmatrix}$	$\begin{pmatrix}-13.1\\-8.5\\-60.4\end{pmatrix}$	$\begin{pmatrix}10.6\\-14.6\\-32.7\end{pmatrix}$	$\begin{pmatrix}9.7\\-12.1\\-39.8\end{pmatrix}$	$\begin{pmatrix}-20.7\\-14.8\\-45.2\end{pmatrix}$	$\begin{pmatrix}-14.7\\-9.6\\-42.6\end{pmatrix}$
$\begin{pmatrix}50\\\infty\\\infty\end{pmatrix}$		$\begin{pmatrix}12.7\\-9.4\\-13.5\end{pmatrix}$	$\begin{pmatrix}-20.2\\-11.1\\-26.1\end{pmatrix}$	$\begin{pmatrix}-14.8\\-1\\-23.2\end{pmatrix}$	$\begin{pmatrix}-22.9\\-11.2\\-50.2\end{pmatrix}$	$\begin{pmatrix}-12.1\\-2.9\\-52.2\end{pmatrix}$	$\begin{pmatrix}12.2\\-13.1\\-29.4\end{pmatrix}$	$\begin{pmatrix}11.2\\-10.5\\-33.1\end{pmatrix}$	$\begin{pmatrix}-19.3\\-14.3\\-39.2\end{pmatrix}$	$\begin{pmatrix}-13.9\\-4\\-34\end{pmatrix}$
$\begin{pmatrix}50\\50\\\infty\end{pmatrix}$		$\begin{pmatrix}11\\-12.1\\-18.8\end{pmatrix}$	$\begin{pmatrix}-25\\-16.4\\-45.2\end{pmatrix}$	$\begin{pmatrix}-15.8\\-6.1\\-27.7\end{pmatrix}$	$\begin{pmatrix}-24.4\\-10.9\\-57\end{pmatrix}$	$\begin{pmatrix}-13.3\\-8.3\\-55.1\end{pmatrix}$	$\begin{pmatrix}10.5\\-16.2\\-35.6\end{pmatrix}$	$\begin{pmatrix}9.6\\-11.9\\-38.4\end{pmatrix}$	$\begin{pmatrix}-20.7\\-14.3\\-47.3\end{pmatrix}$	$\begin{pmatrix}-15\\-10.2\\-39.5\end{pmatrix}$

[a] At $\begin{pmatrix}f_0\\2f_0\\3f_0\end{pmatrix}$.

[b] 0 = short circuit; ∞ = open circuit.

Table 11. Doubler Simulations with Microstrip Transmission Lines (V_{gs} = −0.7 V, P_{in} = −4 dBm, V_{ds} = 3 V)

Input Network $(\Omega)^{a,b}$	Output Network $(\Omega)^{a,b}$:	Output Power (dBm)[a]								
		$\begin{pmatrix}50\\50\\50\end{pmatrix}$	$\begin{pmatrix}0\\50\\50\end{pmatrix}$	$\begin{pmatrix}50\\0\\0\end{pmatrix}$	$\begin{pmatrix}0\\50\\0\end{pmatrix}$	$\begin{pmatrix}0\\50\\50\end{pmatrix}$	$\begin{pmatrix}50\\50\\\infty\end{pmatrix}$	$\begin{pmatrix}\infty\\50\\\infty\end{pmatrix}$	$\begin{pmatrix}0\\50\\\infty\end{pmatrix}$	$\begin{pmatrix}\infty\\50\\0\end{pmatrix}$
$\begin{pmatrix}50\\50\\50\end{pmatrix}$		$\begin{pmatrix}0.5\\-6.7\\-21.3\end{pmatrix}$	$\begin{pmatrix}-32.7\\-6.1\\-34.3\end{pmatrix}$	$\begin{pmatrix}-0\\-10.8\\-33.3\end{pmatrix}$	$\begin{pmatrix}-31.6\\-10\\-48\end{pmatrix}$	$\begin{pmatrix}-25.1\\-6.8\\-46.6\end{pmatrix}$	$\begin{pmatrix}-1.5\\-4.9\\-43.4\end{pmatrix}$	$\begin{pmatrix}-22.8\\-5.1\\-65.9\end{pmatrix}$	$\begin{pmatrix}-35.9\\-4.8\\-60.6\end{pmatrix}$	$\begin{pmatrix}-24.2\\-11.1\\-60.2\end{pmatrix}$
$\begin{pmatrix}50\\0\\50\end{pmatrix}$		$\begin{pmatrix}6\\6\\-13.7\end{pmatrix}$	$\begin{pmatrix}-26.9\\1\\-26.6\end{pmatrix}$	$\begin{pmatrix}5.8\\-4.2\\-25.5\end{pmatrix}$	$\begin{pmatrix}-25.9\\-3.2\\-39.4\end{pmatrix}$	$\begin{pmatrix}-20.8\\-1\\-34.5\end{pmatrix}$	$\begin{pmatrix}4.5\\3\\-36.2\end{pmatrix}$	$\begin{pmatrix}-18.2\\1.5\\-61.9\end{pmatrix}$	$\begin{pmatrix}-29.5\\4.3\\-49\end{pmatrix}$	$\begin{pmatrix}-19.9\\-5.2\\-46.3\end{pmatrix}$
$\begin{pmatrix}50\\0\\0\end{pmatrix}$		$\begin{pmatrix}-4\\-11.8\\-28.2\end{pmatrix}$	$\begin{pmatrix}-29.9\\-2.2\\-28.6\end{pmatrix}$	$\begin{pmatrix}2.7\\-7.4\\-27.3\end{pmatrix}$	$\begin{pmatrix}-28.9\\-6.4\\-41.6\end{pmatrix}$	$\begin{pmatrix}-22.8\\-3.6\\-41.6\end{pmatrix}$	$\begin{pmatrix}1.5\\0.3\\-37.3\end{pmatrix}$	$\begin{pmatrix}-20.4\\-1\\-72\end{pmatrix}$	$\begin{pmatrix}-32.7\\0.8\\-50.2\end{pmatrix}$	$\begin{pmatrix}-22\\-7.9\\-52.9\end{pmatrix}$
$\begin{pmatrix}50\\50\\0\end{pmatrix}$		$\begin{pmatrix}0.2\\-7.1\\-23.7\end{pmatrix}$	$\begin{pmatrix}-33\\-6.1\\-34.9\end{pmatrix}$	$\begin{pmatrix}-0.1\\-10.6\\-32.7\end{pmatrix}$	$\begin{pmatrix}-31.9\\-9.5\\-45.8\end{pmatrix}$	$\begin{pmatrix}-25.4\\-7.6\\-43.8\end{pmatrix}$	$\begin{pmatrix}-1.9\\-5.6\\-53.8\end{pmatrix}$	$\begin{pmatrix}-23.1\\-6.1\\-77.4\end{pmatrix}$	$\begin{pmatrix}-36.3\\-4.4\\-65.1\end{pmatrix}$	$\begin{pmatrix}-24.5\\-11.6\\-54\end{pmatrix}$
$\begin{pmatrix}50\\\infty\\50\end{pmatrix}$		$\begin{pmatrix}-2.4\\-10.1\\-26.2\end{pmatrix}$	$\begin{pmatrix}-35.8\\-9.4\\-39.7\end{pmatrix}$	$\begin{pmatrix}-2.8\\-13.4\\-36\end{pmatrix}$	$\begin{pmatrix}-34.7\\-12.8\\-50.7\end{pmatrix}$	$\begin{pmatrix}-27.7\\-10.1\\-50.6\end{pmatrix}$	$\begin{pmatrix}-4.6\\-9.1\\-57.5\end{pmatrix}$	$\begin{pmatrix}-25.6\\-9\\-75.2\end{pmatrix}$	$\begin{pmatrix}-39.1\\-8.2\\-69.5\end{pmatrix}$	$\begin{pmatrix}-26.8\\-13.9\\-60\end{pmatrix}$
$\begin{pmatrix}50\\\infty\\\infty\end{pmatrix}$		$\begin{pmatrix}0.2\\-7\\-23.1\end{pmatrix}$	$\begin{pmatrix}-33.1\\-6.7\\-37.2\end{pmatrix}$	$\begin{pmatrix}0\\-10.8\\-35.8\end{pmatrix}$	$\begin{pmatrix}-32\\-10.1\\-50.2\end{pmatrix}$	$\begin{pmatrix}-25.3\\-7.1\\-49.6\end{pmatrix}$	$\begin{pmatrix}-2\\-5.7\\-46.2\end{pmatrix}$	$\begin{pmatrix}-23.3\\-6\\-68.7\end{pmatrix}$	$\begin{pmatrix}-36.5\\-5.4\\-66.1\end{pmatrix}$	$\begin{pmatrix}-24.4\\-11\\-58\end{pmatrix}$
$\begin{pmatrix}50\\50\\\infty\end{pmatrix}$		$\begin{pmatrix}-2.6\\-11.1\\-25.1\end{pmatrix}$	$\begin{pmatrix}-35.9\\-10.9\\-38.5\end{pmatrix}$	$\begin{pmatrix}-3.2\\-15.8\\-45.3\end{pmatrix}$	$\begin{pmatrix}-35.1\\-15.3\\-57.6\end{pmatrix}$	$\begin{pmatrix}-27.7\\-11.1\\-46.5\end{pmatrix}$	$\begin{pmatrix}-4.7\\-9.7\\-39.3\end{pmatrix}$	$\begin{pmatrix}-25.6\\-9.7\\-62.9\end{pmatrix}$	$\begin{pmatrix}-39.2\\-10.4\\-58.3\end{pmatrix}$	$\begin{pmatrix}-27\\-15.8\\-62.1\end{pmatrix}$

[a] At $\begin{pmatrix}f_0\\2f_0\\3f_0\end{pmatrix}$.

[b] 0 = short circuit; ∞ = open circuit.

Table 12. Doubler Simulations with Microstrip Transmission Lines (V_{gs} = 0 V, P_{in} = −4 dBm, V_{ds} = 3 V)

Input Network $(\Omega)^{a,b}$	Output Network $(\Omega)^{a,b}$:	Output Power (dBm)[a]								
		$\begin{pmatrix}50\\50\\50\end{pmatrix}$	$\begin{pmatrix}0\\50\\50\end{pmatrix}$	$\begin{pmatrix}\infty\\50\\50\end{pmatrix}$	$\begin{pmatrix}0\\50\\\infty\end{pmatrix}$	$\begin{pmatrix}\infty\\50\\\infty\end{pmatrix}$	$\begin{pmatrix}50\\50\\0\end{pmatrix}$	$\begin{pmatrix}50\\50\\\infty\end{pmatrix}$	$\begin{pmatrix}0\\50\\0\end{pmatrix}$	$\begin{pmatrix}\infty\\50\\0\end{pmatrix}$
$\begin{pmatrix}50\\50\\50\end{pmatrix}$		$\begin{pmatrix}9.1\\-15.5\\-23.5\end{pmatrix}$	$\begin{pmatrix}-23.3\\-14.5\\-38.7\end{pmatrix}$	$\begin{pmatrix}-17.5\\-17.2\\-42.6\end{pmatrix}$	$\begin{pmatrix}-26\\-14.2\\-61.3\end{pmatrix}$	$\begin{pmatrix}-15\\-17.4\\-68.6\end{pmatrix}$	$\begin{pmatrix}8.7\\-18.8\\-38.8\end{pmatrix}$	$\begin{pmatrix}7.8\\-15.1\\-44\end{pmatrix}$	$\begin{pmatrix}-22.3\\-18.2\\-51.7\end{pmatrix}$	$\begin{pmatrix}-16.6\\-20.8\\-54\end{pmatrix}$
$\begin{pmatrix}50\\0\\50\end{pmatrix}$		$\begin{pmatrix}12.2\\-13.4\\-17.8\end{pmatrix}$	$\begin{pmatrix}-20.2\\-16.9\\-29.5\end{pmatrix}$	$\begin{pmatrix}-15.8\\-6.8\\-31\end{pmatrix}$	$\begin{pmatrix}-22.9\\-14.2\\-51.8\end{pmatrix}$	$\begin{pmatrix}-13.2\\-5.8\\-55.7\end{pmatrix}$	$\begin{pmatrix}12\\-16.7\\-32.5\end{pmatrix}$	$\begin{pmatrix}10.9\\-12.3\\-37.6\end{pmatrix}$	$\begin{pmatrix}-19.3\\-20.7\\-42.5\end{pmatrix}$	$\begin{pmatrix}-15\\-11.1\\-45.3\end{pmatrix}$
$\begin{pmatrix}50\\0\\0\end{pmatrix}$		$\begin{pmatrix}10.5\\-14\\-19.4\end{pmatrix}$	$\begin{pmatrix}-21.9\\-16.1\\-34.5\end{pmatrix}$	$\begin{pmatrix}-16.6\\-12.1\\-38.9\end{pmatrix}$	$\begin{pmatrix}-24.7\\-13.3\\-57.5\end{pmatrix}$	$\begin{pmatrix}-14.1\\-10.7\\-75.9\end{pmatrix}$	$\begin{pmatrix}10.1\\-17.7\\-35.7\end{pmatrix}$	$\begin{pmatrix}9.1\\-12.9\\-39\end{pmatrix}$	$\begin{pmatrix}-21\\-20\\-47.5\end{pmatrix}$	$\begin{pmatrix}-15.8\\-15.9\\-49.2\end{pmatrix}$
$\begin{pmatrix}50\\50\\0\end{pmatrix}$		$\begin{pmatrix}9.2\\-15.5\\-24.8\end{pmatrix}$	$\begin{pmatrix}-23.3\\-14.7\\-39.1\end{pmatrix}$	$\begin{pmatrix}-17.2\\-16.2\\-38.5\end{pmatrix}$	$\begin{pmatrix}-26.1\\-14.8\\-61.8\end{pmatrix}$	$\begin{pmatrix}-14.8\\-16.9\\-63\end{pmatrix}$	$\begin{pmatrix}8.8\\-18.5\\-40.9\end{pmatrix}$	$\begin{pmatrix}7.8\\-15.7\\-44.4\end{pmatrix}$	$\begin{pmatrix}-22.4\\-17.9\\-52.7\end{pmatrix}$	$\begin{pmatrix}-16.3\\-19.5\\-51.8\end{pmatrix}$
$\begin{pmatrix}50\\\infty\\50\end{pmatrix}$		$\begin{pmatrix}7.7\\-17.8\\-27.6\end{pmatrix}$	$\begin{pmatrix}-25.1\\-17.4\\-43.3\end{pmatrix}$	$\begin{pmatrix}-18.3\\-20.9\\-46.8\end{pmatrix}$	$\begin{pmatrix}-27.8\\-17.9\\-65\end{pmatrix}$	$\begin{pmatrix}-15.9\\-21.8\\-71.5\end{pmatrix}$	$\begin{pmatrix}7.1\\-20.9\\-41.4\end{pmatrix}$	$\begin{pmatrix}6.2\\-18.6\\-49.2\end{pmatrix}$	$\begin{pmatrix}-24.2\\-20.4\\-56.4\end{pmatrix}$	$\begin{pmatrix}-17.4\\-23.9\\-58.7\end{pmatrix}$
$\begin{pmatrix}50\\\infty\\\infty\end{pmatrix}$		$\begin{pmatrix}9.4\\-14.3\\-22.9\end{pmatrix}$	$\begin{pmatrix}-23.3\\-14.3\\-38.2\end{pmatrix}$	$\begin{pmatrix}-16.9\\-15.7\\-40.3\end{pmatrix}$	$\begin{pmatrix}-26.1\\-14.6\\-61.8\end{pmatrix}$	$\begin{pmatrix}-14.5\\-17\\-67\end{pmatrix}$	$\begin{pmatrix}9\\-17.5\\-39.3\end{pmatrix}$	$\begin{pmatrix}7.9\\-15.2\\-42.9\end{pmatrix}$	$\begin{pmatrix}-22.4\\-17.3\\-51.8\end{pmatrix}$	$\begin{pmatrix}-16.1\\-18.6\\-51.3\end{pmatrix}$
$\begin{pmatrix}50\\50\\\infty\end{pmatrix}$		$\begin{pmatrix}7.5\\-1.9\\-26.9\end{pmatrix}$	$\begin{pmatrix}-30.3\\-16.4\\-45.2\end{pmatrix}$	$\begin{pmatrix}-18.6\\-22.3\\-45.3\end{pmatrix}$	$\begin{pmatrix}-27.8\\-17.5\\-67.4\end{pmatrix}$	$\begin{pmatrix}-16.2\\-23\\-69.5\end{pmatrix}$	$\begin{pmatrix}7\\-22.9\\-43.8\end{pmatrix}$	$\begin{pmatrix}6.1\\-18.6\\-47\end{pmatrix}$	$\begin{pmatrix}-24.1\\-20.8\\-58.1\end{pmatrix}$	$\begin{pmatrix}-17.7\\-26.6\\-57.5\end{pmatrix}$

[a] At $\begin{pmatrix}f_0\\2f_0\\3f_0\end{pmatrix}$.

[b] 0 = short circuit; ∞ = open circuit.

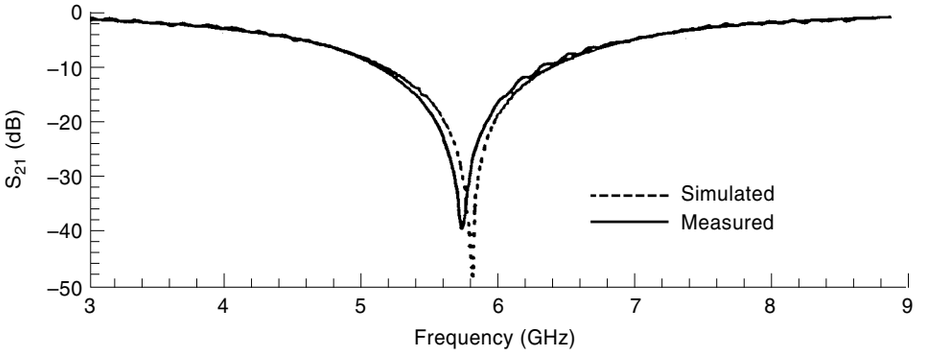

Figure 48. Transmission magnitude for input network (Z_{N_1}).

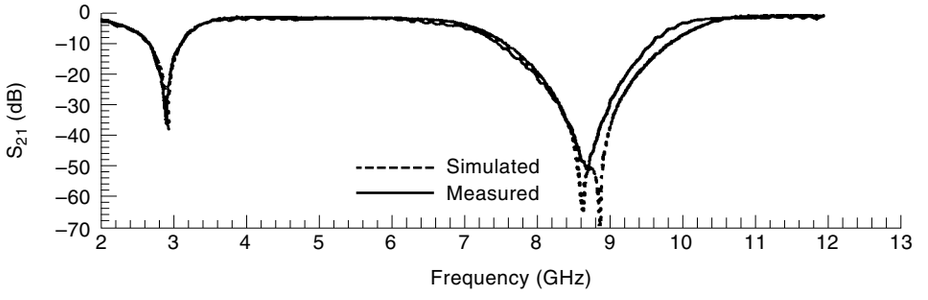

Figure 49. Transmission magnitude for output network (Z_{N_2}).

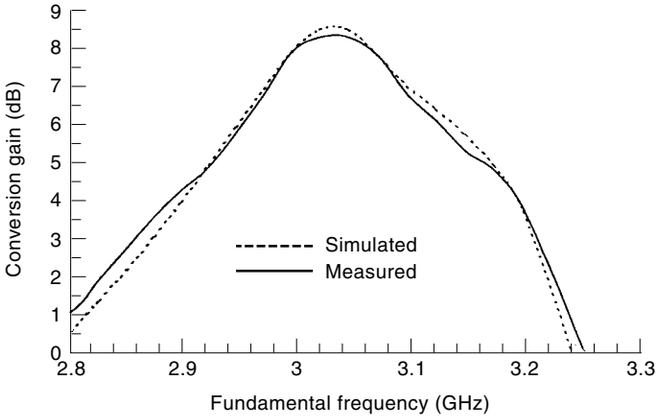

Figure 50. Conversion gain of HEMT doubler using unified technique (P_{in} = 0 dBm, V_{gs} = −0.7 V, V_{ds} = 3.0 V).

microstrip lines. Tables 7 and 8 show the simulations of the output power of the doubler for V_{gs} = 0 V and $V_{gs} = V_p$, utilizing ideal transmission lines. Variations in the conversion gain, as observed in the previous matrix simulation tables, are observed in the simulations that utilize ideal transmission lines as well.

Doubler simulations utilizing practical microstrip lines are considered next. Figures 44–48 show simulations utilizing microstrip lines for V_{gs} = 0 V and $V_{gs} = V_p$ for input powers of 0 dBm and −4 dBm.

A perusal of the matrix tables (specifically Tables 9–12) provides requirements for both input and output network impedances to provide optimal conversion gain performance for a frequency doubler. In Table 9, the optimum conversion gain is shown to be 8.6 dB (row 2, column 4), where the required input termination is a short circuit at the second-harmonic frequency and the output network consists of an open-circuit termination at the third-harmonic frequency along with a short-circuit termination at the fundamental.

After the optimal impedances (Z_{N_1} and Z_{N_2}) have been determined, the impedances have to be synthesized in order to construct a physical frequency doubler to evaluate the efficacy of the results. In this analysis, the synthesis is performed using microstrip transmission lines. Figures 48 and 49 show the transmission response of the input network (short circuit at the second harmonic) and the output network (short circuit at the fundamental and open circuit at the third harmonic), respectively. The measured and simulated responses for $|S_{21}|$ indicate that the desired short-circuit effect is established at the second harmonic (6 GHz) for Z_{N_1} as shown in Fig. 48, and similarly for the measured and modeled response of Z_{N_2} in Fig. 49.

The complete experimental frequency doubler was realized on 50 μm (20 mil) duroid, and its response is shown in Figs. 50 and 51. Figure 50 shows the conversion gain of the doubler using the technique outlined here, and Fig. 51 shows the harmonic suppression. Figure 50 shows that the maximum conversion gain is 8.5 dB with a −3 dB bandwidth of approximately 8% and with harmonic suppression greater than 20 dBc.

Conventional doubler designs have employed a short-circuit termination at the second-harmonic frequency on the input network along with a short-circuit termination at the fundamental on the output network. This conventional design approach (row 2, column 2) shows the simulated conversion gain as 3.2 dB less than the optimal case outlined by this new approach. For comparisons, a frequency doubler utilizing the conventional approach mentioned is developed on 20 mil duroid as well. The measured and simulated conversion gain for the HEMT doubler utilizing this conventional approach is shown in Fig. 52. The circuit is seen to have a conversion gain of approximately 5 dB around the center frequency of 3 GHz, rising to 6.7 dB at 3.08 GHz. As indicated previously, the conversion gain produced by the conventional design approach exhibits approximately 3 dB less conversion gain than doublers designed with the unified approach.

Reflector Method. Another single-ended design technique (93,95,104,109) is based on the use of reflector networks. This section presents examples of doubler designs operating in the *S* and *C* frequency bands incorporating such reflector networks to provide optimized performance. In this presentation, reflector networks are employed simultaneously on both the input *and* output of HEMT based designs. In a common source configuration, the input reflector network passes the fundamental frequency but reflects the desired higher harmonic signal back into the gate of the device at an optimum phase. The output reflector network passes the desired harmonic while reflecting the fundamental frequency back into the drain of the device at the proper phase angle for maximizing the conversion gain. Measured and simulated results are given to strengthen this design philosophy.

Reflector Networks. Numerous techniques exist for the realization of frequency multipliers. All techniques at radio frequencies employ a nonlinear device to generate the desired

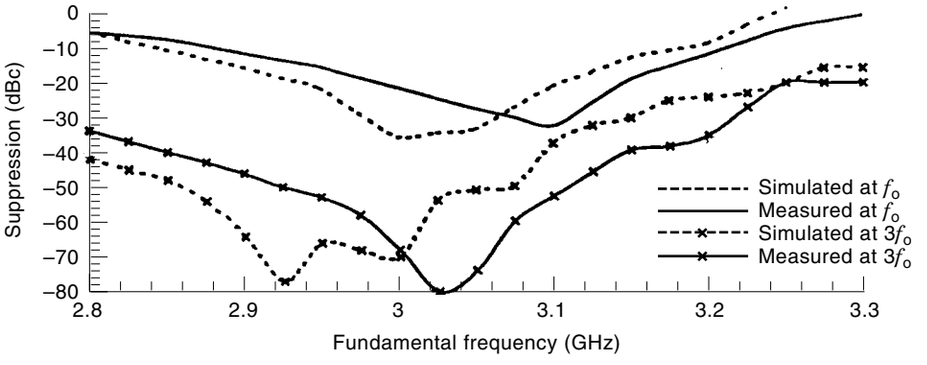

Figure 51. Harmonic suppression of HEMT doubler using unified technique (P_{in} = 0 dBm, V_{gs} = −0.7 V, V_{ds} = 3.0 V).

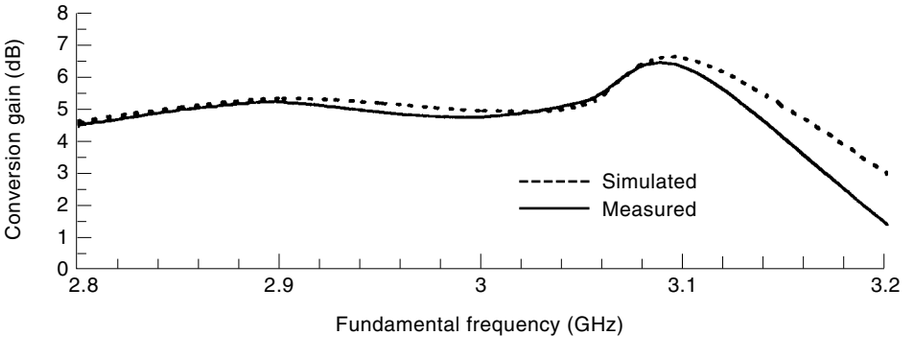

Figure 52. Conversion gain of HEMT doubler using conventional design (P_{in} = 0 dBm, V_{gs} = −0.7 V, V_{ds} = 3.0 V).

frequency multiple. The basic configuration of the single-ended frequency multiplier realization is illustrated in Fig. 24. As mentioned previously, the input network allows the fundamental frequency to pass through to the gate of the transistor, in a common source configuration, while suppressing higher harmonic frequencies. Similarly, the output network suppresses the fundamental and other unwanted harmonics, while allowing the desired harmonic to pass. The frequency multiplier reflector network design philosophy implemented in this section is applied to an HEMT (Fujitsu FHXLG) frequency doubler with a fundamental frequency of 3 GHz.

As stated above, a primary objective of the output and input networks is to suppress select harmonics. In the process of suppressing the undesired signals, it appears that relatively little attention is given the possibility that the unwanted signals can be reflected back into the device from the input *and* output networks *simultaneously*. The nonlinearity of the device causes these harmonics and the fundamental to mix with other frequency components. This mixing process can either enhance or degrade the signal at the desired second harmonic. Therefore, it is important for the reflected signal to be properly phased, such that it interferes constructively with the desired harmonic (second harmonic in the case of the frequency doubler examples presented below). Thus, the input and output networks of Fig. 24 can be designed in such a way that in addition to their primary function of filtering, they are reflector networks meeting the above criteria. Due to the complexity in calculating the actual effects of the reflector networks, there has not been a significant amount of analytical discussion on this topic until recently (157).

Consideration of Reflection Phase Angle. As stated, the input and output networks of Fig. 24 should be designed such that they are reflector networks, in addition to their primary function of filtering. The reflector networks developed in this section are analyzed on a frequency doubler with a fundamental frequency of 3 GHz. For a frequency doubler, the input network of Fig. 24 should be designed to reflect the second harmonic back into the gate of the HEMT at the proper phase angle for constructive interference and optimum conversion gain. Similarly, the output network is designed such that it reflects the fundamental signal back into the drain of the HEMT at the optimum phase. The network of Fig. 53 is a logical choice for the output and input reflector functions described above, although it is not optimal in the input case. In this figure, Z_{IN_2}, Γ_{OUT}, ℓ_1, ℓ_2, R_L, and Z_{IN_1}, ℓ_3, ℓ_4, R_g denote output and input reflector networks, respectively (157), and ℓ_1 and ℓ_3 are fixed at a quarter wavelength of the fundamental frequency and a quarter wavelength of the second harmonic frequency, respectively.

Effect of Reflection Angle on Conversion Gain. Optimization of the conversion gain of an HEMT (FHXLG) doubler can be obtained by varying the reflection angles on both input and output, using ℓ_4 and ℓ_2, respectively. Computer analyses, substantiated by experimental measurements, show that conversion gain variation of over 20 dB and 27 dB result by changes of ℓ_4 and ℓ_2, respectively. Maximum to minimum gain variations have been found to occur for ℓ_4, varying from 0 to ∼200° and ℓ_2 varying from 0 to ∼180°.

Doubler Designs Based on Prior Analysis. It has been shown that optimum multiplier designs in terms of conversion gain can be developed. These designs are based on the proper synthesis of input and output networks with the requisite transfer, input magnitude $|Z_{IN_2}|$ and phase $|Z_{IN_2}|$. Narrow, medium, and wideband designs have been demonstrated employing this approach (157). Fig. 54 shows a wideband design employing this technique.

Summary. This section has presented design techniques for single-ended frequency multiplier designs. These techniques incorporate reflector networks providing excellent performance characteristics, which includes effective conversion gain and harmonic suppression as demonstrated by the results. These results show the improvement in conversion gain using reflector networks with proper phase angles on the input and output network simultaneously, which are useful for narrow band and wideband applications. Due to bandwidth constraints imposed by the use of single stubs, incorporating filters into the designs achieves bandwidth extension and improves harmonic suppression. This improvement in bandwidth and harmonic suppression, however, comes at the expense of conversion gain, as shown by the wideband designs. Another advantage of these designs is that they are single-ended, which alleviates the requirement for complex baluns or transformers.

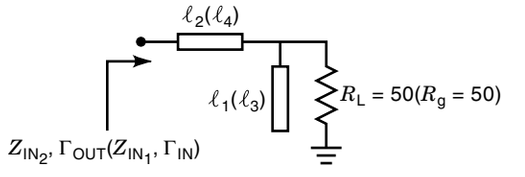

Figure 53. Fundamental output (input) reflector network.

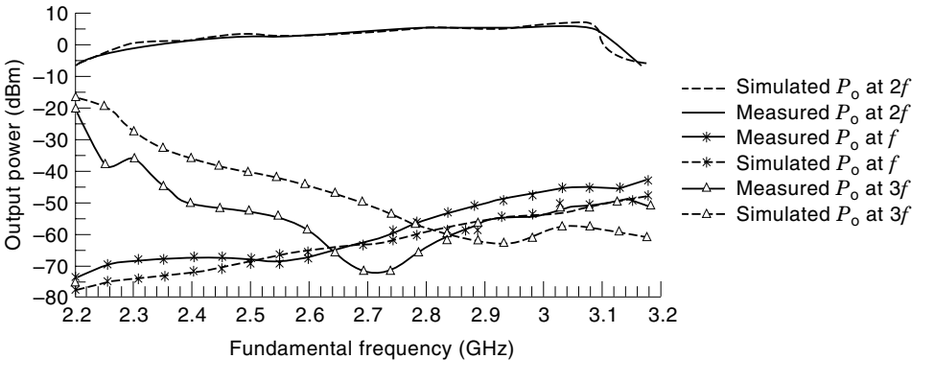

Figure 54. Wideband HEMT doubler design (P_{in} = 0 dBm, V_{gs} = 0.6 V).

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RADIO FREQUENCY NETWORKS. See TRANSMITTERS FOR AMPLITUDE MODULATION BROADCASTING.

RADIO FREQUENCY POWER AMPLIFIERS. See PROSTHETIC POWER SUPPLIES.

RADIOISOTOPE IMAGING. See DIAGNOSTIC IMAGING.

RADIOMETERS. See ELECTRIC NOISE MEASUREMENT.