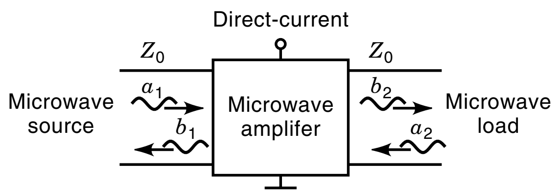
MICROWAVE AMPLIFIERS

A microwave amplifier is a circuit that accepts a signal that is possibly propagating into its input and uses direct current (dc) power to generate a signal capable of propagating away from the output to a specific load. Microwave amplifiers are distinguished from analog amplifiers, which generally assume their inputs and outputs to be nonpropagating signals. Analog amplifiers are often configured using operational amplifiers in modern electronics and are commonly found in audio and video circuits. Signal propagation considerations result in circuit designs that are more general, since a nonpropagating signal can be viewed as a limiting case of propagation, where the signal's wavelength is large compared with the physical dimensions of the circuit. Circuits designed to handle propagating signals are often referred to as radio-frequency (RF) circuits, microwave circuits, or millimeter-wave circuits according to the frequency of operation. In particular, RF usually refers to operations in the very high frequency (VHF) and ultrahigh frequency (UHF) bands, microwave refers to the S through Ka bands, and millimeter wave refers to frequencies above the Ka band. While the different frequencies in these operational regimes often result in the use of different technologies to fabricate a particular circuit, the design techniques are completely general. Therefore, unless otherwise specified, the term "microwave" will be used to include possible operations at any frequencies for which propagation effects need to be considered.



$$S_{11} = \frac{b_1}{a_1}\bigg|_{a_1 = 0} \qquad S_{21} = \frac{b_2}{a_1}\bigg|_{a_2 = 0}$$

$$S_{12} = \frac{b_1}{a_2}\bigg|_{a_1 = 0} \qquad S_{22} = \frac{b_2}{a_2}\bigg|_{a_1 = 0}$$

Figure 1. Propagating signals and scattering parameter definitions.

After the article reviews the basic methodology for characterizing circuits in a propagating signal environment, the topic of dc power coupling into microwave circuits is considered. This is usually referred to as applying a dc bias to the circuit and must be done carefully to ensure proper operation of the amplifier. After this is covered, basic chip and packaged transistors are summarized and characterized according to the above principles. The focus will concentrate on a metal semiconductor field-effect transistor (MESFET), but the techniques are general and the reader should find it relatively easy to translate the details to other transistors. The transistor characterization leads naturally into a development of basic input–output amplifier relationships, which in turn sets the stage for stability considerations. An intuitive stability criterion is shown, and techniques for stabilization are illustrated. Next, gain is defined and the design of unconditionally stable as well as conditionally stable amplifiers is discussed. Noise effects are considered, thereby providing an understanding of low-noise amplifier considerations. Nonlinear amplifier effects are examined with an emphasis on power amplifiers. Multiple device amplifiers and actual amplifier examples follow. The physical characteristics of the amplifiers are included along with theoretical and measured data to permit the reader to gain some appreciation for the technology and for the accuracy of the design techniques.

Since the characteristics of propagation are important, it is best to consider a microwave amplifier and its components in a transmission line environment. One may view an amplifier circuit as being placed in the middle of a transmission line with characteristic impedance designated by Z_0 as shown in Fig. 1. It has become common practice to let this characteristic impedance be 50 Ω, and this is assumed here unless otherwise stated. This characteristic impedance is sometimes referred to as the reference impedance. It is completely arbitrary and should be thought of as an arbitrary transmission line in which to embed microwave circuitry for the purpose of testing its behavior. Signals on the transmission line consist of voltage and current waves that can propagate in both forward and reverse directions. Since a propagating current wave is related to a corresponding propagating voltage wave by the transmission line's characteristic impedance, it has become customary to designate the combined phenomenon of propagating current and voltage as a signal. Sinusoidal voltages and current result in sinusoidal signals, which are usually represented as vectors in the complex plane, called phasors, which rotate at the frequency of operation. The magnitude of the signal vectors is scaled such that their square equates to the power propagating with the wave. The physical units of signals are, therefore, volts per root ohm or, equivalently, amps times root ohm. At any specific time the total current or voltage at a point on a transmission line would be associated with the combined effect of a forward and a reverse propagating signal. In this case $V = \frac{1}{2}(a + b)\sqrt{Z_0}$ and $I = \frac{1}{2}(a - b)/\sqrt{Z_0}$, where V and I are the total voltage and current, and a and b are the forward and reverse signal phasors, respectively.

Since waves can propagate in both directions on a transmission line, it is convenient to measure the effects of an inserted microwave circuit in terms of how it would affect propagating signals on the transmission line. In general, an incident signal hitting the input of the circuit will give rise to two effects. First, a reflected signal will be generated propagating on the line in the opposite direction as the incident signal. Second, a voltage will be generated at the output of the circuit, which in turn will cause a signal to propagate on the transmission line away from the output. It is convenient to view the circuit as a target. Upon being hit by an incident signal, the target scatters energy away; part of it is scattered back, and part of it is scattered forward. These effects are captured using measures referred to as *scattering parameters* or *S parameters,* consisting of the ratio of the scattered signal phasor divided by the incident signal phasor. Usually the input port of an amplifier is designated as port 1 and the output port is designated as port 2. Using this convention, the S parameters are given subscripts showing which port was hit by the incident wave and which port is associated with the resulting scattered wave. For example, S_{11} is the parameter characterizing the reflected wave from the input (port 1) resulting from an incident wave impinging upon the input (port 1). The first index is associated with the scattered port, and the second is associated with the incident port. The S parameter associated with the output signal would be designated S_{21}. The coefficient that relates the output with the input is sometimes called the transmission coefficient to distinguish it from the reflection coefficient.

One could further test the behavior of the amplifier circuit by launching an incident signal that would hit the output of the circuit. As before, a reflected wave would be expected from the output port and a small voltage may be induced at the input terminals of the circuit, resulting in a signal propagating away from the input. In this case, the reflection coefficient would be designated S_{22} and the transmission coefficient would be designated S_{12}. The S parameters are conveniently organized into a matrix referred to as the scattering matrix. For linear circuits, reflected and incident signals are related by matrix multiplication. The scattering matrix contains the input and output reflection coefficients as well as the forward and reverse transfer coefficients. It is important to realize that these coefficients directly describe the behavior of the amplifier circuit when it is inserted in a 50 Ω transmission line. The behavior of the amplifier will differ when it is in another environment (i.e., connected to other circuits), but its behavior in any environment can be calculated from the knowledge of its S parameters. The measurement of S parameters is simplified if both the input and output transmission lines are terminated in matched loads, thereby eliminating any unwanted spuriously propagating signals.

The same circuit can also be represented in terms of an impedance and admittance matrix. All three matrix represen-

Table 1. Circuit Matrix Relationships

	Scattering Matrix	Impedance Matrix	Admittance Matrix
Single definition	$\boldsymbol{a} = \begin{pmatrix} a_1 \\ a_2 \end{pmatrix}, \quad \boldsymbol{b} = \begin{pmatrix} b_1 \\ b_2 \end{pmatrix}$	$\boldsymbol{V} = \begin{pmatrix} V_1 \\ V_2 \end{pmatrix}, \quad \boldsymbol{I} = \begin{pmatrix} I_1 \\ I_2 \end{pmatrix}$	
Matrix definition	$\boldsymbol{b} = \boldsymbol{S} \cdot \boldsymbol{a}$	$\boldsymbol{V} = \boldsymbol{Z} \cdot \boldsymbol{I}$	$\boldsymbol{I} = \boldsymbol{Y} \cdot \boldsymbol{V}$
	$\boldsymbol{S} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix}$	$\boldsymbol{Z} = \begin{pmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{pmatrix}$	$\boldsymbol{Y} = \begin{pmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{pmatrix}$
Matrix relationships	$\boldsymbol{S} = (\boldsymbol{Z} - \boldsymbol{Z}_o)(\boldsymbol{Z} + \boldsymbol{Z}_o)^{-1} = (\boldsymbol{Z} + \boldsymbol{Z}_o)^{-1}(\boldsymbol{Z} - \boldsymbol{Z}_o)$ $\boldsymbol{Z} = \boldsymbol{Z}_o(\boldsymbol{I} + \boldsymbol{S})(\boldsymbol{I} - \boldsymbol{S})^{-1}$ $\boldsymbol{Z} = \boldsymbol{Y}^{-1}$ where $\boldsymbol{Z}_o = Z_o\boldsymbol{I}$ and $\boldsymbol{I}$ is the identity matrix.		

tations are shown together in Table 1 with their matrix relationship.

A microwave amplifier requires one or more amplifying devices. These devices normally require dc power to operate and can be either a tube-type device or a solid-state device. Tube devices are used primarily in applications where a high power output is required—for example, in a radar. Solid-state devices are used in lower-power applications in receivers and transmitter applications less than 25 W. For example, wireless and cellular communications system require solid-state amplifiers. Solid-state devices can be created using a wide range of technologies. Examples include (1) bipolar junction transistors (BJTs) commonly fabricated using silicon (Si) substrates and (2) field-effect transistors (FETs) often fabricated using gallium arsenide (GaAs) substrates. Because of the frequency of operation, BJT devices used in microwave amplifiers are of the NPN type. Additional approaches include heterojunction bipolar transistors (HBTs) and pseudomorphic high-electron-mobility transistors (PHEMTs) designed to improve operations at the high frequencies.

BIAS CIRCUIT

In order for the device to produce an amplification effect, it is necessary to apply a dc voltage at the input and the output. These dc voltages are called the bias voltage, and its value and method of application are options that can affect performance and must be carefully considered in the design. The bias is usually applied to the device through a circuit called a "bias tee." A bias-tee circuit is designed to isolate the dc voltage to the device, thereby ensuring that an unwanted dc voltage does not appear in preceding and succeeding circuitry. Also, the bias tee must isolate the dc source from the microwave signal path to eliminate unintended amplifier sensitivities. Figure 2(a) shows a canonical electrical model for a bias

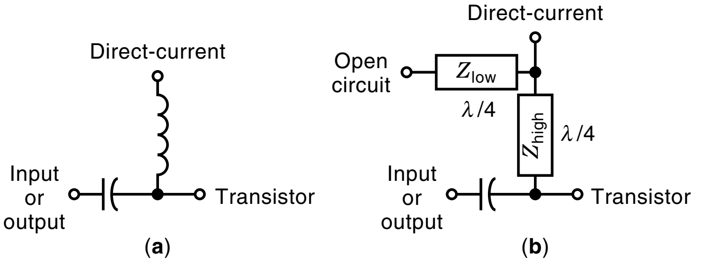


Figure 2. (a) Lumped element bias tee. (b) Distributed element bias tee.

tee consisting of a dc source in series with an inductor comprising the vertical leg of the "tee" structure. The horizontal leg of the "tee" consists of a capacitor and a short circuit. The short-circuit element is oriented to be in series with the transistor device while the capacitor is located in series with the input or output. The inductor chokes off any microwave energy that might try to flow toward the dc source and is usually referred to as a *choke* inductor. The capacitance blocks the dc voltage but not the microwave signal and hence is usually called a *blocking* capacitor. While the blocking capacitor is usually implemented as a lumped element component, the choke may be implemented as either a lumped element or a distributed element component as shown in Fig. 2(b).

DEVICE CHARACTERISTICS

For both BJT- and FET-type solid-state devices, operation is based upon an output current, which is controlled by an input voltage. In the BJT the input controlling voltage exists across a forward-biased diode junction, which can be viewed as emitting charge carriers at a near-constant rate that are collected by an output junction. In a FET, a voltage across a capacitor (which is really a reverse-biased diode) controls the current that can flow from a source region to a drain region of the transistor. In this case, because of the velocity saturation effects, the FET can be operated so that output current is approximately a constant whose value is a function of the input control voltage. To operate at high frequency, FETs utilize a metal semiconductor interface to create the controlling junction, and such FETs are commonly designated MESFETs. To illustrate key concepts, an equivalent circuit for a MESFET and associated characteristics will be used to describe operational characteristics. While the details for other amplifying devices may change, the overall principles are completely general.

Figure 3 shows the most simplified form of a MESFET equivalent circuit consisting of three terminals, a gate, a source, and a drain. The gate-to-source part of the equivalent circuit consists of a resistance, R_i, and a capacitance, C_i, where the "i" subscript can be thought of as "input" since the gate terminal is most often connected to the input of an amplifier. From a physical point of view, the subscript "i" designates the intrinsic resistance and capacitance associated with the metal semiconductor diode junction which controls the flow of current between the other two terminals. The voltage across the capacitor, C_i, is the controlling voltage and is designated V_i. The drain-to-source part of the equivalent circuit

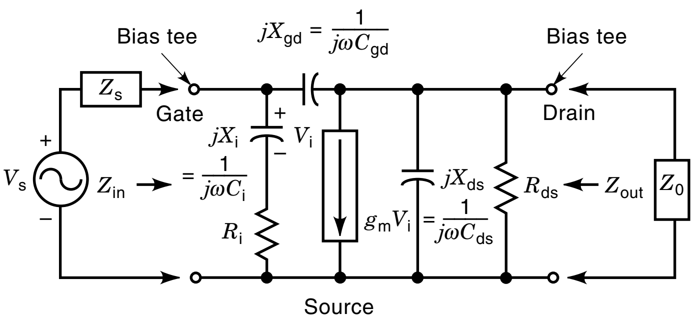


Figure 3. Simplified MESFET equivalent circuit.

consists of a voltage-controlled current source (VCCS) in parallel with a capacitance, C_{ds} and resistance, R_{ds}. The current in the VCCS is a function of the voltage V_i. The gate-to-drain part of the MESFET equivalent circuit is a capacitance, C_{gd}. V_{ds} denotes the voltage across the parallel combination of VCCS, C_{ds}, R_{ds}, and C_{gd}. In general the parameters that are part of the drain terminal are a function of both the intrinsic gate-to-source junction voltage, V_i, and the drain-to-source voltage, V_{ds}. In small-signal applications the capacitance and resistance parameters can be considered to be constant, with the VCCS current proportional only to V_i. The constant of proportionality is called the transconductance and is designated g_m. The large-signal VCCS characteristics approximate a hyperbolic tangent function $I_0 = f(V_i, V_{ds}) \cdot \tanh(\alpha V_{ds})$. The function $f(V_i, V_{ds})$ can be represented by various models. One such example is $f(V_i, V_{ds}) = A(V_{ds} - V_T)^2$, where $V_{ds} \geq 0$, $0.5 \geq V_i \geq V_T$, and V_T is a negative voltage called the threshold voltage. The drain-to-source current, I_{ds}, can be related to the current in VCCS by the relationship $I_{ds} = I_0 + V_{ds}/R_{ds} + C_{ds}(dV_{ds}/dt)$. Provided that the voltage and currents are sinusoidal, this differential equation is equivalent to the alternating current (ac) circuit relationship, $I_{ds} = I_0 + (1/R_{ds} + j\omega C_{ds})V_{ds}$. The dc characteristics for the drain simplify to $I_{ds} = I_0 + V_{ds}/R_{ds}$. S parameters of the MESFET can easily be derived from this model, and the equations are shown in Table 2.

Often an amplifier is constructed using transistor chips that have been placed in a self-contained package. Leads are connected to the gate, source, and drain terminals of the chip using bond wires. The bond wires and the package itself mean

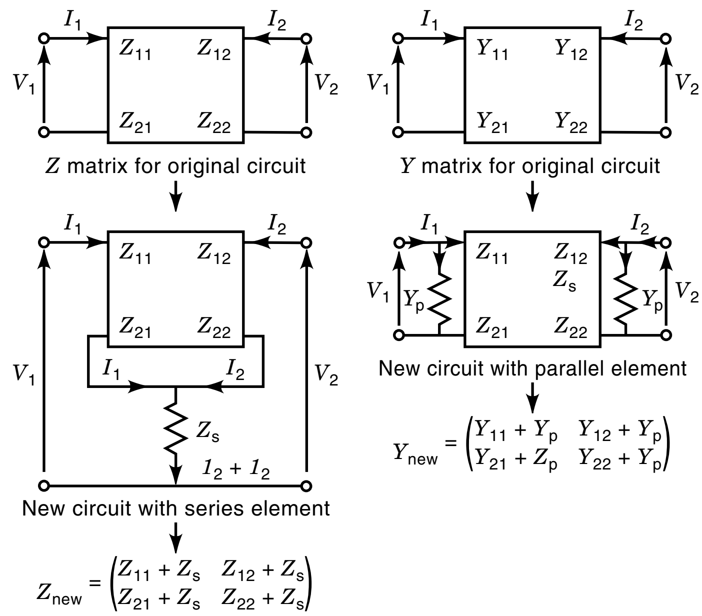


Figure 4. Steps for finding the circuit matrix after adding a series and/or parallel element to the original circuit.

that the equivalent circuit for the transistor must be augmented with equivalent resistance, inductance, and capacitance where appropriate. Packaging effects will modify the S parameters of the transistor. The addition of series and parallel elements is most easily accomplished by considering the modification of the Z and Y matrix for the circuit. Since one can switch between these and the scattering matrix, S, by straightforward matrix operations, then finding the new S parameters is easily accomplished. Figure 4 illustrates these steps. Figure 5 shows a comparison of a bare MESFET chip and its packaged counterpart in layout, equivalent circuit, S parameters, and dc IV characteristics.

BASIC AMPLIFIER RELATIONSHIPS

An understanding of three basic signal situations allows one to understand the operation of a wide range of amplifier issues. In all cases, it is helpful to remember that circuits are

Table 2. *S*-Parameters Formula for the Simplified MESFET Model

S_{11}	$\dfrac{Y_0 - Y_{in}}{Y_0 + y_{in}}$	S_{12}	$\dfrac{Z_P}{jX_{gd}}(1 + S_{22})$
S_{21}	$\left(\dfrac{Z_L}{Z'_L}\right)\left[1 + g_m Z_L \left(\dfrac{jX_i}{Z_i}\right)\right](1 + S_{11})$	S_{22}	$\dfrac{Y_0 - Y_{out}}{Y_0 + Y_{out}}$

$$Y_0 = \frac{1}{Z_0}, Z_i = R_i + jX_i, Z_L = \frac{1}{\left(\dfrac{1}{Z_0} + \dfrac{1}{R_{ds}} + \dfrac{1}{jX_{ds}}\right)}, Z'_L = Z_L + jX_{gd}, Z_P = \frac{1}{\left(\dfrac{1}{Z_0} + \dfrac{1}{Z_i}\right)}$$

$$Y_{in} = \frac{1}{Z_i} + \frac{1}{Z'_L} + g_m \left(\frac{Z_L}{Z'_L}\right)\left(\frac{jX_i}{Z_i}\right)$$

$$Y_{out} = \frac{1}{Z_{ds}} + g_m \left(\frac{Z_L}{Z'_L}\right)\left(\frac{jX_i}{Z_i}\right) + \frac{1}{4jX_{gd}} - \frac{Z_P}{(jX_{gd})^2}$$

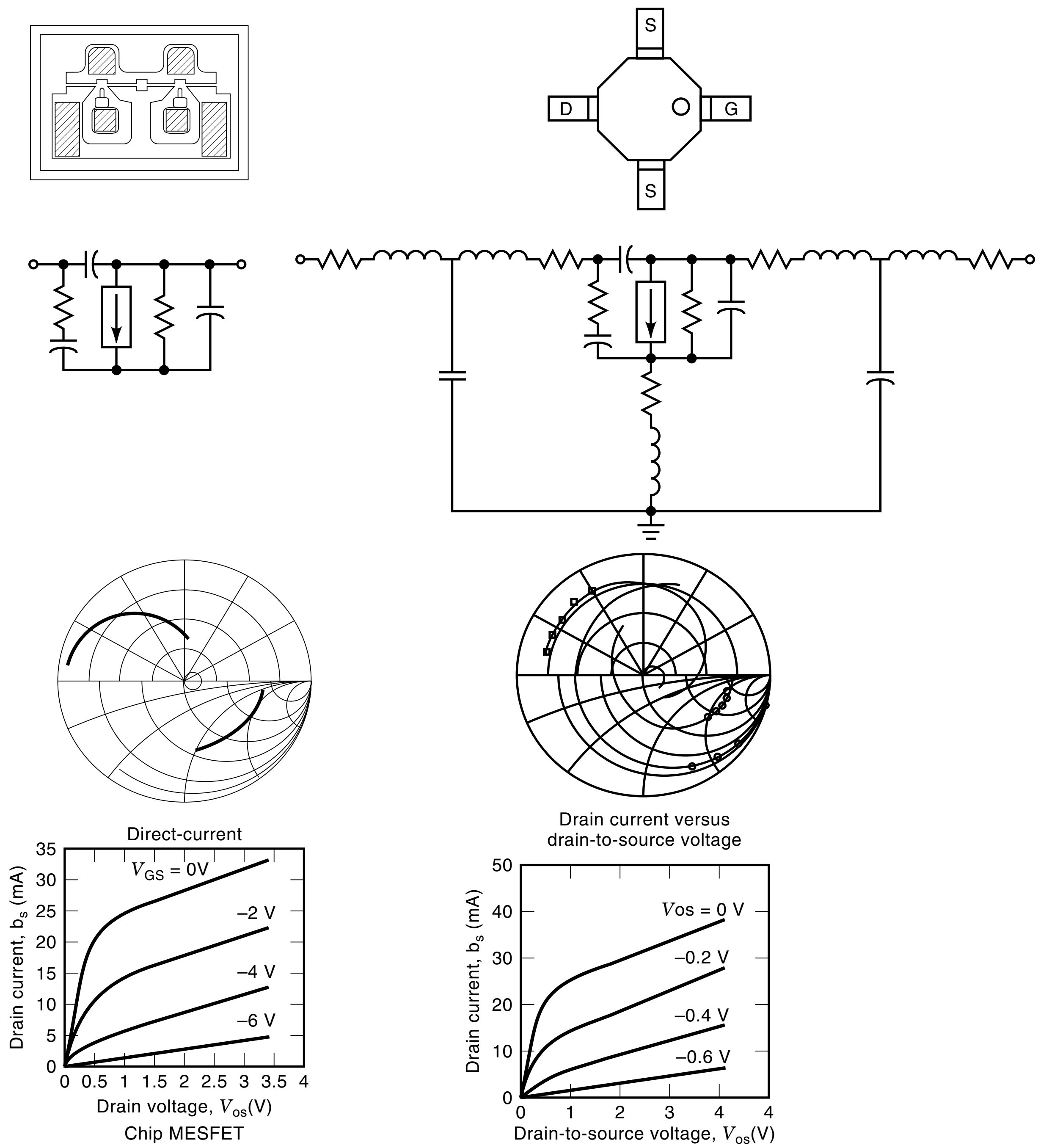


Figure 5. Comparison of a chip and a packaged MESFET (physical appearance, equivalent circuit, S parameters, and IV curves).

being characterized in terms of propagating signals and reflected signals. In the case of a source, one expects a signal to propagate from it. However, in addition, any signal incident upon it will generate reflection by virtue of the source impedance. Hence it is seen in Table 3 that the signal propagating from the source is composed of two parts, one from the actual source voltage and one from reflected energy. The voltage source creates a signal designated as b_s, equating to a normalized voltage launched on a transmission line with characteristic impedance Z_0. In this case, $b_S = (V_S\sqrt{Z_0})/(Z_S + Z_0)$. The second case to consider is that of a load. This is relatively straightforward with a reflected signal equal to an incident signal multiplied by a reflection coefficient. The third case consists of two circuits cascaded, illustrated in Fig. 6. Each of the circuits is characterized by S parameters, the first circuit by $\{U_{11}, U_{12}, U_{21}, U_{22}\}$ and the second by $\{V_{11}, V_{12}, V_{21}, V_{22}\}$. The combined circuit is described by S parameters $\{T_{11}, T_{12}, T_{21}, T_{22}\}$. The relationship between the Ts, Us, and Vs is found by solving for the interface signals and $\{a_2, b_2\}$, eliminating them as variables. The resulting equations relates the signals $\{b_1, b_3\}$ to $\{a_1, a_3\}$, which defines the S parameter for the combined circuit. These results are also summarized in Table 3. Note

Table 3. Signal Relationships for Three Types of Circuits

Source:	$b = \Gamma_S \cdot a + b_S$
Load:	$b = \Gamma_L \cdot a$
Cascade:	$T_{11} = U_{11} + \dfrac{U_{12}U_{21}V_{11}}{1 - U_{22}V_{11}}$
	$T_{21} = \dfrac{U_{21}V_{21}}{1 - U_{22}V_{11}}$
	$T_{12} = \dfrac{U_{12}V_{12}}{1 - U_{22}V_{11}}$
	$T_{22} = V_{22} + \dfrac{V_{12}V_{21}U_{22}}{1 - U_{22}V_{11}}$

that if a two-port circuit is cascaded with a one-port load, the S parameters for this combined circuit can be considered a special case of a previously described cascade of two ports with the right-hand circuit's S parameters being given by $\{\Gamma_L, 0, 0, 0\}$. The only combined circuit S parameter that makes sense in this case is T_{11}.

If a load having an impedance Z_L, equating to a reflection coefficient of Γ_L, is connected to the output of an amplifier, as seen in Fig. 7, then the combination of amplifier and load determine a one-port circuit. Using the cascade relationship with $V_{11} = \Gamma_L$, $V_{12} = V_{21} = V_{22} = 0$, the input reflection coefficient designated by $\Gamma_{in} = T_{11}$ can be found and is represented by the function $f(\Gamma_L)$. The inverse of the transformation is easily found and is designated by $f^{-1}(\Gamma_{in})$. If a source with an impedance Z_S, equating to a reflection coefficient of Γ_S, is connected to the input of an amplifier, then the reflection coefficient looking into the output terminals can be found using the cascade relationship with, $\Gamma_S = U_{22}$, $U_{11} = U_{21} = U_{12} = 0$, $\Gamma_{out} = T_{22}$. This function is designated by $g(\Gamma_S)$, and its inverse is designated by $g^{-1}(\Gamma_{out})$.

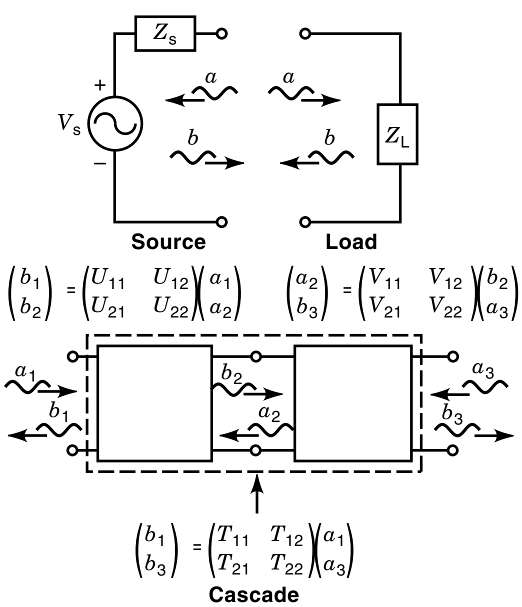


Figure 6. Illustration of three types of circuit in a propagating signal environment.

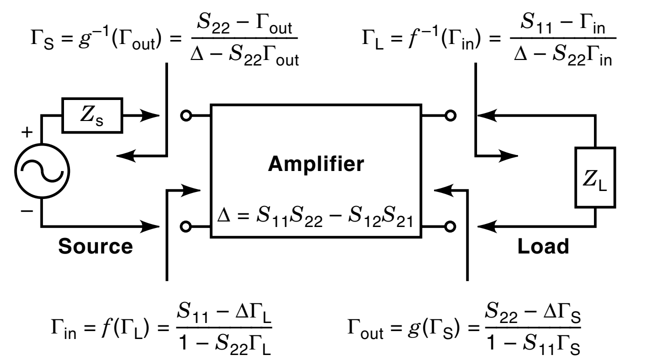


Figure 7. Source, load, input, and output reflection coefficients of an amplifier.

Disk Representation Theorem

The relationships $|Z|^2 - Za - Z^*a^* < b$ or $|Z|^2 - Za - Z^*a^* > b$ or $|Z|^2 - Za - Z^*a^* = b$ and where a is a complex number and b is a real number such that $|a|^2 + b \geq 0$ describe a circular disk, or disk complement, or circle of complex points whose center is $C = a^*$ and whose radius is $r = \sqrt{b + |a|^2}$.

That this is true can be seen by adding the term $|a|^2$ to both sides of the relationships and manipulating the results to get $|z - a^*| < \sqrt{b + |a|^2}$ or $|z - a^*| > \sqrt{b + |a|^2}$, or $|z - a^*| = \sqrt{b + |a|^2}$ circle with radius $r = \sqrt{b + |a|^2}$ and center $C = a^*$.

Using this relationship, one can show that bilinear transformations will map a circle in the complex plane onto a circle or onto a straight line. Similarly, a bilinear transformation will map a straight line in the complex plane onto a circle or onto a straight line. If a straight line is considered to be a circle with its center at infinity, then a bilinear transformation is said to map circles into circles. These results account for the frequent appearance of various circular contours that describe the operation of a linear two-port circuit such as an amplifier.

Matching Networks

Often the amplifier designer is faced with the need to have a specific source or load impedance as viewed from the amplifier for optimum operation. If the actual source or load impedance is different, then a matching network is inserted so that the desired impedance can be presented to the amplifier. If the source impedance is 50 Ω, then the matching network is referred to as an input matching network (IMN). If the actual load is 50 Ω, then the matching network is called an output matching network (OMN). The use of an IMN and OMN gives the designer flexibility in achieving performance; and since they approximate ideal lossless circuits, there is little or no power loss. Such matching networks convert a 50 Ω termination into a specific Γ_S or Γ_L.

Matching circuits are most often created by combining passive elements such as inductors, capacitors, transmission lines, and open-circuited or short-circuited transmission line stubs. It is often a good approximation at RF and microwave frequencies to assume that these elements are lossless. Collin (1) has shown that the S parameters for a passive lossless reciprocal network (PLRN) are of the form

$$\boldsymbol{S}_{\mathrm{PLRN}} = \begin{pmatrix} S_{11} & \sqrt{1 - |S_{11}|^2}e^{j\gamma} \\ \sqrt{1 - |S_{11}|^2}e^{j\gamma} & -S_{11}^*e^{j2\gamma} \end{pmatrix}$$

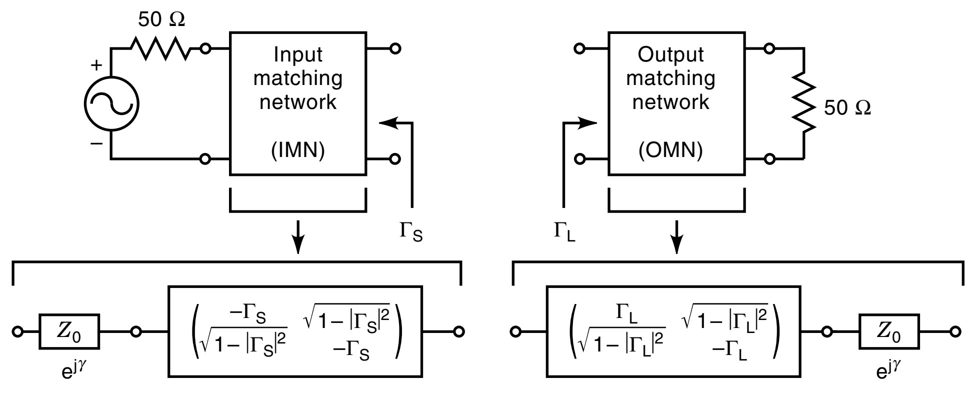


Figure 8. Input and output matching network together with the associated S-parameter equivalent circuit.

Therefore, an OMN that transforms 50 Ω to Γ_L has an S matrix equal to

$$\boldsymbol{S}_{\mathrm{QMN}} = \begin{pmatrix} \Gamma_L & \sqrt{1-|\Gamma_L|^2}e^{j\gamma} \\ \sqrt{1-|\Gamma_L|^2}e^{j\gamma} & -\Gamma_L^* e^{j2\gamma} \end{pmatrix}$$

Similarly, an IMN that transforms 50 Ω to Γ_S has an S matrix equal to

$$\boldsymbol{S}_{\mathrm{JMN}} = \begin{pmatrix} -\Gamma_S^* e^{j2\gamma} & \sqrt{1-|\Gamma_S|^2}e^{j\gamma} \\ \sqrt{1-|\Gamma_S|^2}e^{j\gamma} & \Gamma_S \end{pmatrix}$$

Obviously, the S parameters of the matching network are determined by Γ_S (or Γ_L) and an arbitrary phase γ. Analyzing these expressions using the cascade results allows one to see that a passive lossless reciprocal network consists of (1) a 50 Ω transmission line which determines the phase angle, γ, and (2) a circuit whose S parameters are defined only one parameter (Γ_S or Γ_L) cascaded together. In both the IMN and OMN, the transmission line is connected to the 50 Ω impedance side of the matching network. This is illustrated in Fig. 8.

STABILITY

Stability, meaning the likelihood that a circuit will oscillate, is important when considering active circuits, since a designer is always faced with a trade-off between gain and stability. It is important to also understand that active circuits can have a reflection coefficient that exceeds unity. This means that more power bounces back from a port than was incident upon it. If the reflection coefficient is greater than one, $|\Gamma| > 1$, then $|(Z - Z_0)/(Z + Z_0)| > 1$ and $|(Z - Z_0)/(Z + Z_0)|^2 > 1$, which implies $[(Z - Z_0)/(Z + Z_0)][(Z - Z_0)/(Z + Z_0)] > 1$. Cross-multiplication results in $(Z - Z_0)(Z^* - Z_0) > (Z + Z_0)(Z^* + Z_0)$, which implies that $0 > Z + Z^*$ or, equivalently, $0 > 2\,\mathrm{Re}\{Z\}$; that is, the resistance is negative. Therefore, *the reflection coefficient magnitude is greater than unity if and only if the associated impedance has a negative real part.* This is consistent with the Smith chart representation of reflection coefficients. Recall that constant resistance curve for negative values are circles that are outside of the unit circle. The magnitude of the reflection coefficient is less that unity for a passive load, and hence the conventional Smith chart region is referred to as unit Smith chart (USC).

To facilitate the theoretical development, several useful algebraic combinations of S parameters are defined in Table 4. Additionally, the following easily verified relationships turns out to be useful:

$$|C_1|^2 = |S_{12}S_{21}|^2 + D_1E_1$$
$$|C_2|^2 = |S_{12}S_{21}|^2 + D_2E_2$$

Since an impedance connected to the terminals on one side of an amplifier translates to a different impedance when viewed through the amplifier, it is possible for a passive termination on one side to appear as a negative resistance on the other side. The load impedance is described in terms of a load reflection coefficient, Γ_L, and the source impedance in terms of a source reflection coefficient, Γ_S. The input reflection coefficient, Γ_{in}, is the reflection coefficient seen at the input of a two-port circuit with the load connected. The output reflection coefficient, Γ_{out}, is the reflection coefficient at the output of a two-port circuit with the source impedance connected. The impedance on one side of the circuit can affect the reflection coefficient on the other side.

A negative resistance means that oscillation is possible depending on the impedance of circuitry interfacing with it. A negative resistance equates to a reflection coefficient whose magnitude exceeds unity. Given an amplifier, it is useful to see the set of impedances that produce a reflection coefficient whose magnitude exceeds unity. For example, one could determine the Γ_S values *in the source plane* that result in $|\Gamma_{out}(\Gamma_S)| < 1$. This condition results in a region in the source plane, which is either a disk or disk complement depending on the value of D_1. In either case the boundary is a circle with

Table 4. Useful S-Parameter Relationships

$i = 1, 2$	Source Parameter ($i = 1$)	Load Parameter ($i = 2$)
B_i	$D_1 + E_1$	$D_2 + E_2$
C_i	$S_{11} - \Delta S_{22}^*$	$S_{22} - \Delta S_{22}^*$
D_i	$\lvert S_{11}\rvert^2 - \lvert\Delta\rvert^2$	$\lvert S_{22}\rvert^2 - \lvert\Delta\rvert^2$
E_i	$1 - \lvert S_{22}\rvert^2$	$1 - \lvert S_{11}\rvert^2$
k	$\dfrac{E_1 - D_1}{2\lvert S_{12}S_{21}\rvert}$	$\dfrac{E_2 - D_2}{2\lvert S_{12}S_{21}\rvert}$

Table 5. Stability Circle Parameters

Parameter	Source Plane	Load Plane
Center	$\dfrac{C_1^*}{D_1}$	$\dfrac{C_2^*}{D_2}$
Radius	$\left\lvert\dfrac{S_{12}S_{21}}{D_1}\right\rvert$	$\left\lvert\dfrac{S_{12}S_{21}}{D_2}\right\rvert$
"Outside" stable condition	$D_1 > 0$	$D_2 > 0$

radius r_S and center C_S, given by $|\Gamma_S - C_S| = r_S$. If $D_1 < 0$, then the stable region is the "disk," $|\Gamma_S - C_S| < r_S$, whereas if $D_1 > 0$, then the stable region is the "disk complement," $|\Gamma_S - C_S| > r_S$.

Analogous results exist for the load plane, Γ_L. Formulas for stability circle parameters are shown in Table 5 for both the source and load planes. A designer can plot the stability circle, noting which side is stable, and determine the region acceptable for the source and load impedances. A convention that is very useful in drawing stability circles is to indicate the stable region using tick marks.

There are various configurations of stability circles which could result given the S parameters of a two-port circuit. Figure 9 illustrates the eight topological relationships that the stability regions can have relative to the USC. If the USC is completely contained in the stable region, then the circuit is said to be *unconditionally stable* or *absolutely stable.* If part of the USC is in the stable region and part is in the unstable region, then the circuit is said to be *conditionally stable* or *potentially unstable.* If the USC is completely contained in the unstable region, then the circuit is said to be absolutely unstable.

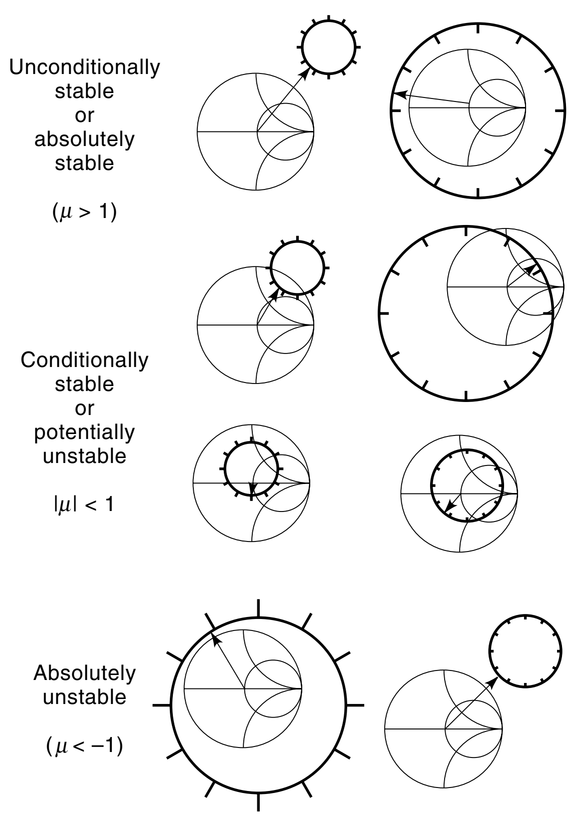


Figure 9. Examples of stability circles. Tick marks designate stable region.

For potentially unstable circuits, note that the stability circle may intersect the USC or it may be contained inside of the USC. It will be shown shortly that by modifying the circuit by the addition of lossy components, the stability circles can be moved away from the center of the Smith chart. Thus, circuits whose stability circles were previously contained within the USC can be modified so the stability circles have moved away from the center and intersect the unit circle. Indeed if one adds enough loss to the circuit the circles can be moved outside of the USC and the new circuit is unconditionally stable.

It is important to realize that this analysis is for a single frequency. In general the S parameters change as a function of frequency. Therefore, it is essential that the designer be aware of the stability circle configuration not only for the operating frequency but for a wide range of frequencies for which oscillations could represent a threat to amplifier performance.

All of this motivates the need for a parameter that would allow one to assess the stability of a circuit as a function of frequency. It would also be desirable for the parameter to be interpretable in terms of the Smith chart and the stability circles. In particular, one would like to know when a particular circuit is unconditionally stable and the margin of safety. For a potentially unstable circuit, one would like to know how much of the USC is encroached upon by the unstable region. The following stability parameter, designated as "μ," meets these requirements.

The stability parameter, μ, is defined using the *load stability circle.* The sign of μ is positive if the center of the USC is stable. If it is unstable, then the sign is negative. The magnitude of μ is determined by the distance from the center of the Smith chart to the nearest point on the stability circle. This is illustrated in Fig. 9, where an arrow is used to indicate the distance. The stability parameter can be calculated using the S parameters of the circuit. It is given by the following formula:

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - S_{11}^*\Delta| + |S_{12}S_{21}|}$$

The criterion for unconditional stability is that $\mu > 1$. In that case it is known that the stability circle does not touch the USC. If $\mu = 1.2$, the designer knows that the nearest-unstable point is 0.2 units away from the outer edge of the USC. If $|\mu| < 1$, then the designer knows that the stability circle is partially or completely within the USC and the circuit is potentially unstable. If $\mu < -1$, then the designer knows that the circuit is absolutely unstable.

In all of the previous discussions, the role of the source can be interchanged with the load if the input is interchanged with the output. Therefore, one can examine what happens to the output for different source impedances. Source stability circles are similarly defined and the distance to the nearest unstable point on the source stability circle is denoted as μ', which is related to the S parameter by

$$\mu' = \frac{1 - |S_{22}|^2}{|S_{11} - S_{22}^*\Delta| + |S_{12}S_{21}|}$$

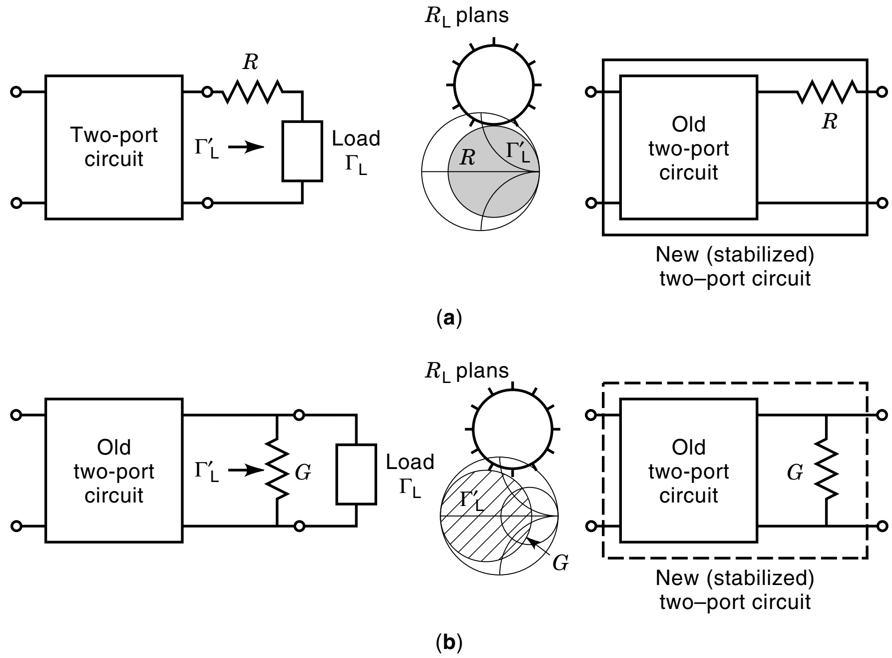


Figure 10. (a) Illustration of series resistive stabilization on the load side. (b) Illustration of shunt resistive stabilization on the load side.

This parameter can be thought of as the dual to the previous one. An important result is that $\mu > 1$ if and only if $\mu' > 1$. This is an important result since *only one parameter need be considered to determine whether a device is unconditionally stable.* Geometrically, it means that source and load stability circles both intersect the USC or they both do not. It is impossible for only one to intersect the USC.

Stabilization

If a two-port circuit is potentially unstable, then it can be stabilized by adding resistors to the circuit. For example, suppose a two-port circuit produces the load stability circle shown in Fig. 10, then a series resistor may be inserted with the load as shown. If the resistance is in series with the load and chosen to equal to or greater than that of the constant resistance circle shown, then *a new two-port that includes the series resistor* will be unconditionally stable. If μ is determined for the new two-port circuit, then it will be found that $\mu > 1$; that is, the new circuit is unconditionally stable. Note that a shunt resistor also could have been used to stabilize the circuit. In this case, its value would have been determined by choosing a conductance that is equal to or exceeds that of the constant conductance circle in the Smith chart as shown. The circuit would look like that shown in Fig. 10. Again $\mu > 1$ for the new two-port circuit.

In a similar manner the circuit can be stabilized by using series or shunt resistors whose values can be determined analogously in the source plane. In general a two-port circuit can be stabilized at the source or load side (or even a combination). Stabilization for a low-noise application is usually accomplished on the load side of a transistor, since resistors represent thermal noise sources, and all other things being equal, one prefers that the noise be introduced after amplification and not before. Likewise, for a power amplifier it is generally better to stabilize the device on the source side, since resistors on the load side will dissipate more power, which is usually undesirable.

Table 6 shows other stability criterion that have been used to determine when a circuit is unconditionally stable. Each criterion requires that two parameters be tested. First k is tested and then an auxiliary test is performed. Since stability must be addressed over a wide frequency range even for narrowband operation, the one-parameter test is preferred by the authors. k provides some interesting geometrical information in that *if* $|k| < 1$, *it can be shown that the stability circle intersects the USC at two distinct points.* The source stability circle satisfies $|\Gamma_L| = 1$, which implies $|\Gamma_L|^2 = 1$ and $|1 - S_{11}\Gamma_S|^2 - |S_{22} - \Delta\Gamma_S|^2 = 0$. This expression can be expanded using $|Z|^2 = ZZ^*$. Substitution of $|\Gamma_S| = 1$ results in an equation for the intersections of the source stability circle and the unit circle; that is, $C_1\Gamma_S + C_1^*\Gamma_S^* - B_1 = 0$. Multiplying this equation by Γ_S and utilizing the quadratic formula gives two solutions:

$$\Gamma_S^{\pm} = \frac{B_1 \pm \sqrt{B_1^2 - 4|C_1|^2}}{2C_1}$$

Since $B_1^2 - 4|C_1|^2 = 4|S_{12}S_{21}|^2(k^2 - 1)$, then $B_1^2 < 4|C_1|^2$. In this case, $|\Gamma_S^{\pm}| = 1$, showing that this is the intersection point with the unit circle.

Table 6. Other Stability Criteria

Condition on k	Auxiliary Condition
$k > 1$	$B_1 > 0$
$k > 1$	$B_2 > 0$
$k > 1$	$\lvert\Delta\rvert < 1$
$k > 1$	$1 - \lvert S_{11}\rvert^2 > \lvert S_{12}S_{21}\rvert$
$k > 1$	$1 - \lvert S_{22}\rvert^2 > \lvert S_{12}S_{21}\rvert$

GAIN

Several definitions of gain are used in describing the performance of an amplifier. Multiple definitions are needed because the actual operation of an amplifier depends on the characteristics of the source and load to which it is connected. In each definition a form of "output" power is divided by a representation of "input" power. The gain can be reported as a unitless ratio or, more commonly, as 10 times the log of the ratio, which is referred to as *decibels* (dB). In preparation for defining gain, the concept of *available power* must be understood. Available power is power delivered by a Thevenin equivalent circuit to a conjugate load. Given a source or a network, available power represents the maximum power that can be delivered to a load. The power available from a source with impedance $Z_S = R_S + jX_S$ and root-mean-square (rms) voltage V_S is given by

$$P_{\mathrm{AVS}} = \frac{|V_S|^2}{4R_S} = \frac{|b_S|^2}{1 - |\Gamma_S|^2}$$

where $b_S = \sqrt{Z_0}V_S/(Z_S + Z_0)$ and $\Gamma_S = (Z_S - Z_0)/(Z_S + Z_0)$.

Given a source and a load, the *transducer gain* of an amplifier is the power delivered to the load divided by the available power from source as shown in Fig. 11(a). In a sense the transducer gain represents the most stringent figure of merit for an amplifier. It compares the actual power delivered to the load with the maximum power that the source could ever produce regardless of whether the source is actually delivering that much power to the input of the amplifier. This is expressed algebraically as $G_T = P_L/P_{AVS}$, where P_L is the power delivered to the load and P_{AVS} is the power available from the source. Three equivalent equations for the transducer gain are given in Table 7.

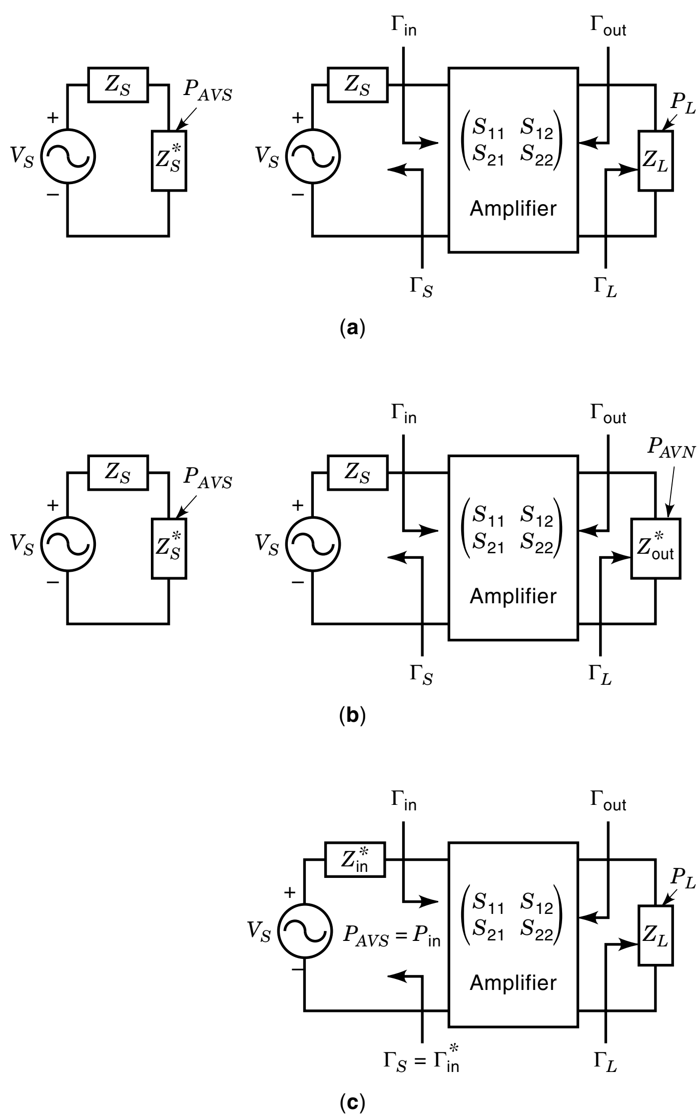


Figure 11. Source and load configurations for determining (a) transducer gain, (b) available gain, (c) operating power gain.

A second type of gain is *available gain,* which is given by power available from source amplifier network divided by the power available from source; that is, $G_A = P_{AVN}/P_{AVS}$. This is a figure of merit that is independent of the particular load that may be connected to the amplifier. The available gain would be the transducer gain, assuming that the load equaled the conjugate of the output impedance, that is, $\Gamma_L = \Gamma_{out}^*$, as illustrated in Fig. 11(b). In fact the formula for the available gain is easily obtained by making this substitution into the transducer equations (see Table 7). Note that $G_A = (P_{AVN}/P_L)G_T$; and since the expression in parentheses is always greater than or equal to unity, it follows that $G_A \geq G_T$.

A third type of gain is the *operating power gain,* which is sometimes referred to as the power gain. It equals power delivered to load divided by the power into the amplifier, that is, $G_A = P_L/P_{in}$. This definition of gain is independent of the source since the input value of the ratio is the power into the amplifier regardless of whether it is matched or not. However, it assumes that an input matching network is used to make the source appear to have an impedance that is conjugately matched to the input then the available power from the source is the power into the amplifier, as seen in Fig. 11(c). The transducer equations can be used to obtain an expression for the power gain (see Table 7). Similar to before, $G_P \geq G_T$.

Gain for $\mu > 1$ (Unconditionally Stable) Case

If $\mu > 1$, then the amplifier is unconditionally stable. In that case it is possible for the input and the output of the amplifier to be simultaneously conjugately matched. A unique pair of source and load impedances must be presented to the circuit. That such a combination of source and loads is possible is not obvious, since choosing the load affects the input impedance and choosing the source affects the output impedance. The simultaneous conjugate match impedances are found by solving the equations $\Gamma_S^* = f(\Gamma_L)$ and $\Gamma_L^* = g(\Gamma_L)$ to get

$$\Gamma_{\mathrm{MS}} = \frac{B_1 - \sqrt{B_1^2 - 4|C_1|^2}}{2C_1}$$

$$\Gamma_{\mathrm{ML}} = \frac{B_2 - \sqrt{B_2^2 - 4|C_2|^2}}{2C_2}$$

For an unconditionally stable device the maximum transducer gain will occur for a source and load whose impedance equates to the simultaneous conjugate match conditions, that is, $\Gamma_S = \Gamma_{MS}$ and $\Gamma_L = \Gamma_{ML}$. This gives

$$G_{\mathrm{T,\,MAX}} = \frac{(1 - |\Gamma_{\mathrm{MS}}|^2)S_{21}|^2(1 - |\Gamma_{\mathrm{ML}}|^2)}{|(1 - S_{11}\Gamma_{\mathrm{MS}})(1 - S_{22}\Gamma_{\mathrm{ML}}) - S_{12}S_{21}\Gamma_{\mathrm{MS}}\Gamma_{\mathrm{ML}}|^2} = \frac{|S_{21}|}{|S_{12}|}\,(k - \sqrt{k^2 - 1})$$

Table 7. Gain Formulas

Transducer Gain $G_T = G_T([S], \Gamma_S, \Gamma_L)$	$G_T = \dfrac{(1-\|\Gamma_S\|^2)\|S_{21}\|^2(1-\|\Gamma_L\|^2)}{\|(1-S_{11}\Gamma_S)(1-S_{22}\Gamma_L)-S_{12}S_{21}\Gamma_S\Gamma_L\|^2}$
	$G_T = \dfrac{(1-\|\Gamma_S\|^2)\|S_{21}\|^2(1-\|\Gamma_L\|^2)}{\|(1-S_{11}\Gamma_S)^2\|1-\Gamma_{out}\Gamma_L\|^2}$
	$G_T = \dfrac{(1-\|\Gamma_S\|^2)\|S_{21}\|^2(1-\|\Gamma_L\|^2)}{\|(1-\Gamma_{in}\Gamma_S)^2\|1-S_{22}\Gamma_L\|^2}$
Available gain $G_A = G_A([S], \Gamma_S) = G_T([S], \Gamma_S, \Gamma_{out}^*)$	$G_A = \dfrac{(1-\|\Gamma_S\|^2)\|S_{21}\|^2}{\|(1-S_{11}\Gamma_S)\|^2(1-\|\Gamma_{out}\|^2)}$
Operating power gain $G_P = G_P([S], \Gamma_L) = G_T([S], \Gamma_{in}^*, \Gamma_L)$	$G_P = \dfrac{\|S_{21}\|^2(1-\|\Gamma_L\|^2)}{(1-\|\Gamma_{in}\|^2)\|1-S_{22}\Gamma_L\|^2}$

Since $\mu = 1$ implies $k = 1$, an amplifier that is just barely stable would have a maximum transducer gain that equals

$$G_{\mathrm{MSG}} = \frac{|S_{21}|}{|S_{12}|}$$

This is referred to as the *maximum stable gain* and serves as a gain figure of merit for a stabilized circuit.

Examination of the available gain yields useful insights. The set of Γ_S values that produce a constant G_A is found by substituting $G_A = g_a|S_{21}|^2$ into the expression for available gain and manipulating the equation to get $(D_1 + 1/g_a)|\Gamma_S|^2 - C_1\Gamma_S - C_1\Gamma_S^* = 1/g_a - E_1$. Using the disk representation theorem, one sees that the set of points produces a circle whose center and radius is given in Table 8.

The constant available gain curves are seen to be nested circles with the peak gain occurring when $r_{g_a} = 0$, which implies that $1 - 2k|S_{21}S_{12}|g_a + |S_{21}S_{12}|^2g_a^2 = 0$ and the normalized gain equals $g_a = (1/|S_{12}S_{21}|)(k - \sqrt{k^2-1})$. The maximum available gain is therefore

$$G_{\mathrm{A,\,MAX}} = \frac{|S_{21}|}{|S_{12}|}\,(k - \sqrt{k^2-1})$$

Similar expressions exist for power gain circles—that is, contours for which G_p = constant. Note also that the maximum available gain and maximum power gain are exactly the simultaneous conjugate match points. Thus, when an amplifier is designed so that the load and source impedances equal the simultaneous conjugate match conditions, then all three definitions of gain are equal, that is, $G_{T,max} = G_{A,max} = G_{P,max}$. Figure 12 illustrates constant gain circles for an unconditionally stable device.

Gain for $|\mu| < 1$ (Conditionally Stable) Case

For the conditionally stable case, it is sufficient to consider that the stability circles intersect the USC. As previously indicated, if this is not true, then the addition of a partially stabilizing resistive network will drive the stability circle away from the center until it intersects the unit circle at two distinct points. The intersection requirement is equivalent to the condition $|k| < 1$. It is instructive to examine the available gain circles under this condition. The formulas previously derived and listed in Table 8 are completely general and apply equally well to the conditionally stable case. It can be shown that the constant gain contours intersect the unit circle and are represented by the complex equation

$$|1 - S_{11}\Gamma_S|^2 - |S_{22} - \Delta\Gamma_S|^2 = \frac{(1-|\Gamma_S|^2)}{g_a}$$

This allows one to substitute $|\Gamma_S| = 1$ for the unit circle and see that

$$|1 - S_{11}\Gamma_S|^2 - |S_{22} - \Delta\Gamma_S|^2 = 0$$

The solution is independent of g_a and hence the gain circle intersects the unit circle at the same point regardless of the gain and consequently is referred to as *invariant points*. Also, this equation is the same as the one determining where the stability circle intersects the unit circle, that is, $\Gamma_S^{\pm}$. Because of the invariant points, the geometric relationship of the

Table 8. Constant Gain Circle Formulas

	Center	Radius
Available gain circle $g_a = G_A/\|S_{21}\|^2$	$C_{ga} = \dfrac{C_1^*}{D_1 + \dfrac{1}{g_a}}$	$r_{ga} = \left\|\dfrac{[1 - 2k\|S_{12}S_{21}\|g_a + \|S_{12}S_{21}\|^2g_a^2]^{1/2}}{1 + g_aD_1}\right\|$
Operating power gain circle $g_p = G_P/\|S_{21}\|^2$	$C_{gp} = \dfrac{C_2^*}{D_2 + \dfrac{1}{g_p}}$	$r_{gp} = \left\|\dfrac{[1 - 2k\|S_{12}S_{21}\|g_p + \|S_{12}S_{21}\|^2g_p^2]^{1/2}}{1 + g_pD_2}\right\|$

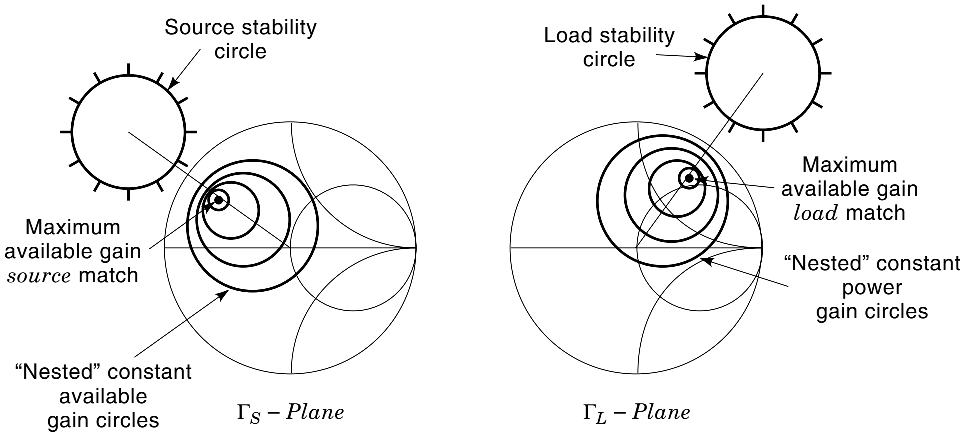


Figure 12. Illustration of available gain and power gain circles for an unconditionally stable device circuit.

source stability circle, gain circles, and the unit circle can be determined solely by the center, as shown in Fig. 13.

The behavior of the gain is now examined as one moves a distance x along the direction $\hat{c}_S$, that is, letting $\Gamma_S = x\hat{c}_S$, where $\hat{c}_S = C_1^*/|C_1|$. Substitution into the gain equation yields

$$g_a(x) = \frac{1 - x^2}{D_1x^2 - 2|C_1|x + E_1}$$

Differentiation of this expression yields

$$g_a' = \frac{2|C_1|x^2 - 2(D_1 + E_1)x + 2|C_1|}{(D_1x^2 - 2|C_1|x + E_1)^2}$$

Since the denominator is always positive, the sign of the derivative is controlled by the numerator. The function g_a is monotonic (always increasing or always decreasing) when the numerator does not change sign as a function of x. This is equivalent to saying that the discriminant of the numerator, a quadratic, is negative, that is,

$$4(D_1 + E_1)^2 - 16|C_1|^2 < 0$$

which is the same as $|k| < 1$. Consequently, the gain function is a monotonic function of x whenever $|k| < 1$. The gain function g_a is singular ($\pm\infty$) whenever Γ_S approaches a value on a stability curve since the denominator vanishes. The sign of the singularity is determined by examining the numerator and denominator. As long as Γ_S remains in the USC, the numerator is positive; and as long as Γ_S is in the stable region, the denominator is positive. This positive monotonic nature of g_a is illustrated in Fig. 13. The gain is zero at the boundary of the USC and approaches $+\infty$ as the stability circle is approached on the stable side, that is, the "tick mark" side.

For high-performance amplifier applications, it is often desirable not to stabilize potentially unstable devices if the source and load impedances are well-controlled. Unfortunately, the design of conditionally stable amplifiers may not be a straightforward process, as illustrated in the MESFET example shown in Fig. 14. For a conditionally stable device it is assumed that the stability circles intersect the USC at two distinct places as previously mentioned.

Here the designer has selected a stable source reflection coefficient Γ_S (based on noise or other considerations) and has designed an appropriate input matching network (IMN) to transform 50 Ω into Γ_S. In an attempt to now match the output, the IMN is connected to the FET gate, and the output reflection coefficient Γ_{out} is observed looking into the drain. An output matching network (OMN) now needs to be designed to transform 50 Ω to Γ_{out}^* so that the drain will see a conjugately matched load. Unfortunately, as seen in Fig. 14, it is possible for Γ_L to be located on the unstable side of the load stability circle.

The above example illustrates that a circuit can be output stable, $|\Gamma_{out}| < 1$, but input unstable, $|\Gamma_{in}| > 1$, conditions manifested by examining the source and load stability circles, respectively. Output matched circuits for which $|\Gamma_{out}(\Gamma_S)| < 1$ and $|\Gamma_{in}(\Gamma_{out}^*(\Gamma_S))| < 1$ are said to be jointly stable. A noniterative process to design a jointly stable output matched circuit is possible by mapping the stable region in the load plane onto the Γ_S plane. This mapped region in the Γ_S plane will be either a disk (region inside of a circle) or a disk complement

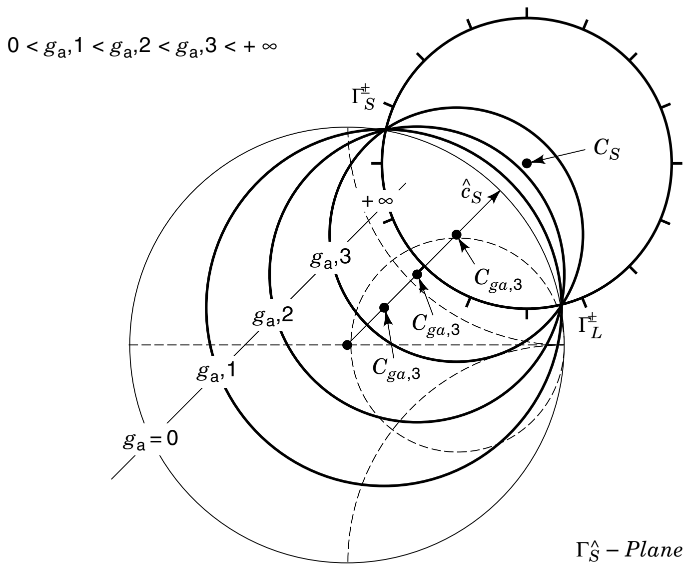


Figure 13. Illustration of invariant points $\Gamma_{\hat{S}}^{\pm}$ for a conditionally stable circuit.

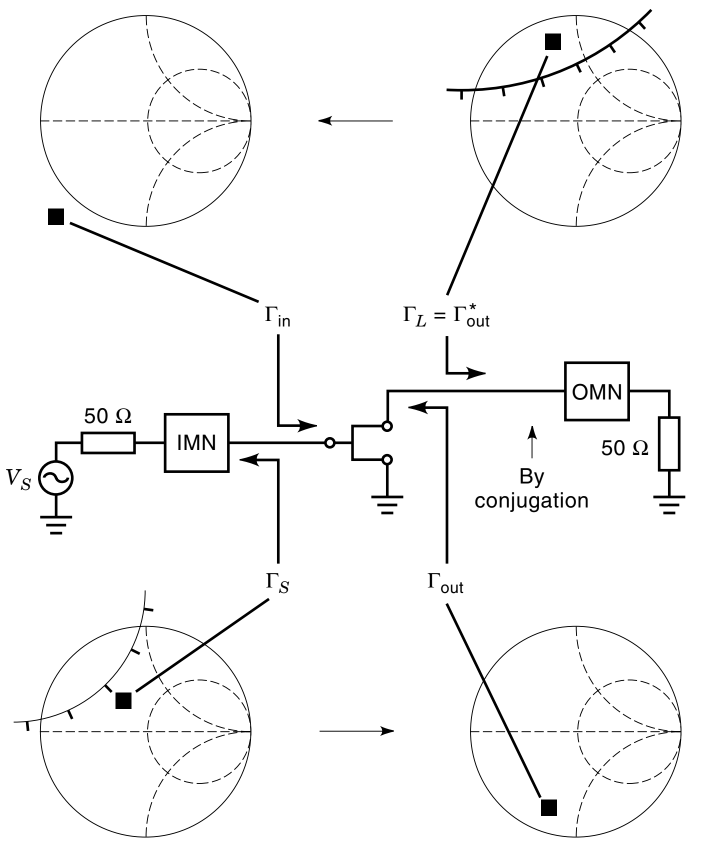


Figure 14. Illustration of how choosing Γ_S in the source plane can result in an unstable conjugate match in the load plane.

(region outside of a circle) since the reflection coefficients are related by linear fractional (or bilinear) transformations; that is, an exact knowledge of this region in the Γ_S plane permits a designer to select source impedances with an *a priori* knowledge that the matched load will be located on the stable side of the load stability circle.

To determine the region in the source plane one examines the inequality

$$|\Gamma_{\text{in}}(\Gamma^*_{\text{out}}(\Gamma_S))| < 1$$

Substitution of the expressions and application of the disk representation theorem shows that the region is a disk or disk complement whose boundary is given by the formulas in Table 9.

The subscript "IS" signifies that the area of interest is the input stability region in the *s*ource plane. Noticing that C_{IS} is collinear with the centers of the available gain circles, C_{ga} (line determined by the unit vector $\hat{c}_S$) motivates an examination of whether the input stable circle intersects the unit circle. Substitution of $|\Gamma_S| = 1$ shows that the input stable circle in the source plane intersects the unit circle at exactly the invariant points and hence *the input stable boundary in the source plane is an available gain circle.* The specific gain value equating to the input stable boundary is

$$G_{\text{IS}} = 2 \cdot k \cdot \left|\frac{S_{21}}{S_{12}}\right| = 2 \cdot k \cdot \text{MSG}$$

where MSG is the maximum stable gain of the device. Because of the monotonic nature of the gain function, this value is an upper bound for the available gain. It also turns out that the same value—that is, $2k$(MSG)—represents and upper bound for the jointly stable operating power gain. A universal figure of merit can be defined and is designated the maximum single-sided matched gain, G_{MSM}, for a conditionally stable amplifier. It is given by

$$G_{\text{MSM}} = 2 \cdot k \cdot \text{MSG}$$

The constant gain circle equating to G_{MSM} in either the source or load planes is called the MSM circle.

Constant μ Contours for Conditionally Stable Designs

Using the previous results regarding gain and previous results for matching networks, it is possible to select a matching point and determine what the final gain (available or power) will be and to also know what the stability of the completed amplifier will be. This is done by substituting the general form of a lossless reciprocal network and computing the S parameters of the final amplifier and substituting them into the formula for μ or μ'. It turns out that after extensive algebraic manipulation the contours of constant stability are gain circles. The results of this analysis are tabulated in Tables 10 and 11. These tables allow one to determine trade-off increased gain with stability risk. This process is illustrated in Fig. 15, where the gain circles (in this case power gain circles) are plotted on a Smith chart. In the figure the gain function for points along the centerline are plotted. Notice that it grows asymptotically as one approaches the stability circle as expected. The MSM circle is plotted, indicating the boundary for which the conjugate match will be stable. The stability

Table 9. Formulas for Conjugately Stable Regions in Source and Load Planes

	Center	Radius
Input stable region in the source plane	$C_{IS} = c_{IS}\hat{c}_S,\ \hat{c}_S = c_1^*/c_1$ $c_{IS} = \dfrac{\lvert C_1\rvert}{D_1 + \dfrac{\lvert S_{12}S_{21}\rvert}{2k}}$	$r_{IS} = \dfrac{\lvert S_{12}S_{21}\rvert}{\lvert 2kD_1 + \lvert S_{12}S_{21}\rvert\,\rvert}$
Output stable region in the load plane	$C_{OL} = c_{OL}\hat{c}_L,\ \hat{c}_L = c_2^*/c_2$ $c_{OL} = \dfrac{\lvert C_2\rvert}{D_2 + \dfrac{\lvert S_{12}S_{21}\rvert}{2k}}$	$r_{OL} = \dfrac{\lvert S_{12}S_{21}\rvert}{\lvert 2kD_2 + \lvert S_{12}S_{21}\rvert\,\rvert}$

Table 10. Formulas for Constant μ' and μ Contours in the Γ_S Plane for the Output Conjugately Matched Conditionally Stable Amplifier

Γ_S Plane	Constant μ' Contour	Constant μ Contour
Center	$\dfrac{\|C_1\|[1-(\mu')^2]}{E_1[1-(\mu')^2]-2\|T_{12}T_{21}\|(k-\mu')}\hat{c}_S$	$\dfrac{2\|C_1\|(k-\mu)}{\|T_{12}T_{21}\|(1-\mu^2)+2D_1(k-\mu)}\hat{c}_S$
Radius	$\left\|\dfrac{(T_{12}T_{21})[(\mu')^2-2k\mu'+1]}{E_1[1-(\mu')^2]-2\|T_{12}T_{21}\|(k-\mu')}\right\|$	$\left\|\dfrac{(T_{12}T_{21})(\mu^2-2k\mu+1)}{\|T_{12}T_{21}\|(1-\mu^2)+2D_1(k-\mu)}\right\|$
Available gain, G_A	$\dfrac{[1-(\mu')^2]}{2\mu'(1-k\mu')}\cdot\text{MSG}$	$\dfrac{2(k-\mu)}{(1-\mu^2)}\cdot\text{MSG}$

parameters are plotted showing that as gain gets larger, μ or μ' gets smaller. These data allow the designer to make a quantitative assessment of the stability risk as compared with the increased gain obtained by working with a potentially unstable device.

NOISE CONSIDERATIONS

Microwave amplifier designers have a wide range of noise models that they can consider. The most basic noise models for a MESFET involves characterizing noise as that which is gate-voltage-related and that which is drain-current-related. One can represent this by adding a noise voltage source as part of the gate equivalent circuit and a noise current source as part of the drain equivalent circuit as shown in Fig. 16(a). Except at lower frequencies, the gate and drain noise can be considered to be Gaussian stationary random processes, each having a mean of zero. In general, there may be a correlation between these random processes. It is customary to consider the noise as a random complex number representing the noise as a phasor in a 1 Hz band. Since the noise sources produce small voltages and current, it is sufficient to consider only linear analysis when evaluating their characteristics. In general, two classes of noise are responsible for the lumped sources discussed here. The first is thermal noise, which has a power proportional to the ohmic resistance and its temperature. A second noise mechanism is shot noise, which is proportional to the dc current flowing over a potential barrier. It is for these reasons that one usually biases a transistor for low-noise operation by choosing the drain current and drain voltage to be in the lower region of the *IV* characteristics.

A linear noisy circuit has an equivalent circuit configuration consisting of an equivalent series noise voltage and an equivalent shunt noise current as can be seen in Fig. 16(b). In general, these equivalent noise sources are only partially correlated. The current noise source consists of an uncorrelated part and a correlated part, that is, $i = i_u + i_c$. The voltage source and the correlated part of the current are related by a correlation coefficient, Y_c, where $i_c = Y_c e$. Since the means are zero, the variance of the random variables are given by $\langle|i_c|^2\rangle = |Y_c|^2\langle|e|^2\rangle$. In general, the noise figure for a circuit is defined as the comparison of signal-to-noise ratio from input to output. This measurement is normally accomplished by comparing the noise presented by the source impedance operating at 270°K with the noise emerging from the output of the circuit scaled by the gain. The ratio, called the noise factor, is a measure of how much noise the circuit is contributing to the process. This additional noise can be modeled as being injected at the front end of the circuit along with that of the actual source. The variance of the noise terms are represented as equivalent resistances and conductance according to the formulas $\langle|e|^2\rangle = 4kT_0R_n$, $\langle|i_u|^2\rangle = 4kT_0G_u$, and $\langle|i_S|^2\rangle = 4kT_0G_S$. The noise factor is given by $F = (\langle|i_S|^2 + \langle|i + Y_Se|^2\rangle\rangle)/\langle|i_S|^2\rangle$, which simplifies to

$$F = F_m + \frac{R_n}{G_S}|Y_S - Y_m|$$

where F_m is the minimum noise factor and Y_m is the value of the source impedance that produces the minimum noise factor. It is interesting to observe that the source impedance can affect the noise that emerges from the output of the amplifier. This is particularly desirable from a design point of view because one can use an IMN to cause the actual input impedance to be transformed to be equal to the optimum and thereby cause the amplifier to have a minimum noise factor. Often the logarithm of the noise factor scaled by 10 is used to report the noise performance of a circuit. In this case the performance merit is called the *noise figure.*

It is instructive to consider the effect of the source impedance on the noise factor as viewed on a USC. Transforming

Table 11. Formulas for Constant μ and μ' Contours in the Γ_L Plane for the Input Conjugately Matched Conditionally Stable Amplifier

Γ_L Plane	Constant μ Contour	Constant μ' Contour
Center	$\dfrac{\|C_2\|(1-(\mu^2)}{E_1(1-\mu^2)-2\|T_{12}T_{21}\|(k-\mu)}\hat{c}_L$	$\dfrac{2\|C_2\|(k-\mu')}{\|T_{12}T_{21}\|[1-(\mu')^2]+2D_2(k-\mu')}\hat{c}_L$
Radius	$\left\|\dfrac{(T_{12}T_{21})[\mu^2-2k\mu+1]}{E_2(1-\mu^2)-2\|T_{12}T_{21}\|(k-\mu)}\right\|$	$\left\|\dfrac{(T_{12}T_{21})[(\mu')^2-2k\mu'+1]}{\|T_{12}T_{21}\|[1-(\mu')^2]+2D_2(k-\mu')}\right\|$
Operating gain, G_P	$\dfrac{(1-\mu^2)}{2\mu(1-k\mu)}\cdot\text{MSG}$	$\dfrac{2(k-\mu')}{[1-(\mu')^2]}\cdot\text{MSG}$

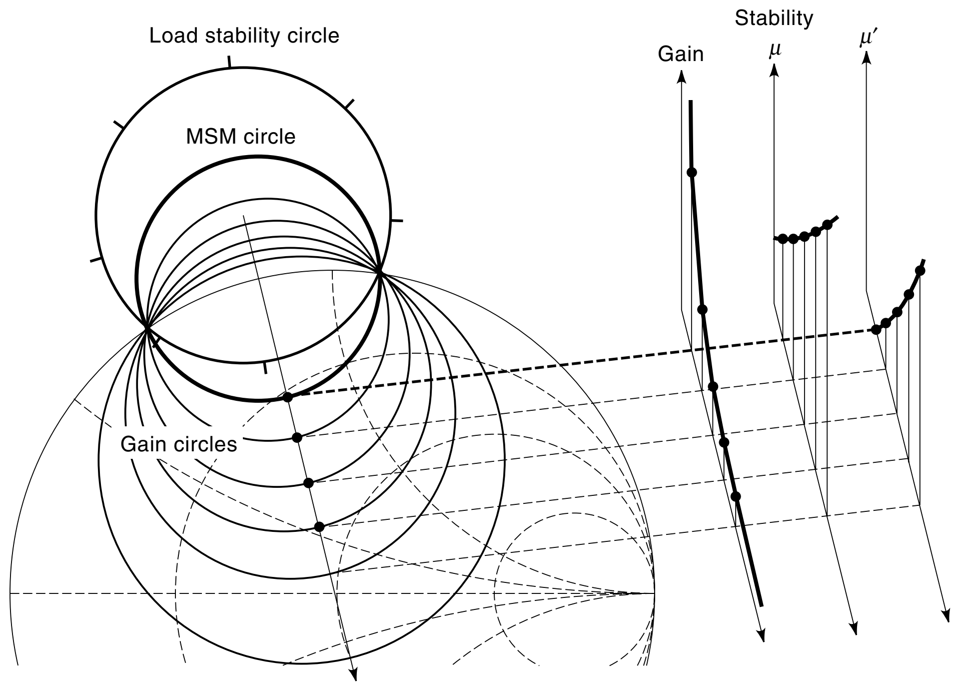
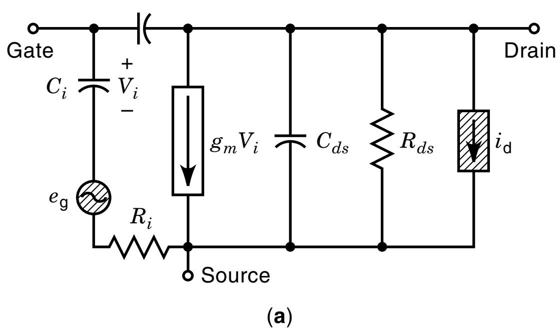


Figure 15. Illustration of the trade off between gain and stability for a conditionally stable amplifier.

impedances and admittances to reflection coefficients results in the expression $|\Gamma_S - C_F|^2 = r_F$, where $C_F = \Gamma_m/1 + N$, $r_F = \sqrt{N^2 + N(1 - |\Gamma_m|^2)}/(1 + N)$, and $N = [(F - F_m)/4r_n]|1 + \Gamma_m|^2$. This of course is recognized as defining a set of nested circles in the source plane illustrated in Fig. 17. The optimum noise figure is obtained if the source reflection coefficient equals the optimum one.

Given the noise parameters F_m, Γ_m, and r_n for a device, one can plot these noise circles and then, depending on the source reflection coefficient, ascertain the expected noise figure of the amplifier. In designing a low-noise amplifier, one must also consider the gain of the amplifier. This is because two cascaded amplifiers have a combined noise figure given by the expression $F_{12} = F_1 + (F_2 - 1)/G_1$. Thus, if the gain of the first



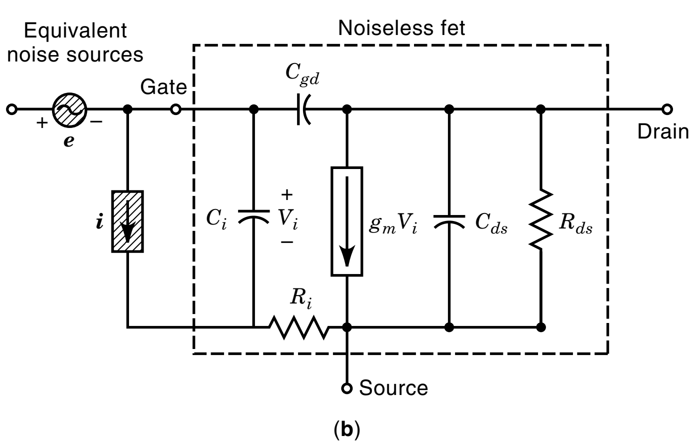


Figure 16. Illustration of (a) gate and drain noise source within a FET, and (b) equivalent noise sources at the input with a noiseless FET model.

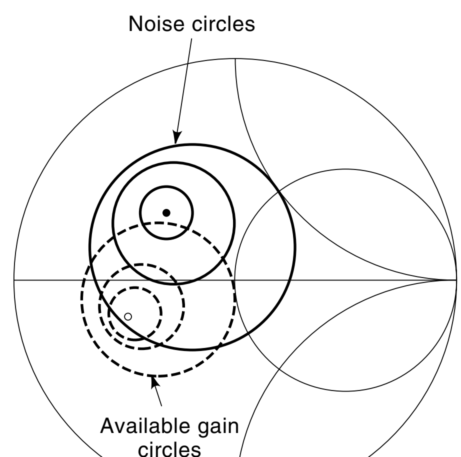


Figure 17. Noise circles and available gain circles on a USC.

amplifier is high enough, it reduces the contribution of succeeding amplifiers. When this is achieved, it is said that the first amplifier has set the noise figure for the system. Therefore, the designer must consider the available gain effects in the selection of the input impedance to be presented to the transistor. In general, a reasonable compromise is possible.

Having selected Γ_S, the input matching network is designed. With the input matching network connected, the output matching network can be designed. Since the noise figure is determined by the IMN, the designer normally elects to have the output conjugately matched so that the predicted available gain is actually achieved. The final amplifier will not be perfectly matched at the input because the IMN was not designed for simultaneous conjugate match. Usually a low-noise amplifier is not well-matched at its input side but is well-matched at its output side.

Sometimes a desirable transistor is potentially unstable and the designer must weigh the benefits of stabilizing the device using resistors which increases the noise. Since only one side of the amplifier is going to be conjugately matched, it may be beneficial to carry out a conditionally stable design omitting stabilization resistors and using the conditionally stable design techniques described earlier to quantitatively assess the risk versus increased performance. The techniques permit one to assess the completed amplifier without having to carry out the actual IMN and OMN design. The resulting amplifier stability factor, μ for the output side and μ' for the input side, can be predicted.

LARGE-SIGNAL (NONLINEAR) AMPLIFIERS

When the signal level within an amplifier is to be (or could possibly be) driven past its linearly operating region, the characterization of the device using only S parameters is no longer sufficient to describe the behavior of the device. Nonlinear effects of the device must therefore be taken into account during the design process. For instance, an unexpectedly large interfering source may be causing the low-noise amplifier at the front end of a receiver to operate nonlinearly. In this case, although the nonlinear operation is unintentional, it could greatly degrade the performance of the receiver. A different example is the intentional (or unavoidable) nonlinear operation of a power amplifier where large output power is required. In order to convert more dc power into microwave signal power, the signal in a power amplifier is usually being driven to the limit of the active device. The following paragraphs discuss the nonlinear effects of amplifiers in general and concentrate on the design issues of power amplifiers.

Since a large-signal amplifier operates into the nonlinear region of the active device, the output signal is more or less distorted compared with the input signal. For a sinusoidal input, the distorted output signal can be decomposed in the frequency domain into various harmonic components of the fundamental frequency, that is, the frequency of the input signal. Usually, the more the signal level is being driven, the more distorted the output signal becomes, and therefore the increment of the signal power falls more and more on the higher harmonic components rather than on the fundamental frequency component. Eventually, the amplifier can no longer put out any higher signal level of the fundamental frequency

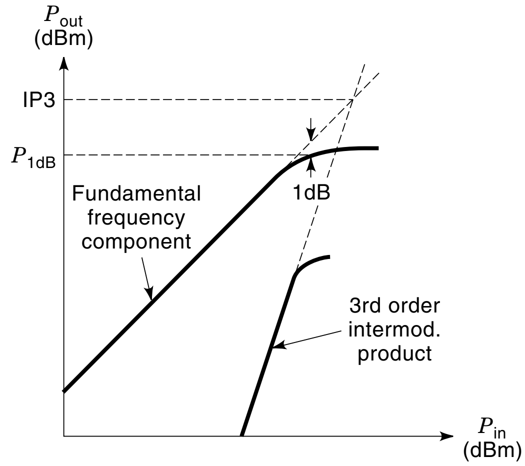


Figure 18. Illustration of 1 dB compression and 3rd order intercept point.

component. A figure of merit, which indicates the output power capability of an amplifier, is called a 1 dB compression point and denoted as $P_{1\,\mathrm{dB}}$. Specifically, $P_{1\,\mathrm{dB}}$ is the level of the output power of the amplifier when the gain of the amplifier at the fundamental frequency drops 1 dB compared with that of the small-signal (linear) level. Figure 18 shows how the 1 dB compression point is defined graphically. Traditionally, a power amplifier is operated at or above the 1 dB compression point to achieve the output power requirement with decent dc to RF power efficiency. Overdriving the amplifier into a deeper compression level may cause reliability problems in the long run, if not immediately, since the signal level may occasionally exceed the absolute maximum rating of the device. As the device technology has improved, it is becoming more common to see power amplifiers capable of working at the 3 dB to 5 dB compression level. This is motivated by the desire to achieve the best power efficiency.

The harmonics in the output signal generated by the nonlinear operation usually fall outside the frequency band of interest and can be removed by filters. However, if two or more strong signals are present in the amplifier at the same time, then the intermodulation products of these signals due to the nonlinear effect could easily fall within the passband and interfere with the desired signals. These unwanted spectral lines (assuming sinusoidal inputs) are called spurious signals. Since the strongest intermodulation signals are usually the third-order products, a fictitious measure of the intermodulation problem called the third-order intercept point (IP3) is defined. IP3 can be found by linearly extending the lines of fundamental output signal versus input signal and the third-order intermodulation signal versus input signal and by finding the output power level at the intercept point of these two lines as shown in Fig. 18. In order to find the signal level of the third-order intermodulation product, one must inject two sinusoidal signals that are very close to each other in terms of frequency within the passband so that the third-order products can also fall within the passband. Because of this, this measurement is commonly known as a two-tone test. Although IP3 is a fictitious number, it is very useful in finding out the spurious free dynamic range of the amplifier. This is because the slope describing the fundamental output is 1

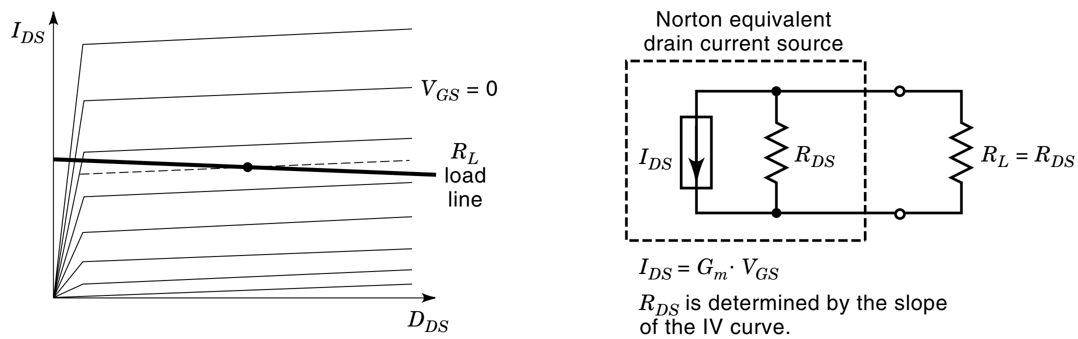


Figure 19. Illustration of conjugate match load line relative to IV curve.

when the units for the x and y axes are dBm or dBw. The slope of the third-order intermod is 3. Thus the knowledge of the intersection of these two linear extensions allows one to compare the intermod signal level for a given input situation. The lower point of the dynamic range is set by the noise level (noise figure); that is, a signal below this level is obscured by the noise. The upper limit for modulated signals occurs if the signal becomes so strong that the Fourier components in the modulation act like that of the two-tone test and produce unwanted intermod distortion in the output. As long as this intermod distortion is itself below the noise, it does not present a problem. However, if the input signal becomes so large that the third-order intermod exceeds the noise, then the distortion becomes unacceptable. The condition of the third-order intermod exceeding the noise floor sets the upper limit of the dynamic range. It is essential to ensure in the design that expected signals of operation will fall in the spurious free dynamic range to guarantee proper operation of the amplifier system.

In power amplifier application a commonly used power efficiency is called *power added efficiency* (PAE) and is defined as $\eta_{\text{PAE}} = (P_{\text{out}} - P_{\text{in}})/P_{\text{dc}} \times 100\%$. This definition differs from the dc to RF efficiency definition ($\eta_{\text{dc}} = P_{\text{out}}/P_{\text{dc}} \times 100\%$) in that it takes into account the gain of the amplifier. This is because usually, in very high power situations, the gain of the power amplifier is comparatively low such that the input power is a significant contributor of the total power calculation of the amplifier. This can be seen by rewriting PAE in the following form:

$$\eta_{\text{PAE}} = \frac{P_{\text{out}}}{P_{\text{dc}}}\left(1 - \frac{1}{G}\right) \times 100\% = \eta_{\text{dc}}\left(1 - \frac{1}{G}\right)$$

Apparently, as G increases, η_{PAE} approaches η_{dc}. The goal of a power amplifier is to transfer as much microwave signal power as possible to the load that is connected to its output port. When the amplifier is working within the linear region, the maximum power transfer occurs when the output port of the active device is conjugately matched. Figure 19 illustrates this situation based on the device model and the dc *IV* characteristics of the device. Ignoring the reactive element in the model, it is clear that the conjugately matched load line has a slope which is the negative of that seen in the saturated region of the *IV* curves. If the *IV* curves consisted only of straight lines, there would be no difference between linear and nonlinear matching of the output. However, there is a low voltage and a high voltage limit to the *IV* curves. The low voltage limit is set by the knee of the curves, and the high voltage limit is set by avalanche breakdown effects. With these constraints, the maximum power output changes from that determined by the small-signal (conjugate match) situation.

A determination of the output power produced by a transistor operating nonlinearly can be made using a variable load, which includes attenuators and tuning elements combined with power-meter measurements. This technique is referred to as making *load-pull* measurements. The output power can then be plotted as a function of load impedance. This is best done using a Smith chart where the load is represented in terms of its reflection coefficient. The data are displayed in terms of contours of constant output power. The contours are closed curves usually oblong in nature. The nature of these curves can be understood by considering the current-limited case and voltage-limited case. The most power will occur when the largest voltage and current swings occur across the load as seen in Fig. 20, with the load line set by output load R_{L1}. If the slope is too low, then the output will be constrained by the drain voltage limit as illustrated by the load line set by R_{L2}, whereas if the slope of the load line is too high, then the output will be constrained by the drain current limit as illustrated by the load line set by R_{L3}.

In the current-limited case a series reactance can be added until the voltage limits are reached. This would produce a circular contour on the Smith chart equating to a constant resistance trajectory. Likewise in the voltage-limited case, a shunt reactance can be added until the current limits are reached. This would produce a circular arc equating to a constant conductance trajectory. These contours would be the load-pull contours if the output of the transistor did not include any reactive elements. In general, the output consists of a series inductor due to bond wires and a shunt capacitance due to the drain to source capacitance. The initially derived load-pull contours can be transformed by extracting the reactance associated with these elements, resulting in closed contours that are composed of distorted arcs rotated counterclockwise as illustrated in Fig. 21.

A technique that provides a good approximation in the design of power amplifiers is known as Cripps's method. In this case the *IV* curves are plotted to determine the optimum bias and load line, which then determines the optimum load resistance as shown in Fig. 22(a). Output data are then taken at that bias condition, and the S parameters are plotted as a function of frequency. Based on these data, a best fit of a series inductance and shunt resistance capacitance combination

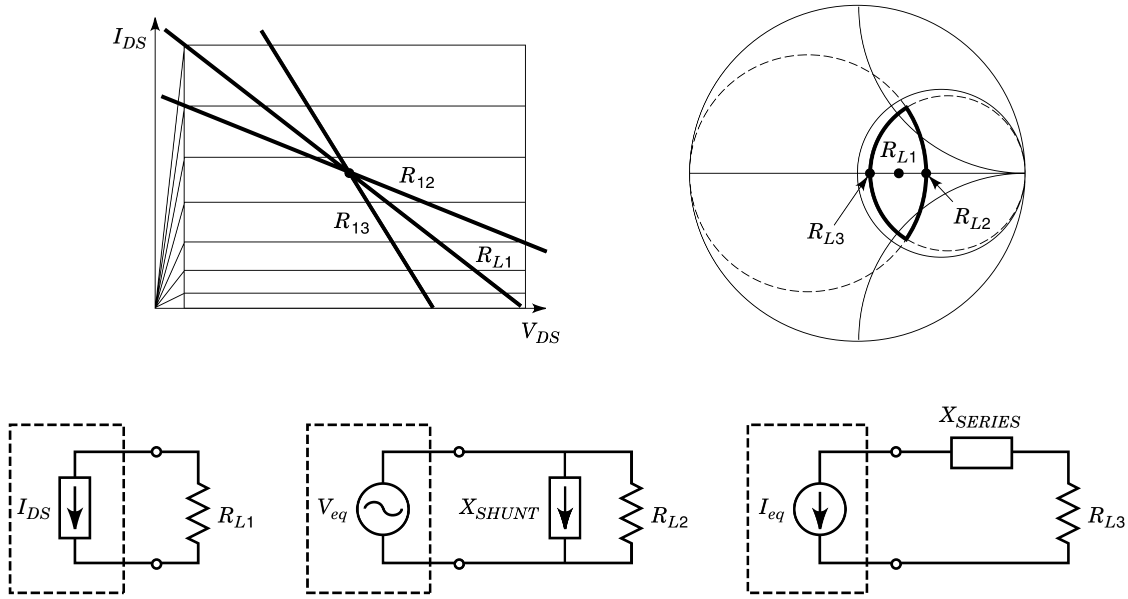


Figure 20. Illustration of load lines which produce optimum power condition, voltage limited condition, and current limited condition.

are determined appropriate for the frequency of operation as shown in Fig. 22(b). The optimum resistance from the load line considerations is substituted for the S-parameter-derived resistance. This new circuit is called the Cripps's load as shown in Fig. 22(c). A matching circuit is created to transform the Cripps's load into 50 Ω. This matching circuit becomes the output matching circuit for the power amplifier.

MULTIDEVICE COMBINATIONS

Often it is desirable to combine multiple devices into a amplifier module. At the lowest scales, this process occurs at the monolithic microwave integrated circuit (MMIC) level, where multiple FETs are combined to increase gain or power performance. At a higher level, combining occurs with connections

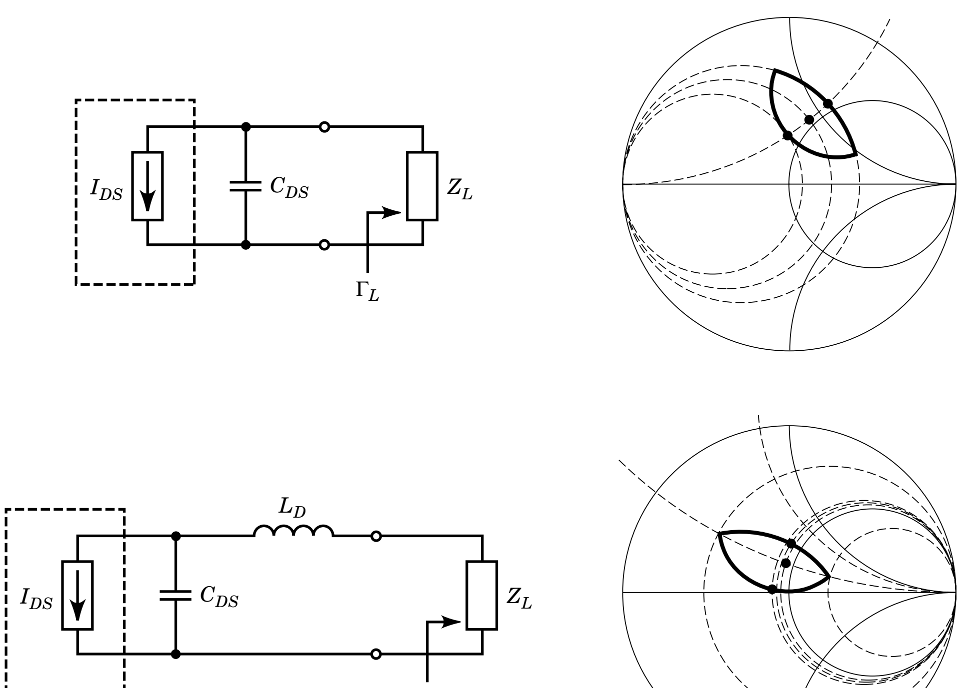


Figure 21. The effect of output reactance on load pull contour.

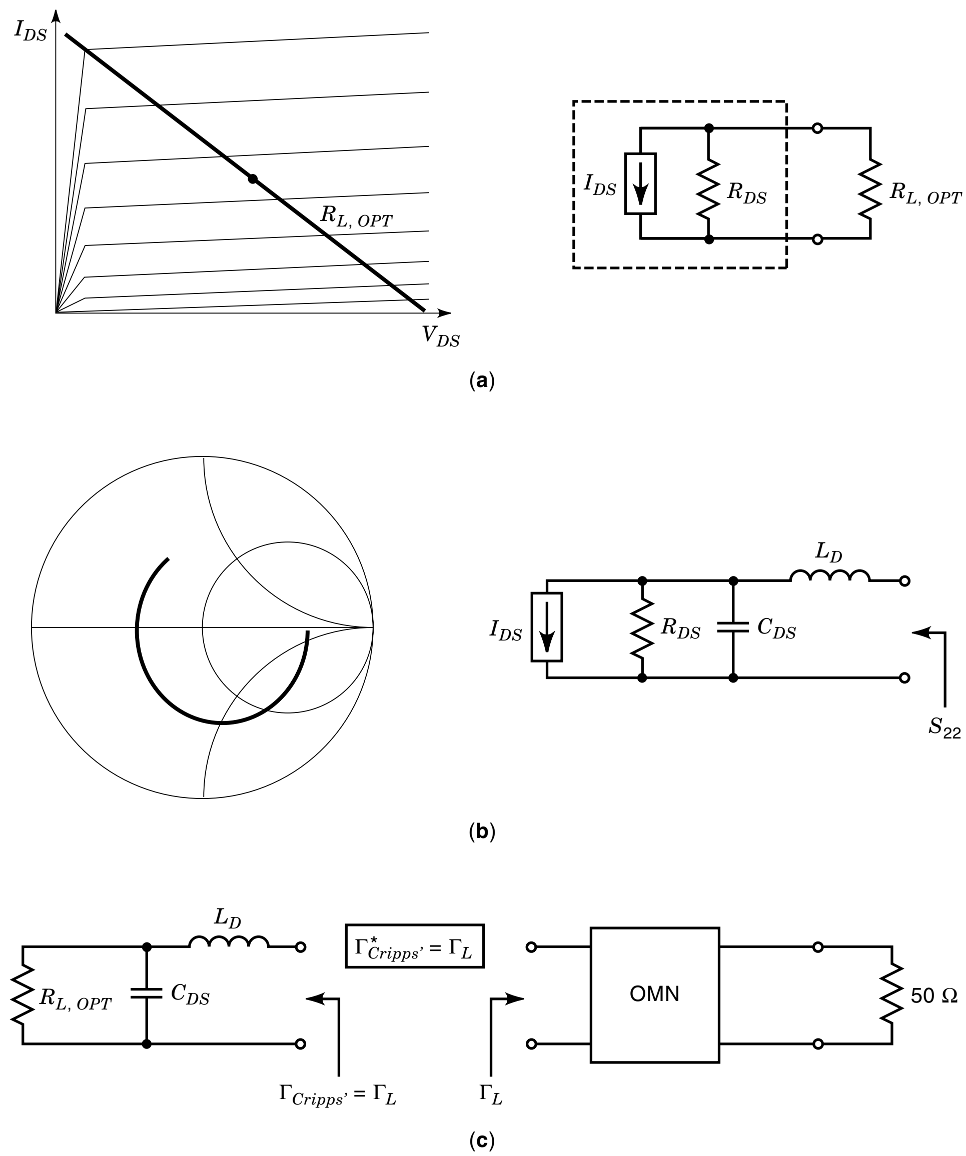


Figure 22. Illustration of Cripps's method for determining the OMN for a power amplifier.

between packaged transistors. A variety of techniques have been developed. A sampling of basic approaches are included here to represent many of the basic ideas with a brief description of associated characteristics.

The first combining approach is referred to as the *series combination* of amplifier elements as illustrated in Fig. 23(a). In this case, transistors with appropriate matching networks and bias circuits are cascaded. The individual transistors and supporting circuitry is referred to as a stage. Hence, an amplifier module created this way is usually called a multistage amplifier. Matching circuits between transistors are called interstage matching networks and are distinguished by the fact that they match a complex source to a complex load as opposed to one side being matched to 50 Ω. With appropriate matching, the gain of the combined amplifier equals the product of the gains produced by the individual stages. Cascading stages provides a technique for increasing the overall gain. Often the type of transistor is tailored to the particular stage. For example, in a two-stage amplifier, the first transistor may be chosen for its small signal gain while the second may be chosen to be capable of delivering a particular output power. As discussed earlier, the noise figure and gain of a cascaded system is such that usually the first stage dominates the noise performance of the combined amplifier. Nonlinear issues require special care in a cascaded system. Generally, one desires all of the stages except possibly the last stage to operate in a linear mode. Likewise, the gains and spurious free dynamic range of the individual stages must complement each other to ensure that the maximum overall dynamic range is achieved.

A second combination of transistors results in a circuit called a *balance amplifier,* as illustrated in Fig. 23(b). In this case, two transistors are connected somewhat in parallel using a 3 dB hybrid network such as a branch-line coupler or a Lange coupler. Both types of couplers are four-port circuits that accept an input signal and generate an in-phase and quadrature phase output, each of which is 3 dB down from the input. The fourth port, called the isolated port, produces no signal, provided that energy flows only in the forward direction, that is, no reflections occur. The coupler circuit is

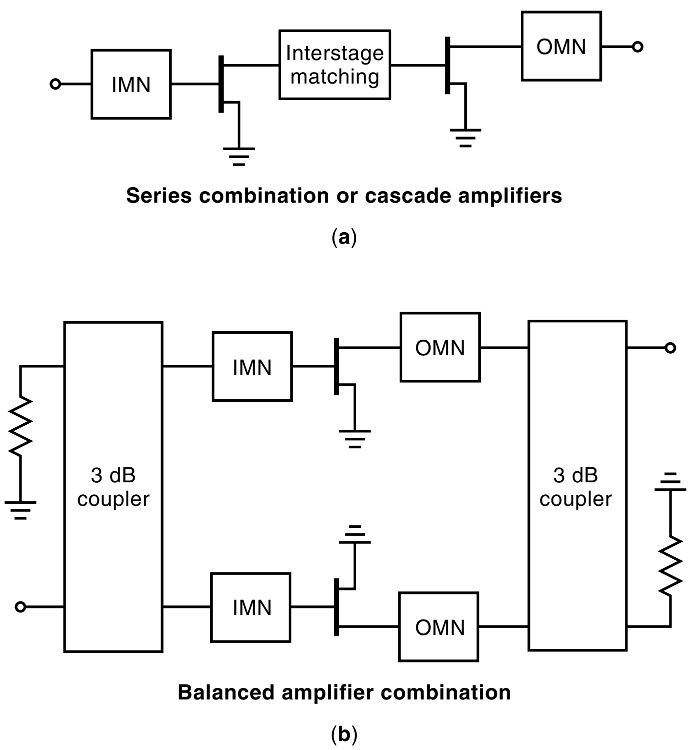


Figure 23. Illustration of (a) series combination of amplifiers, and (b) balanced combination of amplifiers.

symmetric, meaning that any of the ports can become an input port with the other ports assuming the in-phase, quadrature, and isolated roles. Branch-line hybrid couplers are used in narrowband applications and add little to the manufacturing complexity of building the amplifier. On the other hand, a Lange coupler is used in broadband applications. However, a Lange coupler does affect the manufacturing complexity and reliability because the couplers require bonding wires between elements of the circuit. A balanced amplifier is useful in the design of an input matched low-noise amplifier. Assuming ideal matched transistors, the combining coupler cancels out any reflected signals from the transistors' IMN so that the input to the balanced amplifier is matched even if the individual transistors are not matched. This means that the individual transistor can be matched for optimum noise performance while the balanced combination is matched to 50 Ω. The same principle applies to the output side of the balanced amplifier. An additional advantage of the balanced amplifier is that the compression point of the balanced amplifier is 3 dB higher than that of the individual transistors. This is because the power is split between the two devices and the combined compression point occurs only when the reduced power in each transistor begins to compress. Additionally, balanced amplifiers have the advantage of degrading gracefully; that is, if a transistor fails, the amplifier continues operating at reduced performance versus totally failing. The price for these benefits is an extra transistor and extra circuitry. The designer must weigh the cost benefit trade-off for the particular application.

A third type of combining technique results in a *distributed amplifier* or *a traveling wave amplifier* as illustrated in Fig. 24. This novel approach for achieving very wide band amplification has become a practical reality because of monolithic microwave integrated circuit technology. The technique depends upon having multiple amplifying transistors that are closely matched in wideband electrical characteristics. Implementing this approach with packaged devices is extremely difficult and the promise of wideband operation is difficult to achieve. The concept consists of taking two transmission lines that are side by side and connecting amplifiers across from one line to the other. One transmission line serves as the input and is usually terminated in 50 Ω. One side of the output transmission line is terminated to either absorb or reflect energy according to the plan of the designer. Distributed amplifiers are often used as gain block modules where it is desirable to be able to amplify signals that are wideband, perhaps resulting from spread-spectrum modulation, or whose frequency operation covers a wide portion of the spectrum. Since distributed amplifiers involve parallel-like combining of transistors, the overall noise figure is worse than that of the individual transistors.

A fourth technique that is used frequently in power amplifiers is that of parallel combinations as illustrated in Fig. 25. In this case the inputs and outputs of multiple transistors are connected. Special combining circuits may or may not be used. This approach allows for single bias point connections on the gate side and on the drain side of the circuitry to serve a bank of transistors. This technique allows the combining of power but requires careful attention to the phasing of each element of the circuitry. For this reason it is most easily implemented in a monolithic microwave integrated circuit process. The MMIC process also permits the combining to occur before additional parasitics have further complicated the operation. This technique has the effect of lowering the output impedance since the output impedance of many transistors are combined in parallel. Special combining networks can be employed such as Wilkinson couplers, which add to the complexity of the circuit but also increase its stability. A unique characteristic of this type of combining is its ability to support "odd-mode" oscillation, meaning that multiple legs of the circuit may in fact oscillate but do so out of phase with each other, so that the oscillating signal cancels when combining occurs. In this case the oscillation affects the operation of the individual transistors but is not easily observed at the input or output of the combined amplifier. The designer may observe only degraded output power with no immediately obvious explanation. Examination of higher frequencies will sometimes expose the oscillation since the phase cancellation is not necessarily balanced for harmonics. The remedy for odd-mode oscillation is to place stabilizing resistors between the parallel parts of the circuit. Since the desired operation of the amplifier has all of the legs operating in phase, the resistors have no effect. However, for a signal that is out of phase between the parallel elements the stabilizing will conduct, thereby damping the buildup of oscillation. Manufacturers of power transistors will often match the output of a power transistor to a user-specified frequency. The manufacturer can carry out the matching inside the package where the reactive component of the impedance can be dealt with more easily.

DESIGN EXAMPLES

Several examples of microwave signal amplifiers are presented to illustrate the use of the concepts previously pre-

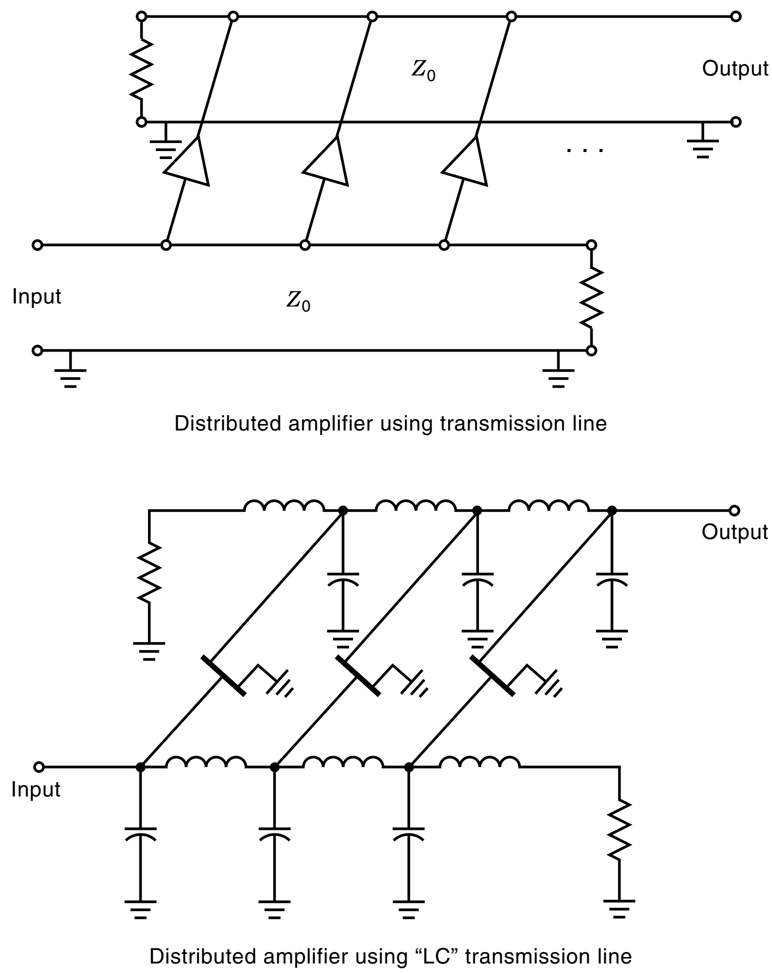


Figure 24. Illustration of distributed amplifier configuration.

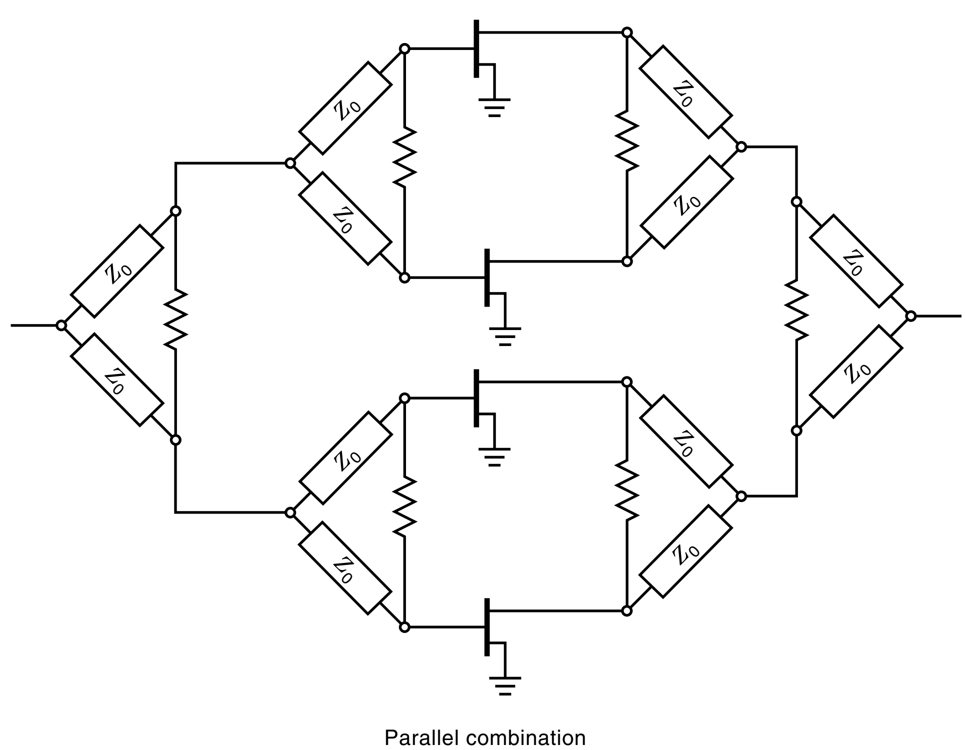
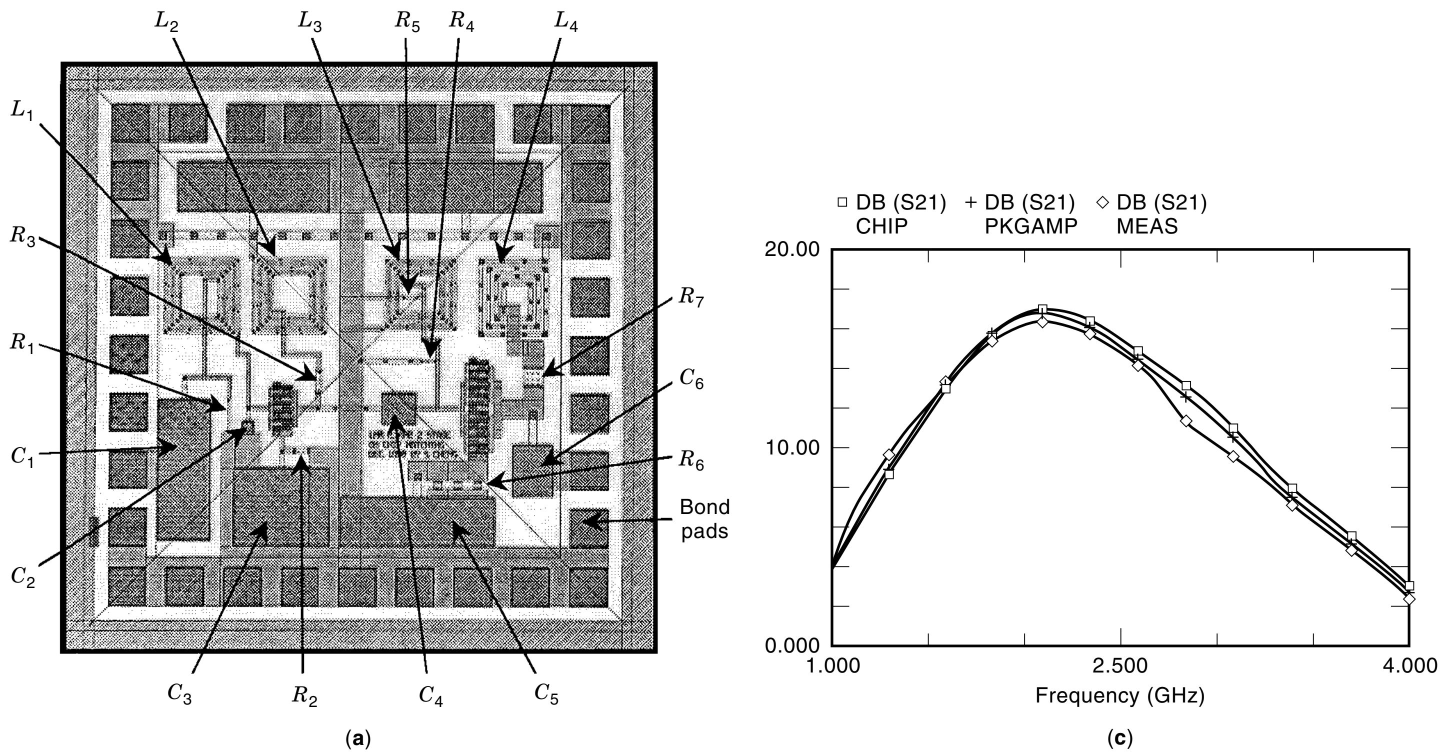


Figure 25. Illustration of a parallel combination of amplifiers.



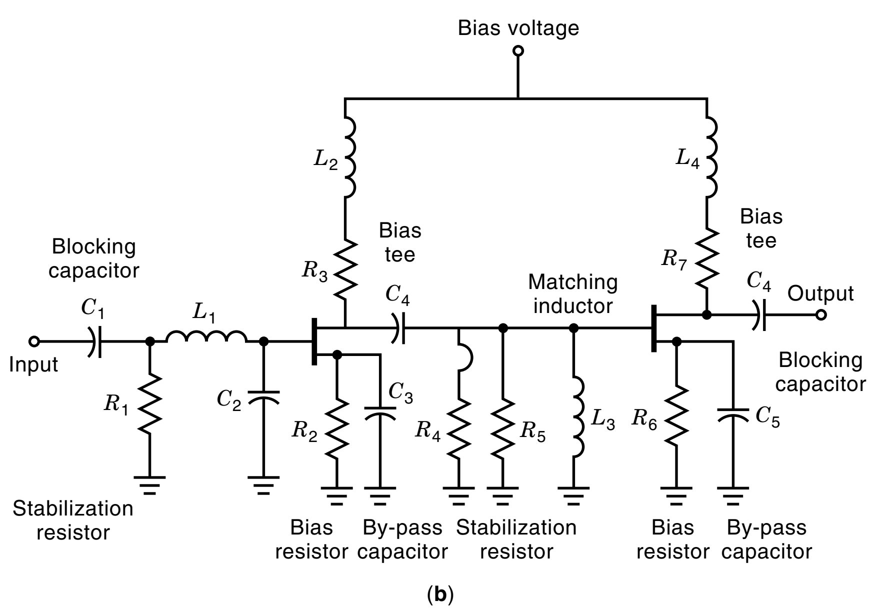


Figure 26. MMIC LNA example. (a) Fabricated GaAs chip, (b) chip schematic, and (c) chip performance and prediction.

sented. In all cases the designs have been implemented, and measured versus modeled data are presented so that the reader can get a sense of the fidelity of amplifier theory. First an MMIC low-noise amplifier (LNA) is illustrated. Annotated schematics are included to facilitate an understanding of the design techniques.

The first example, Fig. 26, illustrates an MMIC implementation of a low-noise amplifier design. The design was fabricated in GaAs technology by TriQuint. The final chip was 58 mm^2 square. Clearly visible bond pads ring the perimeter of the chip. This chip was compatible with a standard TriQuint package and placed within one for testing. The test data include a comparison of the simulated chip both alone and including the package parasitics as well as measured data of the chip in the package. The LNA consists of a two-stage design and includes stabilization resistance, input, interstage, and output matching networks, as well as bias tee circuitry. In this developmental chip, several air-bridge structures were included that could be severed to vary performance and maximize the per-chip developmental value of a foundry run. The models used in the design were implemented in a microwave computer-aided design (CAD) system. The close agreement of the measured and predicted data speaks to the effectiveness of such systems.

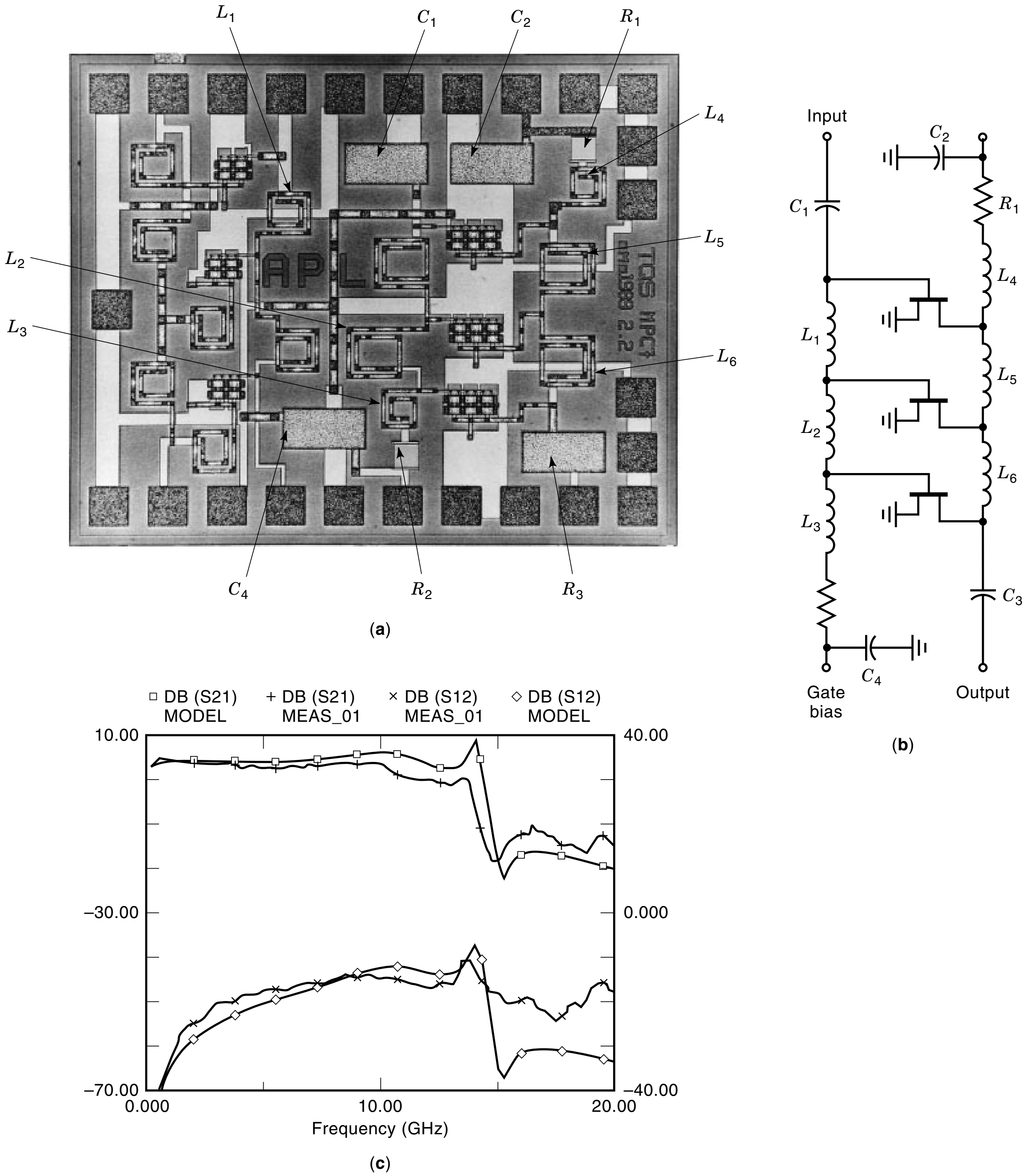


Figure 27. MMIC distributed amplifier. (a) Fabricated chip, (b) electrical schematic, and (c) performance and predictions.

The second example, Fig. 27, illustrates MMIC implementation of a distributed amplifier. This design was also fabricated by TriQuint on a 58 mm^2 chip. The chip actually contains two distributed amplifiers, one occupying the left half of the chip and the other occupying the right half. The left design is cascadable, meaning that multiple chips can be bonded together to make a larger distributed amplifier. The right design includes 50 Ω terminations on the chip so it contains a self-contained distributed amplifier, thereby having one input and one output. A schematic is shown for the right design to again illustrate the principles of amplifier design. Also shown are measurements and predictions on the same graphs.

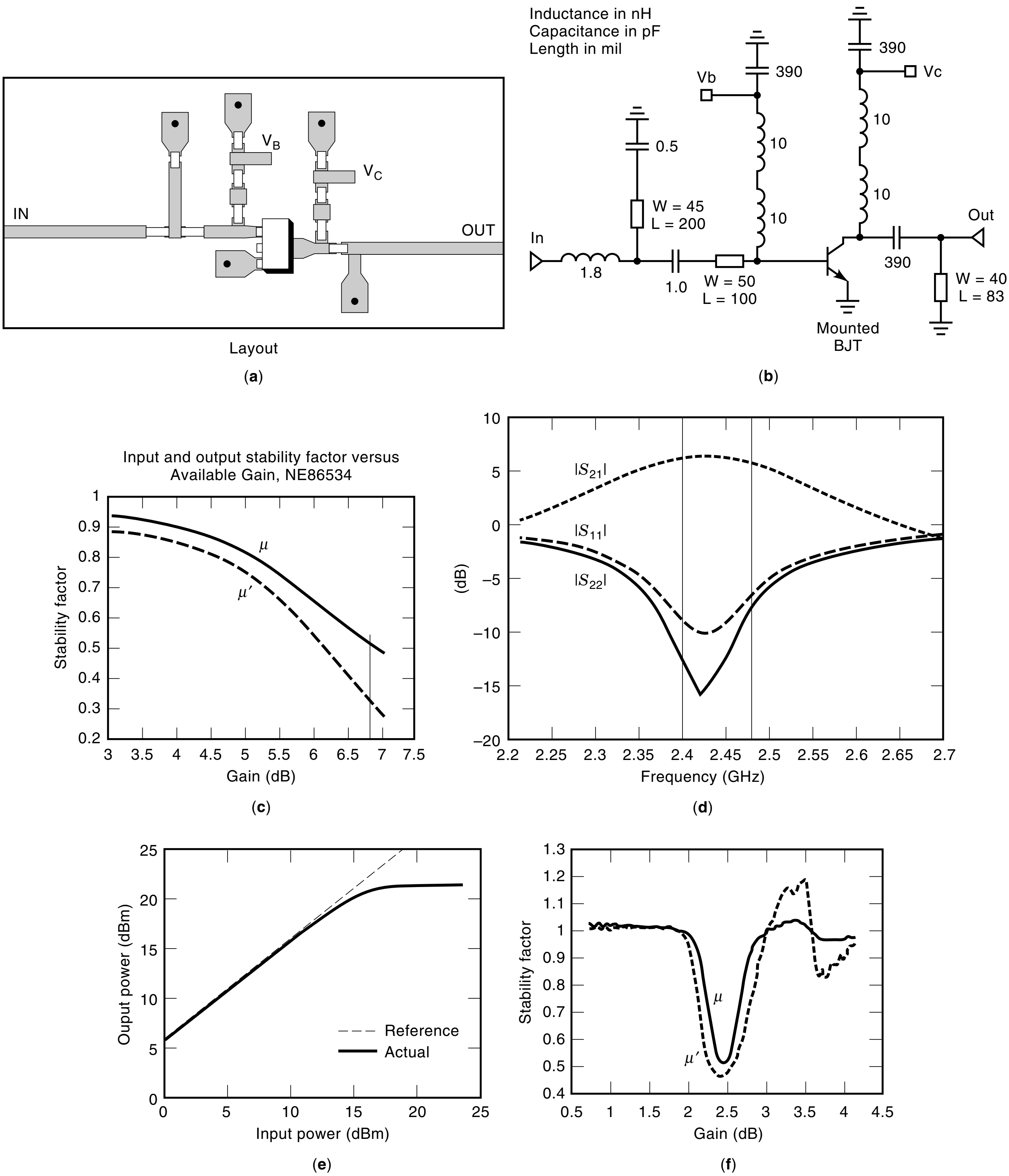


Figure 28. Illustration of a conditionally stable amplifier design.

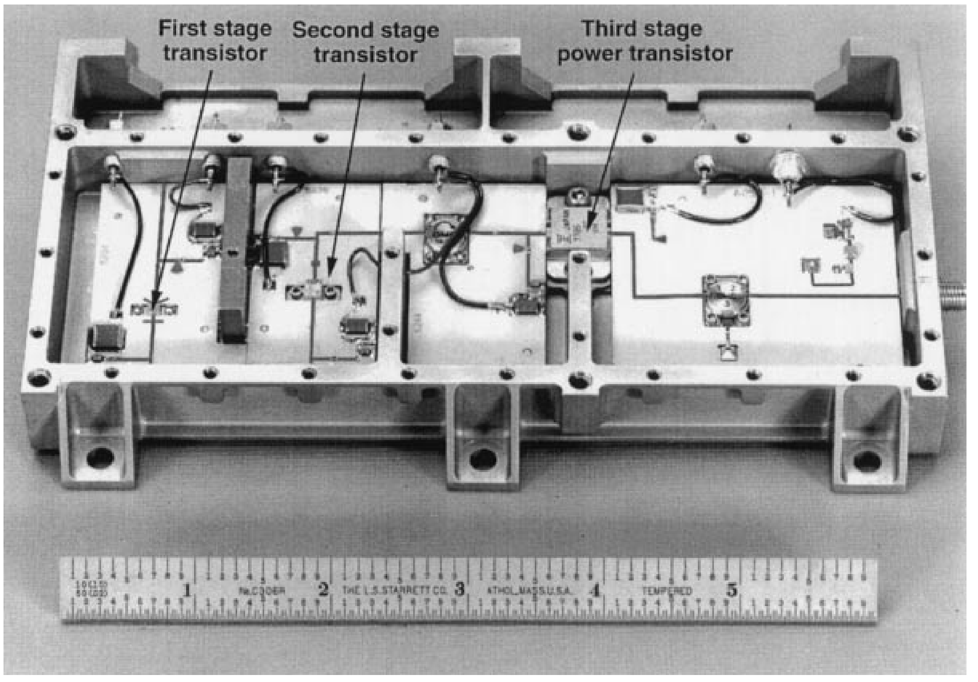


Figure 29. X band power amplifier.

Again, the close agreement reinforces the accuracy of the models discussed previously. The models were implemented in a CAD system to facilitate design.

Cost-conscious wireless designers are always looking for design approaches that permit the use of less expensive parts. The third example, Fig. 28, illustrates a conditionally stable amplifier design and shows that it can be an attractive approach since enhanced gain can translate into reduced cost of RF parts. Such an approach is illustrated for a 2.4 GHz wireless local area network (WLAN) application where device cost is reduced an order of magnitude. All wireless applications include either low-noise or low-power RF amplifiers. From a cost and a power consumption point of view, it is desirable to design the amplifiers using silicon (Si) bipolar junction transistor (BJT) devices. However, Si technology has the disadvantage that performance rapidly falls off in this frequency range and performance is sensitive to the various packaging techniques such as ceramic and plastic packages. It is shown below that the use of a conditionally stable design permits a less expensive plastic packaged part to be used in place of the more expensive ceramic part. Such a design requires a quantitative assessment of stability, achieved by using the stability parameter μ.

The design of the conditionally stable power amplifier is illustrated using a plastic-packaged BJT (NE85634) and Rogers low-cost, commercial substrate (RO4003, 20 mm). The design starts by measuring the S parameters of the mounted BJT. This is important because it includes effects such as vias to ground, mounting pads, and device straps since they represent parasitic impedances that can influence performance. Mounting pads behave as short transmission lines, and via holes behave as equivalent inductances. From the measured S parameters of the mounted transistor the stability circles and power gain circles were generated. Also the maximum single-sided match (MSM) gain circle was plotted and the load impedance was selected to give a stable input match for a gain of 6.8 dB.

The final example, Fig. 29, is a three-stage satellite solid-state power amplifier. The final stage uses a flange-mounted transistor. A flange-type package is often used in a power transistor since heat is more easily transferred to the ground-plane heat sink. The output of the power transistor is matched to produce 5 W of power at X band. Circulators are used to ensure stability. The power amplifier is temperature-compensated to ensure that the power specification is met over a wide temperature range.

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MICROWAVE AMPLIFIERS. See Broadband networks; Klystron.

MICROWAVE AND MILLIMETER WAVE CIRCUITS. See Monolithic microwave integrated circuits.

MICROWAVE ANTENNAS. See Waveguide antennas.