ELECTROSTATIC DISCHARGE

INTRODUCTION

Dissimilar materials brought in contact with each other and then separated often become electrically charged; electrons are removed from one material and remain on the other. One body becomes charged negative and the other charged positive. The process is known as triboelectricity and is well known from everyday experiences. It is the cause of the shock experienced touching a doorknob after walking across a carpet on a dry day and the snapping sounds heard while removing clothing from a clothes drier. The electrical discharge as a triboelectrically charged object loses its charge is known as electrostatic discharge (ESD). ESD is usually a minor annoyance, but it can be destructive and even catastrophic. The electronics industry has incorporated extraordinary levels of functionality into electrical appliances from computers to microwave ovens through miniaturization. As will be shown, the energy contained in even a minor ESD event results in enormous current and power densities when they occur in a state-of-the-art integrated circuit. In other instances, the energy of an ESD event can cause flash fires. An example is dispensing gasoline into an ungrounded metal container. A difference in potential between the gas can and the pump nozzle can result is a spark that ignites the gasoline vapor.

ESD CONCERNS IN MODERN ELECTRONICS

The potential for an ESD event to cause damage in a modern electronic system can be illustrated in several ways. Examples include the high electric fields that can be produced across dielectrics, the high current densities that can flow in conductors, or the energy density that can be released in the small volumes characteristic of circuit elements in state-of-the-art electronics.

A human body has a capacitance of about 100 pF to its surroundings. People begin to feel ESD events from their fingers at potentials of about 3000 V, at which point the body will have a charge of about 300 nC. Other parts of the body can be more sensitive, but it is often the finger that touches an object first. Today, complementary metal oxide semiconductor (CMOS) integrated circuits use layers of silicon dioxide with thickness below 5 nm. The polycrystalline silicon gate electrodes that form the top electrode on the thin gate oxide are electrically connected to the inputs of the circuit. If a 3000 V potential is applied across the 2 nm oxide, an electric field of 3000 MV/cm is produced. This is 1500 times the 10 MV/cm field needed to cause dielectric breakdown of silicon dioxide.

Discharges from human fingers have been found to have effective resistance on the order of a few hundred to a few thousand Ohms with a value of 1500 Ω often used for testing purposes. With a resistance of 1500 Ω and a capacitance of 100 pF, a 3000 V ESD event will have a 2 A peak current with a characteristic decay time of 150 ns. This is similar to the current levels in a household light bulb. Internal wiring of integrated circuits typically use aluminum or copper films approximately 0.5 μm thick, patterned into runners that can be less than 0.5 μm wide. A 2 A current through a metal line this small would have a current density of 8×10^8 A/cm^2, or a million times higher than the current density in 14 gauge household wiring at its allowed current carrying capacity of 15 A. It is clear that every effort must be made to prevent the current from a 3000 V ESD discharge from a human finger from going through one of the smallest metal lines on an integrated circuit.

Hard disk drive data storage systems have made tremendous advances in data storage capacity over the last 20 years. To store greater amounts of data on disk drives with smaller physical size, it has been necessary to store more data per unit area of the disk drives surface. Not only does the quality of the magnetic material have to improve, but also the read and write transducers have to improve in terms of their physical size and in their signal quality. One advance is the magnetoresistive head for reading disk drives. A magnetoresistive material changes resistance because of changes in the magnetic field. Their high sensitivity has made them very popular with disk drive manufacturers, but they have proven very susceptible to ESD damage during manufacture. The magnetoresistive heads have film heights of about 2 μm and a thickness of about 20 nm. Calculations have predicted a failure current of 250 mA for a 1.5 ns pulse through a 30 Ω sensor. This is just 3 nJ, a tiny amount of energy when compared with the approximately 0.9 mJ stored in a person when charged to 3000 V. Although it is true that in most ESD events only a small fraction of the energy of a discharge is actually deposited directly into an electronic component, with the rest of the energy being dissipated in parasitic resistance, it is clear that the energy involved in an ESD event is more than enough to cause damage to a component.

The above examples illustrate that ESD must be considered in the design, manufacture, and use of modern electronic circuits.

FAILURE MODES

There are several ways that integrated circuits can fail when stressed by ESD. Conducting materials may fuse to cause opens or shorts. Metal contacts to diodes can be heated sufficiently that metal diffuses into the silicon far enough to damage the diode junction, a condition known as junction spiking. Thin gate oxides can fail because of high voltage across the oxide. Diode junctions can melt because of heating from high currents. The most prevalent failures in modern CMOS integrated circuits are the failure of n-channel transistor junctions and gate oxide failures. Examples of these types of failures are shown in Figs. 1 and 2.

DEALING WITH ESD

There are two ways that the electronics industry deals with the ESD threat in the use and manufacturing of electronic devices. Precautions are taken to ensure that sensitive devices are not exposed to ESD events, and the electronic devices are also designed and manufactured in such a way

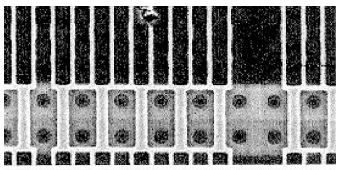

Figure 1. Example of HBM failure. In this failure the damage shows that a current filament formed from the Drain to the Source (SEM courtesy of Texas Instruments).

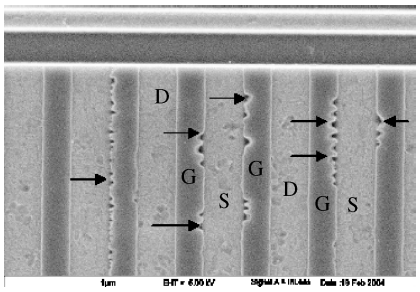

Figure 2. Example of CDM failure. The regions noted as D, G, and S stand for Drain, Gate, and Source, respectively. Note that, in this failure, damage only occurs on the Source side of the Gate and there is no evidence of Drain to Source damage (SEM courtesy of Texas Instruments).

as to make them immune to the levels of ESD to which they might be exposed. In practice both approaches are used extensively. The balance between the two approaches depends on the situation.

Most final products are expected to be immune to damage from ESD under normal use without the user taking any unusual precautions. A person sitting down to use a computer or turning on a television should not be expected to ground themselves before touching the equipment or have to wear special clothing to watch TV. The needed level of robustness is obtained by a combination of proper design, testing, and manufacture. Several aspects exist to good ESD system design. Grounded metal cases can provide excellent shielding of internal parts from the environment, but care must still be used. The case needs to be grounded and should not have large vent holes that restrict current flow during an ESD event or allow an arc to occur through the vent hole, exposing sensitive circuitry. Internal components must also be placed far enough away from the case to prevent arcing. Plastic cases can be used because arcing will not occur through the insulating material, but vent holes and seams can make a system vulnerable, because an arc will not terminate preferentially to a plastic case as it will to a metal case. Special care must be taken with the use of fasteners. Metal screws or fasteners in a plastic case can provide an easy path to sensitive components. How signal wires enter an instrument can also play a role. It is often necessary to include ESD protection devices such as diode based transient voltages suppressors, thyristors, or varistors on signal lines where they enter circuit boards to provide the level of ESD protection needed for system level stress.

To ensure system reliability, it is necessary to test systems for ESD performance. Testing on systems is done by exposing the product to calibrated ESD pulses from an ESD gun. The most commonly used test standard for system-level ESD testing is IEC 61000-4-2 (1). In this test an electronic device such as a cell phone or computer is tested while it is functioning. ESD stresses are applied to points on the unit that would be touched during normal operation or handling. There are four possible responses of the unit being tested to the stress. The desired response is that the unit continues to function without interruption. Less desirable, but often acceptable, is that the unit experiences a temporary upset but resumes normal operation without user intervention. In the third possible response, the unit experiences an interruption that requires user intervention, such as a reboot of a computer or turning the unit off and then on again to restore proper function. Finally the unit may suffer permanent physical damage. Additional information on the design and testing of systems for ESD can be found in References 2 and 3.

System components such as circuit boards are a different situation. Examples include computer mother boards, circuit boards for stereo equipment, or computer plug-ins such as memory upgrades. These components are not intended for use on a day-to-day basis as stand-alone units, and they require careful physical handling and storage until they are mounted in a system that provides physical protection. It is therefore not unreasonable to require special handling to prevent ESD damage. The handling precautions start with shipment in special materials, which do not easily become charged and have an electrical resistivity at a level that allows electrical charge to bleed off from the component at a rate slow enough that damage does not occur. During the installation of the component into a system, the installer needs to ensure that anything that comes in contact with the component is grounded before it contacts the board. This precaution is best done in a properly designed ESD-free workspace as will be discussed below. This situation is not always practical, however, especially for systems like computers, which often are repaired at their point of use rather than in a repair shop. Circuit boards must therefore have some level of ESD robustness, which is accomplished by choosing board components that exhibit good ESD characteristics, as will be discussed below, and by precautions in the design of the board. A variety of aspects exist to good ESD board design. One involves running a ground trace around the outside of the board where first contact is usually made to the board. A second involves avoiding floating metal, which can experience an arc and then have a secondary arc to a sensitive component.

The manufacture of circuit boards presents an even larger challenge because individual integrated circuits must be handled. Even a small percent of failed boards caused by ESD damage during manufacture is a serious financial burden in the highly competitive electronics industry. The first step is to choose components with reasonable levels of ESD robustness. Even when this step is done, precautions must be taken during manufacture. The workplace must be designed to reduce the number and severity of ESD events. A multimillion-dollar industry exists to help in this effort. Specialized workbenches are made that use conductive and electrically dissipative materials that prevent the buildup of charge, special chairs are designed not

to become charged as they roll, and conductive flooring is used to keep personnel from becoming charged. Personnel are also required to wear conductive shoes, grounding ankle straps, or grounded wrist straps, which keep them from becoming charged while handling sensitive components. Air ionization is also used to help dissipate charge, especially on insulating surfaces. Workers must also be trained to ensure that they know the proper procedure for handling sensitive parts, the proper use of ankle and wrist straps, and to understand the consequences of improper handling. Manufacturing machinery such as pick and place machines used to populate circuit boards needs to be designed in a fashion to prevent the machines from becoming charged and discharging to the integrated circuits that are being handled. Details of proper handling of ESD-sensitive circuits can be learned from Reference 4.

ESD issues are also a concern in the manufacture of integrated circuits, especially in the packaging operation. Integrated circuits are manufactured on the surface of single-crystal semiconductor wafers, usually silicon, which are up to 300 mm in diameter. From dozens to hundreds of individual circuits will be on each wafer. Before use the individual circuits must be removed from the wafer and placed into a holder or package that protects the circuit and provides electrical connections between the circuit and electrical contacts on the package, which can be connected to a circuit board. During the packaging operation, final testing of the circuit, storage, and shipping precautions, similar to those used during manufacture of circuit boards, must be used. The level of care needed depends on the ESD robustness of the integrated circuits.

MEASUREMENT OF ESD ROBUSTNESS

The above discussion of dealing with the threat that ESD poses to modern electronic devices always included choosing, whenever possible, devices that have a high level of ESD robustness. This requires measurement procedures and standards for assessing ESD robustness. It is not sufficient to scuff one's shoes on a carefully chosen carpet and touch an electronic component several times and then test to see whether the device is still working. The variables are too great. Each person's capacitance will vary and will depend on ground plane location. Temperature and humidity change the charging and discharge processes. The details of how a device is touched and the day-to-day variability of the resistance of a person's finger also affect the results. There must be a quantitative standard so that similar devices from different manufacturers can be compared and so that tests done by different laboratories yield similar results. There has been extensive work on the development of standards. Three test methods have been developed to test the ability of integrated circuits to withstand ESD events. The human body model (HBM) is intended to simulate a charged person touching an integrated circuit, the machine model (MM) is to replicate a circuit exposed to a charged piece of manufacturing equipment, and the charged device model (CDM) simulates the discharge to its surroundings of an integrated circuit that has become charged. In recent years, MM has become less popular and will not be discussed further, whereas the CDM has been found to better represent the damage that occurs in manufacturing environments.

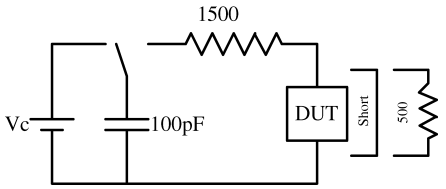

Figure 3. HBM circuit with DUT. The Short and 500 Ω replace the DUT and are used in conjunction with a current probe to verify waveform properties.

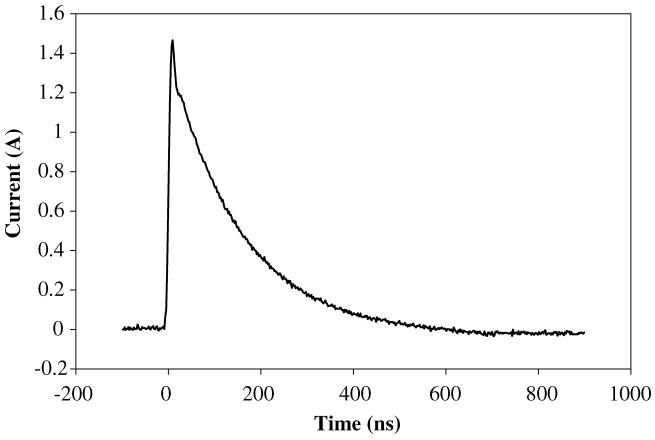

Figure 4. A 2000 V HBM waveform into a short.

HBM is the oldest ESD standard, first standardized in MIL-STD-883C Method 3015.7. HBM testing is illustrated in Fig. 3. As discussed, a person's capacitance is approximately 100 pF and the characteristic impedance of a discharge from a person, although highly variable, can be approximated as 1500 Ω. The 100 pF capacitor is charged to a voltage, usually in the range of 500 V to 4000 V. A switch is then closed to discharge the capacitor through the 1500 Ω resistor. The resultant current is shown in Fig. 4, the current rising rapidly and then decaying with a time constant of about 150 ns depending on the resistance and capacitance of the device under test (DUT). After the device has been stressed with the number of stresses and pin combinations as defined in the standard, the device is tested to determine whether its properties have been degraded. If the device passes its data sheet requirements, the device can be deemed to have passed that level of HBM stress. The level of stress that the device has passed or failed is reported in terms of the voltage at which the capacitor was charged for each stress. The reporting of the stress in terms of volts is a convenience. From the 1500 Ω resistor and the fact that modern integrated circuits typically have some form of breakdown in the 5 to 20 V range, the device never in fact sees the full voltage applied to the capacitor. HBM, and most ESD events, are better classified as high current events. The 1500 Ω also causes most of the energy to be dissipated outside of the device under test.

The HBM standards most accepted today are the JEDEC standard, JESD22-A114D (5), and the Electro-

static Discharge Association (ESDA) standard, ANSI/ESD STM5.1-2001 (6). In addition to the specification of the waveform for the various ESD models, the standards also have to deal with other aspects of ESD testing such as definition of failure, number of devices to be tested, and pin combinations. The pin combinations used in HBM stressing is one of the most challenging aspects of ESD testing. Integrated circuits have multiple contact pins or leads, and a real-life ESD event can stress any combination of the multiple pins. Some possible pin combinations include I/O (Input/Output) pins versus each other, I/O pins versus the ground connections, I/O pins versus power supplies, and power supplies versus ground. With modern circuits frequently having several hundred pins and sometimes dozens of separate sets of power and ground pin groups and each pin combination needing to be stressed with both positive and negative stresses, the amount of individual stresses that a circuit must be exposed to will run into many thousands of individual stresses. The standards require that there be a minimum time period between individual stresses. The result is that ESD testing is a very time-consuming affair often lasting several hours or more, even with the use of automated test equipment. The minimum time between stresses had been 1 s for many years but has been changed to 300 ms and more recently to 100 ms to save test time.

CDM simulates an integrated circuit becoming charged and discharging to a conducting surface. The classic example of CDM is for an integrated circuit in a shipping tube becoming charged while it slides out of the shipping tube and then discharging to a metallic work surface. To simulate this type of stress to a circuit, two conditions need to be met. First a capacitor that scales with the capacitance of the integrated circuit to its surroundings must be charged. Second there needs to be a discharge path with very low impedance to simulate the discharge to a large metal surface. Several methods have been developed to simulate this type of ESD event, but one of the more popular is the field-induced charged device model or FCDM.

A schematic diagram of an FCDM tester is shown in Fig. 5. To form a capacitor that scales with the integrated circuit's capacitance to its surroundings, the circuit is placed lead side up (also known as 'dead bug' position) on top of a thin insulator on top of a field plate. The field plate is connected to a high-voltage power supply through a high-value resistor. Applying a voltage to the field plate will cause the potential of the integrated circuit to be very close to the potential of the field plate, as long as the capacitance between the field plate and the integrated circuit is much larger than the capacitance of the integrated circuit to other parts of the test system. To form a low-impedance discharge path, a small pogo pin at the center of a ground plane is suspended over the circuit being tested. Robotic control of the field plate and the ground plane allows the pogo pin to be brought in contact with the pins of the circuit. A one Ω disk resistor between the pogo pin and the ground plane facilitates the measurement of the current through the pogo pin.

To perform the CDM test, an uncharged integrated circuit is placed on top of the insulator on the field plate, which is at zero potential. The voltage of the field plate

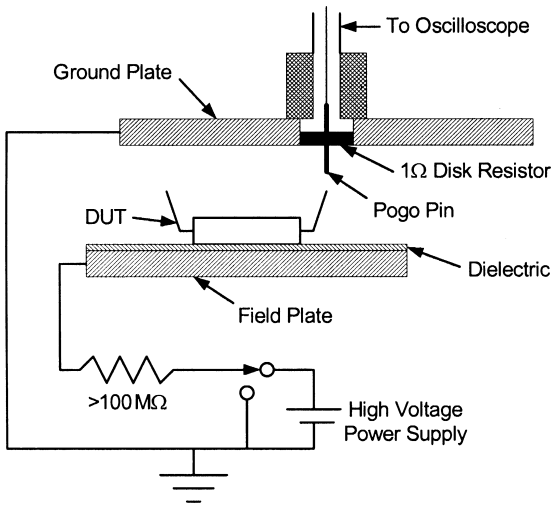

Figure 5. Diagram of FCDM tester.

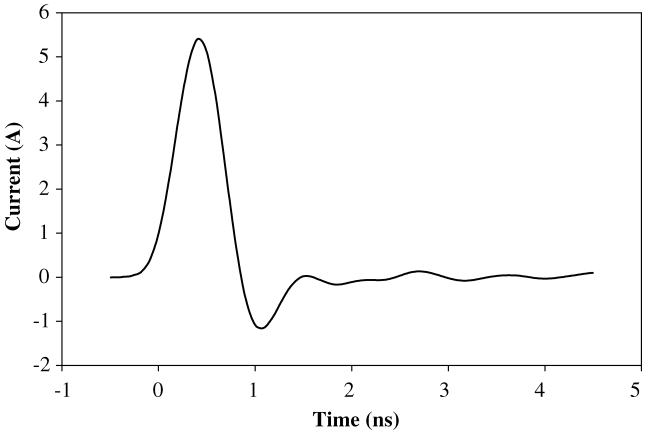

Figure 6. CDM waveform at 500 V for the small JEDEC calibration module.

is then slowly raised to a high voltage, usually in the ±200 to ±750 V range. The integrated circuit will then be at a potential close to the potential of the field plate but with no net charge. The grounded pogo pin is then brought in contact with one of the pins of the integrated circuit. As the pogo pin approaches the IC pin, an arc will occur, and a several amp pulse of current, 1 or 2 ns in duration, will return the integrated circuit to ground potential. This is the simulated CDM ESD event. A typical CDM pulse is shown in Fig. 6. At this point in the test, the circuit is at ground potential but has a net charge on it. The field plate is then slowly returned to zero potential, and the charge on the IC will return to zero. This stress is typically performed three times on each pin of the integrated circuit for both positive and negative polarity. If the circuit still functions, according to the specifications for the device, the device can be said to have passed that level of CDM testing.

The FCDM test is documented in two similar but incompatible standards, the JEDEC JESD22-C101C (7) and the ANSI/ESD STM5.3.1-1999 (8). In addition to the FCDM method, a direct charging method is also included in ANSI/ESD STM5.3.1-1999 and in a different form in the JEITA (Japan Electronics and Information Technology In-

dustries Association) standard EIAJ ED-4701/300-2, Test Method 305 (9).

ESD PROTECTION

The design of ESD protection for integrated circuits is often described as an art and even as black magic. There is some truth to protection design being an art, because currently no single set of equations or simulation tool accurately predicts ESD performance. ESD failures are also a situation of the weakest link breaking, and the weak link is often an unconsidered parasitic element. The result is a history of iterative design, as one weak link is removed only to uncover another weakness at a slightly higher test voltage. This does not mean, however, that there are no sound design procedures to follow in ESD protection. There is a considerable body of knowledge and science in ESD protection.

To protect an integrated circuit from damage by ESD stress, it is necessary to provide current paths for ESD stress between any two contacts on the circuit. For simplicity this discussion will concentrate on CMOS integrated circuits, which are the dominant integrated circuit in use today. Each ESD path needs to be able to carry the ESD current without damage to the path itself, to keep voltages along the path low enough not to trigger breakdown of circuit elements that while not in the primary ESD current paths, are parallel to them, and experience all of the same voltage levels. This is a challenge in modern integrated circuits, where there are hundreds of pins, and often dozens of independent power and ground domains. (A power or ground domain is a set of power or ground pins that are metallically connected together, either by metal on the semiconductor die or within the package containing the semiconductor die.) Fig. 7 illustrates a simplified circuit diagram for an integrated circuit with two power domains, VDD1 and VDD2, and two ground domains, VSS1 and VSS2. All circuits, inputs, outputs, and internal circuits have been illustrated as inverters for this example. The squares in Fig. 7 illustrate package pins or contacts. In Fig. 7, some stress combinations already have paths that might be successful in providing ESD protection. For example, a negative stress of the output O_2 versus the ground VSS2 will have a forward bias diode that is a parasitic element of the nMOS pull-down transistor of the output driver. Conversely other stress combinations have no current paths that would provide protection. For example, any stress of I1 versus any other pin of the circuit has no protective path. The Input leads directly to the gate oxide of the two transistors that make up the inverter.

One of the most popular and effective protection strategies that can be applied to a circuit like that in Fig. 7 is the dual diode strategy coupled with effective power supply clamps. This is shown in Fig. 8. In the dual diode strategy, a pair of diodes is placed on each input and output. During normal operation, the diodes are reverse biased and cause minimal degradation in circuit performance. During an ESD event to an input or output with respect to any other pin on the circuit, one of the two diodes will be forward biased, either to ground or to the power supply. The next feature of this ESD strategy is a power supply clamp in parallel to a diode between VDD and VSS. A power supply clamp is a circuit element designed specifically to carry ESD current during a positive stress of VDD versus VSS. It must have high impedance during normal operation of the circuit, but during an ESD event, it must turn on and have low resistance. A variety of circuits can be used as power supply clamps, and these will be discussed below. The diode between VDD and VSS may be explicitly placed. Alternatively the parasitic diodes formed by all N-Wells in p substrate in a standard CMOS technology can be used as the protection element. The final element of this strategy is the coupling of the VSS buses to each other. In most circuits, one of the ground buses is shorted to the semiconductor substrate, whereas all other ground buses are isolated from the substrate by a diode, as shown in Fig. 7. The isolation of the ground circuits is done for noise consideration. The ESD protection strategy can be greatly improved by adding the anti-parallel diode as shown in Fig. 8.

A variety of stress situations can be illustrated to show how this strategy works. A negative stress of input I1 versus VSS1 is quite straightforward. The current flows through the forward biased diode between I1 and VSS1. For a positive stress between I1 and VSS1, current flows through the forward biased diode between I1 and VDD1 and then through Power Clamp 1 to VSS1. An even more complex path exists for a positive stress of output O2 versus VDD1. In this stress the diode between O2 and VDD2 is forward biased; current then flows through Power Clamp 2, through the forward biased diode of the anti-parallel diodes between VSS2 and VSS1, and finally through the forward biased diode between VSS1 and VDD1. Similar paths exist between any two contacts in Fig. 8.

The concept of primary and secondary ESD protection is often used, which is shown in Fig. 9. A secondary protection element is placed at the most sensitive point of a buffer, such as the gates of MOS transistors. The secondary protection element ensures that voltages do not get to a dangerous level at the most sensitive point of a buffer. A grounded gate nMOS transistor, as shown in Fig. 9, is one of the most popular secondary protection elements. The secondary protection element may, however, not have sufficient robustness to absorb the full ESD current. The secondary protection is supplemented with a resistor, generally referred to as the ESD isolation resistor, and a primary protection element. The primary protection is intended to absorb most of the ESD current. In operation the secondary protection element is triggered at a relatively low voltage and current begins to flow from the pad, through the resistor, and into the secondary element. The current develops a voltage drop across the resistor that helps to trigger the primary protection element. This scheme allows for the use of robust but higher trigger voltage protective elements such as thick oxide transistors or silicon controlled rectifiers (SCRs). Secondary protection and isolation resistors have also been used extensively as a protection for output buffers. Additionally, much care goes into designing ESD protection structures so that they do not interfere with standard circuit performance. This becomes critical when dealing with precision clock circuits, high-speed digital IOs, and sensitive RF and analog circuits.

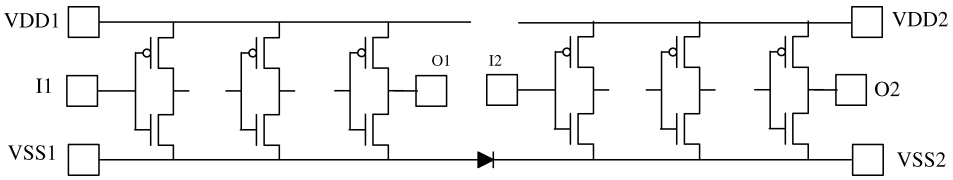

Figure 7. Simplified circuit schematic of an integrated circuit with two power supplies and two independent ground buses.

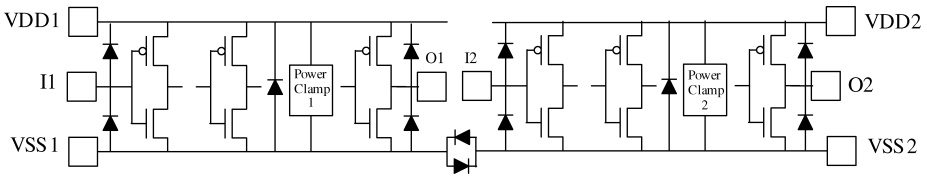

Figure 8. Simplified integrated circuit diagram incorporating a dual diode with power clamp protection strategy.

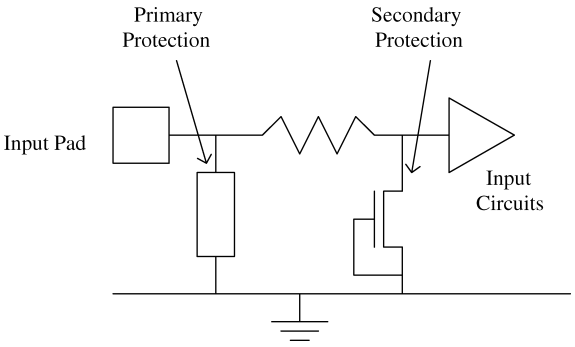

Figure 9. Illustration of primary and secondary protection.

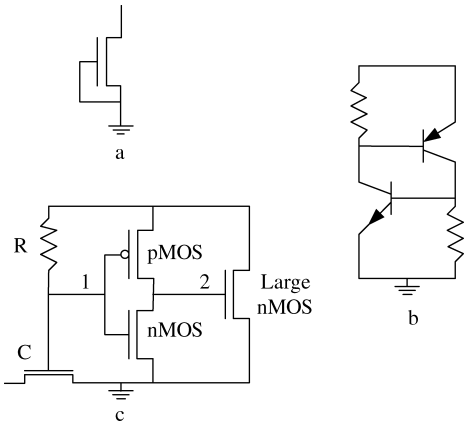

Figure 10. Examples of ESD protection elements. (a) Grounded gate nMOS. (b) SCR. (c) Dynamically triggered large nMOS or BigFET clamp.

Figure 10 shows three of the most commonly used ESD clamps; thin oxide MOS transistors, SCRs, and dynamically triggered MOS transistors. In most cases ESD protection elements are made from structures that are standard elements of the integrated circuit technology, although the layouts of the elements are often very specialized for ESD use or are supplemented with special ESD ion implants that can tailor the properties of the circuit elements for ESD use.

Transmission Line Pulse (TLP)

To improve the predictability of ESD protection design, it is important to know the properties of ESD protection structures such as those in Fig. 10 and the circuit elements that they need to protect in the current, voltage, and time domain of ESD events. The preferred tool for gaining this understanding is the transmission line pulse measurement technique. TLP produces a square stress that can be used to study the ESD properties of circuit elements or full circuits. Standard TLP uses 100 ns pulses to study the time domain of HBM, whereas very fast transmission line pulse (VF-TLP), with pulse lengths from 10 ns down to as little as 1 ns, to explore the CDM time domain.

The most common form of TLP is the time domain reflection (TDR) method shown in Fig. 11. In this technique, a transmission line, typically a length of 50 Ω coaxial cable, is charged to a voltage. A relay is then switched to initiate the pulse. The length of the pulse depends on the length of the charged transmission line. The pulse passes through an impedance matched attenuator, typically 10 ×, and then through a transmission line to the DUT. At the DUT the signal is reflected with a characteristic depending on the impedance of the DUT with respect to the impedance of the transmission line. Voltage and current probes capture the incident and reflected pulses. The impedance matched attenuator prevents the DUT from seeing multiple reflections of the original pulse. Any pulse reflected from the DUT will need to pass through the attenuator twice before returning to the DUT, making the reflected pulse too small to be of concern in the measurement. The voltage and current that the DUT experience are the sum of the incident and reflected pulses. If the connection between the relay and the DUT is much less than the length of the charged transmission line, the incident and reflected pulses will overlap and the voltage and current at the DUT can be directly measured in the overlapping region of the pulses. This is shown in Fig. 12 for a DUT whose impedance is less than 50 Ω. Overlapping incident and reflected pulses are the norm for 100 ns TLP systems. For VF-TLP systems, the incident and reflected pulses usually do not overlap and the voltage and current at the DUT need to be calculated from the separately measured incident and reflected pulses.

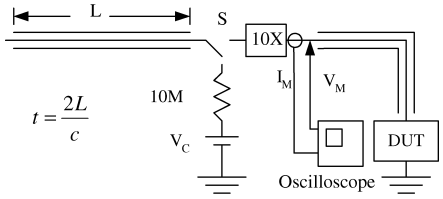

Figure 11. Time domain reflection TLP.

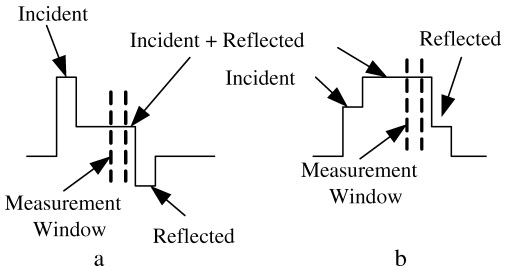

Figure 12. Schematic views of captured voltage and current versus time on a less than 50 Ω load. (a) Voltage. (b) Current.

The most common use of TLP measurements is to produce an I-V curve to characterize a device's performance in the ESD time, voltage, and current domain. A series of pulses on the DUT are made with increasing charging voltages on the transmission line. For each pulse the voltage and current are averaged within a time window to produce a current–voltage pair that can be plotted on an I-V curve. This is shown in Fig. 12. Several examples of TLP I-V curves will be presented when discussing the properties of ESD protection elements. Some TLP systems can deliver current pulses of up to 20 A. In addition to measuring I-V curves with short pulses, TLP can also be used to observe the turn on characteristics of protection elements. This form of measurement is particularly popular in the time domain of VF-TLP where the turn on characteristics of protection elements is examined for CDM protection. Most TLP systems also include the ability to measure the leakage of the device under stress after each pulse. This allows for the detection of damage after each stress pulse. TLP systems have also been built with resistors in series with the device under test to increase the source impedance from 50 Ω to 500 or 1000 Ω. The increase in the system's load line resistance allows more information to be obtained in the region of snapback. Snapback is a feature of a current versus voltage curve in which increased current results in a drop in voltage across a circuit element. This is usually associated with a new conduction mechanism turning on. Examples of snapback will be discussed below.

ESD Circuit Element Characteristics

The forward biased diode is the most important protection circuit element. A sample TLP I-V curve of an n+ to substrate diode is shown in Fig. 13. The forward bias diode properties important for ESD are quite different than the forward bias diode properties usually considered. Most discussions of forward biased diodes begin with the exponential increase in current as a function of applied bias, and the turn on voltage of the diode is considered to be approxi-

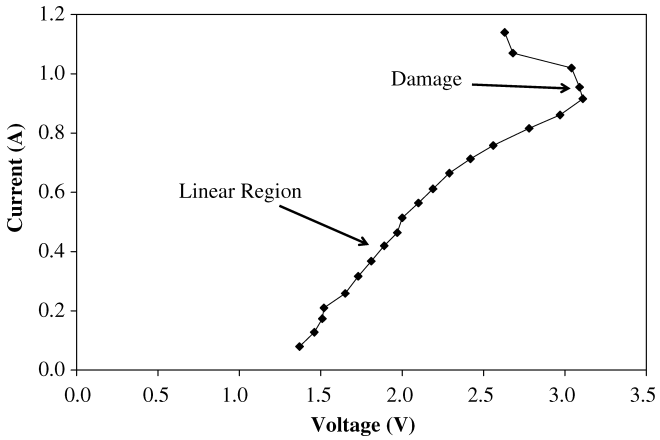

Figure 13. Sample TLP curve of an n+ to p-Well diode. The point of damage was determined by a leakage measurement after the TLP pulse.

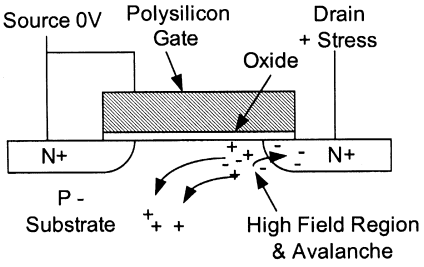

Figure 14. Cross section of an nMOS device showing the onset of snapback.

mately 0.6 to 0.7 V. At this point the diode begins to deviate from its exponential behavior under high injection conditions. For ESD protection the properties of interest are at higher voltages and currents as shown in Fig. 13. At ESD voltage and current levels, the diode shows a region of linear behavior with a voltage intercept at or above 1 V. In this range the behavior of the diode is less dependent on the diode properties than on the resistances of diffusions, contacts, and metallization that connect to the diode. At higher current levels, resistive heating and velocity saturation effects begin to dominate and the resistance begins to increase until resistive heating results in damage to the diode.

The most studied protection element is the n-channel MOS transistor, as shown in Fig. 10a. A cross section of an nMOS transistor with its gate grounded is shown in Fig. 14. NMOS transistors in ESD have a split personality. As they are used in most of an integrated circuit's circuitry, they are very sensitive to ESD damage, but with the correct layout, they can often carry considerable current in an ESD event. As a protection element the nMOS transistor is often used with the gate tied to the source, usually called the grounded gate nMOS or ggNMOS. As will be discussed below, nMOS devices often play a dual role in output buffers, and the prime role is as a pull-down element in the driver, whereas ESD protection is a secondary role.

As a protection element, the ggNMOS device employs the parasitic bipolar transistor formed by the two n+ regions, which form the emitter and collector, and the p-

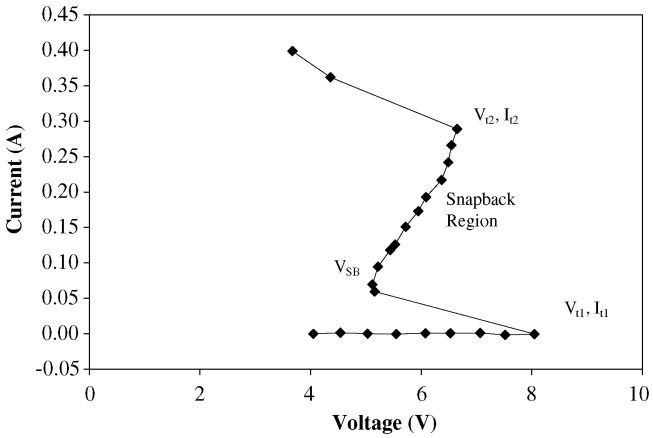

Figure 15. Sample TLP measurement of a single-finger nMOS transistor.

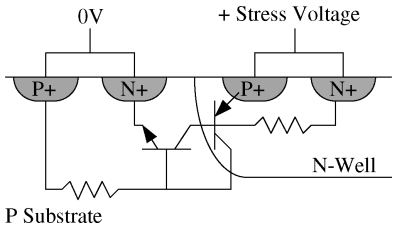

Figure 16. Cross section of an SCR used as an ESD protection element.

substrate, which forms the base. The ggNMOS will start to carry current when the diode, which makes up the drain of the nMOS device, goes into avalanche breakdown. Avalanche breakdown occurs when the voltage across the diode is so high that carriers are accelerated to sufficient energy that they generate electron-hole pairs. This results in a large increase in current over a very narrow voltage range. Fig. 14 illustrates the current paths taken by the various parts of the avalanche current, and Fig. 15 shows a TLP I-V curve of a single-finger nMOS transistor. The substrate current, as it flows into the bulk of the silicon, will raise the voltage in the region of the source and eventually forward bias the source diode. The nMOS will then begin to act as a bipolar transistor, with the source becoming the emitter; the p doped silicon on which the transistor is built, will act as the base, and the drain will be the collector. The turn on of the bipolar transistor provides a second current carrying mechanism in addition to the avalanche breakdown. The added current carrying mechanism reduces the resistance of the nMOS transistor, which results in a drop in the voltage across the transistor. This condition is known as bipolar snapback. The current and voltage conditions on the drain to trigger snapback are V_{t1} and I_{t1}. The snapback region of current flow is characterized by the slope of the I-V curve and the snapback voltage V_{SB}, the lowest voltage at which the snapback condition can be maintained. The large currents that flow in snapback cause device heating, and at a high enough current, a condition known as second breakdown occurs. The voltage and current at which second breakdown is triggered is characterized by the parameters V_{t2} and I_{t2}. After the second breakdown, the nMOS transistor is usually damaged. The damage will be characterized by leakage between the drain and substrate or even between the drain and source. In bipolar snapback, considerable current can be carried before the second breakdown, typically in the range of 8–12 mA/μm of width for a 100 ns pulse for a transistor optimized for ESD performance as will be discussed below.

The details of a second breakdown are not fully understood, but there is a general understanding of what happens. The temperature in the silicon rises until the silicon becomes intrinsic. A semiconductor becomes intrinsic when the amount of thermally generated carriers, holes, and electrons, becomes equal to the amount of carriers that are present because of the n and p doping of the silicon. At this point any further increase in temperature results in a decrease in the resistivity of the silicon as more carriers are created. At temperatures below the intrinsic point, an increase in temperature results in a decrease in mobility, which makes currents flow uniformly across the width of a transistor. At temperatures above the intrinsic point, increased temperature reduces the resistance. The result is 'Thermal Runaway' as current crowds into regions of high temperature.

Another protection element that will be discussed is the SCR observed in Fig. 10b. An SCR is shown in cross section in Fig. 16. SCRs are formed in CMOS integrated circuits by parasitic circuit elements formed as a byproduct of the standard production sequence. The SCR consists of a pair of bipolar transistors formed by the p substrate, n diffusion in p substrate, N-Well and p diffusion in N-Well, and resistors formed by diffusions. In the course of a voltage transient, such as an ESD event, one of the collector to base junctions breaks down, the resultant current will forward bias the emitter base junctions, and the bipolar devices can turn on. Base currents through the parasitic resistors can be sufficient to keep the two bipolar transistors on, even if the voltage across the SCR drops well below the initial breakdown voltage. The on voltage of an SCR can be very low. A schematic of an SCR current versus voltage curve can be observed in Fig. 17. The low voltage and low resistance of a turned on SCR make it a very attractive device for ESD protection. There are several disadvantages of the SCR. One is its relatively high turn on voltage. A variety of schemes have been developed to lower the turn on voltage of SCRs to increase their effectiveness as an ESD protection element. Another concern is that the device will be turned on during standard device operation. Finally the device's operation is sensitive to details of the integrated circuit technology, sometimes making it necessary to modify the protection elements for different manufacturing locations or when a circuit is manufactured in a more advanced technology. In practice, several manufacturers have been successful using SCRs as protection elements.

One of the biggest factors in the use of any of the above protection devices is correct layout of the protection circuitry. An n-channel thin oxide MOS transistor will be used as an example. N-channel MOS transistors can be the most sensitive devices to ESD on an integrated circuit. In some technologies, with proper layout, this potentially weak element can become a major part of the protection scheme

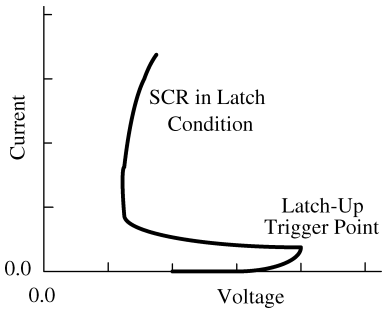

Figure 17. Schematic of the I-V curve of an SCR structure.

of the circuit. Fig. 18 shows a schematic of a simple output driver of a CMOS digital integrated circuit. The purpose of this circuit is to invert the signal, make high values low and low values high, and to provide the current drive capability to overcome wiring capacitance, so that the signal can reach its intended destination. To provide the current drive capability, both the p-channel pull-up transistor and the n-channel pull-down transistor must be wide, because the drive capability of MOS transistors scale with width. The needed large width for drive capability is a help for ESD protection because the ESD current can be sunk over a wider device, reducing current density. Proper layout is also needed. The n-channel devices will be considered in detail because the p-channel devices have inherently better characteristics for surviving ESD stress. Fig. 19 shows two possible top-down layouts for the n-channel pull-down transistor. Because of the large transistor width needed, drive transistors are usually laid out as multiple finger devices. To save space in the circuit's design, it would be desirable to have the contacts to the transistors as close to the transistor gates as possible as in Fig. 19a. Figure 20, however, shows TLP measurements of two single-finger transistors with different geometries. One has a contact to gate spacing of 1 μm on both the source and the drain sides, and the other has a contact to gate spacing of 3 μm on the drain side. The initial breakdown voltage and snapback voltage are not greatly affected by the contact to gate separation. The slope of the snapback region is reduced by the extra contact to gate separation, and the amount of current carried before the onset of second breakdown is increased. The most important result of these changes is the relative values of the voltage at which second breakdown occurs, V_{t2}, and the triggering of bipolar snapback, V_{t1}. For the 1 μm separation, V_{t2} is well below V_{t1}. The situation is reversed for the 3 μm contact to gate separation. The difference is important for transistors laid out as parallel fingers. If the voltage for the onset of second breakdown is below the junction breakdown voltage, it is possible for one finger of the transistor to experience the second breakdown without any of the parallel fingers conducting any current. If the voltage for the onset of second breakdown is above the junction breakdown voltage, all fingers will be triggered into snapback before any individual finger can experience second breakdown. A layout with a wide contact to gate separation on the drain side as shown in Fig. 19b will greatly increase the robustness of the multifinger transistor to ESD events and will make it an effective part

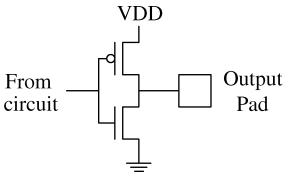

Figure 18. Circuit diagram of a simple CMOS output driver.

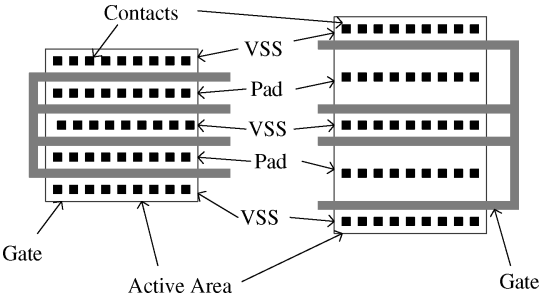

Figure 19. Layouts of nMOS transistors optimized for (a) Area and for (b) ESD robustness.

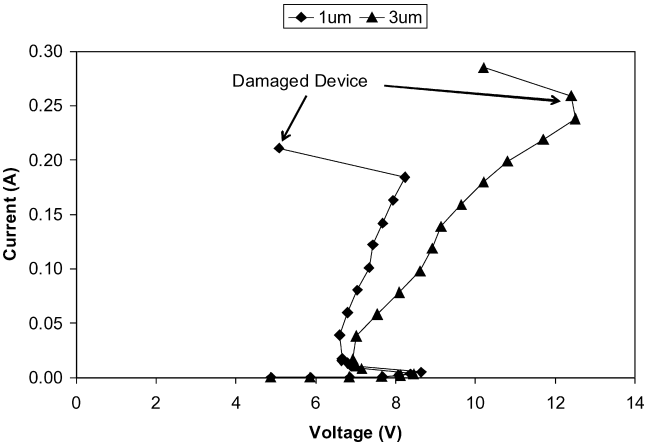

Figure 20. TLP I-V curves for two different nMOS transistor layouts.

of the overall protection strategy for the integrated circuit. The addition of resistance to the drain side of transistors is often referred to as drain ballasting. (The above discussion of contact to gate separation for the nMOS transistor assumes a technology without a silicide layer to reduce the source and drain diffusion resistance. In a silicide technology, a silicide block layer is often used to provide the benefits of the extra resistance provided by contact to gate separation. The width of the silicide block will be analogous to the contact to gate separation. Other techniques of drain ballasting include the use of n-Well resistors and poly-silicon resistors.)

In recent years there has been a trend away from using ESD protection schemes that rely on trigger mechanisms such as avalanche breakdown and conductance mechanisms such as bipolar snapback. It is often hard to predict the behavior of protection mechanisms that rely on junction breakdown and snapback. Junction breakdown and snapback are also mechanisms that are not routinely monitored, controlled, or specified in an integrated circuit

technology. This makes these protection mechanisms more difficult to transfer between technologies or different manufacturers. The result has been a trend toward protection strategies that use circuit elements within their normal range of operation. When this is done, ESD protection behavior can be predicted using the same simulation tools that are used in standard circuit design. One of the mainstays of this trend is the BigFET clamp shown schematically in Fig. 10c. A very large nMOS device, the BigFET, is used as the current carrying element in the clamp. The transistor is large enough that, when turned on, it can carry the full ESD current, without damage to itself, using standard inversion currents. The gate of the large nFET is controlled by a circuit that turns off the transistor during normal device operation but turns it on during an ESD event. In Fig. 10c, node 1 is held high in normal operation by the pull-up device. The inverter made up of the nMOS and pMOS transistors then holds node 2 low, keeping the Large nFET turned off. During a transient of VDD positive with respect to VSS, such as an ESD event, node 1 will be held low for an RC time constant determined by the capacitor C and the resistance R. Node 2 would then be held high for the same RC time constant, providing a low-resistance current path between VDD and VSS for the ESD current to follow.

ESD TRENDS

ESD will continue to be an active area of work as long as the electronic industry continues on the aggressive trend of increased miniaturization and higher functionality of electronic systems. As the challenge increases, the tools available to meet that challenge will grow. It is expected that there will be new simulation tools that will become available to aid in the design of protection circuits. The circuit simulation tools used for the design of integrated circuits and systems will be expanded so that they will be able to simulate ESD events, which allows much better prediction of ESD performance. It is expected that the trend to protection strategies using normal device operation modes such as the BigFET clamp will continue.

Two-and three-dimensional process and device simulation programs have become increasingly sophisticated in recent years, and with faster and less expensive computers, they have become an important tool in the development of new integrated circuit technologies. Process simulators are numerical simulators that solve the basic physical equations such as the diffusion equations and oxide growth equations and allow the prediction of the integrated circuit manufacturing process. Device simulators take the output of the process simulation and solve the electrical equations and predict the electrical performance of the transistors, resistors, and diodes that make up an integrated circuit. These simulation programs are providing increased understanding of what happens in circuit elements during an ESD event and in the future will provide predictive information on a new integrated circuit technology's ESD capabilities.

HBM has been the mainstay of ESD testing for many years, but as manufacturing procedures continue to migrate toward less and less direct human handling of circuits, CDM will be an increasingly important test method. The competitive pressures in the electronics industry have resulted in increased integration of functions onto a smaller number of components within systems. This has resulted in an increase in integrated circuits that have direct connection to the pins of system interface connectors for Firewire, USB, and Ethernet. The profusion of such interfaces and the desire to be able to plug and unplug these connections while a system is on has lead to a new ESD threat, the cable discharge event (CDE). A cable is dragged across carpet or through plenums in a building and becomes triboelectrically charged and is then plugged into a running system. The resulting discharge of the cable to the connector and then to the integrated circuit can cause system interrupt but can also cause permanent physical damage. It is expected that, within the next few years, a new standard will emerge to cover the CDE event.

It is an open question whether ESD could present a technical barrier to further miniaturization of electronic systems and therefore stop the trend of increasingly powerful electronic systems at lower prices. The breakdown voltage of gate oxides is falling below the breakdown voltage of diodes in advanced technologies. Protection strategies that rely on the avalanche breakdown of junctions are becoming ineffective. This makes protection strategies that use circuit design techniques a critical tool in ESD protection. It is clear, however, that success in meeting the ESD challenge is crucial to the success of any electrical system and the corporations that seek to produce them.

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