J. Webster (ed.), *Wiley Encyclopedia of Electrical and Electronics Engineering*

QUANTUM STORAGE DEVICES

The semiconductor industry has used the ability to develop smaller and faster devices to fuel the explosive growth in productivity and functionality of electronic products. However, as devices shrink below 0.1 μm in size, physical phenomena must be identified that can produce devices that work as well or better than the larger devices utilized over the last 40 years. In particular, quantum devices that work because of their small size, rather than in spite of it, become more attractive. It is critical to explore the potential of this new class of ultra-small devices.

The continued trend in the integrated circuit industry toward smaller individual devices (transistors) has actually become part of the financial structure of the industry. There is a focus in every area of device fabrication toward next generation technologies that scale (shrink) in a favorable way. Unfortunately, the resources and technology required to decrease minimum feature size in each generation of semiconductor devices continue to increase. Industry is now wrestling with fundamental physical device size limitations that threaten to limit further scaling. This suggests that new device building blocks need to be developed whose ideal size is in the new operating regimes. Many quantum phenomena evidence themselves most strongly in this sub-100 nm size range. This gives quantum devices, which may have no intrinsic scaling limitations, a potential role in the future of the industry.

Definition of Quantum Storage

Quantum storage cells are composed of a device or of several devices which depend on quantum confinement, tunneling, or an interaction between these phenomena and space charge or other effects. Preferably, quantum storage cells should be composed of a single device that has multiple, electrically distinguishable, stable states accessed through one line and set through another. To be useful these memory cells should have terminal characteristics which allow them to drive variable-length interconnects with acceptable noise margins and fan out.

Quantum storage-based memory may be volatile or nonvolatile, static or dynamic, as in other types of memory. Nonvolatile memory retains its memory state when power is turned off. Static random access memory (*SRAM*) is an example of volatile static memory. Dynamic random access memory (*DRAM*) is volatile and dynamic, requiring regular refresh cycles that consume significant amounts of power that must be dissipated as heat. DRAM is significantly slower than SRAM but it is often used because of its low cost and smaller memory cell size. There would be an enormous amount of interest in a device with SRAM performance at cost and densities of conventional DRAM. Quantum storage-based memory has the potential to accomplish this.

There are two methods of achieving quantum storage. One is to use logic devices whose operation is based on quantum phenomena to make memory circuits. The other is to use a single device that exhibits memory characteristics using quantum phenomena. It is difficult to imagine a single device that is robust enough to perform all of the functionality of a memory cell so most cases are a hybrid of these two methods. In either

case, there is a significant advantage in compatibility with established fabrication methods and with existing linear and digital electronics families.

Cellular Automaton. There are several examples of quantum phenomena-based logic which may be used to make memory. Lent and co-workers (1,2,3,4,5) have proposed a family of logic based on coupled quantum dots that can be used to make interconnect lines and perform basic logic functions. These are known as quantum cellular automata (*QCA*). It is tempting to design devices from low-dimensional structures, such as quantum dots whose charge is governed by quantization effects, particularly for digital logic. In order to be small enough to benefit from quantum confinement a quantum dot must be a few tens of nanometers in diameter or smaller. This makes it difficult to make physical contact between a quantum dot and a metal interconnect. The QCA is a suggested solution.

In this scheme each cell is composed of five quantum dots, as shown in Fig. 1. Each dot is about 20 nm across and 10 nm from its nearest neighbor. Interaction between cells is governed by Schrödinger's wave equation

$$H\psi = E\psi \tag{1}$$

$$\begin{aligned} H_0^{\text{cell}} = &\sum_{i,\sigma} E_0 n_{i,\sigma} + \sum_{i,j,\sigma} t_{i,j}(a_{i,\sigma}a_{j,\sigma} + a_{j,\sigma}a_{i,\sigma}) \\ &+ \sum_i E_Q n_{i,\uparrow} n_{i,\downarrow} + \sum_{i>j,\sigma,\sigma'} V_Q \frac{n_{i,\sigma} n_{j,\sigma'}}{|r_i - r_j|} \end{aligned} \tag{2}$$

where H is the Hamiltonian, $\psi$is the wave function solution, E is the energy eigenvalue, E_0 is the on-site energy which is the same for all sites, $n_{i,\sigma}$ is the number operator generating an electron at site i with spin σ, $t_{i,j}$ is the tunneling energy from site i to site j, and E_{Q} is the coulombic energy required to have two electrons of opposite spin on the same site. The interactions between cells are predominantly controlled by the coulombic perturbation between neighboring cells so that the Hamiltonian at cell 1 due to cell 2 is given by

$$H^{\text{cell}} = H_0^{\text{cell}} + H_{12}^{\text{cell}} \tag{3}$$

where

$$H_{12}^{\text{cell}} = \sum_{i,j,\sigma} V_Q \frac{\rho_{2,j} - \rho}{|R_{2,j} - R_{1,j}|} \tag{4}$$

where ρ is some assumed fixed positive charge to achieve space charge neutrality. The polarity of a cell may be defined as

$$P = \frac{(\rho_1 + \rho_3) - (\rho_2 + \rho_4)}{(\rho_1 + \rho_3) + (\rho_2 + \rho_4) + \rho_0} \tag{5}$$

where ρ_n is the charge at location n. This is the numbering scheme for calculating the polarization of each cell, and it has values in the range of -1 to 1. The lowest energy and preferred solution occurs when neighboring cells align themselves with the same polarization. If an initial polarization is supplied by a driver to a QCA quantum interconnect, within a couple of cells alignment to a polarization of 1 or -1 occurs and continues to subsequent cells (1).

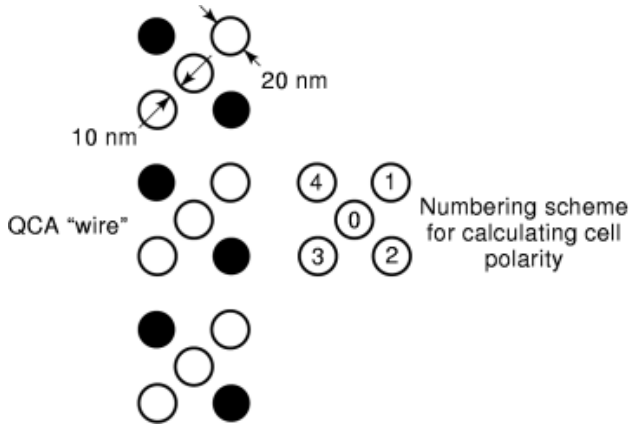

Fig. 1. Numbering scheme used to determine the polarity of a cell. In a QCA wire's lowest energy configuration, each cell has the same polarity.

A range of logic circuits has been designed using QCA including fundamental AND and OR gates as well as more complicated circuits like a full adder. It may be dangerous to make assumptions about the state of a cell when the polarizing effects of the driver are removed, say to infinity. Since work is done in reading the state of a cell the very act of determining its state may change the polarity of a cell or an entire QCA wire in an unpredictable way. In order to reliably achieve memory functions, a memory cell constructed of basic QCA logic elements must function without making any assumptions about the volatility of the data in each cell.

Figure 2 shows an SR latch composed of two NOR gates constructed from QCA logic. One NOR gate is outlined for reference. The cell size is about 0.3 μm by about 0.4 μm. This quantum dot-based SRAM cell is comparable in size to current conventional DRAM cells.

A more critical assessment of this logic family should, however, be considered. For instance, the thought experiment used to determine how the QCA operates is carried out at $T = 0$ K. The devices could be tested at 4 K but would probably have to work at least at 77 K (liquid nitrogen) to be useful. In addition, for space charge neutrality there must be a charge of $+2q$ (where q is the magnitude of the charge of an electron) on each cell. This suggests precise placement of exactly two donor dopant ions in each cell would be required. Unfortunately, current doping processes always produces a distribution of dopant atoms. Expected statistical variations in doping would significantly change the electrical characteristics of each cell. Finally, although direct write methods of photolithography do have the resolution required to create these patterns of dots, these methods have not been used for production. At the time of this writing QCAs have not been demonstrated in the laboratory.

Resonant Tunneling Diode-Based Memory. Another example of a novel family of logic that may be used to create memory is based on resonant tunneling diodes (*RTD*s). RTDs are ultrahigh frequency, generally two terminal, majority carrier devices composed of a heterostructure quantum well usually built from III/V materials using *MBE* (molecular beam epitaxy). The quantum well is usually on the order of 5 nm in width, formed by sandwiching a low conduction/valence band offset material (e.g., GaAs or $In_xGa_{1-x}As$) between barriers made of high conduction/valence band offset materials (e.g., AlAs). These devices are characterized by an "N"-shaped current–voltage (*I*/*V*) curve with a peak in current when the bias aligns a large carrier population at the contacts with a resonance in the well (6). A valley in the *I*/*V* curve occurs when the applied bias aligns a very small carrier population in the contacts with resonances in the quantum well. Hence, the *I*/*V* curve of these devices may have negative differential resistance (*NDR*); an example of the *I*/*V* curve of a typical AlAs/InGaAs RTD is shown in Fig. 3. Since transport is ballistic, to the first order, carriers do not scatter from

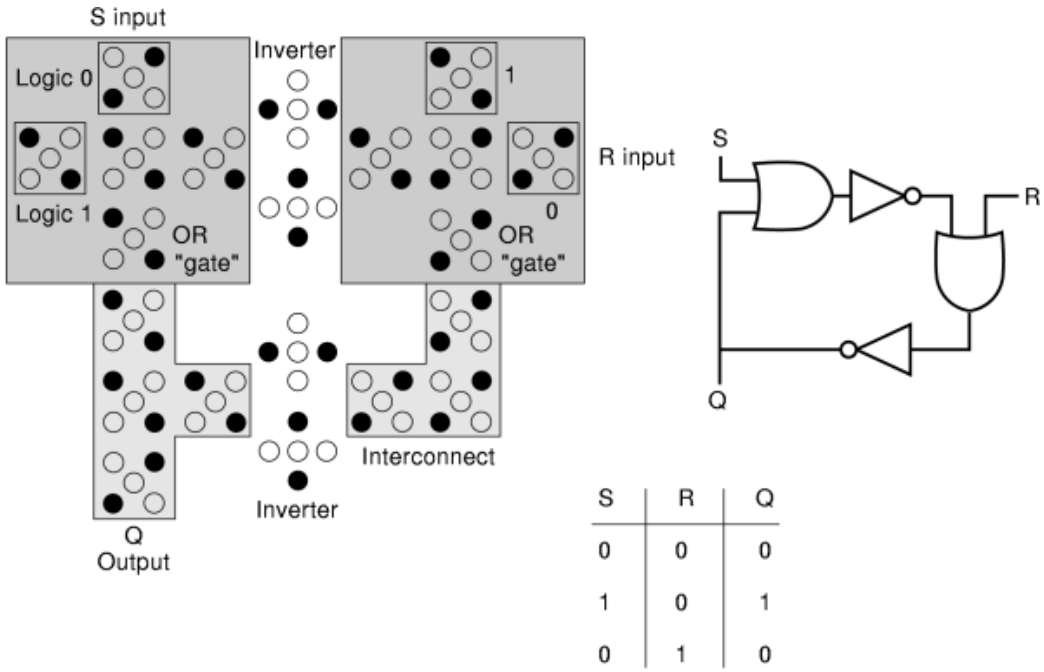

Fig. 2. QCA-based SR latch (8) divided into functional units: A full logic family may be constructed.

one energy to another. Tunneling through a quantum well is a quantum phenomenon typically producing peak currents in the hundreds of kiloamperes/cm^2. In contrast, if classical physics is used to analyze these devices essentially no current would flow at all. Operating by ballistic transport they may be assumed to be, and are, high-speed devices.

The switching characteristic used to achieve memory operation from RTDs can be divided into three categories. The first category is load line switching, where more than one intersection may occur between the *I/V* characteristics of a nonlinear device and the load line. The history of the operation of the device governs which of these intersections is the operating point. This may be used to make logic. The second category is intrinsic bistability which occurs in some devices where charge is stored in the device during rising bias and removed during decreasing bias. This induces a hysteresis loop in the *I/V* curve, producing two possible operating voltages at a given current. Both load line switching and intrinsic bistability produce volatile memory. A third category, memory switching, refers to a case in which there are two stable states maintained with no power dissipation and without input, and hence, is nonvolatile. Any of the discussed approaches might be used to create memory devices since they provide multiple operating voltages at the same current dependent on prior history.

Load Line Switching and Intrinsic Bistability Devices. A number of attempts to make fast RTD-based logic devices have been made (7) that are based on load line switching. Load line switching RTDs maintain their state only while under load. Unfortunately, as isolated devices they generally have poor terminal characteristics. Various schemes have been used to overcome these shortcomings by adding conventional devices to the memory cell. A representative approach is shown in Fig. 4 (8). This design from Texas Instruments employs "ultra-low" current density RTDs that dissipate 50 nW of standby power. These devices are constructed in the InGaAs/InAlAs and InP materials system. *HFET*s (heterostructure field effect transistors) are used for the switching transistors. This cell does not require a refresh cycle, giving the functionality of an SRAM cell

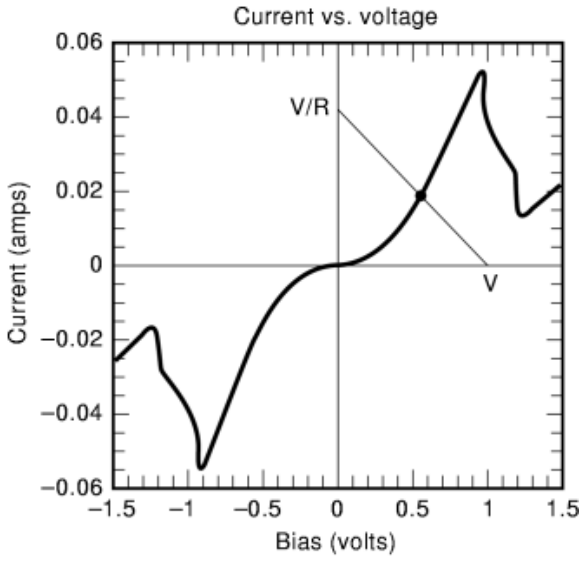

Fig. 3. RTD *I/V* curve. The peak current is about ±0.9 V and the valley is about ±1.2 V. An example load line is shown with drive voltage V and resistance R. The intersection (large dot) between this load line and the *I/V* curve of the RTD is the operating point. Multiple intersections between the two curves occur for a range of values of V (and R).

while occupying an area comparable to a DRAM cell. Access times below 0.5 ns have been demonstrated. This architecture lends itself to vertical integration that aids in achieving high density. Multiple valued logic can also be achieved by using cascaded RTD structures. The device count to perform basic logic functions is much lower than a standard SRAM cell (typically six transistors). Variations on this scheme use cascaded RTDs to achieve multilevel logic and intrinsic bistability (9,10).

Memory Switching. Memory switching is less developed in RTD research for making memory cells. A number of nonquantum memory switching devices have been reported in the literature. Since they are nonvolatile and static the device count to create functional memory cells is very low. Langmuir–Blodgett film/metal sandwiches, for instance, show conductivity changes due to light irradiation or applied voltages (11). For electrically switchable metal/film/metal structures a preliminary high voltage is applied as a forming procedure; these devices then display memory switching characteristics. A film thickness of 18 nm has been used and the off-state resistance is 10^6 Ω while the on-state resistance is 20 to 100 Ω. The structure of the film may actually change during switching to cause this phenomenon. This device is simple to fabricate and is not necessarily incompatible with standard silicon fabrication procedures. One negative possibility is that switching is due to filamentary pathways. Sandwiches of metal/SiO_2/metal have also been observed to show memory effects after a similar forming procedure, but these have been attributed to highly conductive filamentary pathways of heavily doped silicon which form and are destroyed during switching (12).

Typically, observations of memory switching are difficult to explain. Charge trapped in interface layers at a metal/semiconductor boundary can result in memory switching. Such devices are generally not useful because they are difficult to reproduce. In any case, two terminal devices that change resistance when a voltage is applied are difficult to use without supporting active electronics. For instance, on/off state resistances must not be ambiguous when observed through an interconnect of varying length/resistance to any particular memory cell.

Flash memory is a conventional type of memory that attempts to use trapped charge in a reproducible way. In this device a floating gate accumulates charge that affects the source drain current characteristics of

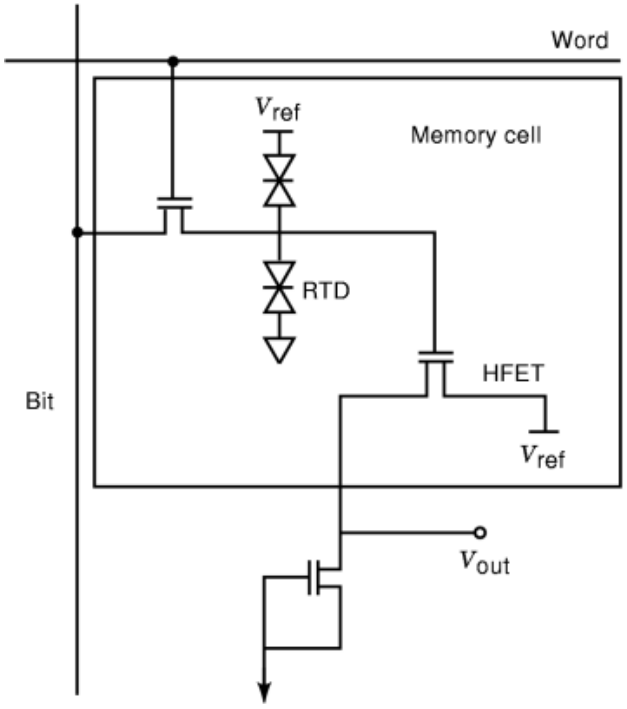

Fig. 4. Proposed memory cell. The transistors are HFETs and the bidirectional diodes are RTDs. Bit and word lines allow random addressing of each memory cell.

the device. In the *EEPROM* (electrically erasable programmable read-only memory) hot electrons are used to reset the memory state of the device. They do have comparatively very long write times and some long-term deterioration with the number of write cycles. Even so, for a variety of applications these are very useful devices.

A flash memory cell which accumulates charge on a floating quantum dot above the channel has been built by IBM (13). This device is an excellent example of the concept of a quantum device whose operating principles become more favorable as it becomes smaller. The change in threshold voltage (ΔV_t) resulting from charge trapped in the quantum dot increases as the quantum dot size decreases. This device is interesting because it has very small off currents in the 10 pA range, small operating voltages, and potentially excellent scaling characteristics. It is not clear whether write times, which have always been the major drawback for electrically erasable flash memory, will improve in this design.

Quantum Storage Device. Gullapalli and Neikirk have proposed a method to engineer charge trapping in an attempt to build a memory switching device. The *QSD* (quantum storage device) is a modified quantum well diode that relies on the interaction of a quantum well region with $N^-/N^+/N^-$ doped layers to achieve multiple conduction states (14,15,16). Unlike other multiple state quantum structures, the QSD has different current versus voltage curves corresponding to the different conduction states. Preliminary experimental findings indicate that these states remain stable even under short circuit conditions and can only be switched from one state to another with the application of bias in excess of certain threshold voltages. Furthermore, calculations using a self-consistent coherent tunneling model indicate that it is possible to design QSD cells with more than two states, creating the possibility of multistate logic and multibit storage (15,16,17).

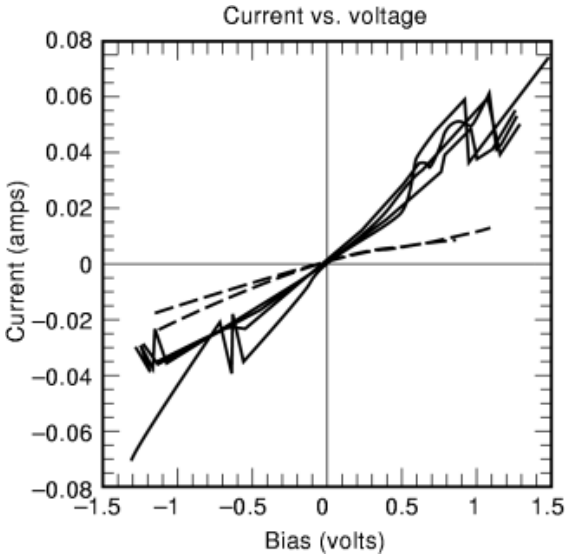

Fig. 5. *I/V* curve for a QSD showing four cycles of the memory switching operation. The two curves are multiple solutions for the same device. These solutions are accessed by applying a switching voltage of about ±2.0 V to the terminals.

QSDs are functionally dissimilar to Shockley diodes or thyristors, which also change resistance at a break over voltage but return to the original resistance at low voltage. The distinct differential resistance corresponding to each state in a QSD is retained even at zero bias until another switching voltage is applied, at which point it changes to that associated with the other state, as shown in Fig. 5.

This multi-state behavior has been shown to occur in two terminal devices with a thin heterobarrier structure in close proximity to $N^-/N^+/N^-$ doped layers. For instance, a double barrier structure consisting of a thin, lightly doped *n*-type GaAs layer surrounded by thin AlAs barriers has been used. The double barrier quantum well structure is then placed within a few nanometers of an $N^-/N^+/N^-$ doped GaAs structure that itself forms a shallow quantum well. The doping sequence is crucial to device operation. Only devices with quantum interference between a barrier structure and a well with a highly variable charge distribution show evidence of multiple conduction curves. In particular, conventional *DBRTD*s (double barrier RTDs) with monotonically doped layers show no evidence of multistate behavior.

The device possesses memory, in that once the device is placed in one state it will remain in that state over a wide range of bias voltages, including zero bias (i.e., the multiple states exist even at zero bias). Once the device is placed on one branch of its *I–V* characteristic, it will remain on that branch at zero bias. The state of the device at zero bias (which can be sensed via the value of its differential resistance), is determined by whether the device was last switched to the high current curve or to the low current curve. Even when the device is completely disconnected from the bias supply, or its terminals are short circuited, upon reconnection the differential resistance is unchanged from its preset value. In this sense, the device possesses memory of its state, that can be retained without requiring any bias or dissipating any power. Simulations suggest that multistate behavior occurs in other structures including single and triple barrier devices as long as a $N^-/N^+/N^-$ doped layers are in near proximity to the heterobarrier.

The potential advantages of the QSD over existing technologies are significant. First, the QSD can be scaled down to the limit of the photolithography system. From initial findings, it appears that the cell should work at mesoscopic geometries creating the possibilities of extremely high-density memory or logic. However, unlike mesoscopic systems which require milli-Kelvin temperatures, the QSD has the advantage of operating

at room temperature. Furthermore, there is a possibility that the QSD can serve as static, nonvolatile memory element or logic device with zero holding power, since the multiple conduction states are stable for extended periods of time even when completely disconnected from any power supply. Finally, since the QSD is a simple two-dimensional structure, memory cells may be stacked on top of each other. This fact, coupled with the possibility of more than two conduction states per cell, offers other possibilities of achieving very high densities.

There are several problems that must be overcome before the QSD can be a viable alternative to conventional memory. First the switching characteristics of the two terminal devices built to date are poor: write currents are high, and on/off resistances are at best differ by a factor of two. Resistive memory elements require supporting electronics to make viable memory cells, as in Fig. 4. The devices that have been made so far have been in the GaAs/AlAs materials system which is costly and difficult to integrate with conventional silicon technology. Attempts have been made to develop a three terminal version by making direct contact to the N^+ layer (18) that may overcome some of the deficiencies in present devices.

Summary

In each technology generation, scientists and engineers are called on to help identify the directions of the next generation. The technology to make the next generation of devices, however, by definition does not exist. Determining which developments will thrust any particular technology into the forefront is obviously difficult. At any particular instant it is important to be aware of the short comings of proposed new technologies without assuming these difficulties will necessarily be fatal ones. With this in mind, a critical assessment of the new quantum technologies discussed herein should be considered (19).

In some schemes new, novel devices are used in memory cells containing conventional devices in order to improve functionality. It is important to note that the fundamental size limitation of a cell is determined by the largest device in the cell. Although lower device counts would be extremely important, the cell size decrease possible without fundamental changes in the technology of all the components is limited to a few generations.

Even given advances in device technology, interconnects are becoming an increasing bottleneck in performance. Although they have not been built, Lent's QCA *wires* may pose a solution to interconnect limitations. Interconnect problems may also be mitigated by moving components closer together. For instance, the main advantage of smaller SRAM would be the inclusion on a central processing unit of large amounts of fast memory, eliminating or reducing caching requirements and reducing interconnect lengths. This would require a compatible materials system with the CPU technology, which may in some cases be difficult to achieve. In any case, as we go to smaller devices, design assumptions must take into account statistical variations inherent in using nanostructures (20).

Regardless of the problems inherent in developing quantum devices that work because of their small size, their potential to provide new generations of technology still warrants extensive study. The first steps toward implementing real logic and memory circuits have already been taken, and in the near future their contributions to future electronic systems should become clear.

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