TERNARY SEMICONDUCTORS

High efficiency, Cu(In,Ga)Se_2 (CIGS)-based photovoltaic (PV) devices have been fabricated by four different processes. Each process may be characterized as either sequential or concurrent deposition of the metals, with or without an activity of Se. A world-record, total-area efficiency of 17.7% has been achieved by the concurrent delivery of the metals in the presence of Se. Ga has been introduced into the device, in a such a manner as to produce homogeneous, normal profiling, and double-profiling graded band gap structures. This has resulted in an open-circuit voltage (V_{oc}) parameter of 680 mV, and a fill-factor over 78%. The quality of CIGS-based films and devices is becoming decoupled from the method of film delivery. This leads to novel, fast, and low-cost methods for absorber fabrications. Two such deposition techniques, sputtering and electrodeposition, will also be discussed, and results to date will be presented. Finally, a fabrication model has been developed, allowing for simple translation of these processes to a manufacturing environment for the large-scale production of modules.

The National Renewable Energy Laboratory (NREL), under contract to the United States Department of Energy, has been involved in the research and development of thin-film PV since 1982. The primary charter of the Photovoltaics Program is to develop new and better PV technologies, and to support industry in doing the same. The goal is to introduce PV as a cost-effective alternative to conventional utility power generation. This goal is accomplished by an approach that first considers basic materials research, followed by solar cell development, and concludes with technology transfer to industrial organizations and market development.

To establish cost effectiveness in PV technology, both performance and cost are considered. Solar cells and modules fabricated from polycrystalline CIGS-based thin films are strong candidates for high performance and low cost (1). Laboratory-scale device efficiencies in excess of 15% have been reported by several groups (2–4). The low-cost criterion is satisfied for most thin-film technologies through low materials usage, monolithic integration, and low manufacturing costs, to name a few. Several industrial groups have produced large-area (sub)modules with performance in excess of 7% (5,6). One company has successfully produced a 10% module, with an aperture area near 4000 cm^2 (4). In this work, laboratory-scale device absorbers are fabricated by physical vapor deposition (PVD) processes, which may be conducive to industrial scale-up (7,8). An additional advantage for the thin-film CIS technology developed at NREL is the potential for high yield through greater-than-average process tolerances and self-limiting process chemistry.

In this work, device performance and manufacturability issues will be discussed. This work is supported by extensive fundamental materials research, which is reported elsewhere in the literature (9–16). Four PVD absorber fabrication processes are currently being investigated. The associated champion device performance ranges from 12.6% to 17.7%. In each case, the process is described in a fashion that allows for transfer to industrial-scale deposition systems (17). Growth models have also been developed to describe the formation chemistry (9). The incorporation of Ga to raise the absorber band gap has been accomplished successfully and in such a manner that a V_{oc} of 680 mV has been accomplished (8). The higher V_{oc} and lower J_{sc} translate into lower interconnect losses at the module level.

This article presents a generic flowchart for the fabrication of CIGS absorbers, which takes into consideration the critical processing parameters. By breaking the process into stages, there are clear opportunities to use a variety of deposition techniques separately and to reduce the time of processing segments, as well as introduce intelligent process control.

EXPERIMENTAL

CIGS thin films are grown by physical vapor deposition (PVD) of the constituent elements under a vacuum of 10^{-8} Pa ($^a10^{-6}$ Torr) onto 5 cm × 5 cm (2 in. × 2 in.) Mo-coated soda-lime silica (SLS) glass. The PVD process may consist of coevaporation of the four elements simultaneously, sequential evaporation of the metals, followed by exposure to a Se species, or sequential evaporation of the metals in the presence of Se. Some details of the process specifics will be provided later in this article. Control of the Cu, In, and Ga fluxes is accomplished by electron impact emission spectroscopy (EIES) of the vapor trail and of the Se flux by quartz crystal monitoring (QCM). Substrate temperatures of 300° to 600°C are achieved by heating from quartz-halogen lamps or resistive heating. Warping of the SLS substrate at temperatures above 500°C was minimized by the appropriate combination of SLS glass type and thickness and Mo film deposition parameters. In many cases, an intentional compositional gradient of about 2 at.%Cu was introduced across the 5 cm dimension, in order to study material and device variations as a function of composition. Films were also deposited by sputtering and electrodeposition. The experimental details are given elsewhere (18,19).

PV devices are completed by chemical bath deposition (CBD) of about 500 Å of CdS, followed by RF sputtering of 500 Å of intrinsic ZnO and 3000 Å of Al-doped ZnO. The CBD process has proven to be the only successful means of delivering a thin, conformal layer of CdS to the surface of the absorber. Several groups are looking at the role of CdS in the device (18), while others are looking to replace the CdS with a non-Cd-containing layer buffer layer by either chemical (19) or physical (20) deposition means. Ni/Al grid contacts are applied with approximately 4% coverage. I–V characterization is carried out at AM1.5 illumination, and device efficiencies are quoted as "total-area" to include grid losses. Quantum efficiency measurements are made in the dark, and under voltage and light bias in the wavelength range 380 nm to 1500 nm.

PVD PROCESS DESCRIPTION

The absorber fabrication process is defined by a variety of parameters. These include time-dependent profiles of the total Cu, In, Ga, and Se metal fluxes (deposition rate) in atoms/cm^2-sec (Å/s), Cu/(In + Ga) metal flux ratios, Se/(Cu + In +

Ga) flux ratios, and substrate temperature. In Fig. 1, flux profiles for the fabrication of $Cu(In,Ga)Se_2$ are shown for three such processes (17). The total metal flux determines the overall growth rate of the thin-film, which is about 15 Å/s. For processes where the metals are delivered sequentially in the presence of Se [Fig. 1(a)], "material delivery" may be accomplished much faster than "compound formation," resulting in "effective" growth rates. In future work, efforts may be to push the envelope on these delivery and formation rates, in order to minimize total deposition time, a significant manufacturing issue. The Cu/(In + Ga) metal flux ratio controls the formation chemistry during growth and, hence, the resulting microstructure and electronic quality. The Se/metal flux ratio is held above the lower limit established for the formation of stable binary and ternary phases during growth. The ratio is typically 3 : 1 for the ternary, 5 : 1 for the (In, Ga) : Se binaries, and 3 : 1 for the Cu : Se binaries. The Se overpressure is required to produce a filled anion sublattice and, thus, a valent-neutral semiconductor. The substrate temperature governs the adatom mobility and the phase nature of the binary and ternary constituents during growth.

One way to visualize the formation of the compound from its constituent elements is to consider the Cu–In–Se ternary phase diagram (Fig. 2). At first glance, it simply appears as if stoichiometric amounts of Cu, In, and Se can be added together in any manner to produce the ternary compound. This is not the case. Instead, the "chemical reaction path" is described in terms of a formation chemistry, which is driven by thermodynamics (12,23) and kinetics. For example, in the selenization process (Fig. 2, point 1, and Table 1, part 4), there is a clear separation of the metal and selenide deposition steps. During the metal deposition, Cu and In interact to form Cu-rich and In-rich alloys (24). Upon the introduction of the Se species, In_ySe and Cu_xSe binaries precede the $CuInSe_2$ (CIS) formation. The exact nature of the binaries is dependent upon time, temperature, and whether elemental Se or H_2Se gas is used as the Se source (13). In Table 1, the processes are described pictorially, with a suggestion as to the possible chemical reaction path leading to the compound. Here the process issues that are attractive for manufacturing are highlighted.

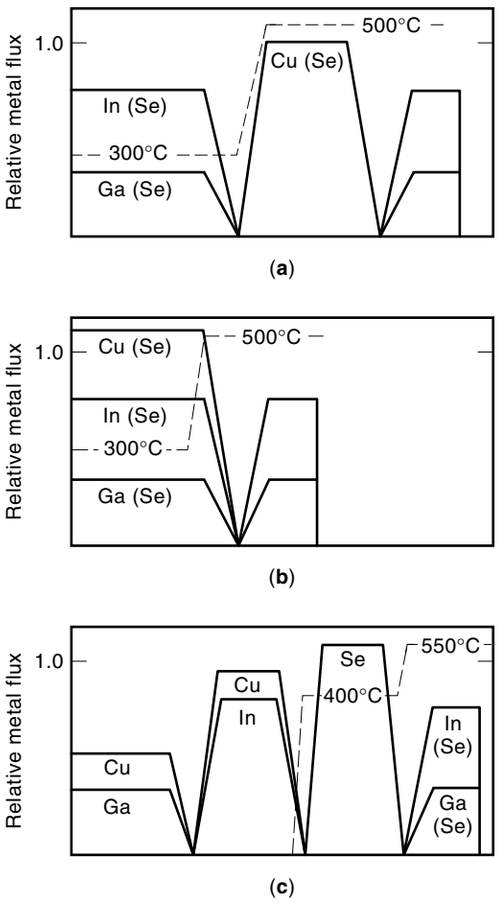


Figure 1. Source flux profiles for the (a) 3-stage, (b) 2-stage, and (c) Se-vapor selenization processes.

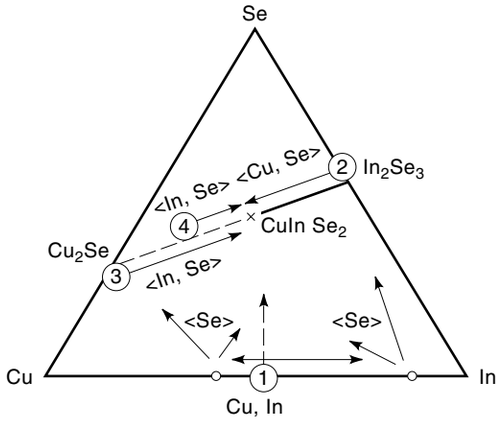
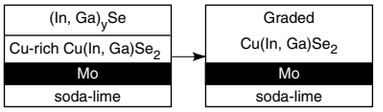
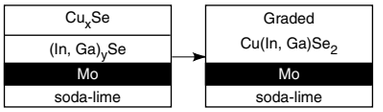
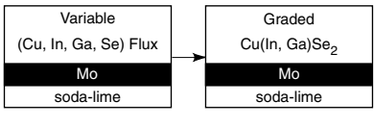
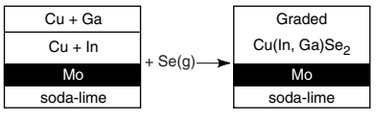


Figure 2. Cu–In–Se ternary phase diagram with suggested chemical reaction paths to the CIS product.

RESULTS AND DISCUSSION

The authors' laboratory has investigated several absorber structures based upon the $Cu(In,Ga)Se_2$ material system: (1) homogeneous CIS (E_g = 1.0 eV), (2) CIS on a $CuGaSe_2$ (CGS) buffer layer, (3) homogeneous CIGS (E_g = 1.0 eV to 1.14 eV), (4) graded CIGS (E_g = 1.0 eV to 1.7 eV) with a normal profile, and (5) graded CIGS with a double profile. These are represented pictorially in Fig. 3 as a depth profile of the semiconductor band gap. A discussion of the rationale behind these absorber designs is presented elsewhere (8,25). In Fig. 4 and Table 2, the current-voltage (I–V) and quantum-efficiency (QE) results are presented for representative cells fabricated by the above-mentioned processes. The 17.7% total-area device performance level represents the NREL-confirmed world record for all polycrystalline and amorphous thin-film technologies (26). The authors have, furthermore, reported a 1 cm^2 cell at 16.4% with very high V_{oc}, a 4.85 cm^2 cell at 15.3%, and a 0.074 cm^2 cell operated under 22-sun illumination at 17.7%, a 2.8% absolute improvement over the 1-sun control (2). The exceptional parameter among theses cells is a 1-sun V_{oc} value of 678 mV. This has positive implications for module

Table 1. Description of Absorber Processes Utilized to Fabricate CIGS Absorbers

Pictorial Description Start ⟶ Finish	Chemical Reaction Path	Manufacturing Issues
(1) **17.7%**–Concurrent delivery of the metals in the presence of Se (2-stage)		
	• Cu + (In, Ga) + Se **500°C** ⟶ $Cu(In, Ga) + Se_2 + Cu_xSe$ • CIGS : Cu_xSe + (In, Ga) + Se **500°C** ⟶ **$Cu(In, Ga)Se_2$**	• Stage 1 Cu-rich precursor can be easily synthesized • Stage 2 conversion does not require Cu
(2) **17.1%**–Sequential delivery of metals in the presence of Se (3-stage)		
	• $(In, Ga)Se_x + Cu_xSe + Se$ **500°C** ⟶ $Cu(In, Ga)Se_2 : Cu_xSe$ • CIGS : Cu_xSe + (In, Ga) + Se **500°C** ⟶ **$Cu(In, Ga)Se_2$**	• Separates Cu and (In, Ga) delivery • Simplifies *in situ* process control • Conducive to large-area deposition technology
(3) **15.1%**–In-line / Variable Flux Process (1-stage)		
	• Cu + (In, Ga) + Se **500°C** ⟶ $Cu(In, Ga)Se_2 : Cu_xSe$ • CIGS : Cu_xSe + Cu + (In, Ga) + Se **500°C** ⟶ **$Cu(In, Ga)Se_2$**	• Designed for in-line, continuous, large-area deposition • Process design flexibility
(4) **12.6%**–Sequential delivery of metals without Se followed by compound formation in Se vapor (2–3 stages)		
	• Cu, In + Cu, Ga $Cu_xIn + Cu_yGa + Cu + In + Se$ **300°C** ⟶ $Cu_xSe_2 + (In, Ga)_ySe + Se$ **450°C** ⟶ **$Cu(In, Ga)Se_2$**	• Separates deposition processes from thermal/chemical processes • Utilizes established large-area metal deposition technology

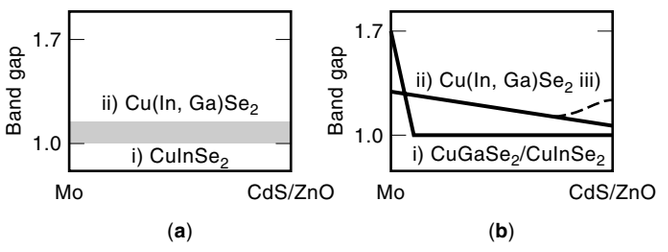
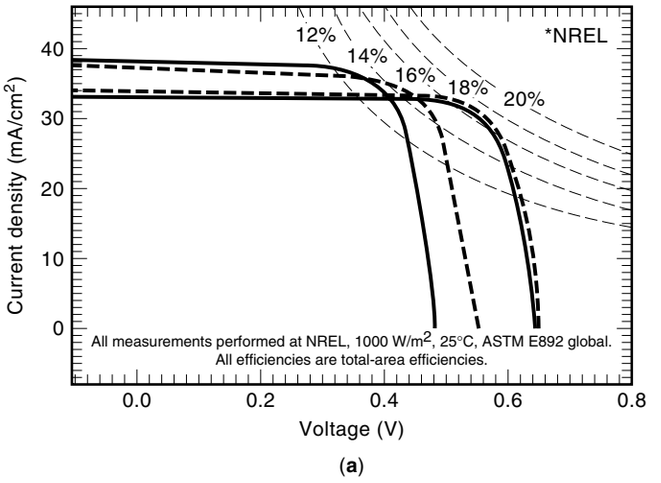


Figure 3. Pictorial of band gap variation in CIGS absorber bulk. (a) Homogeneous i) CIS and ii) CIGS, (b) graded band gap i) CIS on CGS, ii) CIGS with a "normal" profile, and iii) CIGS with a "double" profile.

fabrication, in that interconnect and series-resistance losses will decrease with larger cell widths and smaller operating currents, respectively.

Variations in performance are a result of both process and design variations. In Fig. 4 and Table 2, device (a) is a homogeneous CIS absorber, device (b) is a CIS absorber grown on 2000 Å of CGS, and devices (c) and (d) are CIGS absorbers grown on a CGS buffer layer. Devices (b) and (d) were grown by process (1) in Table 1 (2-stage), while all others were grown by process (2) (3-stage). Note the improved spectral response and enhanced V_{oc} in the CIS device incorporating the CGS buffer layer at the Mo back electrode [Fig. 4(b)]. Only trace amounts of Ga are detected near the absorber surface in this device, suggesting a band gap effect unrelated to alloying. This phenomenon is currently under investigation.



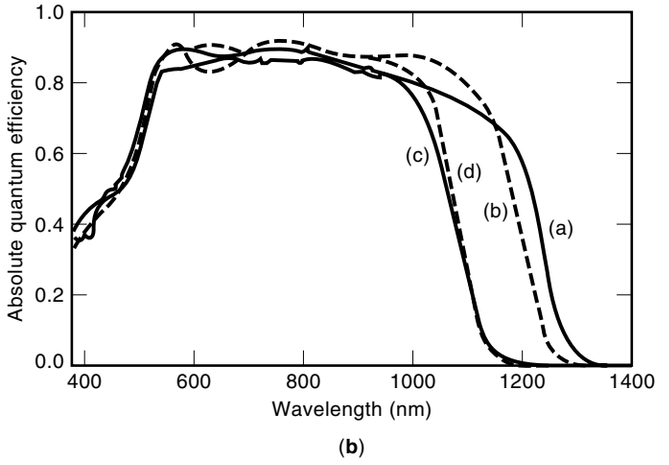


Figure 4. *I–V* (a) and quantum-efficiency (b) measurements of CIGS-based device structures.

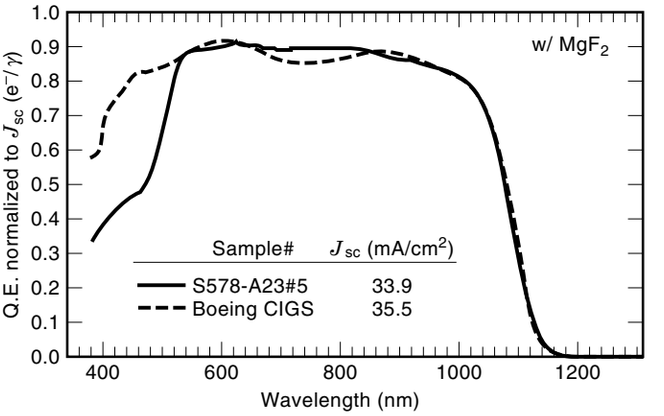


Figure 5. External quantum efficiency comparison of two high-efficiency CIGS-based solar cells.

The details of the relationship between the intended device structure and the resulting $Cu(In,Ga)Se_2$ phase distribution in the absorber continue to be investigated (8,14,27). In general, the homogeneous structures are straightforward to fabricate and characterize. The spectral response and V_{oc} are mutually consistent with the band gap of the absorber. This is not the case for the graded-band-gap absorbers. Growth of the absorber within the $Cu(In,Ga)Se_2 : Cu_2Se$ two-phase region for any period of time will enhance grain growth and In,Ga interdiffusion. Likewise, the more arduous the path from the metal constituents to the final compound, that is, $(In,Ga) \rightarrow (In,Ga)_ySe \rightarrow Cu(In,Ga)Se_2$, the more likely In and Ga will spatially polarize. Finally, the film roughness is influenced by both the degree of excess Cu and by the surface roughness of intermediate film layers that are present during growth. Smooth, specular films are desired, in order to minimize junction area, although reflection losses may be enhanced.

Absorber optimization will result from smooth surfaces and a controlled (In,Ga) profile throughout the absorber. Device optimization will result from improvements in the short-wavelength response (500 nm). Comparison of the spectral response of the authors' best cell with a champion Boeing cell (28) (Fig. 5) indicates room for improvement in the short-circuit current density (J_{sc}) with modifications to the window-layer processing. Combining the best parameters of cells with the high J_{sc} yields an 18.7% total-area performance level.

PROCESSING CHALLENGES

One difficult issue that is being addressed is irreproducibility associated with changes in the Mo/SLG substrate system.

Table 2. Summary of Device Performance for Champion Cells Made with Different Absorber Structures by Various Processes.

Sample	Area (cm^2)	V_{OC} (mV)	J_{SC} (mA/cm^2)	FF (%)	Total-Area Efficiency (%)	Comments
M1201	0.395	484	36.3	75.1	13.2	4 (a), CIS
S573	0.413	552	37.1	72.1	14.8	4 (b), CIS/CGS
C362	0.437	652	33.2	77.4	16.8	4 (c), CIGS/CGS, double
S773	0.414	674	34.0	77.2	**17.7**	4 (d), CIGS/CGS, normal
C371	1.025	**678**	32.0	75.8	16.4	CIGS/CGS, double
C371	**4.85**	657	31.1	74.7	15.3	CIGS/CGS, double
S773	0.103	**714**	**628.4**	78.6	**17.7**	CIGS/CGS, double, 20-sun

4(a–d) refers to Fig. 4. "Double" and "normal" refer to the realized band gap profile. All I-V data are derived from official NREL measurements.

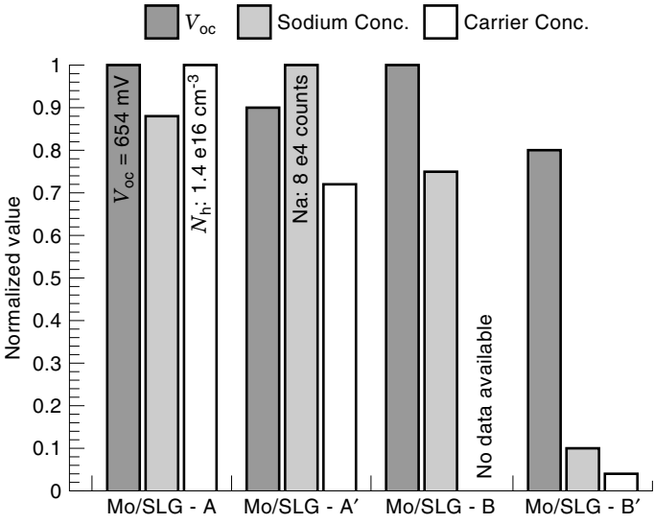


Figure 6. Variation of V_{oc}, carrier concentration (N_h), and Na content with substrate type and history.

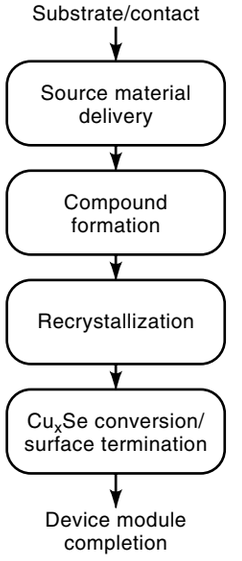


Figure 8. CIGS absorber fabrication process flowchart.

The irreproducibility may be characterized by a long time-constant, which is related to process variations from one supplier, or a very short time-constant, resulting from parallel processing of substrates from different suppliers. This issue has been investigated by a combined effort of material and device characterization. In Fig. 6, the results of a matrix experiment are presented, whereby two sources of Mo/SLG substrates, A and B, from two time periods, past and present (A and A′, B and B′), are processed into CIGS absorbers and devices. I–V and C–V measurements are performed on the devices to determine V_{oc} and the carrier concentration, N_h, at zero bias, respectively. SIMS analysis is performed on absorber and Mo layers prior to device fabrication to quantify elemental (constituent and impurity) profiles. Devices fabricated from A and B were of very high quality at 17.7% and 16.8%. A′ and B′ were processed simultaneously.

Two conclusions can be drawn from these data. The first is that there is a relationship between the sodium (Na) concentration within the absorber and the resulting N_h and V_{oc} of the device. The second is that there is a level of consistency over time in the substrate A and inconsistency in B, in terms of the Na migration from the substrate to the absorber film.

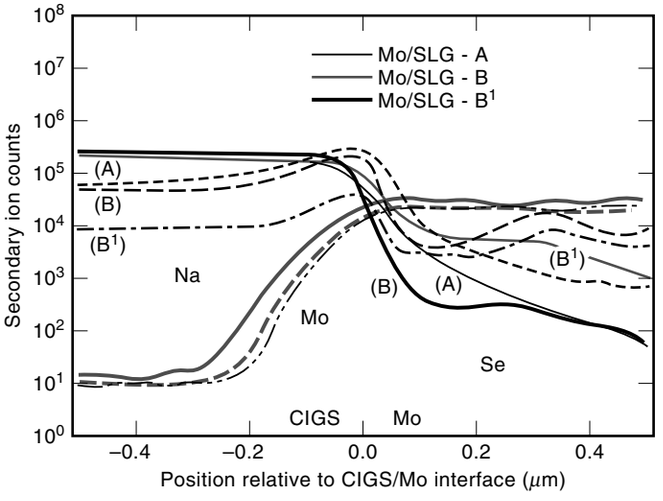


Figure 7. SIMS analysis of CIGS/Mo interface. Sample B′ has a greater than ten times the Se content in the Mo back electrode.

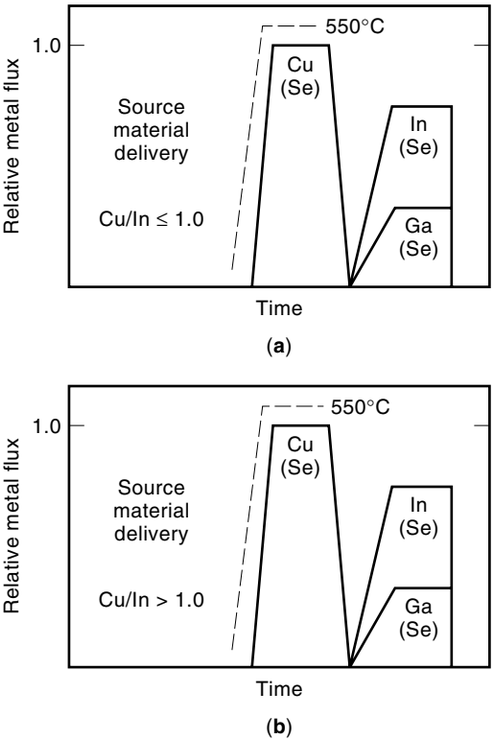


Figure 9. Alternative "fast" CIGS absorber fabrication processes.

Table 3. Device Parameters Resulting from Alternative Processing of CIGS Absorbers

Process	V_{OC} (mV)	J_{SC} (mA/cm^2)	FF (%)	η (%)	Comments
Evaporation	623	32.9	75	15.3	**CIGS** + (Cu, Se) + (In, Ga, Se)
Evaporation	605	31.4	73	13.9	**CIGS:CS** + (In, Ga, Se)
Sputtering	508	24.3	57	7.0	**CIGS** + Cu + Se + (In, Ga, Se)
Electrodeposition	689	27.7	71.6	13.6	**CIGS:CS** + (In, Ga, Se)

SIMS analysis (Fig. 7) of the CIGS/Mo/SLG stack suggests a possible cause of this phenomenon. Samples A, A′, and B contain equivalent amounts of Na and a sharp transition between the CIGS and Mo layers (as measured by the simultaneous drop and rise in the Se and Mo signals, respectively, at the CIGS/Mo interface). Sample B′, on the other hand, suggests the presence of a Mo_xSe interlayer between the absorber and Mo. This sample contained an order of magnitude less Na in the absorber and, with it, an associated decrease in N_h and device V_{oc}. It can be concluded, therefore, that the nature of the Mo surface, and its reactivity with Se, can substantially influence the characteristics of the absorber and the performance of the device. Future work will focus on characterizing the Mo surface and identifying the characteristics that lead to this performance.

NEW DIRECTIONS

The next-generation CIGS-based thin-film device will ideally have the following characteristics: The back contact and substrate combination will offer superior reproducibility to the present Mo/SLG system through controlled introduction of required impurities (e.g., Na, O). This will expand the list of potential substrates and back-contact metals to those that may be more optimally suited to CIGS thin-film processing. The absorber will be fabricated in a manner that minimizes *in situ* process control and high-temperature processing. This will drastically reduce the cost of manufacturing equipment. Finally, the heterojunction partner will be formed in situ with the absorber, to relieve the necessity for a vacuum break and a CBD process. This will improve reliability and throughput and will reduce cost.

The critical absorber process parameters have been considered, and a generic flowchart developed for the fabrication of CIGS absorbers (Fig. 8). By breaking the process into three or four independent stages, there are clear opportunities to use a variety of deposition techniques, separate and reduce the time for high-temperature (High-T) process segments, and introduce intelligent process control.

Figure 9, presents two absorber processing scenarios that target manufacturability. In (a), CIGS source material is delivered in such a manner as to produce a low-quality, fine-grain precursor film. It is subsequently exposed to (Cu,Se) and (In,Ga,Se) at high-T to complete the absorber. In (b), the source material is a similar, low-quality CIGS:CS mixture. The CS is activated with Se activity at high T, followed by (In,Ga,Se). In these experiments, the process segment times are 3 min, resulting in a total high-T time of 6 min. This represents a 2 to 3× factor reduction, compared with the two- and three-stage processes previously described.

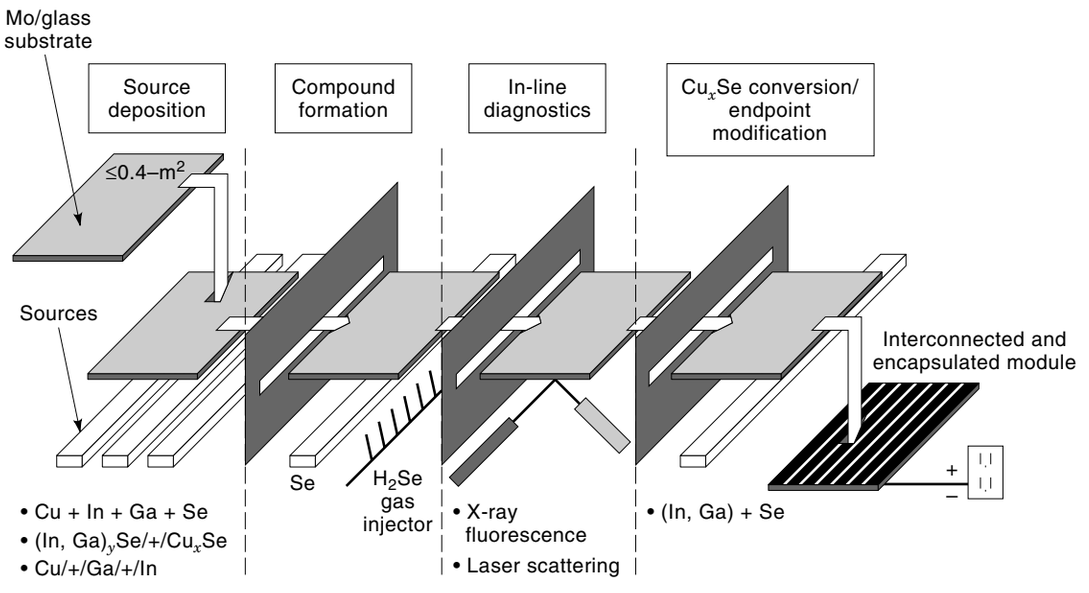


Figure 10. Scenario for the manufacture of CIGS-based modules.

Three source-material delivery techniques are under investigation: rapid evaporation, sputtering, and electrodeposition. Table 3 presents the best results to date using these delivery techniques, in conjunction with processing described in Fig. 9. The results reflect more of the relative time investments involved in each of the processes than their potential. The authors enthusiastically contend that each of these techniques, in conjunction with the appropriate recrystallization treatment, will produce material of equivalent quality.

GENERIC MANUFACTURING SCENARIO

A growth model describing the formation of $Cu(In,Ga)Se_2$ absorbers from a Cu-rich precursor has previously been presented (9). A consequence of formulating this model is an understanding of how to translate these technologies from the laboratory to the factory. Figure 10 presents a manufacturing scenario that is generic to any of the above-mentioned processes. One of the exemplary aspects of this scenario is the inclusion of in situ/in-line diagnostics and end-point detection. The diagnostics involve the nondestructive determination of Cu and (In,Ga) contents in the absorber film after intermediate deposition steps. This allows feedback into subsequent processing areas, to assure an optimum composition in the final product. Likewise, the termination of the process can be detected by either a phase or compositional change in the absorber surface. In this way, the process is designed for maximum yield and optimum performance. The authors' laboratory is currently investigating industrial-scale processes at the 100 cm^2 submodule level.

CONCLUDING REMARKS

As device efficiencies rise and processes are simplified, one can expect to see the introduction of high-performance, high-yield, reliable PV modules based upon the $Cu(In,Ga)Se_2$ absorber. Additional improvements will come with optimized device designs and a better understanding of the $CuInSe_2 : CuGaSe_2$ alloying process. The authors' laboratory is dedicated to realizing this goal through continued research into the basic science of the materials and devices, as well as the development of process technologies that are transferable directly to industrial interests.

Acknowledgments

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TERTIARY STORAGE DEVICES. See DISTRIBUTED MULTIMEDIA SYSTEMS.

TEST EQUIPMENT. See AUTOMATIC TEST EQUIPMENT FOR INSTRUMENTATION AND MEASUREMENT.

TESTING. See AUTOMATIC TESTING.