SEMICONDUCTOR–INSULATOR INTERFACES

This article describes the formation of a thin insulator layer on bulk semiconductors and the properties of the semiconductor–insulator interface. The semiconductors considered here are Si and the compound semiconductors that are most important in the electronic and electrical industry. The first section deals with the unique properties of the Si–SiO_2 interface. It also discusses possible replacements for SiO_2, oxidation mechanisms at the Si surface, the transition from the crystalline Si to the amorphous SiO_2, chemical bonding at the interface, thickness uniformity of very thin SiO_2 films, SiO_2 as diffusion barriers, and the electrical charge traps at the interface. The second section summarizes present information on compound semiconductors, and includes GaAs, InGaAs, InP, GaP, InSb, GaSb, AlSb, $Hg_xCd_{1-x}Te$, GaN, and AlN. On GaAs substrates, various methods of insulator formation have been investigated that lead to different interface properties. The second section also gives some details on the comparison of thermal oxides, anodic oxides, UV and ozone oxides, photochemical oxides, beam-assisted oxides, and deposited insulators on GaAs substrates.

Si–SiO_2 INTERFACE

Introduction

During the last several decades, semiconductor devices (e.g., Fig. 1) fabricated on layered structures of metal–oxide–semiconductor (MOS) films have penetrated almost every aspect of our daily life. These devices are the basic building blocks of the integrated circuits (ICs) (1) that exist in all the electronic components surrounding us, inside our watches,

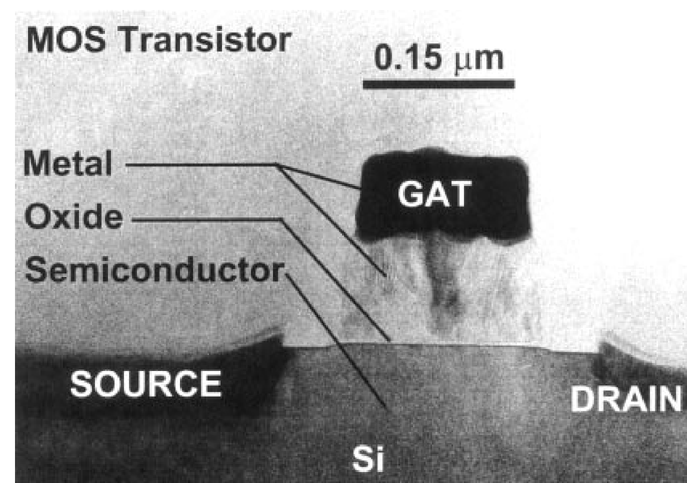

Figure 1. The cross section of a metal–oxide–semiconductor (MOS) transistor, taken by transmission electron microscopy (TEM). The layers of materials are, from top to bottom, a composite two-layer metal, thin SiO_2, and Si substrate. The metal layers are 80 nm WSi_2 and 100 nm polycrystalline Si doped with $10^{20}/cm^3$ boron or phosphorus to make it highly conducting. The SiO_2 is 5 nm, thermally grown on the Si. The composite layers make up the gate terminal of the transistor. The material of the source and drain terminals is 50 nm $TiSi_2$ formed on the Si substrate outside the gate areas. More details of the MOS transistor structures can be found in Ref. 1.

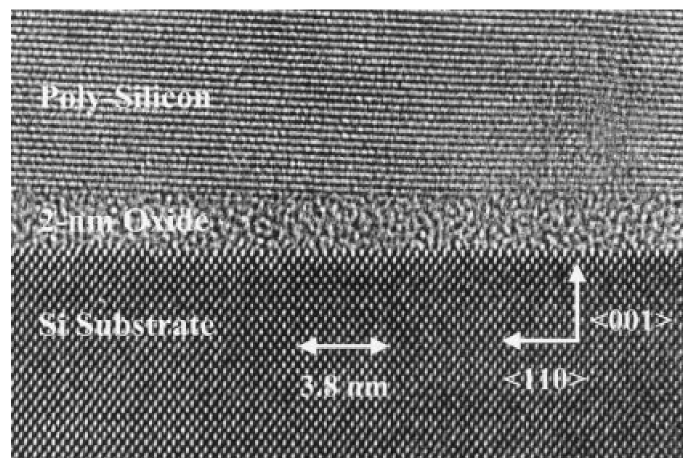

Figure 2. The cross section of a Si–SiO_2 interface taken by TEM. The SiO_2 layer is 2.5 nm (25 Å). It is sandwiched between the bottom crystalline Si substrate and the top polycrystalline Si.

cars, stereos, televisions, microwave ovens, telephones, hospital utilities, and even children's toys. Although each integrated circuit actually takes up a very small space, typically smaller than 1 cm by 1 cm, it accomplishes a large number of extremely complicated computational or logic functions at a speed of roughly one million operations per second. A comprehensive review of the MOS technology was given recently at the 50th anniversary of the invention of the MOS transistor (2).

The wide application of the integrated circuits could not have been realized without the unique properties of the thermally grown Si–SiO_2 interface (3–5). In Fig. 1, the thin SiO_2 layer acts as an insulator that separates two electronic signals. One travels between the *source* and *drain* terminals in the semiconductor layer underneath the SiO_2, and the other flows in the semimetallic layer (the *gate*) above the SiO_2. At the same time, in a capacitive fashion, the SiO_2 film also couples the two signals. Since the metallic gate is routed to go above more than one discrete device, signals in separated devices are also nested, and thereby, integrated circuits are formed. In order to function predictably and reliably, the circuit makes several demands on the insulator film between the semiconductor and the metal layers. Compared to other insulators that might be used as the gate dielectric, SiO_2 is currently the only one that possesses all the necessary properties. Scientists, however, are actively seeking replacements for SiO_2 for future generations of the electronic devices.

Unique Properties of Si–SiO_2 Interfaces

In the following sections, the unique properties of thermally grown SiO_2 films will be discussed. These properties include: (1) atomic phase transitions from the crystalline Si to the amorphous SiO_2 (Fig. 2), (2) extreme smoothness at the interface, (3) controllable growth rates, (4) very good thickness uniformity across large areas [currently on 6 in. (15 cm) Si wafers, and moving toward 8 in. (20 cm) and 12 in. (30 cm)], (5) low densities of Si–SiO_2 interface states, (6) electrically stable interface, (7) electrically stable SiO_2 film, (8) high dielectric breakdown strength (6), (9) thermal stability at high temperatures (above 1000°C), (10) good immunity to impurity pene-

J. Webster (ed.), *Wiley Encyclopedia of Electrical and Electronics Engineering*. Copyright © 1999 John Wiley & Sons, Inc.

tration as diffusion barriers, (11) low leakage of electrical currents, and (12) low processing defect densities, enabling high yields.

From 1960 to Years Beyond 2000

When SiO_2 was first used as a gate dielectric in the 1960s, the reproducibility of the film characteristics was poor for two main reasons: surface conditions leading to high densities of interface states, and ionic contamination from metallic impurities and sodium ions. These problems were solved by chemical cleaning for surface preparation, and by minimizing the sources of sodium ions in the processing tools. Over the years, the quality of SiO_2 thin films has been greatly improved, so that it has been possible to scale down the film thickness continually in order to improve the device performance. Currently, films as thin as 4 nm are used in mass production without concern about instabilities. It is expected that soon after the turn of the century, SiO_2 films thinner than 3 nm (roughly 10 monolayers of the SiO_2 atomic structure) will be used in mass production of integrated circuits that are composed of more than 1 billion MOS devices. Meanwhile, great efforts have been made to investigate on (1) alternative growth techniques for SiO_2 in order to go beyond 3 nm and (2) alternative dielectrics having higher dielectric constants in order to gain more effectiveness in the capacitive control than in 3 nm SiO_2 (Table 1). The former include deposition of SiO_2 with plasma (7), laser (8), or chemical vapor deposition (CVD) (9). The latter include Si_3N_4 (10), Al_2O_3 (11), Ta_2O_5 (12), TiO_2 (13), and others. In Ref. 14, a case study of SiO_2 films thinner than 3 nm is described. Based on circuit requirements and integration challenges, the study also considers the prospects for thin dielectrics for ultrasmall MOS transistors.

Potential Replacement of SiO_2

In addition to the benefit of gaining more device efficiency, it is also important to develop high-*k* dielectrics in order to reduce the leakage current of the gate insulator (Fig. 3). High-*k* dielectrics allow the use of a physically thicker film (to reduce the tunneling current) while maintaining the same effectiveness of the gate capacitance. In Fig. 3, the leakage current of SiO_2 and several high-*k* dielectric films is plotted for a voltage bias of 1 V across the films. As the thickness decreases, the leakage current of SiO_2 increases exponentially. For example, between 10 nm and 1 nm, the leakage current increases by more than 40 orders of magnitude. With high-*k* dielectrics of 1 nm equivalent SiO_2, the leakage current is dramatically controlled. If TiO_2 ($\epsilon = 30$) is used to replace SiO_2, the leakage current is reduced by roughly 35 orders of magnitude. Although the barrier height of the high-*k* dielectrics to the Si substrate is smaller than the barrier height of the Si–SiO_2 interface (Table 1), the leakage reduction achieved from increasing the thickness is many orders of magnitude larger than the penalty due to the barrier height reduction (Fig. 3 and Fig. 4). In the case of TiO_2, the penalty is only 3 (out of 35) orders of magnitude. The benefit of using high-*k* dielectrics is particularly large in the direct tunneling regime, where the voltage across the dielectrics is smaller than the barrier height.

Table 1. High-*k* Dielectrics: A Comparison of Their Energy Bandgap E_g, Conduction-band Discontinuity ΔE_c (Barrier Height for Electron Tunneling), and Dielectric Constant ε

	E_g (eV)	ΔE_c (eV)	ε
Si_2O	9	3.1	3.9
Si_3N_4	5	2.0	7.5
Al_2O_3	8.7	3–4	10
Ta_2O_5	4	1.45	25
TiO_2	3.3	1.1	30–80

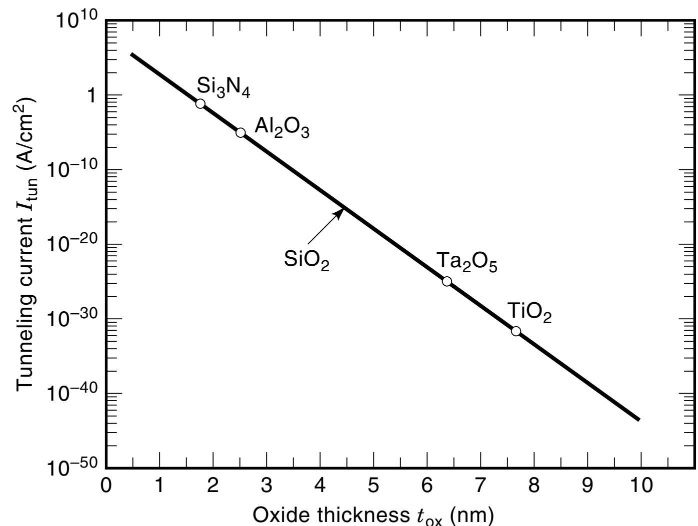

Figure 3. Calculated dielectric leakage current for SiO_2 as a function of the thickness (line), and the leakage current of several high-*k* dielectrics of 1 nm equivalent SiO_2 thickness (symbols) as listed in Table 1. In the calculation, all quantum-mechanical effects are considered. However, the interface between the dielectrics and the Si substrate is assumed to have no charge traps or defect-related energy states. Refer to Ref. 18 for more details of the calculation.

Unfortunately, it has been problematic to integrate high-*k* dielectrics in the production of integrated circuits, due to such issues as interface states, high-temperature incompatibilities, and defect-related leakage. For example, Ta_2O_5 and TiO_2 exhibit superior dielectric constants (Table 1 and Fig. 3), but they crystallize at 800°C and 400°C, respectively. In their

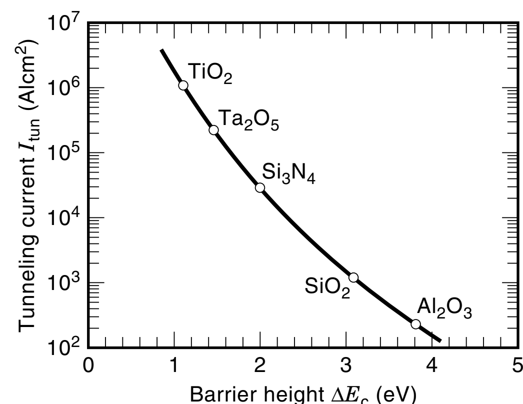

Figure 4. Calculated dielectric leakage current as a function of the energy barrier height of the leakage. For electron tunneling current, the barrier height is the conduction band discontinuity between the dielectrics and the Si substrate.

polycrystalline form, the leakage current becomes orders of magnitude higher. Therefore, the processing temperature of the Si wafers is limited once they are deposited.

Si Oxidation

Oxidation of a Si surface can occur even at room temperature, once the Si surface is exposed to the air. In the manufacture of integrated circuits, oxidation takes place in a furnace where the temperature and ambient can be manipulated during the oxidation. The furnace temperature is typically at 750°C or above, and the ambient contains either pure oxygen or water vapor. Oxygen or water vapor reacts with the Si surface and forms SiO_2. The chemical reaction is $Si + O_2 \rightarrow SiO_2$ for dry oxygen and $Si + 2H_2O \rightarrow SiO_2 + 2H_2$ for water vapor. After an initial layer of SiO_2 is formed, both water vapor and oxygen can diffuse easily through SiO_2 at the elevated temperatures, and the oxidation process continues at the Si–SiO_2 interface. Gradually, Si is consumed as the oxide grows, and the resulting Si–SiO_2 interface moves layer by layer into the Si. Approximately 54% of the final oxide thickness is above the original Si surface and 46% is below the original surface. As the oxide grows thicker, the diffusion path for the oxygen or water vapor to reach the Si surface becomes longer, and as a consequence, the growth rate of the oxide decreases. The entire process of oxidation can then be characterized by two periods: the initial linear stage, where the oxidation is governed by the surface reaction, and the second stage, where a parabolic growth rate is controlled by the diffusion mechanism (15).

The filled symbols in Fig. 5 plot the oxide thickness as a function of the oxidation time for two oxidation temperatures, 800°C and 900°C. Typical examples are 5 nm grown at 800°C for 25 min and 15.5 nm at 900°C for 35 min. Before 1990, when the oxide thickness was typically 10 nm or more, the oxidation temperature was in the range of 900°C to 1100°C. Since 1990, as the thickness was scaled down below 10 nm, the oxidation temperature has dropped to the range between 750°C and 900°C. At the same time, the oxygen content in the oxidation ambient has also been diluted with inert gas such as N_2 in order to slow down the oxidation rate for a better control of the thickness uniformity and process repeatability. As the thickness continues to decrease to 4 nm and below, the technique of rapid thermal oxidation (RTO) will become more and more important for sustaining the high quality of SiO_2 films. The fast temperature ramping of RTO makes it possible to grow a very thin film at 1000°C or above in less than a minute, with the same thickness and uniformity control obtained by 750°C furnace oxidation over 20 min. The high oxidation temperature improves the oxide quality significantly.

The oxidation rate is also affected by doping of Si. In Fig. 5, the open symbols show how the oxide thickness is affected by the doping of the Si substrate with nitrogen. Prior to the oxidation, nitrogen was implanted into the Si substrate through a sacrificial oxide layer (16–18). With a nitrogen dose of $5 \times 10^{13}/cm^2$ to $1 \times 10^{15}/cm^2$, the oxidation rate is reduced by 20% to 50%. For example, with $5 \times 10^{14}/cm^2$ nitrogen dose, the thickness grown at 800°C for 25 min is reduced from 5 nm to 4 nm, and the thickness grown at 900°C for 35 min is now reduced to 8.5 nm from 15.5 nm.

Interface Transition

In Fig. 2, a cross section of a 2 nm oxide film taken by transmission electron microscopy (TEM) (19) is shown. The oxide was grown at 800°C on the ⟨100⟩ lattice orientation (20) of the Si substrate. It was then covered with a polycrystalline Si layer as shown in the figure (bottom layer of the two layers in Fig. 1). The polycrystalline Si was deposited at 620°C in a CVD furnace. In the Si substrate, the TEM also reveals the lattice images of two sets of parallel planes in ⟨001⟩ and ⟨110⟩ crystal orientations (20). The physical spacing between the ⟨110⟩ parallel planes is 0.38 nm (20), and can be used to determine the thickness of the oxide layer in the picture to an accuracy within 0.1 nm.

A highly uniform transition from the crystalline Si substrate to the amorphous SiO_2 is revealed in Fig. 2. At the Si–SiO_2 interface, the Si crystal transforms into the amorphous oxide abruptly, almost on the same ⟨100⟩ plane (20) within the scope of the TEM. The short-range (2 nm to 4 nm apart) and long-range (20 nm to 50 nm apart) interface roughness is only 0.2 nm to 0.4 nm, determined from a total

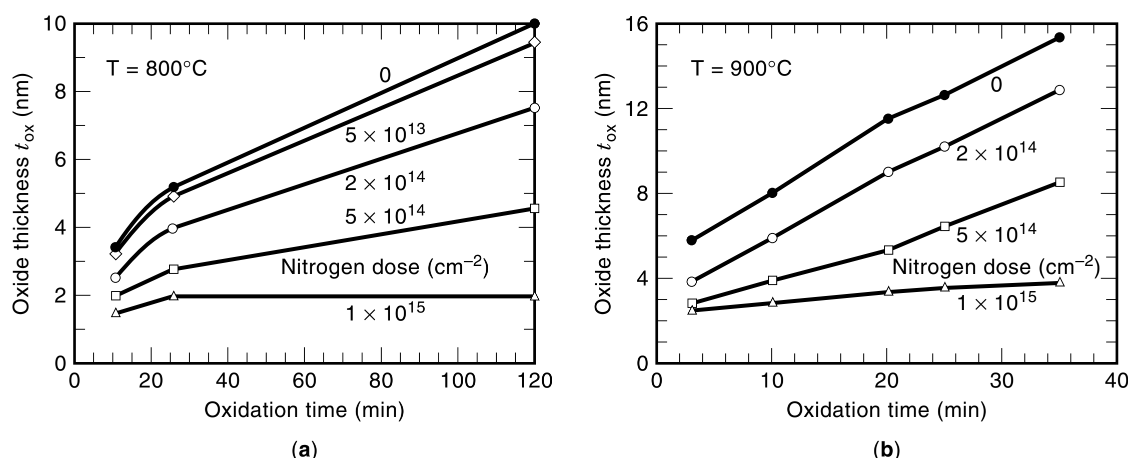

Figure 5. SiO_2 thickness versus oxidation time at (a) 800°C and (b) 900°C. Filled symbols are oxides grown on Si substrates without nitrogen doping, and open symbols are oxides grown on Si substrates doped with various nitrogen doses.

TEM range of 450 nm. Such a sharp phase transition on the atomic scale is one of the most important stoichiometric properties of Si–SiO_2. It is the fundamental reason for the stable Si–SiO_2 interface. For example, if one implants a sufficient amount of oxygen into a Si substrate and heats up the Si substrate to 900°C, some atomic layers of the Si will turn into SiO_2 and the transition interface from Si to SiO_2 will be formed on an atomically sharp scale. Nevertheless, there exists a certain amount of mechanical stress at the interface due to lattice mismatch and thermal expansion differences. The degree of stress depends on the oxidation temperature and the ambient.

Interface Bonding

The oxide thickness can also be measured optically with ellipsometers. Multiangle ellipsometry can be used to extract the thickness and dielectric constant of the film, based on the reflectance on the oxide surface. By comparing the TEM measurement and ellipsometry measurement, one can plot the dielectric constant as a function of the dielectric thickness, and thus study the molecular structure at the interface. For SiO_2, the dielectric constant of a thick film is known to be 1.458. It has been suggested that, if the oxide thickness is smaller than 10 nm, its dielectric constant could go up to 1.7 (21). In recent studies (16,22), however, it has been found that the dielectric constant stays at 1.458 for films as thin as 2.5 nm. It is very likely that the dielectric constant of extremely thin films is affected by the growth conditions, including the growth temperature, the ramp rate of the temperature, and the growth ambient. The variation of the dielectric constant is related to the chemical bonding of the Si and oxygen atoms with their neighbors at the interface.

An alternative probe of the chemical bonding is achieved with X-ray photoemission spectroscopy (XPS), which, instead of giving a collective measure of the behavior of all the molecules in the film, provides a detailed spectrum of the energies of all the chemical bonds. From XPS study, it is confirmed that indeed a suboxide structure exists in films that are 2.5 nm or thinner (Fig. 6), even when the ellipsometer cannot tell a change in the dielectric constant. In Fig. 6, the binding energies of the Si–Si 2p and Si–O 2p covalent bonds are plotted for three oxide films of different thickness, 4 nm, 2 nm, and 1.3 nm. For the thin oxide films, the binding energy of the Si–O bond has shifted to the right, toward the Si–Si 2p bond. The relative peak intensity of the spectrum also changes as the XPS probes further into the Si substrate for the thinner films.

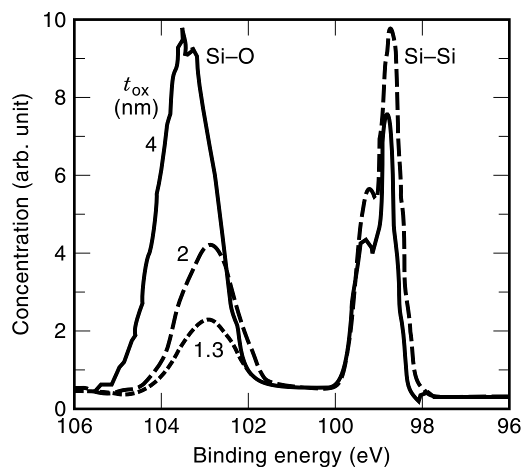

Figure 6. XPS spectrum of thin SiO_2 films. The signal intensity is normalized to the peak intensity of each spectrum, and it is plotted as a function of the binding energy of the chemical bonds. The peak position of the Si–Si 2p bond is used as the reference energy.

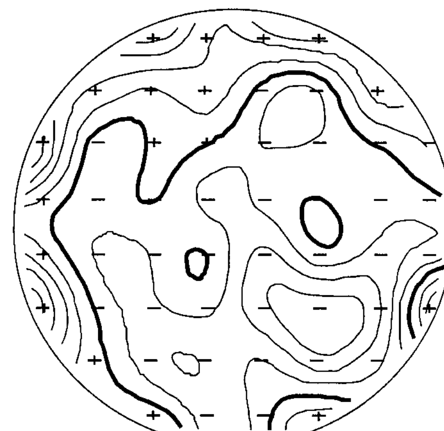

Figure 7. Contours of SiO_2 film thickness on a 8-in. (20-cm) Si wafer. The average thickness is 4.2 nm, and the contour interval is 0.021 nm. The standard deviation across the entire wafer is 0.038 nm (0.89%).

In the crystalline Si, each Si atom has four Si neighbors, while in SiO_2, each Si has two Si and two O neighbors. With photoemission spectroscopy (PES) using an advanced synchrotron radiation source, it is possible to study the binding energies of the Si atoms with one (Si^{+}), two (Si^{+2}), or three (Si^{+3}) Si–O bonds in the transition layers at the interface. The binding energies of the Si^{+}, Si^{+2}, and Si^{+3} atoms are located between the binding energies of the Si–Si (Si^{0}) and Si–O (SiO_2) peaks in Fig. 6 (23).

Thickness Uniformity

In Fig. 7, the thickness contours of a SiO_2 film grown on a 8 in. (20 cm) Si wafer are plotted with a contour interval of 0.021 nm. The average film thickness is 4.2 nm, and the standard deviation of the thickness across the entire wafer is as small as 0.038 nm, which accounts for only 0.89% of the average thickness. As a matter of fact, the minimum thickness (4.1 nm) on the entire wafer is only 0.2 nm smaller than the maximum thickness (4.3 nm). Such high uniformity of the oxide thickness is one of the most important attributes that account for the high manufacturing yield of Si integrated circuits. As the SiO_2 becomes thinner in advanced technologies, the electric field across the SiO_2 also becomes higher. Therefore, any thickness nonuniformity can easily cause electrical breakdown of the SiO_2 and degradation of device performance.

If the Si substrate is doped with nitrogen, the modified surface reaction also changes the SiO_2 thickness uniformity, as presented in Fig. 8. In the figure, experimental data are plotted for two nitrogen doses, $2 \times 10^{13}/cm^2$ and $2 \times 10^{14}/cm^2$. The former does not change the oxidation rate, and it does not change the thickness uniformity. The later slows down the oxidation, and it also improves the thickness uniformity, i.e., the thickness variation is reduced. In other words, nitrogen doping in the Si substrate modifies the surface reaction, and affects the oxidation rate and thickness uniformity at the same time. For example, with 10-min oxidation and without the nitrogen doping, the average thickness is 3.4 nm with ≈1.3% variation. When the wafers are doped with $2 \times 10^{13}/cm^2$ nitrogen, neither the average thickness nor the thickness variation is influenced. However, when the wafers are doped with $2 \times 10^{14}/cm^2$ nitrogen, the average thickness becomes 2.5 nm and the thickness variation drops to only 0.4%.

Diffusion Barrier

By blocking the penetration of impurities, SiO_2 films can also serve as diffusion barriers. Typical impurities include boron and phosphorus atoms. Owing to the bonding differences inside the SiO_2 film and at the Si–SiO_2 interface, diffusion of impurities encounters different stopping forces. Inside the film, impurity diffusion walks through imperfect bonds of SiO_2, while at the interface impurities tend to pile up. Therefore, there are at least two activation energies required in bulk diffusion: the creation of the imperfect bonds (if they do not exist), and the breakup of the impurity atom from its bonds to the neighboring Si or oxygen atoms (24). As the film thickness decreases, the blocking efficiency of the SiO_2 films also decreases. Boron was the first species to be noticed that affects the reliability of the SiO_2 films as well as the characteristics of the associated MOS device (25). As a consequence, there has been extensive research devoted to in solving the problem of boron penetration through thin SiO_2 films. Since nitrogen is known to convert dielectric and metal films into good diffusion barriers, the incorporation of nitrogen in thin SiO_2 has been the common theme of all efforts. For example, it is very easy to add a certain amount of nitrogen to the SiO_2 by introducing N_2O (26) or NO (27) gases in the oxidation ambient.

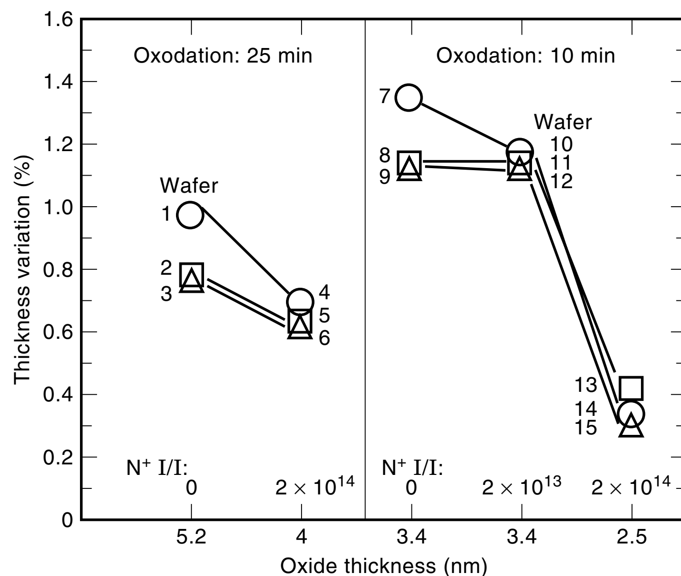

Figure 8. Thickness variation (standard deviation divided by the averaged thickness) as a function of the averaged thickness for two oxidation times: 25 min and 10 min. Wafers 1, 2, and 3 are three different wafers located at the top, middle, and bottom of the vertical furnace, respectively.

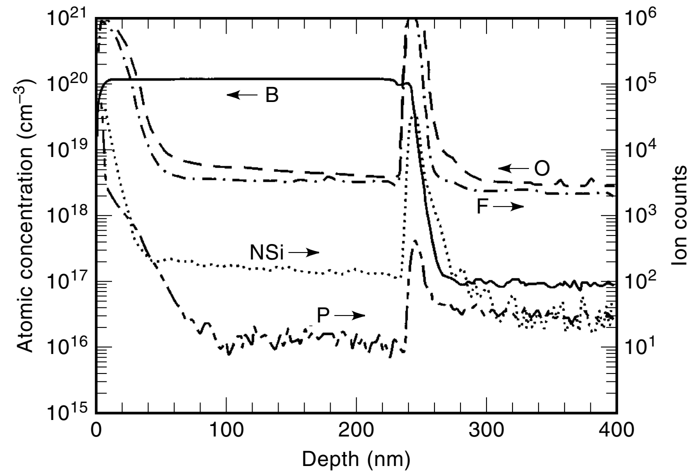

Figure 9. Secondary-ion mass spectroscopy (SIMS) profiles for O (oxygen), N (nitrogen), B (boron), F (fluorine), and P (phosphorus) in a sample containing a sandwiched structure as in Fig. 2 (top polycrystalline Si layer, 2.5 nm SiO_2, and Si substrate of the MOS structure). For better resolution, an NSi signal was used to take the N profile.

For 2.5 nm SiO_2 films, it has been demonstrated that the nitrogen implant approach, as described above, can effectively stop the boron penetration (17,28). Figure 9 shows the secondary-ion mass spectroscopy (SIMS) profiles for O (oxygen), N (nitrogen), B (boron), F (fluorine), and P (phosphorus) in the sample. Fluorine was introduced with B in order to enhance the B penetration (29). From the left to the right of Fig. 9 are the layers corresponding to the ones in Fig. 2, i.e., the top polycrystalline-Si layer, 2.5 nm of SiO_2, and the Si substrate of the MOS structure. For better resolution, NSi signal was used to take the N profile. The Si profile was also analyzed, but it is omitted from the figure for clarity. It is flat through out the entire spectrum, with a single dip that coincides with the O peak. The O peak identifies the location of the SiO_2. To the left of the O peak is the polycrystalline-Si layer, where the B doping is above $10^{20}/cm^3$ and is the source of B atoms for penetration through the 2.5 nm SiO_2. To the right of the O peak is the Si substrate, and the penetrated boron has to be detected. A N peak is observed within the SiO_2 layer, while no N is seen in the substrate within the SIMS resolution of $10^{17}/cm^3$. Thus, the entire implanted N has been incorporated in the SiO_2 during the thermal oxidation of the Si surface. The B profile drops sharply right before the N peak, and no B is observed beyond the SiO_2 layer. Therefore, the SIMS profile indicates no B penetration. The amount of B penetration can also be probed with the threshold variation of the associated MOS device (17,28).

Interface Charge Traps

At the transition from the crystalline Si to the amorphous SiO_2, charge traps exist at the interface and affect the stabil-

ity of the SiO_2. The traps lower the SiO_2 quality and the dielectric strength. When a MOS device is built on a SiO_2 film with a large density of interface traps, the performance and lifetime of the device is also significantly degraded (30). Unfortunately, there are always some traps at the Si–SiO_2 interface. Typically, a high-quality Si–SiO_2 interface has $10^{10}/cm^2$ traps or less, and a poor one has $10^{12}/cm^2$ traps or more.

One traditional measurement of the trap density is with the C–V (capacitance–voltage) curves. The measurement setup utilizes a capacitor fabricated with the SiO_2 as its dielectric (pretty much the same structure as Fig. 2), and probes the small-signal variation of the electrical charge added to or removed from the capacitor (31). The C–V curves are normally taken at two different frequencies of the small signal. At around 1 MHz, the energy states corresponding to the charge traps cannot be reached by the small signal, while at around 10 Hz they can be probed. Therefore, information on the traps can be extracted. Figure 10 shows a typical example of the C–V measurement (32) taken on a MOS capacitor fabricated with a 2.5 nm SiO_2 film. The top flat region in the 1 MHz curve between -1.5 V and -1 V reflects the thickness of the SiO_2, and the bottom flat region of the same curve between 1 V and 1.5 V reflects the substrate doping concentration. The slopes of both curves and the distortion of the 20 Hz curve are related to the density of the traps.

However, as the SiO_2 thickness decreases, the static leakage current increases exponentially (Fig. 3) and the small-signal C–V measurement becomes less reliable. An alternative probe of the interface traps measures the tunneling current as a function of the voltage drop across the SiO_2 (Fig. 11) (32). As shown by the difference between curve 1 and curve 2 in Fig. 11, the leakage current is very sensitive to the interface properties. In addition, after the SiO_2 is subjected to a high-field stress, more traps are generated. The stress-induced traps cause further damage of the SiO_2, and they also result in the degradation of the MOS device. Both the intrinsic and stress-induced traps can be characterized with the leakage current. In Fig. 11, one can also notice that the tunneling current becomes very noisy after the SiO_2 has been stressed. There are several causes of the noise. For example, it can be a result of electrons going from the Si substrate to the traps or vice versa, and changing the electric field locally. Therefore, a third approach to studying the interface traps is to measure the noise spectrum of the leakage current (33). Similar noise behavior also exists in the drain current of the associated MOS device (34,35). The noise behavior is a phenomenon that involves the quantum-mechanical properties of the Si–SiO_2 interface.

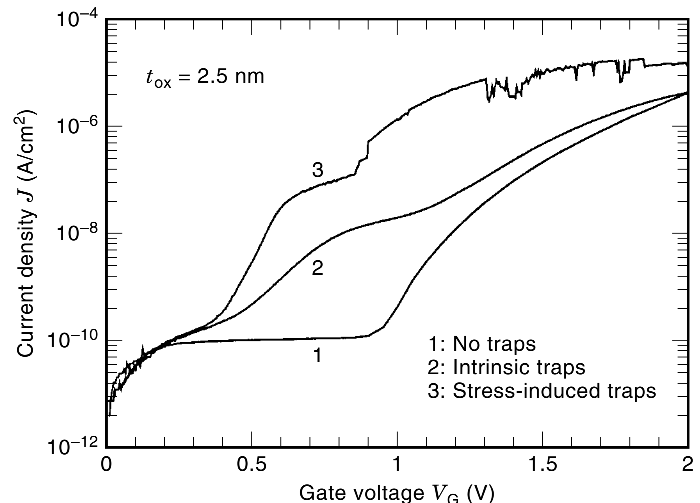

Figure 11. Leakage current of a 2.5 nm SiO_2 film as a function of the bias potential across the film. Curve 1 is theoretical calculation assuming no interface traps, that is, a perfect Si–SiO_2 interface. Curve 2 is the measured leakage current. The difference between curves 1 and 2 reflects the existence of interface traps. Curve 3 is taken after the oxide has been stressed with a high electric field that produces 50 mA/cm^2 leakage current for 20 s.

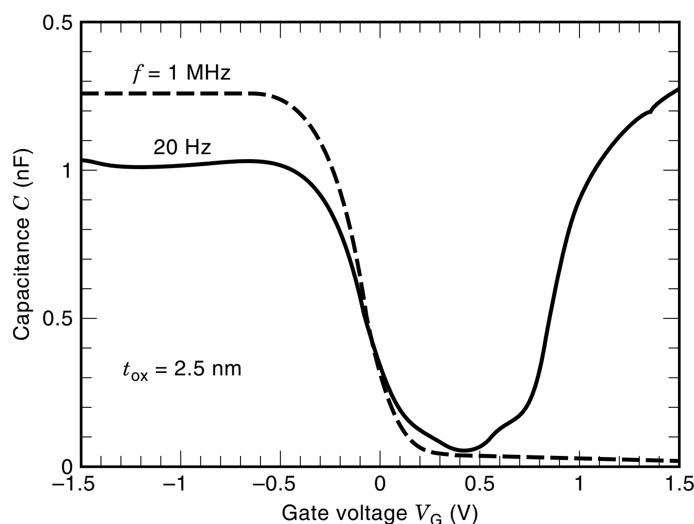

Figure 10. Measured C–V curves of a MOS capacitor fabricated with a 2.5 nm SiO_2 film. The range of the measurement voltage (x axis) scales linearly with the oxide thickness. The top flat region in the 1 MHz curve between -1.5 V and -1 V reflects the thickness of the SiO_2, and the bottom flat region of the same curve between 1 V and 1.5 V reflects the substrate doping concentration. The slope of both curves and the distortion of the 20 Hz curve reflect the density of the traps.

COMPOUND-SEMICONDUCTOR–INSULATOR INTERFACES

Introduction

The as-grown Si–SiO_2 system, after some additional thermal treatments, yields a high-quality interface and an electronically stable oxide, which has become the backbone of all integrated circuits and electronics today. The quest for competitive compound-semiconductor–oxide-insulator systems has not produced comparable results. After 35 years and hundreds of thousands of experiments, the first GaAs MOSFETs were announced in 1996 by Bell Labs (36), where the first transistors were invented. What is the difference between the two systems? As-grown compound-semiconductor–native-oxide systems have pinned surfaces (Fig. 12) (37), which severely limit the field effects on the band bending and quench the ability to modulate the carrier density in the semiconductor. The surface and thermal treatments employed in the Si system do not affect the compound semiconductor systems in the same manner.

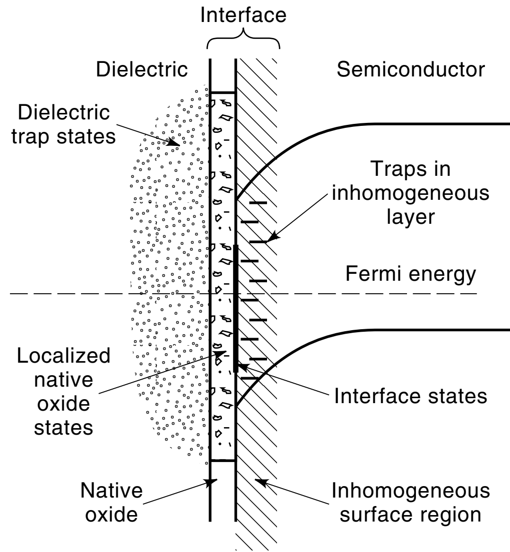

Figure 12. Schematic band diagram illustrating the potential sources of surface and interfacial trapping to be expected in a compound-semiconductor–native-oxide heterostructure.

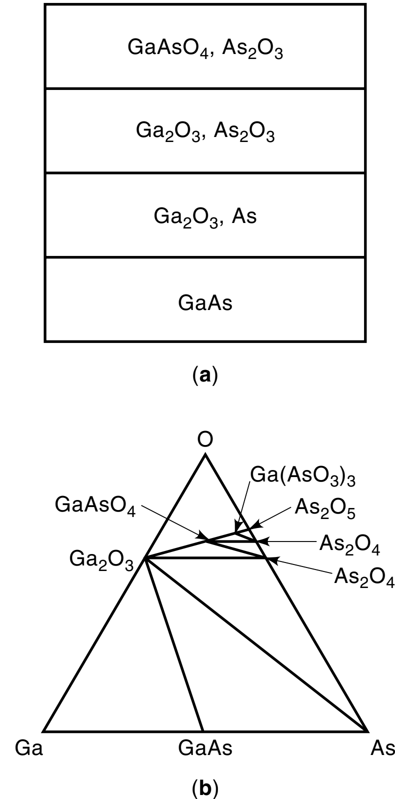

Figure 13. (a) Thermal oxide formation process in GaAs. (b) Ternary phase diagram for Ga–As–O.

One of the key challenges in compound-semiconductor device technology is to find thermodynamically stable insulators on the compound semiconductors that provide a low density of interfacial states (D_{it}). The most intensively studied and widely used compound semiconductor is GaAs. Thermal, anodic (including plasma), and photochemical oxidation of GaAs surfaces produced highly resistive films, but could not provide oxide–GaAs interfaces with a low D_{it}. Approaches using various dry, wet, and photochemical surface treatments prior to the deposition of insulating films produced limited success, since major sources of interfacial states such as nonstoichiometry, structural defects, and surface contamination still existed. The research efforts on the passivation of compound semiconductors are related not only to GaAs but also to other compound semiconductors. In this article, we summarize the different techniques that researchers have employed to fabricate the compound-semiconductor–insulator structures. The understanding that has been gained from characterizing various types of semiconductor–insulator interfaces will help, in turn, to obtain better material properties and achieve better device performance.

GaAs

Thermal Oxidization. The two primary methods used with GaAs are the formation of the native oxide upon heating GaAs directly in an ambient, and the transformation of the Al-containing layer in an $Al_xGa_{1-x}As$–GaAs structure. The first method involves dissociation of As oxides and outdiffusion of elemental As, but due to the multiple product species of the equilibrium process, the oxides are generally rough and cracked at the onset of oxidation (38). The thermal oxide formation process is schematically shown in Fig. 13(a), which can be understood using the ternary phase diagram of Ga–As–O shown in Fig. 13(b) (39). In 1981, Wilmsen compared the properties of the thermal and anodic oxides (Table 2) (40). The elusive interface was examined using X-ray photoelectron spectroscopy (XPS), which probes chemical bonding on the order of 0.5 eV, and Rutherford backscattering spectrometry (RBS), which provides a composition profile.

The first selective wet thermal oxidation experiment was carried out in 1978 (41). Using material grown with molecular beam epitaxy (MBE), Tsang selectively oxidized the AlAs over GaAs, in an O_2–N_2 ambient with and without water vapor at a temperature of 70°C to 130°C. The dry thermal process was much slower than the wet thermal process, keeping all other conditions the same. The oxide was thicker than the starting AlAs layer and contained $Al_2O_3(OH)$ complexes that weakened the oxide. Electrical measurements such as I–V and C–V showed low resistivities (10^{11} $\Omega \cdot$cm) and severe hysteresis that would lead to inaccurate capacitance values (42), and thus the traditional Terman method could not be used. (The Terman method models surface states in MOS structures from C–V, and provides an upper limit on surface states (43).) All initial results pointed to high densities of oxide traps and interfacial states and ill-defined dielectric properties such as breakdown field and dielectric constants.

After Tsang did the first experiments on wet thermal oxidation, Dalessase et al. in 1990 (44) found that the selective

Table 2. Summary of Results

Growth Temp.	Oxide Comp.	Interface Comp.
Low	As–Ga oxides	?
Medium	As, As–Ga oxides	As, Ga oxides
High (>500°C)	β-Ga_2O_3 polycrystal	As, Ga_2O_3
Post-dep. annealed	Ga_2O_3 (>430°C)	?

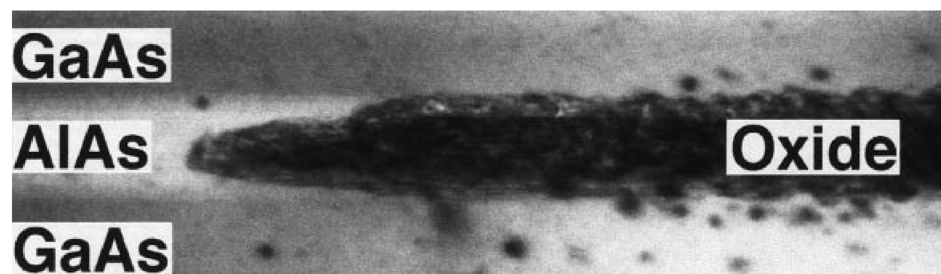

Figure 14. Cross-sectional TEM picture of wet-oxidized AlGaAs.

oxidation of AlGaAs at much higher temperatures (400°C) provided a more mechanically and chemically stable oxide. Samples are placed in a typical quartz furnace (>300°C) while N_2 gas is bubbled through H_2O held at 80°C to 90°C. The mechanism has three stages: the reaction of water vapor with the AlGaAs layer, the indiffusion of reactants, and the outdiffusion of As and As-containing products (45). A cross-sectional TEM picture of the wet-oxidized AlGaAs is shown in Fig. 14.

However, since the bulk is still a mixture of Ga oxides, the electrical properties remained poor (46). Chen et al. oxidized 500 Å of MOCVD-grown AlAs on an AlGaAs buffer on a Si-doped (10^{17} cm^{-3}) GaAs channel at 400°C for 200 min. The depletion-mode field-effect transistor (FET) had a $\approx 4\ \mu m$ gate length, $g_m \approx 1.2$ mS, $V_{th} = -10$ V, and $V_{br} \approx 10$ MV/cm. Unlike previous samples, this oxide was a thinner (by 20%) material and had a smaller refractive index than the starting AlAs. This technique has also been applied to other Al-containing materials such as AlInAs and AlInGaP (47). In addition, new optoelectronic devices were engineered as a result of this slightly modified technique (48).

Anodization. Anodic oxidation is the electrochemical formation of native oxides. The semiconductor anode and an inert metal (Pt) cathode are placed in a solution (tartaric or citric acid in water) or in a plasma (dc or RF magnetron). In the first approach, the oxide and interface qualities depended mainly on precursor layers, the input and output of oxidizing ions through the oxide, and the dissolution of As oxide byproducts. A schematic of the anodization of GaAs in a solution is shown in Fig. 15 (49). In the second method, sometimes referred to as plasma anodization, the solution is replaced by plasma generated by dc or RF fields. If a dc bias is applied to the substrate during the plasma process, oxidation takes place in a similar way to the wet anodization. There are many other similarities between oxidation processes in an aqueous solution and in plasma (50).

The first reported anodic oxide in solution was in 1963 by Revesz, but the surface was pitted and rough (51). Other electrolyte solutions sometimes had undesirable effects; for example, anodic oxidation by H_2O_2 in water led to the creation of an etching solution with acid contamination (52). In 1975, Hasegawa proposed anodic oxidation using tartaric or citric acid with ethylene or propylene glycol as the electrolyte ($V_{br} = 5$ MV/cm and $J = 1$ nA/cm^2) (53). As recently as 1996, Schmuki et al. (54) deposited anodic oxides in aqueous solutions of either borate buffer, pH 8.4, or 0.3 M $NH_4H_2PO_4$, pH 4.4, and all oxidation experiments were carried out in the dark. XPS spectra showed that both conditions produced mixed Ga and As oxides. Both oxides dissolved in water, but the oxides formed in borate solution dissolved much faster. Since holes are needed in the semiconductor to continue the reaction, oxidizing n-type GaAs required a laser at an energy above the bandgap.

Due to weak oxides, the C–V data showed severe hysteresis and peeled off upon annealing. Others continued to examine the properties of this oxide by fabricating metal–insulator–semiconductor (MIS) capacitors or FETs and analyzing the electrical responses. The first n-channel normally-off FET using anodic oxide as the gate dielectric was fabricated in 1976 (55) ($t_{ox} = 1000$ Å, $L = 15\ \mu m$, $V_{br} = 8$ MV/cm, and $g = 20\ \mu A/V$), with the gate annealed in N_2 at 600°C

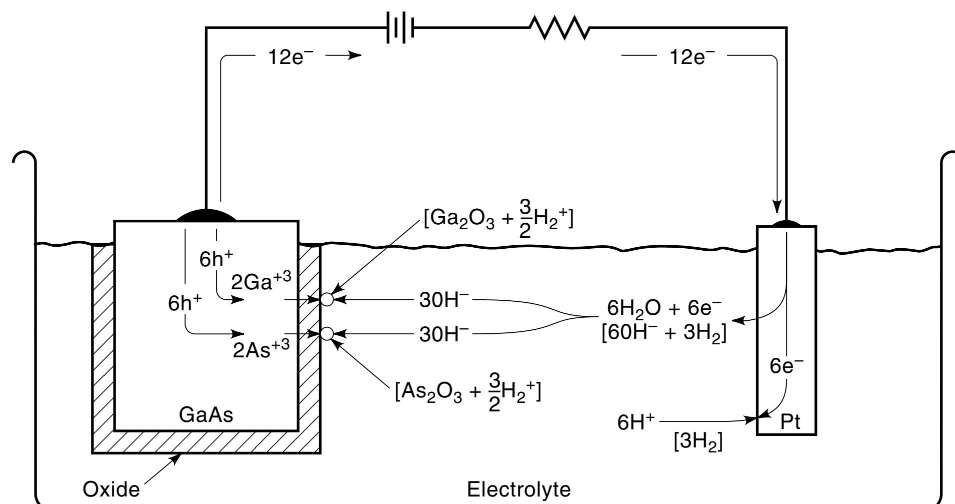

Figure 15. Chemical processes, mass flow, and current during anodization of GaAs.

for 5 min. In 1977, a normally-off FET ($V_{th} \approx -1$ V) and a normally-on FET ($V_{th} \approx -3$ V, $t_{ox} = 900$ Å, and $L_g = 20$ μm) were fabricated (56) using the self-aligned gate technique.

The plasma anodization technique produced oxides of similar quality. In 1966, Weinreich oxidized ⟨110⟩ or ⟨111⟩ tin-doped *n*-type GaAs at 70°C substrate temperature in an oxygen plasma at 0.2 Torr to 0.6 Torr (30 to 80 Pa) (57). The amorphous films ($t_{ox} = 300$ Å to 4000 Å, $n = 1.7$, $\epsilon = 3.9$ by C–V, and $V_{br} = 5$ MV/cm) were soluble in hot water. They had certain advantages over thermal oxides, including lower oxidation temperature (70°C versus 500°C to 900°C) and more uniform films; thermal oxidation produced pitted oxides due to As loss from substrate. In comparison, Revesz's anodic oxide was not soluble in water. One reason why the oxides were weak is the high-energy plasma at 10^{13} particles/cm^3 and 1 kW. Ten years later, in 1976, a similar experiment was performed by Chang et al. at 27 MHz and 300 W (lower power) and 10^{10} particles/cm^3 (58). The oxidation took place at 40°C with Te-doped (100) GaAs substrate at a dc bias of 50 V to 90 V. The films were amorphous by X-ray diffraction ($n \approx 1.9$) and also etched in HCl, but only slowly in boiling water (100 Å/min). Chang et al. observed Frenkel–Poole emission form J versus $E^{1/2}$, which is the field-enhanced thermal excitation of electrons from traps over the conduction band of the dielectric. After annealing in H_2 at 450°C for 30 min, the trap states of a film 10 μm thick were reduced. However, the hysteresis in the C–V curve remained. They concluded from temperature-stressed data that the slow trapping of holes, instead of mobile charge in the oxide, caused the leaky I–V characteristic.

In 1978, GaAs microwave metal–insulator–semiconductor field-effect transistors (MISFETs) were fabricated with S-doped *n*-GaAs films grown on semiinsulating (SI) GaAs substrates in the Ga–$AsCl_3$–N_2 system (59). Using plasma oxidation at 150 W, 13 MHz, and 0.04 Torr (5 Pa), a magnetic flux of 600 G (0.06 T), and a substrate temperature of 90°C, the *n*-GaAs was oxidized to form the gate insulator material. No pinholes were observed in an oxide 1000 Å thick over an area of 2.5 cm × 3 cm. Mimura et al. annealed the MOS structures and found that annealing below 450°C did not change the C–V characteristics, but annealing above 450°C actually worsened the oxide quality. This suggests that the oxide is composed of Ga and As oxides, the latter of which is unstable. Normally-on and normally-off *n*-channel devices were fabricated, and compared with a metal–semiconductor field-effect transistor (MESFET) as the reference. The depletion-mode MISFET had a current-gain cutoff at 4.5 GHz, and the MESFET at 3.7 GHz. At zero gate bias and 8 V drain bias, the MISFET had 0.4 W power with 4 dB gain at an input power of 0.15 W. The device was not a MOSFET in the sense of Si MOSFETs, since there was no confirmed inversion.

Other Methods of GaAs Oxidation

Ultraviolet–Ozone Oxidation. UV–ozone oxidation of GaAs has produced a mixture of stoichiometric Ga and As oxides with a thickness less than 10 Å (60,61). In contrast, native oxides grown in air have not yielded a stoichiometric surface after thermal desorption (62). The UV wavelengths of interest are 184.9 nm and 253.7 nm. The first wavelength is absorbed by O_2 to produce O_3 (ozone). Ozone then reacts with carbon on the GaAs surface, forming CO_2, and thus reducing carbon contamination (63). The latter wavelength is adsorbed by ozone, forming O_2 and atomic oxygen, whose indiscriminate reaction with GaAs may lead to the attainment of stoichiometric Ga and As oxides. However, upon prolonged oxidation the oxides were found to be less stoichiometric.

Photochemical Oxidation. Photochemical oxidation was achieved with collimated white light from a tungsten lamp and running DI H_2O over the sample from a glass reservoir where high-purity oxygen was dissolved (64). Prior to oxidation, the surface was etched with $NH_4OH:H_2O_2:H_2O$ in a ratio of 1 : 1 : 50. XPS showed that the oxide was not only Ga_2O_3, and the oxide was easily wiped off from the GaAs substrate. Compared to anodic oxidation, in which there was no photoexcitation, photoluminescence (PL) measurements showed that the photochemical oxide interface was better, but this was only due to extra fixed surface charges generated during oxidation that changed the position of the pinned Fermi level according to Hasegawa's DIGS model (65). The interface is still poor, due to the presence of arsenic oxides.

Beam-Assisted Oxidation. A beam-assisted oxidation method was employed in 1995 by Alay et al. (66), in which GaAs and AlGaAs were exposed to oxygen irradiation. While Al_2O_3 was stochiometric on AlGaAs, Ga oxides on GaAs were mixed with very small amounts of As oxides and elemental As compared to anodic or thermal oxidation.

Deposition of Insulators

Oxidation of GaAs by thermal, anodic, or other treatments produces, in general, amorphous mixtures of Ga_2O_3 and As_2O_3 with some inclusion of elemental As. They tend to be poor in terms of thermal stability, chemical stability, and compatibility with other processing technologies (67). Deposited insulators are increasingly being used in practical devices. Deposition techniques have increased in popularity with each additional method of growing semiconductor materials. The two most popular techniques are CVD and MBE, the former allowing a wide range of precursors and the latter using multiple-chamber UHV and/or controlling processes to avoid contamination.

SiO_2. The most plausible insulator to deposit onto GaAs was SiO_2 in view of its performance on Si. In comparison with most other oxidation techniques, surface treatment prior to deposition is important in insulator deposition. In 1965, Becke et al. (68) deposited SiO_2 on $(\overline{111})$ GaAs pyrolytically, starting at 600°C and heating to 730°C for the remainder of the deposition. The devices were *n*-channel normally on ($V_{th} \approx -4.5$ V) and normally off ($V_{th} \approx 2$ V) FETs. The gate was 26 μm in length, and $t_{ox} = 2300$ Å, postdeposition annealed at 800°C for 16 h. However, the high temperature produced surface states, which invalidated calculations using the Terman method. This is supported by their changing capacitance as seen in high-frequency C–V measurements. Other groups proved that SiO_2 was a good candidate for deposition, but the main problem resided in the interface. Since it was known that Si–SiO_2 has both a good oxide and a good interface, Tiwari et al. (69) and Freeouf et al. (70) grew Si on GaAs and used CVD plasma to deposit SiO_2. However, they observed no inversion due to Fermi pinning at midgap.

Ga_2O_3. Besides SiO_2, the best candidate for deposition was Ga_2O_3, which is the most stable native oxide. Since it was difficult to isolate this species, all attempts produced a nonstoichiometric oxide. One of the more interesting results was

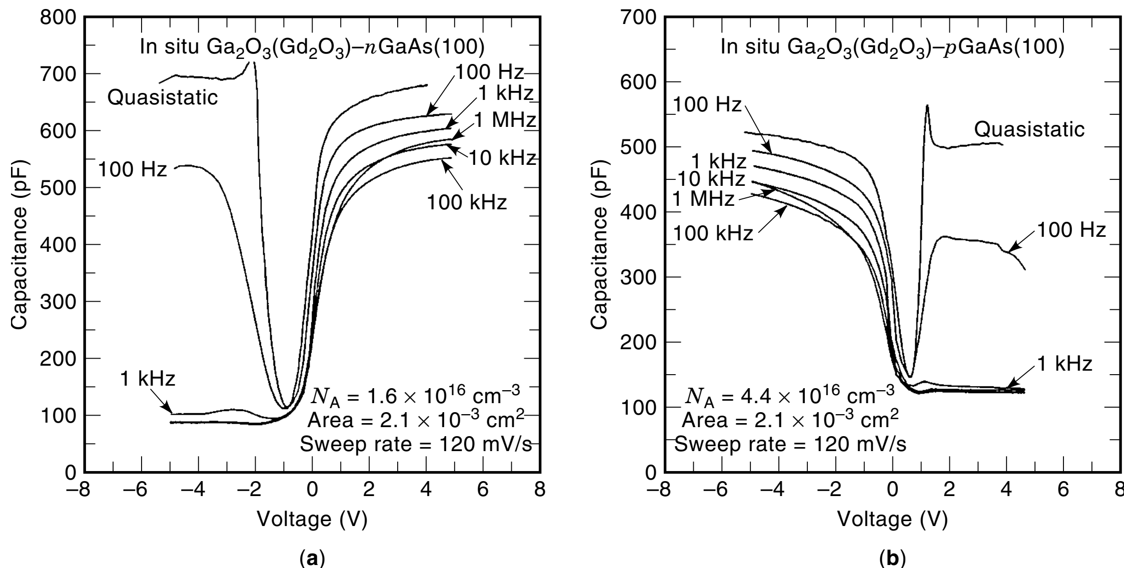

Figure 16. *C–V* characteristics of $Ga_2O_3(Gd_2O_3)$–GaAs: (a) *n*-type and (b) *p*-type.

due to Callegari et al. (71), who deposited amorphous Ga_2O_3 films with an RF O_2 plasma; a GaAs substrate was placed in O_2 plasma while an electron beam evaporated Ga metal. The substrate temperatures (30°C and 200°C) were below the native Ga and As oxide desorption temperature of ≈580°C. Without additional postdeposition treatments, the interface would be pinned. The H_2 plasma removed the native oxide while the N_2 passivated the Ga and As dangling bonds, forming a thin layer of nitride. Although, the oxide was not dense or robust, the interface seemed to improve tremendously. In addition, Aydil et al. (72) achieved passivation of surface states during a H_2 or NH_3 plasma treatment at room temperature by removal of excess As and As_2O_3, and subsequent formation of a Ga_2O_3 film (a few monolayers thick) on a GaAs surface.

E-Beam-Deposited $Ga_2O_3(Gd_2O_3)$. Using a multichamber ultrahigh-vacuum (UHV) system in which an oxide growth chamber is separated from a GaAs-based MBE chamber and the two chambers are connected via UHV transfer modules, Hong et al. deposited a mixture of Ga_2O_3 and Gd_2O_3 on GaAs (100) using electron-beam evaporation from a single-crystal $Ga_5Gd_3O_{12}$ garnet (GGG) (73). The GaAs surface can be freshly prepared from the MBE chamber or thermally desorbed in the UHV oxide chamber (74). GaAs MOS diodes were fabricated with establishment of accumulation and inversion in both *n* and *p* channels (Fig. 13). An interfacial state density in the low 10^{10} cm^{-2} eV^{-1} range was demonstrated (73–75). With this high-quality $Ga_2O_3(Gd_2O_3)$ as a gate dielectric and a conventional ion implantation process, enhancement-mode GaAs MOSFETs with inversion were demonstrated on semiinsulating GaAs substrates in *n*- and *p*-channel configurations (Fig. 17) (36,76). Furthermore, depletion-mode GaAs MOSFETs were fabricated (77), with a 1 μm × 100 μm device showing excellent dc and microwave characteristics with low output conductance. Complete pinch-off at $V_g = -2.5$ V and operation in the accumulation mode of up to $V_g = 2.5$ V were measured. The maximum transconductance was 100 mS/mm, with a high drain current density of 315 mA/mm. Microwave measurements yielded an f_T of 14 GHz and an f_{max} of 35 GHz. The $Ga_2O_3(Gd_2O_3)$–GaAs interface, studied by high-resolution TEM (Fig. 18) and X-ray reflectivity, is very smooth, with roughness as small as one atomic layer of GaAs (78). These $Ga_2O_3(Gd_2O_3)$ films, of thickness varying from 500 Å to 50 Å, showed leakage current densities as low as 10^{-9} A/cm^2 at low gate bias up to 2.5 V, and electrical breakdown fields as high as 9 MV/cm (79).

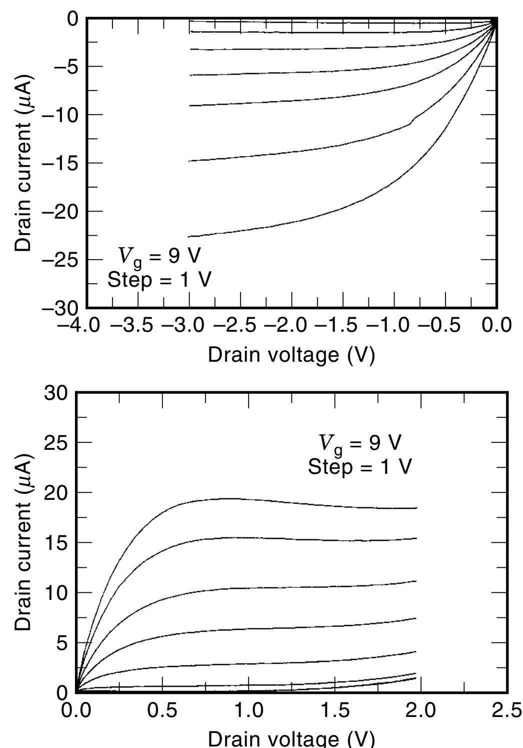

Figure 17. Drain *I–V* characteristics of typical enhancement-mode inversion-channel (top) *p*- and (bottom) *n*-GaAs MOSFETs with a gate geometry of 4 μm × 50 μm.

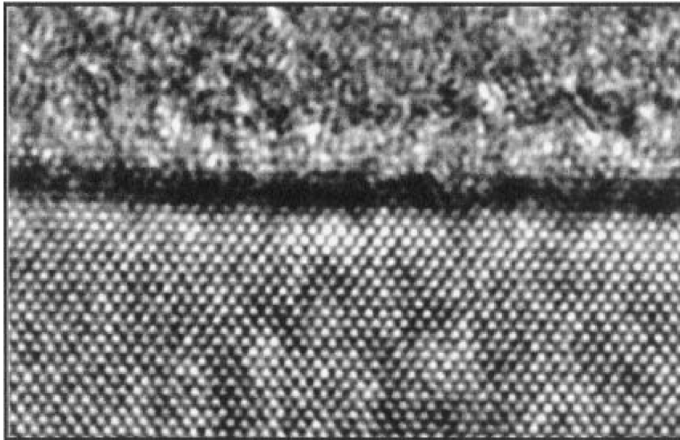

Figure 18. Cross-sectional high-resolution TEM image of a $Ga_2O_3(Gd_2O_3)$–GaAs sample prepared by *in situ* deposition in a UHV system. The amorphous nature of the $Ga_2O_3(Gd_2O_3)$ (upper part) is in gross contrast to the lattice image of the crystalline GaAs substrate (lower part). The interface roughness is on the order of a few monolayers.

Other Insulators. In 1979, Yokoyama et al. (80) used MBE to grow Al_2O_3 on GaAs with Al and O_2 beams, but without any success in obtaining good MIS measurements. In 1994, Jeong et al. (81) sulfide-treated a (100) n-GaAs substrate, formed 1000 Å of P_3N_5 in PCl_3–NH_3–H_2 at $T_d = 200°C$ by photo-CVD, and annealed at 300°C. Normally-on-mode devices were fabricated, but showed hysteresis. At the same time, another interesting CVD deposited insulator was developed by Reed et al. (82). First, Ge was deposited at a low substrate (n-GaAs) temperature 250°C using GeH_4 and remote-plasma-excited He, and after subsequent Si_3N_4 and Si depositions on top of the Ge layer, the structure was annealed by rapid thermal annealing (RTA), which improved the hysteresis dramatically, with a D_{it} of 10^{11} $cm^{-2} \cdot eV^{-1}$.

One unlikely candidate for GaAs insulator came out of the MIT Lincoln Laboratory in the 1980s: low-temperature-grown GaAs (LTG). While standard GaAs is grown at 600°C, LTG GaAs is grown at 200°C to 250°C. It is highly nonstoichiometric and has ≈2% excess As that precipitates out upon annealing at $T > 500°C$. The as-grown material is dominated by hopping conduction, but becomes highly resistive after annealing (10^6 $\Omega \cdot cm$) as the material becomes single-crystal GaAs with As precipitates embedded. However, if the LTG GaAs is not annealed with AlAs caps on either side, all the excess As will diffuse out of the material and no precipitate features will be observed. Chen et al. (83–85) published MISFET results from 1991–1996 using LT GaAs as the gate insulator. However, no inversion was achieved, and the devices, unlike the Si MOSFETs, operated in depletion mode.

Wet chemical sulfur (S) passivation has been applied to a GaAs (100) surface. The optical photoluminescence and electrical measurements showed a large reduction in the surface recombination centers. The surface structure of the S-passivated GaAs (100) surface is very complex. The S atom forms a stable bridge bond with two Ga atoms along the [011] azimuth, and on top of this ordered surface layer is a disordered arsenic sulfide film. The As sulfide can be rinsed off the surface by DI water (86).

Other Compound Semiconductors

InGaAs. The ternary alloy $In_{0.53}Ga_{0.47}As$, lattice-matched to InP substrates, has a large ΓL intervalley separation and high low-field electron mobility and saturation velocity. These characteristics should lead to devices with a high cutoff frequency and switching speed. Despite all the advantages of InGaAs, the Schottky gate characteristics on it are very poor, and MESFETs cannot be realized. Through the years, a variety of techniques such as plasma oxidation, and deposition of silicon dioxide and silicon nitride, have been used to passivate the InGaAs surface to form a MISFET structure for better gate characteristics (87,88). Both depletion- and enhancement-mode MISFETs have been demonstrated (89,90). However, the devices still showed current drifting, hysteresis, and negative threshold voltage for the intended enhancement-mode device due to traps in the dielectrics and to surface conversion during the implant-doping activation annealing. With $Ga_2O_3(Gd_2O_3)$, electron-beam-deposited from a high-purity single crystal $Ga_5Gd_3O_{12}$ source, as an insulated gate and with a conventional implantation process, n-channel enhancement-mode $In_{0.53}Ga_{0.47}As$ MOSFETs on InP semiinsulating substrate were fabricated (Fig. 19). A 0.75-μm-gate-length device exhibits an extrinsic transconductance of 190 mS/mm, which is an order-of-magnitude improvement over previously reported enhancement-mode InGaAs MISFETs. The device shows no leakage current and no hysteresis. A current-gain cutoff frequency f_t of 7 GHz and the maximum frequency of oscillation, f_{max}, of 10 GHz were obtained for the device, with gate dimensions 0.75×100 μm^2 at a gate voltage of 3 V and drain voltage of 2 V (Fig. 20).

Phosphides: InP and GaP. Thermal and plasma oxides in the phosphide system possess characteristics similar to other III–Vs in that the composition is $InPO_4$ mixed with In_2O_3 (91), but there is no elemental accumulation of phosphorus (P) at the interface at high oxidation temperatures. At very high

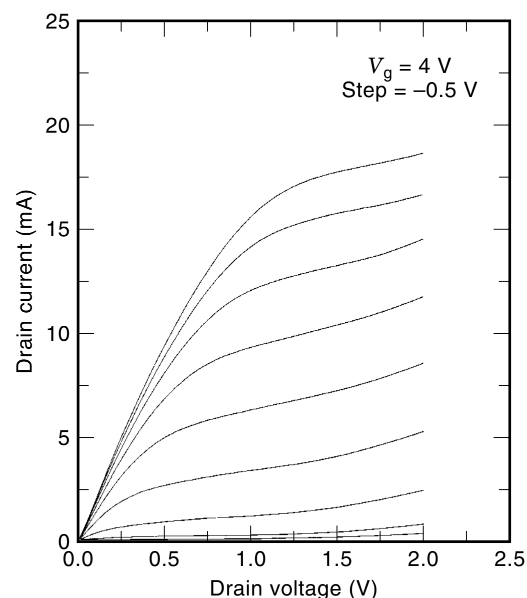

Figure 19. Drain I–V characteristics of a typical 1×50 μm^2 enhancement-mode n-channel InGaAs MOSFET.

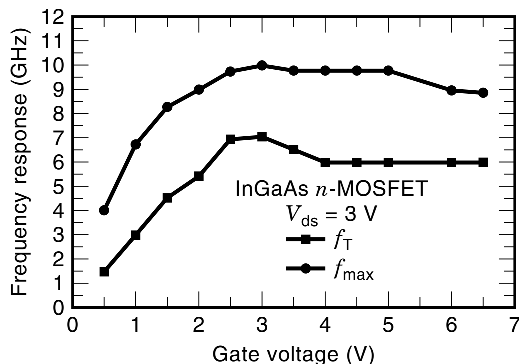

Figure 20. RF frequency response as a function of the gate voltage of an InGaAs MOSFET with a gate dimension of $0.75 \times 100\ \mu m^2$.

temperatures (>600°C), the surface roughens tremendously (92). These are comparatively "soft" III–V materials and have no suitable native oxides, since the oxides are unstable at all temperatures.

Wet chemical $(NH_4)_2S$ treatment has been found to one of the most successful methods to remove defective surface native oxides on InP (100). The treated surface is reasonably stable in ambient atmosphere. Surface analysis on the treated sample revealed that the surface is covered by one monolayer of S. The S atom occupies a P vacancy site, forming a bridge bond with two In atoms along a [011] azimuth, as shown schematically in Fig. 21 (93). The surface energy band structure is altered dramatically by the S passivation. For example, the surface bandgap of S–InP(100) is found to be about 5 eV.

The GaP thermal oxide has uniform $GaPO_4$ and no P at the interface, and is smooth up to 950°C, but has voids at the interface. Although no voids exist for wet oxides, the film cracks due to thermal stress (94). Anodic oxides are slightly better according to the first MIS results obtained by Wilmsen (95).

The first depletion-mode FET was demonstrated by Messick et al. using pyrolytically deposited SiO_2 (96). These devices did not show degradation in low-frequency response, such as was reported in GaAs MISFETs. Although this result is not always reproducible due to uniformity problems, it translates to less influence from surface traps and the ability to set dc levels. Since then, more MISFETs produced by deposited oxide on InP have been characterized. Hbib et al. used PON–n-InP by vapor transport (280°C to 350°C), characterized by XRD, XPS, and secondary-ion mass spectroscopy (SIMS), and reported an interfacial state density of 10^{11} $eV^{-1} \cdot cm^{-2}$ at 0.48 eV below the conduction band (InP E_g = 1.3 eV) (97). CCDs and solar cells have also been fabricated from this system.

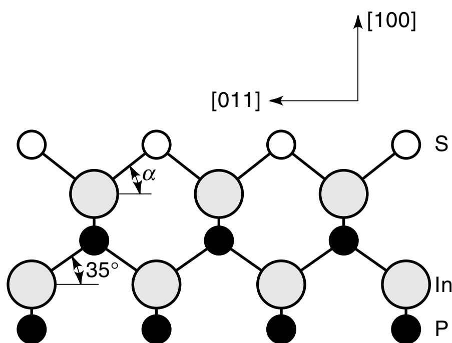

Figure 21. Structure of the sulfur-passivated InP (100) surface, viewed in the [1,−1,1] direction.

Antimonides: InSb, GaSb, and AlSb. As in GaAs, the thermal oxidation process in InSb and GaSb (250°C to 500°C) produces mixed group III and Sb oxides (38) with pitted and rough interfaces (98). Since the outdiffusion of Sb is slow and the free energy of formation associated with group III is high, the Sb accumulates at the interface. Rosenberg first detected a metallic layer of Sb in the interface of thermally oxidized InSb (99). The anodic oxides do not improve the situation. More recent results reported an interfacial state density at 10^{13} $cm^{-2} \cdot eV^{-1}$ (100), which implies limited field effect modulation. As with all other anodic oxides, annealing lifts off the oxide, which then dissociates. In general, the electrical characteristics of InSb and GaSb thermal or anodic oxide MISFETs are plagued by hysteretic C–V curves, dc drift, and high dc conductance.

$Hg_xCd_{1-x}Te$. Mercury cadmium telluride is a narrow-bandgap II–VI material employed extensively in infrared detectors. Some earlier experiments on annealed anodic MIS structures were done by Stahle et al. in 1987 (101). C–V and Auger analysis elucidated serious stability problems; the annealed (100°C) p-type MIS became an n-type MIS due to excess charge diffusion. In addition, fixed charges and slow traps plagued the oxide and the interface. Thus, researchers have concentrated most of their efforts in the more successful MCT-IR detectors for defense and astronomy applications.

GaN and AlN. Recent oxidation studies in this material system have been stimulated by the success of blue LEDs and lasers. Oxidation experiments have been performed by researchers who are interested in making power electronics. Because nitride materials are grown at high temperatures (>1000°C), thermal oxidation may also require such temperatures. To study the stability of GaN in potentially oxidizing environments, Wolter et al. (102) used XPS to analyze GaN epilayers exposed to dry air at various temperatures for 1 h to 25 h. They found a reaction-rate-limited process that oxidized at temperatures above 900°C.

A number of GaN FETs and AlGaN–GaN heterostructure FETs have been reported (103,104). However, the conventional low-resistance n^+-cap layer structure for the GaAs technology cannot be applied in the nitride system to reduce parasitic resistances, because no adequate gate recess technology is available. Hence, a viable MOSFET approach is desirable. GaN MIS diodes were demonstrated utilizing $Ga_2O_3(Gd_2O_3)$ as an insulator (105). The MIS diode showed good charge modulation from accumulation to depletion at different frequencies. The interfacial roughness of $Ga_2O_3(Gd_2O_3)$–GaN is as small as ≈3 Å, as estimated by X-ray reflectivity.

Conclusion

From the large amount of research results (both experimental and theoretical) accumulated over the last 35 years on the compound semiconductor–insulator interfaces, we have learned that the aspects of (1) surface exposure, stoichiometry, and defects, (2) thermodynamic stability, and (3) intrinsic

Fermi-level pinning have to be addressed in overcoming major sources of interfacial states. Besides the electronic interfacial states, other practical criteria for choosing a passive insulating films include film density, adherence, chemical stability, mechanical stress at the interface, electrical resistivity, and electrical breakdown field strength (67). Oxidation of compound semiconductors by thermal, anodic, or other exotic treatments as discussed in this section produces pinned surfaces. Although deposited insulators are presently used in practical devices, most of them still have a high density of electronic interfacial states, the major difficulty of compound-semiconductor passivation.

Experimentally, deposition in UHV is preferred to minimize surface exposure (particularly to avoid oxidation) and to achieve an atomically ordered, chemically clean, and stoichiometric compound semiconductor surface before the deposition of insulators. However, it is not clear how to avoid the introduction of compound-semiconductor gap states by the electronic structures of the deposited species. With the evaporation of $Ga_2O_3(Gd_2O_3)$ on GaAs and InGaAs, the first compound-semiconductor interfaces with thermodynamic stability and low D_{it} were achieved. Furthermore, with the aiding of a conventional ion-implant technology, the first enhancement-mode GaAs MOSFETs were demonstrated in 1996. Research efforts are now in progress to understand the fundamental aspects of attaining low D_{it} in this novel oxide on GaAs and InGaAs.

BIBLIOGRAPHY

1. C.-T. Sah, Evolution of the MOS transistor—From conception to VLSI, *Proc. IEEE,* **76** (10): 1280–1326, 1988.
2. The Transistor 50th Anniversary: 1947–1997, *Bell Lab. Tech. J.,* **2** (4): Autumn 1997.
3. B. E. Deal and A. S. Grove, General relationship for the thermal oxidation of silicon, *J. Appl. Phys.,* **36**: 3770, 1965.
4. D. Kahng and M. M. Atalla, Silicon–silicon dioxide field induced surface devices, *Solid State Res. Conf.,* Pittsburgh, PA, 1960.
5. M. M. Atalla, E. Tannenbaum, and E. J. Scheibner, Stabilization of silicon surface by thermally grown oxides, *Bell Syst. Tech. J.,* **38** (3): 749–783, 1959.
6. K. F. Schuegraf and C. Hu, Reliability of thin SiO_2, *Semicond. Sci. Technol.,* **9**: 989–1004, 1994.
7. J. R. Ligenza, *J. Appl. Phys.,* **36**: 2703, 1965.
8. I. W. Boyd, *J. Appl. Phys.,* **54**: 5361, 1983.
9. L. G. Meiners, *J. Vac. Sci. Technol.,* **21**: 655, 1982.
10. K. Kobayashi et al., *Symp. VLSI Technol.,* 1990, p. 119.
11. W. H. Lee et al., *Symp. VLSI Technol.,* 1997, p. 117.
12. Y. Takashi et al., *Tech. Dig., Int. Electron Devices Meet. (IEDM '94),* San Francisco, 1994, p. 839.
13. H. S. Kim, S. A. Campbell, and D. C. Gilmer, *IEEE Electron Devices Lett.,* **18** (10): 465.
14. C. T. Liu, Circuit requirement and integration challenges of thin gate dielectrics for ultra-small MOS transistors, *Tech. Dig. Int. Electron Devices Meet. (IEDM '98),* San Francisco, (to be published).
15. R. C. Jaeger, *Introduction to Microelectronic Fabrication,* Modular Series on Solid State Devices, New York: Addison-Wesley, 1990.
16. C. T. Liu et al., Light nitrogen implant for preparing thin gate oxides, *IEEE Electron Devices Lett.,* **18** (3): 105, 1997.
17. C. T. Liu et al., 2.5 nm gate oxide without boron penetration for 0.25 and 0.3 μm PMOSFETs, *Dig. Tech. Pap., Symp. VLSI Technol.,* 1996, p. 18.
18. C. T. Liu et al., High performance 0.2 μm CMOS with 2.5 nm gate oxide grown on nitrogen implanted Si substrates, *Tech. Dig., Int. Electron Devices Meet. (IEDM '96),* San Francisco, 1996, p. 499.
19. Courtesy of F. H. Baumann of Bell Labs, Lucent Technologies, Murray Hill, NJ.
20. C. Kittel, *Introduction to Solid-State Physics,* New York: Wiley, 1956, 2nd ed.
21. N. Gonon et al., Growth and structure of rapid thermal silicon oxides and nitroxides studied by spectroellipsometry and Auger electron spectroscopy, *J. Appl. Phys.,* **76** (9): 5242, 1994.
22. S. J. Fang et al., Comparison of Si surface roughness measured by atomic force microscopy and ellipsometry, *Appl. Phys. Lett.,* **68** (20): 2837, 1996.
23. Z. H. Lu, in E. Garfunkel (ed.), *Fundamental Aspects of Ultrathin Dielectrics on Si-based Devices,* Amsterdam: Kluwer, 1998, pp. 49–63.
24. R. B. Fair, Physical models of boron diffusion in ultrathin gate oxides, *J. Electrochem. Soc.,* **144** (2): p. 708, 1997.
25. D. M. Brown and P. R. Kennicott, *J. Electrochem. Soc.,* **118**: 293, 1971.
26. H. G. Pomp et al., Lightly N_2O nitrided dielectrics grown in a conventional furnace for E2PROM and 0.25 μm CMOS, *Tech. Dig., Int. Electron Devices Meet. (IEDM '93),* Washington, DC, 1994, p. 463.
27. L. K. Han et al., Highly suppressed boron penetration in NO-nitrided SiO_2 for p^+ poly-Si gated MOS device applications, *IEEE Electron Devices Lett.,* **16** (7): 319, 1995.
28. C. T. Liu et al., Preventing boron penetration through 2.5 nm gate oxides with nitrogen implant in the Si substrates, *IEEE Electron Devices Lett.,* **18** (5): 212, 1997.
29. J. M. Sung et al., Fluorine effects on boron penetration of p^+ gate devices, *Tech. Dig., Int. Electron Devices Meet. (IEDM '94),* San Francisco, 1994, p. 447.
30. C. T. Liu et al., A new mode of hot carrier degradation in 0.18 μm CMOS technologies, *Dig. Tech. Pap., Symp. VLSI Technol.,* 1998.
31. E. H. Nicollian and J. R. Brews, *MOS Physics and Technology,* New York: Wiley, 1982.
32. C. T. Liu et al., Intrinsic and stress-induced traps in the direct tunneling current of 2.3–3.8 nm oxides and unified characterization methodologies of sub-3 nm oxides, *Tech. Dig., Int. Electron Devices Meet. (IEDM '97),* Washington, DC, 1997, p. 85.
33. M. Depas, T. Nigam, and M. M. Heyns, Soft breakdown of ultra-thin gate oxide layers, *IEEE Trans. Electron Devices,* **43** (9): 1499, 1996.
34. C. T. Liu et al., Reduced $1/f$ noise and G_m degradation for sub-0.25 μm MOSFETs with 2.5–5 nm gate oxides grown on nitrogen implanted Si substrates, *Proc. 55th Device Res. Conf.,* Colorado, 1997, p. 124.
35. Z. J. Ma et al., New insight into high-field mobility enhancement of nitrided-oxide n-MOSFET's based on noise measurement, *IEEE Trans. Electron Devices,* **41** (11): 2205, 1994.
36. F. Ren et al., *IEDM Tech. Dig.,* 1996, p. 943.
37. D. L. Lile, in C. W.Wilmsen (ed.), *Physics and Chemistry of III–V Compound Semiconductor Interfaces,* New York: Plenum, 1985, p. 332.
38. K. Navratil, I. Ohlidal, and F. Lukes, *Thin Solid Films,* **56**: 163, 1979.
39. G. P. Schwartz, *Thin Solid Films,* **103**: 3, 1983.
40. C. Wilmsen, *J. Vac. Sci. Technol.,* **19** (3): 279, 1981.

41. W. T. Tsang, *Appl. Phys. Lett.,* **33**: 429, 1978.
42. D. Butcher and B. Sealy, *Electron. Lett.,* **13**: 558, 1977.
43. L. M. Terman, *Solid-State Electron.,* **5**: 285, 1962.
44. J. Dalesasse et al., *Appl. Phys. Lett.,* **57**: 2844, 1990.
45. R. Naone and L. Coldren, *J. Appl. Phys.,* **82**: 2270, 1997.
46. E. Chen, N. Holonyak, Jr., and S. Maranowski, *Appl. Phys. Lett.,* **66** (20): 2688, 1995.
47. N. Holoynak, Jr. and J. Dallesasse, U.S. Patent No. 5,262,360, 1993.
48. K. Choquette et al., *IEEE J. Sel. Top. Quantum Electron.,* **3**: 916, 1997.
49. C. W. Wilmsen, in C. W. Wilmsen (ed.), *Physics and Chemistry of III–V Compound Semiconductor Interfaces,* New York: Plenum,1985, p. 435.
50. H. L. Hartnegal and R. Reimenschneider, in M. R. Brozel and G. E. Stillman (eds.), *Properties of Gallium Arsenide,* London: INSPEC, Institution of Electrical Engineers, 1996, 3rd ed., p. 482.
51. A. Revesz and K. Zaininger, *J. Amer. Ceram. Soc.,* **46**: 606, 1963.
52. R. Logan, B. Schwartz, and W. Sundburg, *J. Electrochem. Soc.,* **120**: 1385, 1973.
53. H. Hasegawa, K. Forward, and H. Hartnagel, *Appl. Phys. Lett.,* **12**: 567, 1975.
54. P. Schmuki et al., *J. Appl. Phys.,* **79** (9): 7303, 1996.
55. B. Bayraktaroglu, E. Kohn, and H. Hartnagel, *Electron. Lett.,* **12** (2): 53, 1976.
56. E. Kohn and A. Colquhoun, *Electron. Lett.,* **13**: 73, 1977.
57. O. Weinreich, *J. Appl. Phys.,* **37**: 2924, 1966.
58. R. Chang and A. Sinha, *Appl. Phys. Lett.,* **29**: 56, 1976.
59. T. Mimura et al., *IEEE Trans. Electron. Devices,* **25**: 573, 1978.
60. S. Ingrey, W. M. Lau, and N. S. McIntyre, *J. Vac. Sci. Technol. A,* **4**: 637, 1985.
61. G. Hollinger, R. Skheyta-Kabbani, and M. Gendry, *Phys. Rev. B,* **49**: 11159, 1994.
62. G. Cossu et al., *Appl. Surf. Sci.,* **56–58**: 81, 1992.
63. M. G. Proietti et al., *J. Phys. Condens. Matter,* **5**: 1229, 1993.
64. T. Sawada, H. Hasegawa, and H. Ohno, *Jpn. J. Appl. Phys.,* **26**: L1871, 1987.
65. H. Hasegawa et al., *J. Vac. Sci. Technol. B,* **5** (4): 1097, 1987.
66. J. Alay, W. Vandervorst, and H. Bender, *J. Appl. Phys.,* **77** (7): 3010, 1995.
67. H. Hasegawa, in M. R. Brozel and G. E. Stillman (eds.), *Properties of Gallium Arsenide,* London: INSPEC, Institution of Electrical Engineers, 1996, 3rd ed., p. 447.
68. H. Becke, R. Hall, and J. White, *Solid-State Electron.,* **8**: 812, 1965.
69. S. Tiwari, S. Wright, and J. Batey, *IEEE Electron. Devices Lett.,* **9** (9): 488, 1988.
70. J. Freeouf et al., *Appl. Phys. Lett.,* **57** (18): 1919, 1990.
71. A. Callegari et al., *Appl. Phys. Lett.,* **54** (4): 332, 1989.
72. E. S. Aydil et al., *J. Vac. Sci. Technol. B,* **11**: 195, 1993.
73. M. Hong et al., *J. Vac. Sci. Technol. B,* **14** (3): 2297, 1996.
74. M. Hong et al., *Solid-State Electron.,* **41**: 643–646, 1997.
75. M. Passlack et al., *IEEE Trans. Electron Devices,* **44** (2): 214–225, 1997.
76. F. Ren et al., *Solid-State Electron.,* **41** (11): 1751, 1997.
77. M. Hong et al., *J. Vac. Sci. Technol.,* **B16** (3): 1398, 1998.
78. M. Hong et al., *J. Vac. Sci. Technol.,* **B16** (3): 1395, 1998.
79. M. Hong et al., in H. Q. Hou et al. (eds.), *State-of-the-Art Program on Compound Semiconductors XXVII,* Princeton, NJ: Electrochemical Society, 1998.
80. S. Yokoyama et al., *Surf. Sci.,* **86**: 835, 1979.
81. Y. H. Jeong, K. H. Choi, and S. K. Jo, *IEEE Electron Devices Lett.,* **15** (7): 251, 1994.
82. J. Reed et al., *J. Appl. Phys.,* **75** (3): 1826, 1994.
83. C. L. Chen et al., *IEEE Electron Devices Lett.,* **12** (6): p. 306.
84. C. L. Chen et al., *IEEE Electron Devices Lett.,* **17** (8): 413, 1996.
85. C. L. Chen et al., *Electron. Lett.,* **32** (4): 407, 1996.
86. Z. H. Lu and M. J. Graham, *Phys. Rev. B,* **48**: 4604, 1993.
87. A. S. H. Liao et al., *Appl. Phys. Lett.,* **41**: 280, 1982.
88. H. H. Wieder et al., *IEEE Electron Devices Lett.,* **EDL-2**: 73, 1981.
89. F. Schulte et al., *Proc. 4th Int. Conf. InP Relat. Matter.* RI, 1992, pp. 503–506.
90. L. C. Upadhyayula et al., *IEEE Electron Devices Lett.,* **7**: 390–392, 1986.
91. A. Nelson, K. Geib, and C. Wilmsen, *J. Appl. Phys.,* **54**: 4134,1983.
92. J. McLaren et al., *J. Vac. Sci. Technol. A,* **1**: 1486, 1983.
93. Z. H. Lu et al., *Appl. Phys. Lett.,* **60**: 2773, 1992.
94. K. Kato et al., *J. Vac. Sci. Technol. A,* **2**: 588, 1984.
95. Wilmsen, *CRC Crit. Rev. Solid State Sci.,* **5**: 313, 1975.
96. L. Messick, D. Lile, and A. Clawson, *Appl. Phys. Lett.,* **32**: 494, 1978.
97. H. Hibb et al., *Thin Solid Films,* **310** (1–2): 1, 1997.
98. M. Korwin-Pawlawski and E. Heasell, *Phys. Status Solidi A,* **27**: 339, 1975.
99. A. Rosenberg and M. Levine, *J. Phys. Chem.,* **64**: 1135, 1960.
100. G. Houston et al., *Semicond. Sci. Technol.,* **12** (9): 1140, 1997.
101. C. Stahle, C. Helms, and A. Simmons, *J. Vac. Sci. Technol. B,* **5** (4): 1092, 1987.
102. S. Wolter et al., in C. Abernathy, H. Amano, and J. Zolper (eds.), *Gallium Nitride and Related Materials II,* San Francisco: 1997.
103. S. C. Binari, *Proc. Electrochem. Soc.,* **95** (21): 136, 1995.
104. W. Kruppa, S. C. Binari, and K. Doverspike, *Electron. Lett.,* **31**: 1951, 1995.
105. F. Ren et al., *MRS Fall Mtg. Symposium D Nitride Semiconductor Materials,* 1997 (to be published).

M. Hong
C. T. Liu
Bell Laboratories, Lucent Technologies
H. Reese
University of California
J. Kwo
Bell Laboratories, Lucent Technologies