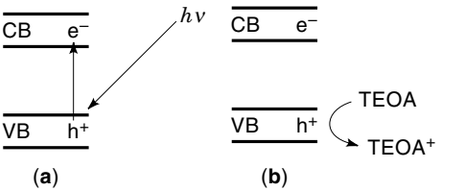

Figure 1. An example on the band diagram of a photo-induced surface electron accumulation layer is shown. (a) Holes and electrons are generated due to the shining of light. (b) The holes are subsequently removed by the hole scavenger TEOA.

ACCUMULATION LAYERS

An accumulation layer is a region in a semiconductor where a free carrier concentration exceeds that provided by dopants. The carriers can be electrons or holes. Accumulation layers exist in many solid state devices, such as microelectronics, optoelectronics, sensors, and solar cells. They are critical to the performance of these devices. The accumulation layer is usually located on the surface, in the bulk, or at the interface of a semiconductor and another film.

SURFACE AND BULK ACCUMULATION LAYERS

The surface accumulation layer is often formed by exposing the semiconductor surface to an optical, plasma, or chemical source. For example, when a nanocrystalline titanium dioxide film immersed in an aqueous solution is illuminated with a 380 nm wavelength light, holes and electrons are generated on the surface. When these holes are instantaneously removed by the hole scavenger, that is, triethanolamine (TEOA), in the solution, the surface contains an electron-rich accumulation layer. Figure 1 shows the band diagrams of this process (1). In other cases, an accumulation layer is formed on the ZnO surface that is exposed to a plasma source or is in contact with an electrolyte solution (2,3). There are many reports that an electron or a hole accumulation layer is formed on a semiconductor surface by depositing a tiny amount of element or a very thin film on top of it. Characteristics of these surface accumulation layers are commonly used to fabricate devices such as sensors.

The accumulation layer can exist in the bulk of a semiconductor, such as GaAs and InP (4). It starts from the locally excess charges, which could be due to the crystal defects, the nonuniform doping, the random noise fluctuation, and so on. When an electric field greater than a certain value is applied across this semiconductor, an accumulation layer can be formed and moved along the current path. This phenomenon is commonly applied to high-frequency microwave devices.

INTERFACE ACCUMULATION LAYERS

For most microelectronics applications, the term "accumulation layer" means the interface accumulation layer located at the interface of two films, such as between two semiconductors, between one semiconductor and one metal, or between one semiconductor and one insulator. An accumulation layer is formed from the potential difference in a specific region of the semiconductor, which bends its energy band. The potential difference can be originated from the intrinsic material properties or from the application of an external force, such as an electrical potential, optical illumination, or radiation exposure.

For example, for a crystalline heterojunction structure, the lattice mismatch between two semiconductors can cause the band bending of a semiconductor layer and generate an interface accumulation layer (5). In another case, when two amorphous semiconductors are in contact and their Fermi levels are aligned, there is a band bending at the interface. This

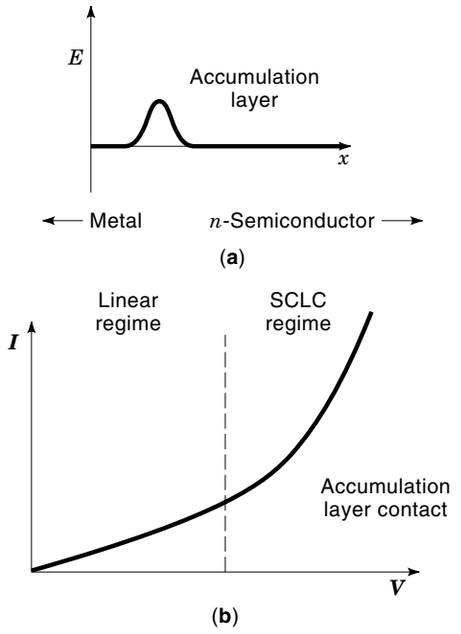

Figure 2. (a) The electric field E peaks at the interface of a metal and an n-type semiconductor due to the existence of an accumulation layer. (b) The current–voltage curve of a metal–semiconductor contact structure is a function of the carrier concentration. At the low-voltage region, the contact injects sufficient carriers for the bulk semiconductor. At the high-voltage region, the accumulation layer functions as a carrier reservoir, which adjusts its current supply with the voltage.

kind of accumulation layer is commonly found in quantum well devices.

Under a proper bias condition, an accumulation layer can be formed at a semiconductor interface when it is in contact with a metal. For example, Fig. 2(a) shows an electric field distribution of the accumulation layer at the metal–n-type semiconductor contact (6). The current–voltage characteristics of the above contact are shown in Fig. 2(b). In the low-voltage range, the current increases linearly with the voltage due to the sufficient supply of majority carriers from the contact. In the high-voltage range, the current supply is in the space charge limited current (SCLC) regime. It increases proportionally to the square of the voltage because of the existence of the accumulation layer. The contact with an accumulation layer functions as a carrier reservoir that adjusts itself with the current demand of the bulk semiconductor. This is called "ohmic" contact, which has a contact resistance lower than the bulk resistance. If the accumulation layer is replaced by a depletion layer, the current at the high-voltage range will increase little with an increase of voltage because of the limited supply of carriers. This is called "blocking" contact, which has a contact resistance much higher than the bulk resistance. The accumulation layer at the metal–semiconductor contact is most important to all devices that require a minimum contact resistance.

An insulator film, such as silicon oxide or silicon nitride, usually contains positive charges that are fixed or trapped in the bulk, at the surface, or at the interface with a semiconductor film. These charges can bend the energy band of the adjacent semiconductor and induce an accumulation layer at the interface. Figure 3 shows the charge distribution in a metal–insulator–semiconductor (MIS) structure, which has a positive charge of Q_0 residing in the insulator layer. No voltage is applied to the metal. The two groups of negative charges—that is, one at the metal interface ($-Q_m$) and the other one at the semiconductor interface ($-Q_s$)—are induced by charges in the insulator layer. In addition to the semiconductor properties, such as the dopant type and concentration, the amount of charges accumulated at the semiconductor interface is a function of the location, distribution, and density of the charges in the insulator layer. They are determined by the film's composition, morphology, dangling bond concentration, deposition condition, and mobile ion contamination. This type of accumulation layer has been observed in various film deposition sequences, such as silicon nitride on top of an n-type silicon wafer or a plasma enhanced chemical vapor deposition (PECVD) amorphous silicon (a-Si : H) film above a PECVD silicon nitride (SiN_x) film (7,8).

The MIS structure is most commonly used to study the characteristics of the semiconductor–insulator interface accumulation layer. For example, an accumulation layer can be induced by the work function difference (Φ_{ms}) between the metal (Φ_m) and the semiconductor (Φ_s). Figure 4(a) shows the band diagram of the electron accumulation layer induced by a negative Φ_{ms} between the metal and the n-type semiconductor. Figure 4(b) shows the hole accumulation layer formed from a positive Φ_{ms} between the metal and the p-type semiconductor. Any factor that affects the Φ_{ms} value can influence the accumulation layer process. For example, when the metal layer is replaced by another conductor, such as a heavily doped silicon, the Φ_m changes. The Φ_s of a semiconductor is a function of its band gap energy, crystallinity, interface states, dopant type, and concentration. Figure 5 shows the relation among Φ_{ms} and various material parameters of a metal oxide–

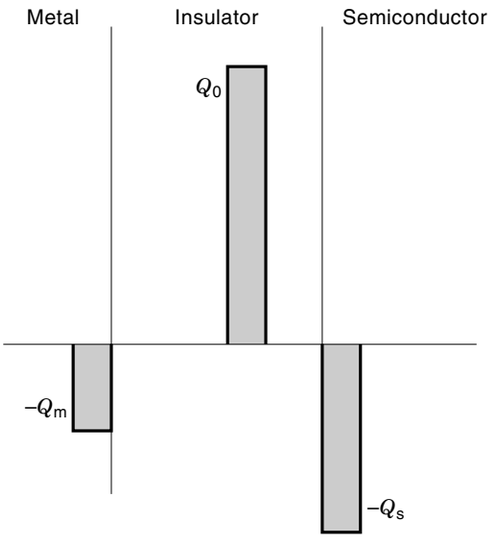

Figure 3. Interface accumulation can be formed by the induction of positive charges in the insulator layer in an MIS structure without biasing the metal electrode. The amount of charges at the semiconductor interface is a function of the semiconductor properties as well as the location and density of charges in the insulator layer.

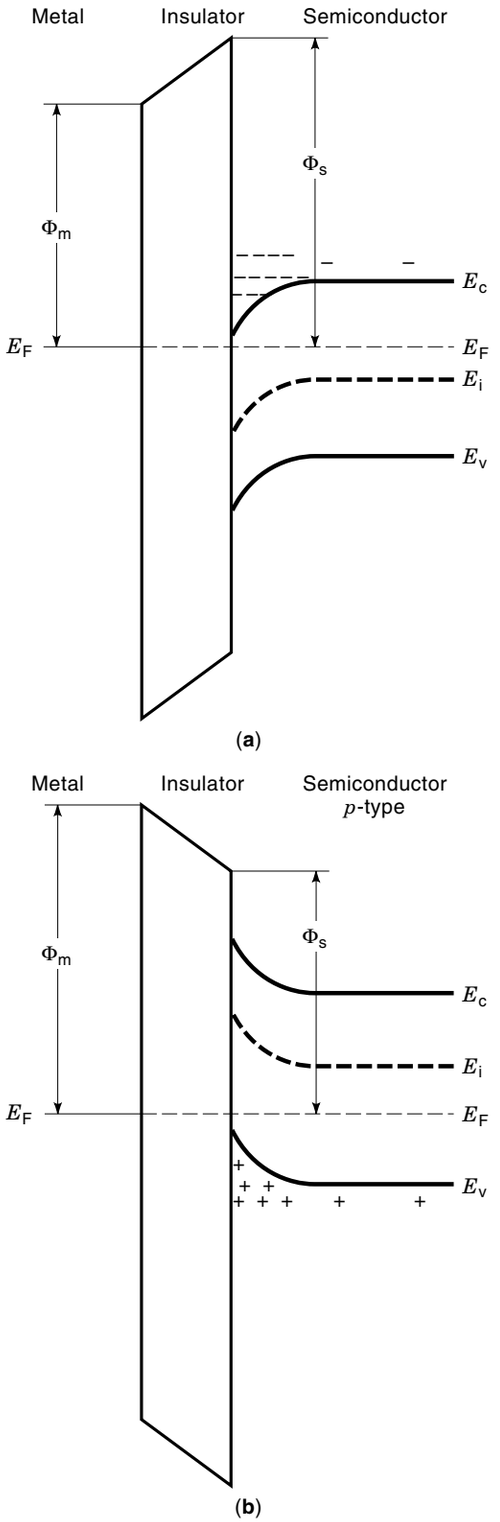

Figure 4. (a) An electron accumulation layer is formed at the *n*-type semiconductor interface of an MIS due to the negative Φ_{ms}. No voltage is applied to the gate electrode. (b) A hole accumulation layer is formed at the *p*-type semiconductor interface of an MIS due to the positive Φ_{ms}. No voltage is applied to the gate electrode.

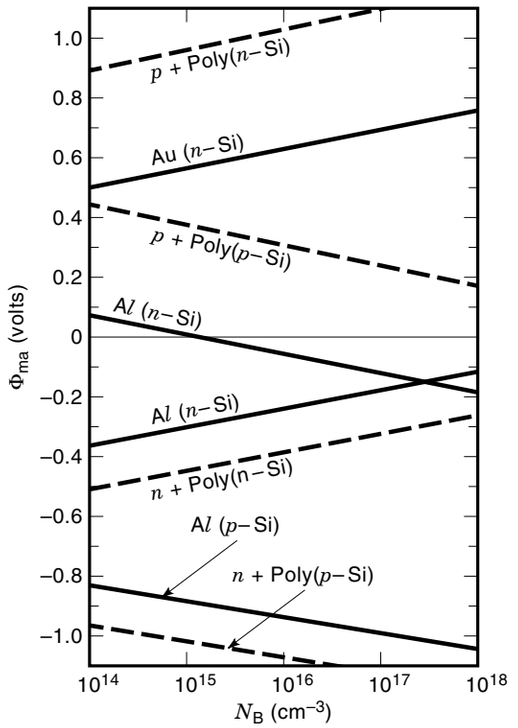

Figure 5. The work function difference Φ_{ms} of a MOS is dependent on the type of metal, which includes heavily doped semiconductors, and the properties of the semiconductor, such as the dopant type and concentration.

semiconductor (MOS) (9). When the material properties of a MOS structure are known, one can use the Φ_{ms} value in Fig. 5 as a first-order estimation to predict if an accumulation layer is formed at the interface. The charge content and location in the insulator layer should also be taken into consideration. In general, only certain combinations of materials can induce the accumulation layer formation without requiring an external electric potential.

CHARACTERIZATION OF MIS ACCUMULATION LAYERS

For most microelectronic or optoelectronic device applications, the accumulation layer is formed by applying an electric potential perpendicular to the insulator–semiconductor interface. Since this potential can be much higher than the Φ_{ms}, many restrictions on the selection of thin film materials are eliminated. Figures 6(a) and 6(b) show the band bending diagrams of accumulation layers due to the application of external potentials (9). For the *n*-type semiconductor, a positive potential is required to generate an electron accumulation layer; for the *p*-type semiconductor, a negative potential is required to generate a hole accumulation layer. The carrier concentration decreases from the interface to the bulk of the semiconductor. The motion of electrons in the accumulation layer is quantized in the direction normal to the interface (10). Therefore we have a quasi-two-dimensional system in the accumulation layer.

Since the accumulation layer is a high carrier-concentration region extending from the surface to the bulk of the semi-

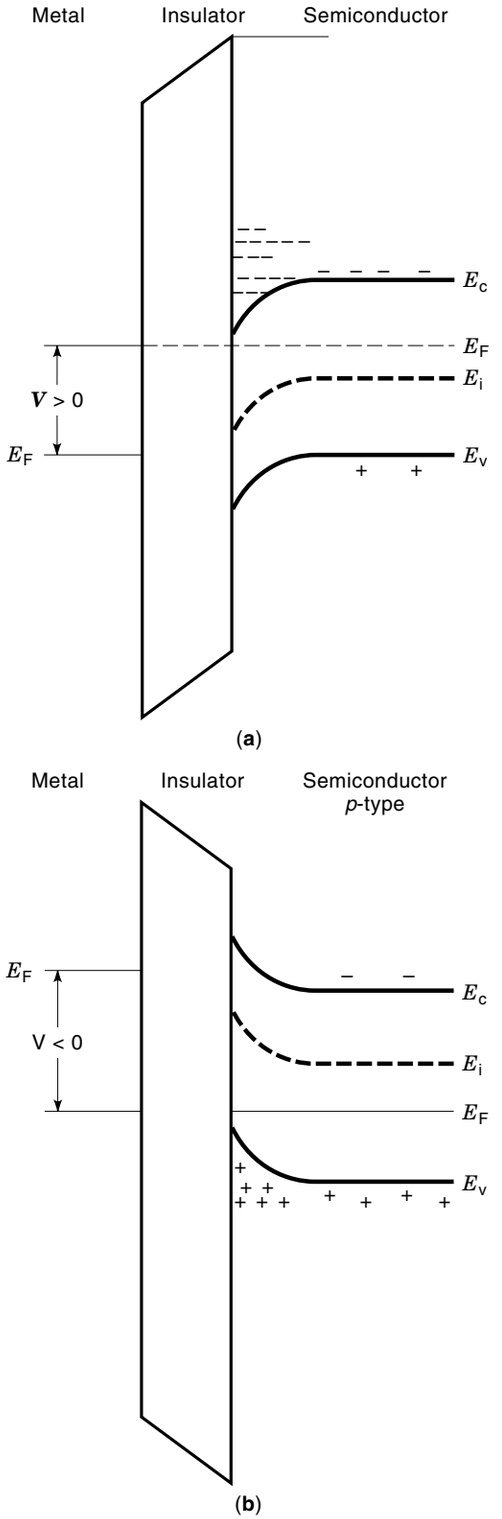

Figure 6. (a) An electron accumulation layer is formed at the *n*-type semiconductor interface of an MIS due to the application of a positive voltage to the gate electrode. (b) A hole accumulation layer is formed at the *p*-type semiconductor interface of an MIS due to the application of a negative voltage to the gate electrode.

conductor layer, it is important to know (1) what the highest charge density is in this region, that is, charge per unit area Q_s at the semiconductor surface; and (2) how deep this accumulation layer penetrates into the bulk of the semiconductor. An approximate method of calculating Q_s is shown in Eq. (1):

$$Q_s \approx e^{(q|\Psi_s|/2kT)} \tag{1}$$

where q is the electronic charge, Ψ_s is the semiconductor's surface potential, k is Boltzmann's constant, and T is the absolute temperature (K). A detailed derivation of the more complete equation can be found in Ref. 9. This equation clearly shows that the charge density at the semiconductor surface is roughly proportional to the exponential of the surface potential. Since Ψ_s is the metal voltage minus the voltage drop across the insulator, the interface charge density is tremendously influenced by the gate voltage.

The exact thickness of the accumulation layer is difficult to determine because the carrier concentration decreases gradually and smoothly. However, the extrinsic Debye length L_D is a good reference of this layer thickness. Physically, all carriers that are located at a distance longer than the Debye length from the semiconductor surface are shielded from the potential applied to the semiconductor surface. For the *p*-type silicon MOS, the extrinsic Debye length is defined as

$$L_D = (kT\epsilon_s/P_{p_0}q^2)^{1/2} \tag{2}$$

where ϵ_s is the permittivity of the semiconductor and P_{p_0} is the equilibrium hole concentration in the bulk silicon (11). Therefore the Debye length decreases with the increase of the carrier concentration. The higher the dopant concentration is, the shorter is the depth of the accumulation layer.

Capacitance–Voltage Measurement

The simplest method to characterize the accumulation layer of a MIS diode is to measure the capacitance–voltage ($C-V$) curve. Figure 7(a) shows a MOS capacitor and an equivalent circuit. The space charge region can be a carrier concentration or depletion area. Figure 7(b) shows the $C-V$ curves of a MOS with the *p*-type silicon substrate. Two frequencies, that is, a low frequency (LF) and a high frequency (HF), are used in the test (11). Previously, it was shown in Fig. 6(b) that, for this kind of diode, an accumulation layer is formed by applying a negative voltage to the metal electrode. This phenomenon is not influenced by the measurement frequency. When the voltage is moved from negative toward zero, the carrier concentration in the accumulation layer is lower and is close to the bulk carrier concentration. The depth of the accumulation layer becomes wider. When the voltage increases further into the positive range, the semiconductor forms a depletion layer and eventually an inversion layer.

The total capacitance of the capacitor in Fig. 7(a) results from two sources: one from the silicon oxide C_{ox} and the other one from the bulk silicon C_s, connected in series. In Eq. (1), we see that the semiconductor's surface charge density Q_s increases with the surface potential. Therefore, when the gate voltage is highly negative, the accumulation layer contains a very high concentration of carriers and acts like a metal plate. The total capacitance is close to that of the silicon oxide layer.

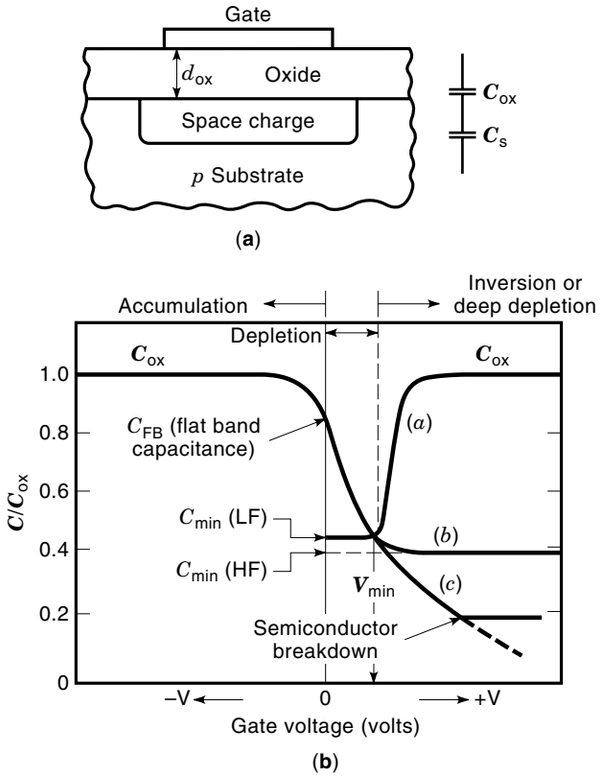

Figure 7. (a) A MOS capacitor is composed of two capacitors—one with oxide insulator layer and the other one with the silicon layer, connected in series. The space charge layer may be a carrier accumulation or depletion region, depending on factors such as the type of dopant in the semiconductor substrate and the voltage applied to the gate electrode. (b) The capacitor–voltage curves of a MOS can be used to delineate the operation range of the accumulation layer. The substrate is a p-type silicon. The flat band capacitance C_{FB} is the capacitance at $\Psi_s = 0$. An accumulation layer is formed when a negative voltage is applied to the gate.

The total capacitance of the MOS is defined as the flat band capacitance (C_{FB}) at $\Psi_s = 0$. The $C - V$ curve can be shifted along the voltage axis by factors such as the fixed charge density in the oxide layer or the work function difference Φ_{ms}. The shape of the curve is stretched if the charge in the fast surface states is high. Therefore the C_{FB} shifts with the curve. Under the conditions of (1) $\Phi_{ms} = 0$ and (2) no charges existing in the bulk of the insulator film or at the insulator–silicon interface, one can estimate C_{FB} using the following equation:

$$C_{FB} = C_{ox}/[1 + (\epsilon_{ox}/\epsilon_s)(L_D/d)] \tag{3}$$

where d is the insulator (i.e., oxide) layer thickness. A detailed derivation of this equation can be found in Ref. 9. We can extract the C_{FB} value from an experimental $C - V$ curve and then back-calculate the Debye length L_D using Eq. (3). Therefore the limitation of the depth of the accumulation layer is obtained.

In summary, the $C - V$ measurement is an effective tool in evaluating the accumulation layer properties, such as the maximum charge density at the semiconductor surface and the layer thickness.

APPLICATIONS

The surface accumulation layers are most often used in sensors or detectors. However, the interface accumulation layers are widely applied in many microelectronic or optoelectronic devices. One can improve the device performance by controlling factors that influence the accumulation layer formation, such as selection of proper materials, lowering the film–film stress, and optimizing fabrication processes. On the other hand, an improper accumulation layer can deteriorate the device. For example, the accumulation layer on the ZnO surface of a pin diode cell (p layer on ZnO-coated SnO_2:F) causes the low filling factor. This problem is solved by introducing a μc-n Si layer between ZnO and the p layer (3). A strong electron accumulation layer can be formed at the interface of amorphous silicon (a-Si:H) and a SiN_x film. It induces a high leakage current on the back channel of an inverted, staggered thin film transistor (TFT). The leakage current can be suppressed with a proper SiN_x composition.

Table 1 lists some examples of device applications of accumulation layers. The location of the accumulation and the types of carriers are also included. These devices include a wide range of materials, for example, single crystal silicon, amorphous silicon (a-Si:H), and III-V compounds for semiconductors; and silicon oxide, silicon nitride, and undoped $Al_xGa_{1-x}As$ for insulators. The criteria of metal selection are dependent on device applications. For MOS transistors, the

Table 1. Example of Device Applications of Accumulation Layers

Devices	Examples	Location of Accumulation Layer	Carrier Type
Diode	MOS capacitor	In silicon interface	Electrons or holes
	Photoluminescence (12)	In n-type InP near interface	Electrons
	Gunn	In bulk GaAs or InP	Electrons
	Resonant-tunneling light-emitting diode (RTLED) (14)	Near $Al_{0.14}Ga_{0.86}As$ shallow barrier layer	Holes
Heterostructure	Quantum dots (13)	In quantum wells near interface	Electrons
	Heterojunction phototransistor (15)	In p-GaAs base layer	Holes
Transistors	Bipolar	In emitter	Electrons
	MOS	In single crystalline silicon interface	Electrons or holes
	a-Si:H TFTs	In a-Si:H interface	Electrons

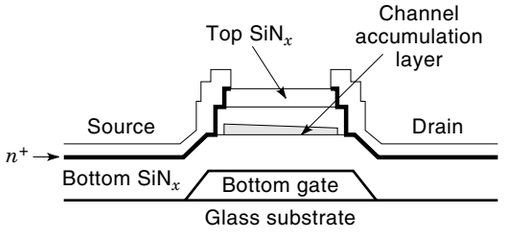

Figure 8. The cross-section view of an inverted, staggered, trilayer TFT can be used to express the relationship between the accumulation layer and the operation of the transistor. At the on-stage, the current flows through a thin accumulation layer adjacent to the gate dielectric interface.

low threshold voltage V_t is critical. Therefore the minimum work function difference is the preferred character for the gate conductor. For the large-area a-Si : H TFTs, since the V_t is usually high, the low gate conductivity is the most important issue. For field-effect transistors, the channel accumulation layer is connected to the source and drain. Therefore the source and drain contacts should be ohmic to maximize the function of the transistor.

The contribution of an accumulation layer to the device is strongly dependent on the structure. For example, for an MIS, the carrier concentration gradient as well as the potential gradient in the accumulation layer is vertical to the interface of the insulator and the semiconductor. There is no current flowing in the accumulation layer. For an *npn* bipolar junction transistor, the hole accumulation layer is formed in the base region. During the operation, the current flows through the accumulation layer in the same direction as the potential gradient, that is, vertically through emitter, base, and collector. For the operation of a MOS transistor or a TFT, the source to drain current flows through the channel accumulation layer in the direction parallel to the interface of the insulator and the semiconductor. Therefore any structure change in these devices can affect the location and generation mechanism of the accumulation layer, which either enhances or deteriorates the device performance.

One example of structure influence on the accumulation layer is the *n*-AlGaAs/*p*-GaAs/*n*-InGaAs heterojunction phototransistor (HPT) (15). This transistor has a bipolar structure with a multiple quantum well (MQW) collector. The device performance is strongly dependent on the hole accumulation in the base. The lattice mismatch in the quantum well can influence the defects in the base layer. When the quantum well thickness increases, the concentration of the mismatch-induced dislocations increases. There exists a critical thickness above which the dislocations become so serious that the hole accumulation in the base region decreases. This results in the reduction of the current gain in the transistor.

Another example of structure influence is the single-gate multichannel TFT. Figure 8 shows the structure and the on-state current path of an inverted, staggered, trilayer a-Si : H TFT. The typical a-Si : H layer thickness is less than 1000 Å. The channel current is restricted to a thin accumulation layer, for example, less than 200 Å from the a-Si : H–gate insulator interface. This accumulation layer is induced by the gate voltage (16). A detailed discussion of the TFT subject can be found in THIN FILM TRANSISTORS.

Figures 9(a) and 9(b) show the cross-section view of a single-gate, three-channel TFT and its transfer characteristics (17). The transfer characteristics curve of a conventional single-channel TFT is also included for comparison. The single-channel TFT is sharply turned on at the gate voltage V_g of about 2 V. The three-channel TFT is turned on in two stages: first at about −5 V and then at 2 V. For the single-channel TFT, with the increase of V_g, the large number of traps in a Si : H are filled first and the channel electron accumulation layer is then formed. However, for the three-channel TFT, ac-

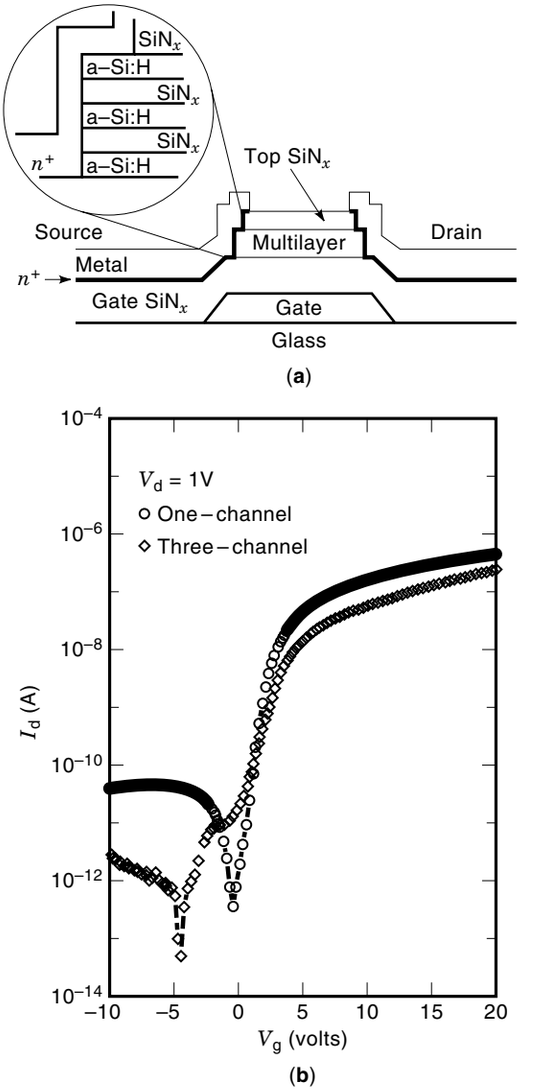

Figure 9. (a) The cross-section view of a single-gate, three-channel TFT is a useful tool in explaining the complicated relationship between the transistor operation and various accumulation layers. All channels share the same gate, source, and drain. (b) Transfer characteristics of the single-channel and the three-channel TFTs are shown in the same figure. The single-channel TFT has a sharp turn-on mechanism. The three-channel TFT has a two-stage turn-on mechanism due to the involvement of several electron accumulation layers at interfaces of a-Si : H and SiN_x.

cumulation layers formed locally at all the a-Si : H–insulator interfaces play important roles. When V_g increases from highly negative to less negative, the transistor function starts from filling traps in all three channels. If the three channel TFT is taken as a single-channel TFT, the channel can be taken as *n*-type because of the many electron-rich local accumulation layers at the a-Si : H–insulator interfaces. Therefore a negative gate voltage is required to shift the Fermi level to the minimum conduction band at low V_g (18). The TFT is turned on at a negative V_g. As the V_g increases further, the gate-induced electron accumulation layer starts to form. Since the bottom channel has the highest potential, a strong accumulation layer is in this channel. The TFT functions like a conventional single-channel TFT with the further increase of V_g. Therefore the accumulation layer formation mechanism in a TFT is affected by its structure.

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