THIN FILM DEVICES

An electronic device is classified as a *thin film device* when it is made from one or more thin films of conductor, insulator, or semiconductor, deposited onto a carrier substrate, which is not generally part of the device itself. The devices are called "passive" when they exhibit only simple resistive, capacitive, or inductive properties, but are "active" when they are capable of nonlinear, diode or transistor action. It is the active transistor and diode devices which are considered here. Thin film transistors (TFTs) [by which we mean field effect transistors (FETs) rather than bipolar junction transistors] have been studied from the early days of semiconductor devices in the 1950s, and a whole range of semiconducting materials have been investigated including cadmium selinide, cadmium sulfide, indium arsenide, lead telluride, tellurium, germanium, and of course silicon. An interesting historical review is given by Brody (1). However, only hydrogenated amorphous silicon (αSi : H) and polycrystalline silicon (poly-Si) are in significant usage today; and the main areas of application are in the field of "large area electronics" (LAE), which includes active matrix liquid crystal displays (AMLCDs), image sensors, x-ray sensors, memories, and fingerprint scanners. Poly-Si TFTs show much improved performance in comparison with αSi : H TFTs, allowing circuit functions to be added in addition to simple matrix switching but at the expense of a more complex device fabrication process. AMLCD principles and amorphous silicon TFTs are described elsewhere. The rest of this article describes thin film transistor principles from a poly-Si TFT perspective, and it refers to amorphous silicon only in conjunction with the diodes and photodiodes which are used in large-area electronics.

POLYCRYSTALLINE SILICON THIN FILM TRANSISTORS

Poly-Si TFTs can be formed on a whole range of substrate materials, including quartz, silicon, glass, and even some plastics such as polyimide and polyethersulfone. There are various methods by which the basic silicon material can be deposited, and by which it is converted into polycrystalline material. Furthermore, the electrical performance of TFTs made in these films depends strongly upon these methods and upon the way they are implemented in a complete device process.

Material Properties

Polycrystalline silicon is made up of many small crystallites with varying grain size and crystallographic orientation, and

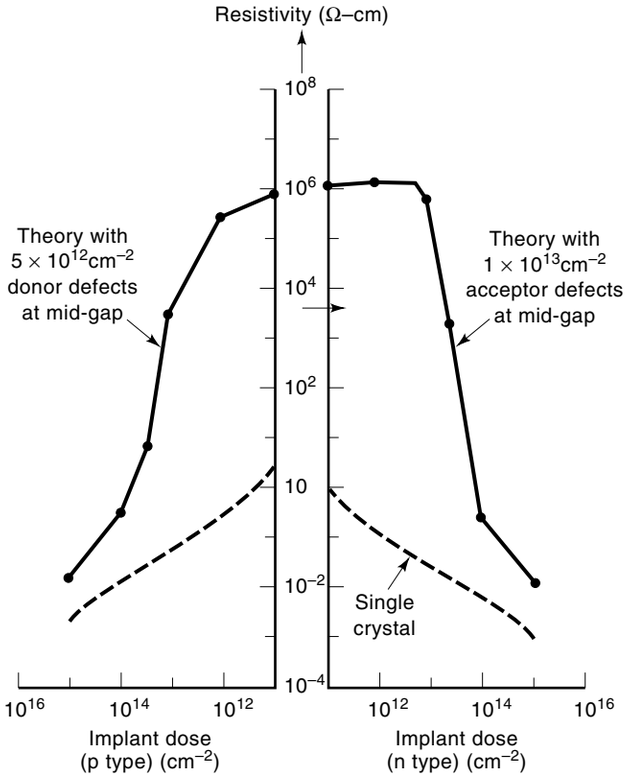

Figure 1. The resistivity of *n*- and *p*-doped poly-Si compared with that of mono-Si. The curve fitted to the poly-Si data is based upon the model of Seto (7).

these are delineated by grain boundaries where there is a lattice mismatch between the adjacent grains. There are crystallographic defects at the grain boundaries, and to a lesser extent in the bulk of the grains, which influence the electrical properties of the material. There are three commonly used techniques for forming poly-Si: (1) the direct deposition of poly-Si by low pressure chemical vapor deposition (LPVCD); (2) the deposition of amorphous silicon by one of several techniques, followed by solid-phase crystallization (SPC) of the material at $T \geq 600$°C; (3) the deposition of amorphous silicon followed by liquid-phase crystallization (LPC) of the material at $T \geq 1400$°C using an ArF, KrF, or XeCl excimer laser, or alternatively an argon gas laser. The direct deposition of poly-Si by LPCVD from silane at $T \geq 550$°C leads to a columnar textured material with a grain size of about 0.1 μm (2). This material has a high density of defects both at the grain boundaries and within the grains themselves, and this gives rise to a low electron mobility of 5–10 cm^2/V-s. Amorphous silicon can be deposited by LPCVD from silane at 550°C (or from disilane at 450°C), or by PECVD at 150–300°C, or by RF sputtering at room temperature. Solid-phase crystallization of low-impurity amorphous silicon can be achieved by heating at ≥600°C for long times (e.g., 600°C for 20 h or 700°C for 10 min), leading to larger grain sizes of 0.2–1.0 μm and an electron mobility of 20–50 cm^2/V-s (3). Generally, LPCVD is the preferred method (provided that the substrates can withstand the high temperatures) because PECVD material contains high concentrations of hydrogen and because both PECVD and sputtered materials contain high concentrations of impurities (such as C, N, and O). The time and temperature of the SPC process can be greatly increased by these impurity concentrations. However, they can also be reduced by using certain metal or alloy seeding layers, such as $NiSi_2$ (4). Crystallization from the liquid phase using laser melting leads to grain sizes of 0.1–1.0 μm and a high electron mobility of 100–400 cm^2/V-s (5,6). A high mobility results because the grains and grain boundaries formed are of high quality, with fewer crystallographic defects than the deposited poly-Si and SPC poly-Si films. From an electrical point of view, all of these forms of poly-Si behave as "intrinsic" material unless they are intentionally doped with group III or group V impurities. This is not because the inherent impurity levels are extremely low, but instead because the defect levels (or traps) are relatively high. In this case, any electrons or holes provided by the inherent dopants become trapped at the defects and thus are unable to contribute to conduction. The resistivity of poly-Si is compared to that of single-crystal silicon (mono-Si) in Fig. 1. This shows a transition from conducting to intrinsic behavior when the dopant density is reduced below the defect density. The theoretical curve fitted is based upon an early model for poly-Si of Seto (7) which describes conduction by the thermionic emission of carriers over grain boundaries.

Device Structures

The two most commonly used poly-Si TFT device architectures are shown in Fig. 2. Both structures have the gate electrode at the top of the structure; this is in contrast to αSi : H TFTs, which are most commonly bottom-gated. The poly-Si regions are typically 50 nm or less in thickness to avoid leakage paths at the back interface which cannot be modulated by the gate, and to reduce photosensitivity (8). The source and drain regions (and also the gate region in the case of the self-aligned device) are typically formed by ion implantation of

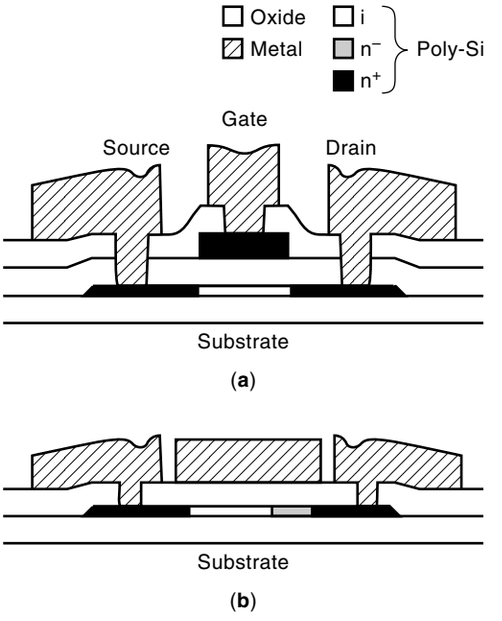

Figure 2. Commonly used poly-Si TFT structures with (a) self-aligned poly-Si gate and (b) gate-overlapped lightly doped drain.

phosphorus (for n-channel devices) or boron (for p-channel devices). In addition, a lightly doped drain (LDD) may be formed by implantation in n-channel devices [as shown in Fig. 2(b)] to reduce the electric field at the drain. The gate oxide is typically 100–150 nm thick and can be formed by a variety of techniques. Thermal oxidation at $T > 900$°C is favored when silicon or quartz substrates are being used; but for lower temperature materials such as glass or plastic, this is not possible, and the oxides are formed alternatively by chemical vapor deposition. Atmospheric pressure chemical vapor deposition (APCVD) can be used on glass substrates, provided that the oxide can be densified at 600°C to remove instabilities related to its porosity to water (9). At lower temperatures, PECVD with helium dilution can be used for the gate oxide, though this material becomes porous below ~230°C (10). A thin (5–10 nm) phosphorus rich (1–3 at%) oxide is often added to the top of the gate dielectric to getter out any alkali metal ion contamination which may occur during device fabrication. Usually, aluminum or an aluminum alloy is chosen for the gate electrode and for source and drain contacts. Defects within the poly-Si and at the $Si–SiO_2$ interface are then reduced as far as possible by furnace bakes in N_2/H_2 at 350–450°C, or by exposure to a hydrogen plasma at 350°C.

Device Characteristics

Figure 3 shows typical current–voltage characteristics of n-channel poly-Si TFTs formed using the excimer laser crystallization of PECVD silicon and using PECVD for the gate oxide. Figures 3(a) and 3(b) show the drain current–gate voltage curves, or "transfer characteristics," on linear and semilogarithmic scales, and Figs. 3(c) and 3(d) similarly show the drain-current–drain-voltage curves, or "output characteristics." These show certain similarities to the characteristics of mono-Si MOSFETs and silicon-on-insulator (SOI) transistors, though most of the basic device parameters are poorer because of the high density of carrier trapping states in the poly-Si. The trapping states are distributed in energy across the band gap in a "U" shape on a semilogarithmic plot, as shown in Fig. 4. This distribution can be measured directly in the devices using deep-level transient spectroscopy (DLTS) (11); or it can be deduced from the temperature dependence of the transfer characteristics, following the method of Fortunato (12). For the purposes of device modeling, the distribution is often approximated by the sum of four exponentials, two describing the "band tail" states near the conduction and valence band edges, respectively, and the other two describing "deep states" in the upper and lower half of the band gap, away from the tail states (13). A similarly shaped distribution of trapping states is seen in αSi:H TFTs, though the total density of states is much higher in that material.

Threshold Voltage. The expressions for the threshold voltage of a MOSFET relate to strong inversion of the semiconductor surface, and this is controlled by the dopant density in the channel (14). Such expressions are not applicable to poly-Si TFTs because the surface potential is governed in a much more complex manner by the distribution of deep states in the bulk of the poly-Si. Commonly, the threshold voltage V_T is defined by plots of drain current I_D versus gate voltage V_G as shown in Fig. 3(a), where a straight line is fitted to the (near) linear data at high gate voltage and is extrapolated to zero drain current. However, if the trapping state density is high enough, and varying rapidly enough across the band gap, then the high gate voltage data can be far from linear, and this extrapolation becomes much more subjective. If small changes in threshold voltage need to be studied during testing (for example, during stability testing) then it is better to define the threshold voltage to be the point at which a specific drain current is reached—that is, at a constant value of surface potential (provided that the state distribution within the poly-Si has not changed too significantly).

Mobility. The field effect mobility μ_f can be deduced from measurements taken in the linear and saturation regions, just as is the practice for MOSFETs. In the linear region (i.e., $V_D \ll (V_G - V_T)$ the mobility is deduced from the slope of the transfer characteristic above the threshold voltage, that is, from the expression

$$\mu_f(V_G) = \left(\frac{L}{W}\right) \cdot \left(\frac{1}{C_i V_D}\right) \cdot \frac{\partial I_D}{\partial V_G}$$

where W is the channel width, L is the channel length, and C_i is the capacitance per unit area of the gate insulator. The mobility can also be obtained from the saturation region (i.e., beyond the pinch-off point) via

$$\mu_f(V_G) = \left(\frac{L}{W}\right) \cdot \left(\frac{1}{C_i(V_G - V_T)}\right) \cdot \frac{\partial I_D}{\partial V_G}$$

though care is necessary with this because (1) V_T is a function of V_G for either high doping or for high defect state densities and (2) poly-Si TFTs can show a "kink effect" (i.e., an unsaturated current) above pinch-off.

Generally, the field effect mobility differs from the band mobility μ_B (as is deduced from Hall effect measurements) because of the band tail states near the conduction band and valence band edges. In the case of an n-channel device, when a positive charge Q_G is put on to the gate electrode, a fraction of it appears as free electrons in the channel qN_e (as measured by the Hall effect) while the rest appears as trapped charge at the defects Q_T, such that

$$Q_G = -qN_e + Q_T$$

Thus, as the gate voltage is varied in field effect measurements, we obtain

$$\frac{\Delta Q_G}{\Delta V_G} = -q\frac{\Delta N_e}{\Delta V_G} + \frac{\Delta Q_T}{\Delta V_G}$$

and this differs from the true free electron quantity $q\Delta N_e/\Delta V_G$ by the trapped charge term, $\Delta Q_T/\Delta V_G$. However, for devices of reasonable quality, the Hall effect and field effect mobilities lie in reasonable agreement because the band tail state density is low, as can be seen in Fig. 5.

Subthreshold Slope. The subthreshold slope (i.e., $S = \partial V_G/\partial \log_{10} I_D$) of the transfer characteristic is dominated by the deeper defect states from near mid-gap to the edge of the band tails. The simplest, and most common, interpretation of the subthreshold slope is provided by Levinson's method (15), where the states are assumed to be monoenergetic and situated at mid-gap. In this case, the drain current can be deduced from a simple thermionic emission over the grain

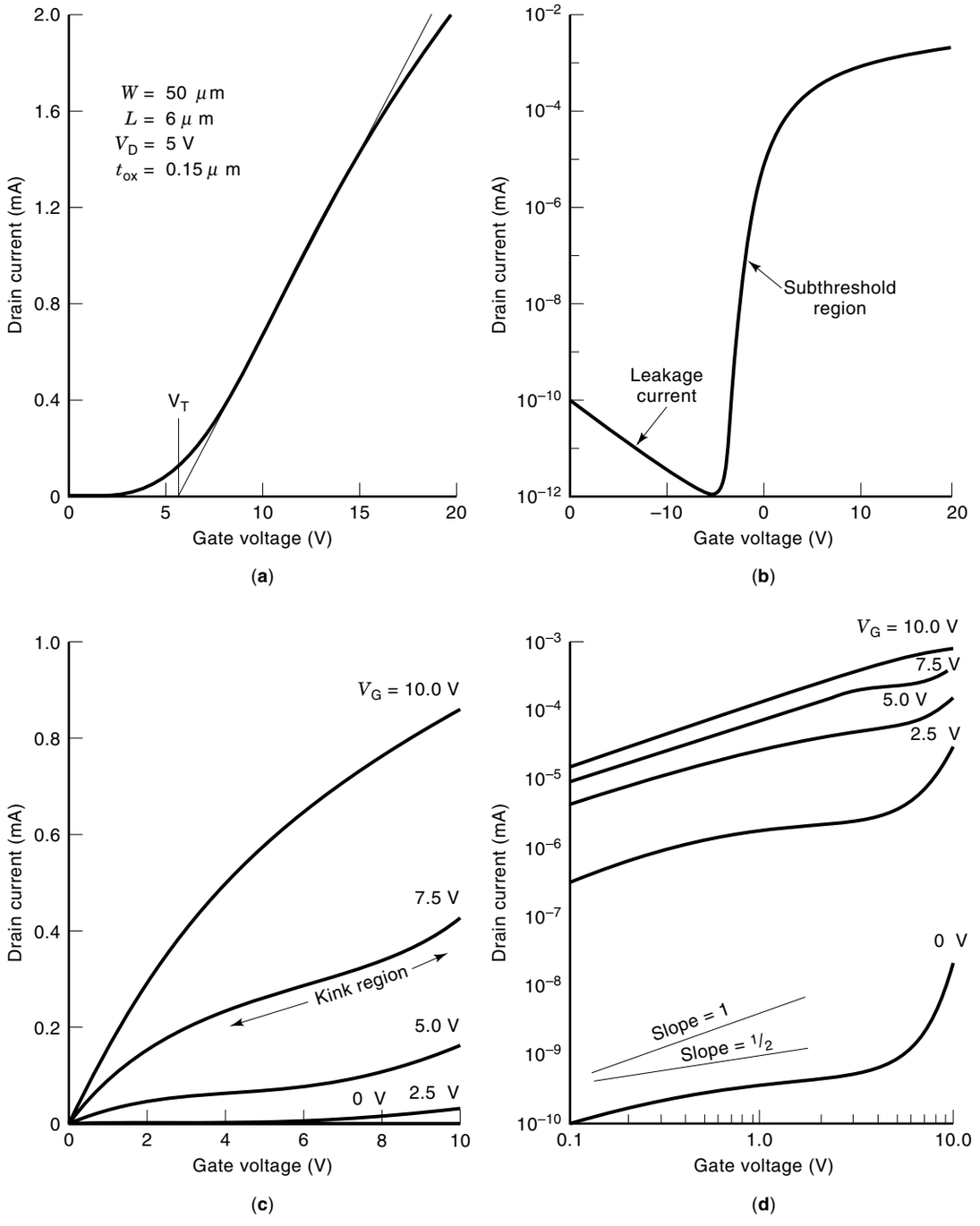

Figure 3. Device characteristics for poly-Si TFTs formed by excimer laser crystallization. (a,b) Transfer characteristics on linear and semilog scales, respectively. (c,d) Output characteristics on linear and log–log plots, respectively.

boundary model (as is used for the resistivity data in Fig. 1), which gives

$$I_D = \left(\frac{W}{L}\right) \cdot \mu_B \cdot V_D \cdot V_G \exp\left[\frac{-q^3 N_T^2 t}{8\epsilon\epsilon_0 C_i V_G}\right]$$

where N_T is the trapping state density per unit area of grain boundary, and t is the film thickness, provided that the dopant concentration is lower than the defect state density. The trapping state density is then estimated from a plot of $\log_{10} I_D$ versus $1/V_G$. These estimates are within a factor of 2–3 of values deduced more rigorously by full 2-D device modeling with traps distributed across the band gap (16).

Leakage Current and Photocurrent. The leakage current of poly-Si TFTs rises very rapidly with applied gate bias [as is evident in Fig. 3(b)] for drain biases in excess of ~3 V. This

has been attributed to phonon-assisted tunneling from deep traps near mid-gap, and this is analyzed in detail by Brotherton et al. (8). Significantly, it was shown in that work that the drain field at high biases is controlled by 2-D coupling to the gate, rather than by the space charge associated with the deep trapping states. At lower drain biases [i.e., 0.3–3 V in Fig. 3(d), for $V_G = 0$ V] the current rises as $V_D^{1/2}$ (giving a slope of 0.5 on the log–log plot), indicating a normal generation current at the drain. This is given by

$$I_D = \tfrac{1}{2} W \cdot W_D \cdot q N_T n_c \sigma v_t \cdot \exp(-E_g/2kT)$$

where n_c is the density of states at the conduction band edge, σ is the trap cross section, v_t is the thermal velocity of the carriers, and E_g is the band gap. W_D is the bias-dependent depletion region width at the drain which gives rise to the $V_D^{1/2}$ dependence. At even lower drain bias the current becomes ohmic (giving a slope of 1.0 on a log–log plot), because it is limited by drift along the channel rather than by the drain junction.

The photocurrent can be attributed to the photogeneration of electron–hole pairs, and is controlled by recombination at the near mid-gap deep states at the drain. It is found that the photocurrent can be suppressed in films <40 nm by additional recombination at the surfaces of the poly-Si (17).

The "Kink Effect" and Stability. The output characteristics of poly-Si TFTs do not saturate above pinch-off but continue to rise, often displaying kinks, as is evident in Fig. 3(c). This effect is strongly channel length dependent, and it is caused by weak avalanche multiplication in conjunction with hole trapping and storage near the drain (18) rather than by bipolar gain (which only occurs if recombination is so low that the holes can diffuse from the drain region to the source contact). When the devices are biased in this region, hot carriers are produced, and these can cause degradation to the device characteristic by the generation of interface states or by the trapping of charges in the gate oxide (19).

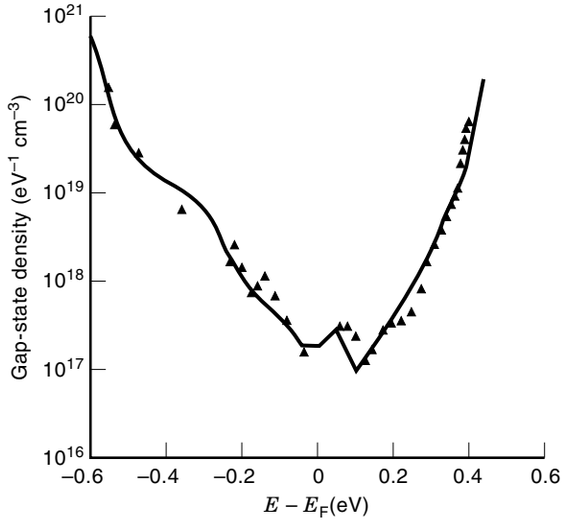

Figure 4. Typical gap state density deduced from conductance measurements (16). Reprinted with permission from T.-J. King, M. G. Hack, and I.-W. Wu, *J. Appl. Phys.,* **75**, 908, 1994. Copyright 1994 American Institute of Physics.

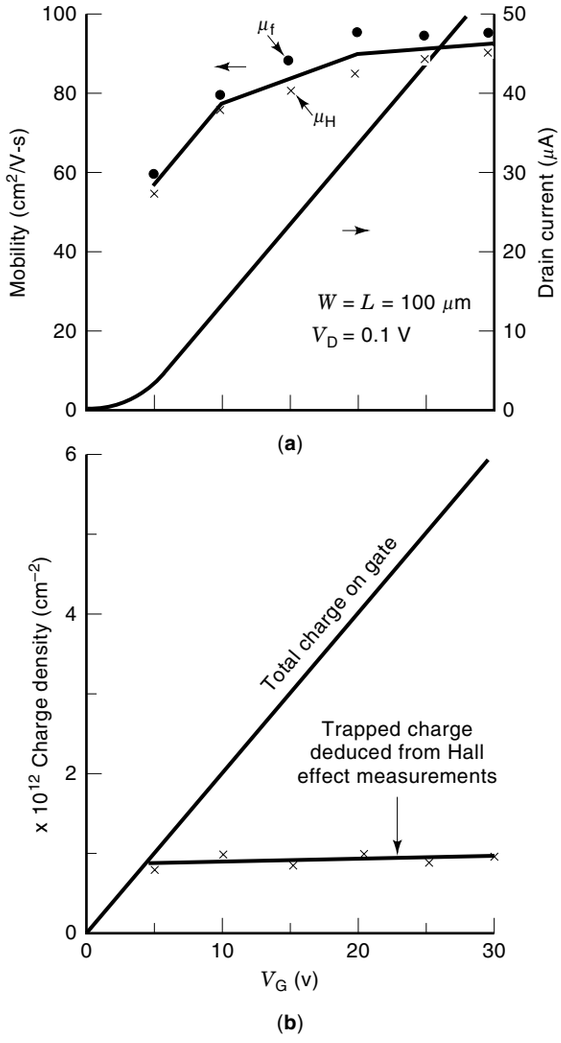

Figure 5. (a) A comparison between Hall effect and field effect mobilities for poly-Si TFTs and (b) the charge trapped in the band tail states, as deduced from the Hall effect measurement.

Recent Developments and Areas for Study

Recently, poly-Si TFTs have been fabricated on glass substrates with mobilities which are nearly as high as those found in mono-Si devices (20). It is believed that this will extend the current situation (i.e., displays with simple integrated drive circuits) to one in which entire systems are integrated on a single panel. Furthermore, recent work has realized EEPROM memory devices using poly-Si TFTs (10), and promising devices have also been realized on polymer substrates at 200 °C (21). In the future, device geometries need to be reduced so that performance can be improved further.

THIN FILM DIODES

Thin film diodes (TFDs) are currently used on glass substrates for active-matrix addressing, image sensing, and solar

power. The diodes can be of p–i–n (22), Schottky barrier (23), or metal–insulator–metal (MIM) (24) type, of which only p–i–n diodes can be used for photovoltaic applications.

Diode Characteristics

The thin film diodes in use today for active-matrix addressing are of Schottky barrier type, and typical arrangements are given in Figs. 6(a) and 6(b). Current–voltage characteristics for the metal–semiconductor–n^+ (MSN) and metal–semiconductor–metal (MSM) structures are given in Fig. 6(c) for cases in which the amorphous silicon is undoped, or doped with nitrogen to form semiconducting silicon nitride (αSi : N$_x$/H) (25). The introduction of nitrogen into the silicon (to up to 20–25 at%) has the effect of increasing the band-gap of the material to ~2 eV (and therefore increases the Schottky barrier height) and it gives much lower leakage current than with undoped αSi : H. The current mechanism in these devices has been identified to be the tunneling of electrons through a triangular barrier at the electrode (26). At high fields this is limited by thermionic emission, and the current can be approximated by

$$J = A^* T^2 \exp\left[-\left(\frac{q}{kT}\right)(\phi_e - \alpha E_s)\right]$$

where A^* is the effective Richardson constant, E_s is the modulus of the electric field, ϕ_e is the barrier height, and α is an effective tunneling constant (~0.4 nm, corresponding to an electron effective mass in αSi : H of 0.1 m_e (26), where m_e is the free electron mass). The image force lowering of the barrier is taken into account in this expression. If there is significant trapped charge in the nitride, then E_s is reduced, and a corresponding change in $\partial \ln J/\partial V$ is observed.

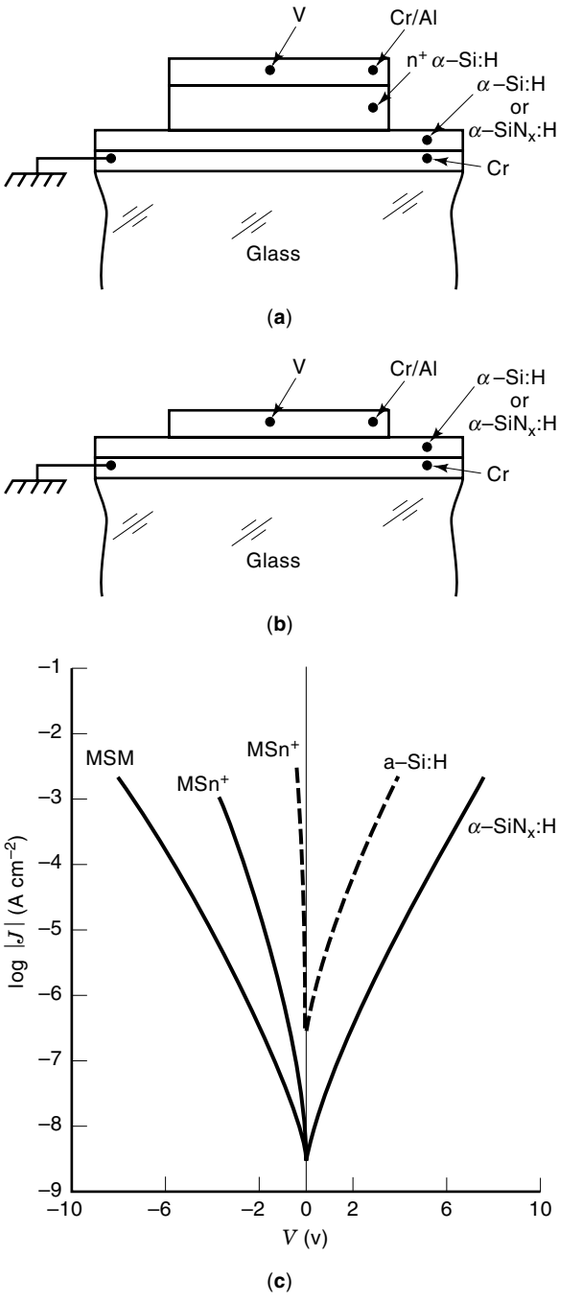

Figure 6. Typical thin film diode structures (a) M-S-n^+ and (b) M-S-M. (c) shows diode characteristics for αSi : H and αSi$_x$: H with a silicon to nitrogen ratio of 2 : 1 (26). Reprinted with permission from J. M. Shannon, J. N. Sandoe, I. D. French, and A. D. Annis, *Mater. Res. Soc. Symp. Proc.,* **297**, 987, 1993.

Device Stability

It is found that the characteristics of the device degrade as a result of high current flow. This is due to (1) the production of defects in the semiconductor and (2) the subsequent trapping of electrons and holes at these defects. Eventually (once the defect state density has become high enough), the current flow becomes controlled by the Frenkel–Poole mechanism, with carriers "hopping" from state to state. The defects are believed to be formed by the breaking of weak Si–Si bonds as energy is released by the recombination of injected electrons and holes (27). Devices stable enough for AMLCD applications can be made by a combination of device engineering and drive signal shaping (28).

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