SUPERCONDUCTING ELECTRONICS

Since the late 1980s, rapid advances have been made in superconducting electronics. For example, it is now possible to fabricate low-temperature superconductor (LTS) digital circuits with thousands of active devices. These circuits operate at tens of gigahertz clock speeds and with several orders of magnitude less power consumption than conventional room-temperature electronics. Furthermore, high-temperature superconductor (HTS) devices are gradually entering the commercial market. One example is the demonstration HTS filter systems that are operational in a number of cellular phone base stations in the United States. This section gives the reader an overview of the broad field of superconducting electronics (1–3) with a description of applications and provides a historical perspective of technological development. A more in-depth description of a few specific aspects of superconducting electronics are given in the following sections.

Superconductivity was discovered in 1911 in the laboratory of Kamerlingh Onnes, as a direct consequence of Onnes' invention of a method to liquefy helium. Helium becomes a liquid below 4.2 K (−268.8°C) so that with liquid helium one could study the properties of materials at very low temperatures. Researchers were measuring the resistance of mercury, lead, and tin and found that below a characteristic transition temperature T_c for each material, the resistance drops to zero. Subsequent experiments revealed that many metals become superconducting at very low temperatures. More recently, in 1986 Bednorz and Müller (4) discovered that certain ceramic materials are superconducting at relatively high temperatures. The most developed of these materials is $YBa_2Cu_3O_{7-\delta}$ (YBCO) which undergoes a superconducting transition at approximately 90 K (−183°C).

Two fundamental characteristics of a superconductor are zero dc electrical resistance and the exclusion of internal magnetic fields, called the Meissner effect (5–7). A direct consequence of the second property, the Meissner effect, is that a magnet floats above the surface of a superconductor. The Railway Technical Research Institute in Tokyo, Japan, is using this property to develop a very fast magnetically-levitated train (8). Zero electrical resistance means that one can construct ideal lossless cables, wires, and transmission lines. Note that the resistance is really zero, and experiments have shown that for most cases a dc current flowing in a superconducting ring will persist for a million or more years. One application of superconducting cables is the coils of high-power electromagnets for magnetic resonant imaging (MRI).

As an example of a superconducting electronic application (1), see the analog filter shown in Fig. 1 (9). The resistance of the superconductor is zero at dc and very low at high frequencies. This property makes superconductors ideal for very sharp microwave frequency filters. Figure 1(a) shows a high-temperature superconductor (HTS) filter manufactured by Conductus Inc. (10), and Fig. 1(b) shows the frequency response of the circuit (9). The filter consists of a single layer of YBCO patterned into strips. These strips, coupled together by the electrical and magnetic fields from currents flowing in the superconductor, are designed to resonate at specific frequencies. These resonant frequencies define the frequency response of the filter. This is due to the low insertion loss of the filter when incorporated into the front end of the receiver. Furthermore, the sharp edges of the filter characteristic allow

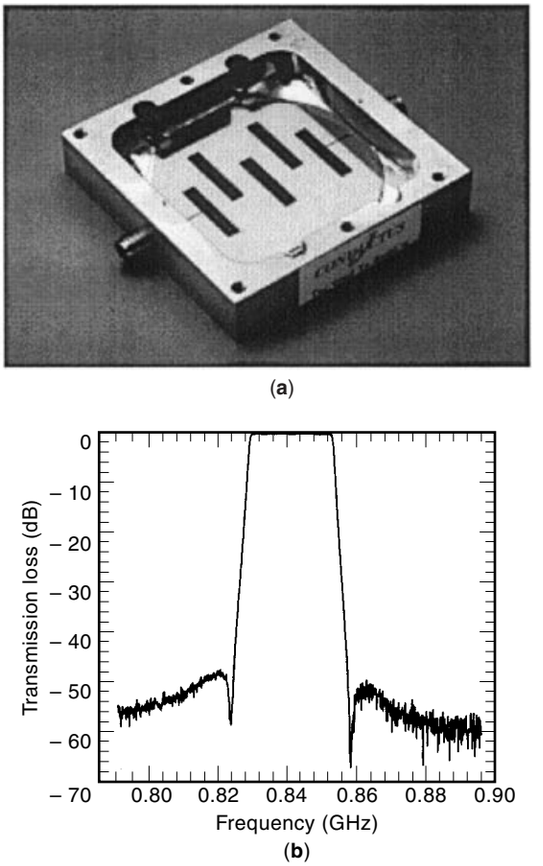


Figure 1. (a) A high-temperature superconducting filter and (b) the frequency response of a typical filter. Data courtesy of D. Zhang and co-workers at Conductus Inc..

frequency bands to be more closely spaced, which in turn allows more channels in a given bandwidth. Note that the HTS circuit in Fig. 1 requires a refrigerator to operate in the field, which is approximately the size of a large coffee can.

Other electronic applications include the superconducting mixer and the bolometer used in radio astronomy (1). In a typical bolometer, millimeter wave or infrared radiation is incident on a thin superconducting film, or microbridge. The high frequency radiation causes the superconductor to go normal, and the resistance of the film is proportional to the amplitude of the radiation. The bolometer is used in radio astronomy as a sensitive broadband detector.

The reader may be wondering how materials such as lead, niobium, or mercury become superconductors when cooled to very low temperatures? The mechanism for low-temperature superconductivity was not completely understood until 1957 when Bardeen, Cooper, and Schrieffer (BCS) (11) proposed a microscopic theory. The basic idea of their theory is that electrons pair up in a superconductor, see Fig. 2, to form so-called Cooper pairs. This electron pairing takes place throughout the superconductor so that all of the electrons are correlated with one another, as components of Cooper pairs. This correlation means that all of the electron pairs move together and do not experience collisions with other particles which would cause resistance. The BCS theory also showed that the mech-

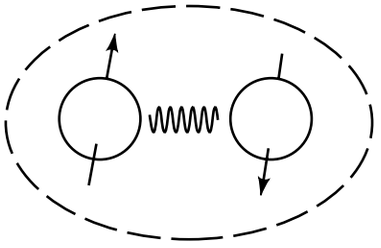


Figure 2. Paired electrons in a superconductor. The arrows represent the spin of the electrons, and the oscillating line represents the interaction force. In each electron pair the spins of the electrons align opposite one another, so that the total Cooper pair spin is zero.

anism, or force, keeping the electron pairs together is the vibrations of the crystal lattice. This explains why a definite transition temperature T_c exists for each material where the binding action of the lattice vibrations are strong enough, compared to the Coulomb electrical repulsion, to make the material superconducting. The BCS theory accurately describes low-temperature superconductors. However, now the mechanism for high-temperature superconductivity is not completely understood.

Prior to the BCS theory, London in 1935 proposed a phenomenological theory of superconductivity which derived from Maxwell's equations and Newton's laws (7). Later, in 1950, Ginzburg and Landau developed a more sophisticated phenomenological theory incorporating quantum mechanics (7). The BCS theory focuses on the microscopic electron-to-electron physics of a superconductor, whereas the London and Ginzburg–Landau theories give a very useful description of macroscopic phenomena that result from the electron pairing. Today both the London and the Ginzburg–Landau theories are often used to understand the dynamics of superconductors for electronic applications (2). Furthermore, these phenomenological theories are also useful in that they are applicable to high-temperature superconductors.

In 1962 B. D. Josephson predicted two dynamic properties of superconductivity (12). He analyzed two superconductors separated by a thin barrier through which quantum tunneling is possible. This device, called a Josephson junction today, can consist of a superconductor–insulator–superconductor sandwich, of which the insulator is approximately as thick as the Cooper pair diameter. Josephson's first prediction was that current can flow between the superconductors with *zero* applied dc voltage. Today this phenomenon is called the dc Josephson effect. Josephson's second prediction was that if a dc voltage V_{dc} is applied to the junction, then an alternating (ac) current will flow between the two superconductors with a very high frequency $f = (2e/h)V_{dc}$, where e is the magnitude of the charge of the electron and h is Planck's constant. This phenomenon is called the ac Josephson effect. Both the dc and the ac Josephson effect are a consequence of tunneling of Cooper pairs from one superconductor through the insulating barrier to the other superconductor. The Josephson junction has many applications in superconducting electronics. One of the first applications was to make a very sensitive magnetic field detector called a superconducting quantum interference device (SQUID) (13).

There are two types of SQUIDs: the direct-current (dc) SQUID and the resonant-frequency (RF) SQUID.

A dc SQUID consists of a parallel combination of two Josephson junctions in a superconducting (inductive) loop; see Fig. 3(a). The most sensitive SQUIDs are made with low-temperature metal superconductors. Figure 3(b) is a photograph of an YBCO HTS dc SQUID fabricated on a strontium titanate ($SrTiO_3$) bicrystal substrate. When a dc current is applied, the output voltage measured across the two junctions is modulated by the magnetic field through the loop enclosed by the two junctions, see Fig. 3(c). This modulation is relatively large and is a function of the applied magnetic field. Using feedback electronics, one can measure magnetic fields extremely accurately and with a high dynamic range. The operating principle of the dc SQUID is described in more detail in the following section.

The RF SQUID is perhaps the simplest Josephson circuit and consists of a single Josephson junction in a superconducting loop, shown schematically in Fig. 3(d). The superconducting loop has an inductance and is magnetically coupled to a resonant circuit with an oscillating RF current input. Magnetic field coupled into the SQUID loop has the effect of detuning the resonant circuit, and this modulates the output voltage. The RF SQUID readout electronics is similar to the dc SQUID, and consists of feedback and lock-in amplification of the tuned circuit output voltage. The magnitude of the magnetic field input to the RF SQUID can be measured to an accuracy similar to the dc SQUID (14).

SQUIDs are the most sensitive magnetometers and can even be used to measure the magnetic fields generated by neurons firing in the human brain. Typical magnetic field sensitivities for LTS and HTS dc SQUIDs in the white-noise limit are 2 fT/$\sqrt{\text{Hz}}$ and 10 fT/$\sqrt{\text{Hz}}$ respectively (1 fT = 10^{-15} T = 10^{-11} G). Figure 4 shows one application of the dc SQUID as a scanning microscope (15). The image was generated by a HTS SQUID microscope developed by Clarke and co-workers at the University of California at Berkeley (UC Berkeley) (16). The image shown in Fig. 4 is a magnetic field map of the magnetic ink for a small portion of a one-dollar bill, and was first observed by Welstood and coworkers at the University of Maryland (15). The image was obtained by scanning the SQUID at a distance of 150 μm from the sample surface. The microscope resolution in Fig. 4 is approximately 130 μm, but decreasing the size of the SQUID pickup loop can increase the resolution. For example, the IBM scanning SQUID microscope with a 4 μm pickup loop has a resolution of approximately 4.5 μm (15). The HTS SQUID in Fig. 4 operates at 77 K and is separated from the room temperature sample by a small window.

In addition to SQUID magnetic field sensors, the Josephson junction has other important applications, such as the international volt standard (17). The volt standard uses the ac Josephson effect. When tunnel junctions are irradiated by microwaves they produce constant voltage steps $n(h/2e)f$, where n is an integer, and f is the frequency of applied microwave radiation. A large number of junctions in series irradiated by a microwave source produces a large constant voltage step. The present standard for 1.2 V is maintained at the United States National Institute of Standards and Technology (NIST) by an array of approximately 2000 Josephson junctions irradiated by a 94 GHz microwave source. Figure 5(a) shows the commercial volt-standard system manufactured by HYPRES, Inc. (18). Note that the system incorporates a 5 K closed-cycle refrigerator. In recent years, Josephson fabrica-

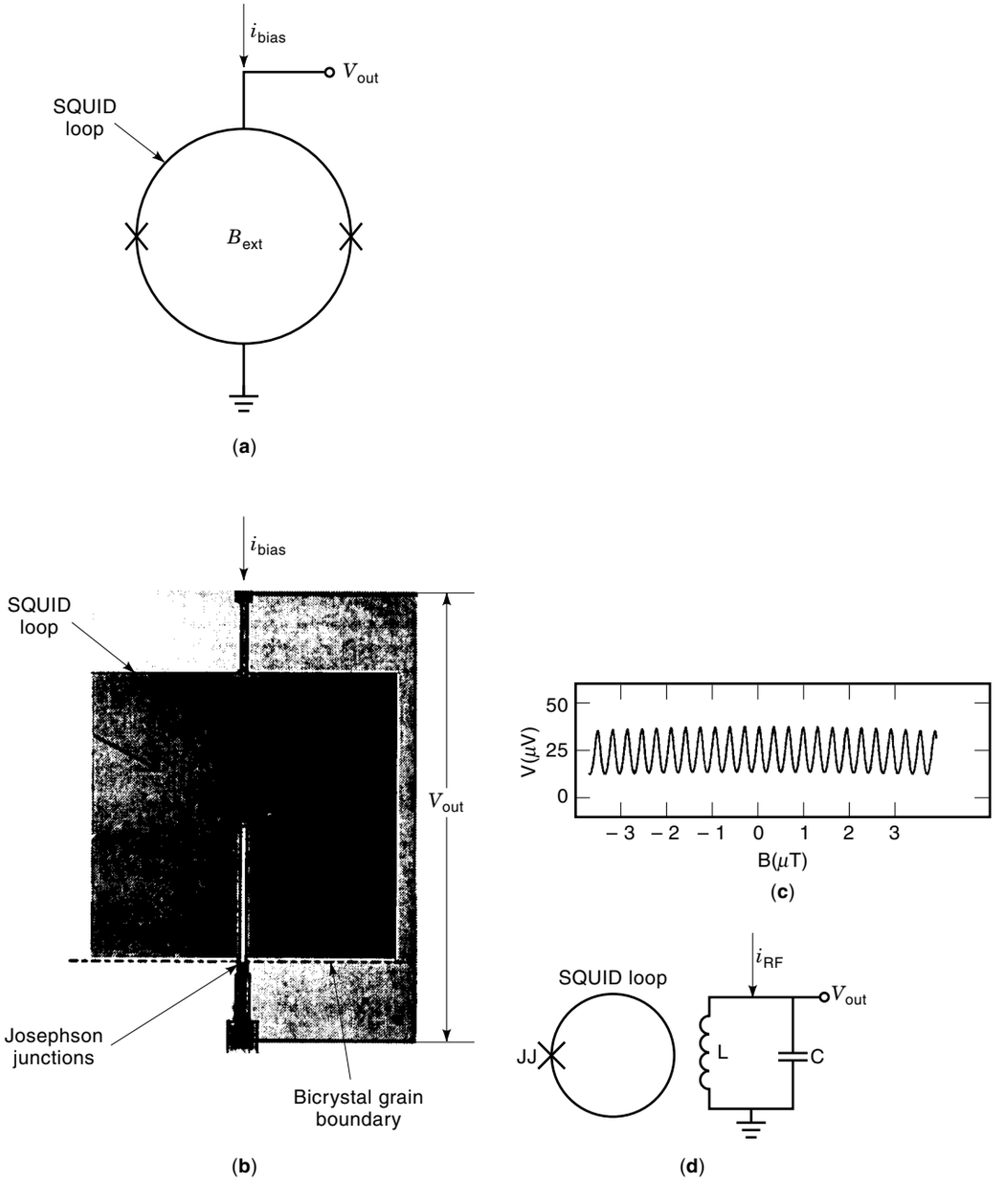


Figure 3. (a) Circuit diagram of a SQUID where the X's represent Josephson junctions. (b) An HTS SQUID fabricated on a $SrTiO_3$ bicrystal. The SQUID is patterned from a thin film deposited on the bicrystal, and the Josephson junctions are formed on the grain boundary of the crystal. (c) Typical modulation data for a dc SQUID. The output voltage V_{out} in (b) is a periodic function of the magnetic field B coupled into the SQUID loop. Data provided courtesy of J. Clarke and E. Dantsker, University of California, Berkeley. (d) Schematic diagram of an RF SQUID.

tion technology has improved so that much larger arrays with a voltage of 10 V can be used as a standard. The 19-mm-long 20,208 junction array chip for the 10 V voltage standard is shown in the photograph in Fig. 5(b).

As another application example, researchers at TRW have recently demonstrated a dc to 10 GHz phase-shifter based upon a nonlinear transmission line (19). The circuit resembles the voltage standard, and consists of many RF SQUIDs weakly coupled along the length of a superconducting transmission line. The RF SQUIDs add inductance along the transmission line, with the amount controlled by the current along the transmission line. The phase shifter has been successfully fabricated and tested using both low temperature (180,000 junction circuit) and high temperature (30,000 junction circuit) superconductor fabrication processes (19).

The near-instantaneous phase response of the phase shifter enables an additional new device, the superconducting upconverting parametric amplifier. Using a superconducting phase-shift transmission line, designers propagate a pure microwave tone (the "carrier") through the phase shifter. Simul-

Figure 4. Inset shows the magnetic image of a portion of George Washington's face on a $1 bill observed with an HTS SQUID microscope. Data provided courtesy of T. S. Lee, G. Dantsker, and J. Clarke University of California, Berkeley.

taneously, low frequency signal current is also sent along the phase shifter. The low frequency signal varies the phase shift of the carrier, producing a phase-modulated carrier at the output. In addition to converting the low frequency waveform up to the higher frequency range, the phase-modulation mechanism produces power gain, with as much as 10 times (20 dB) gain demonstrated in some experiments (19).

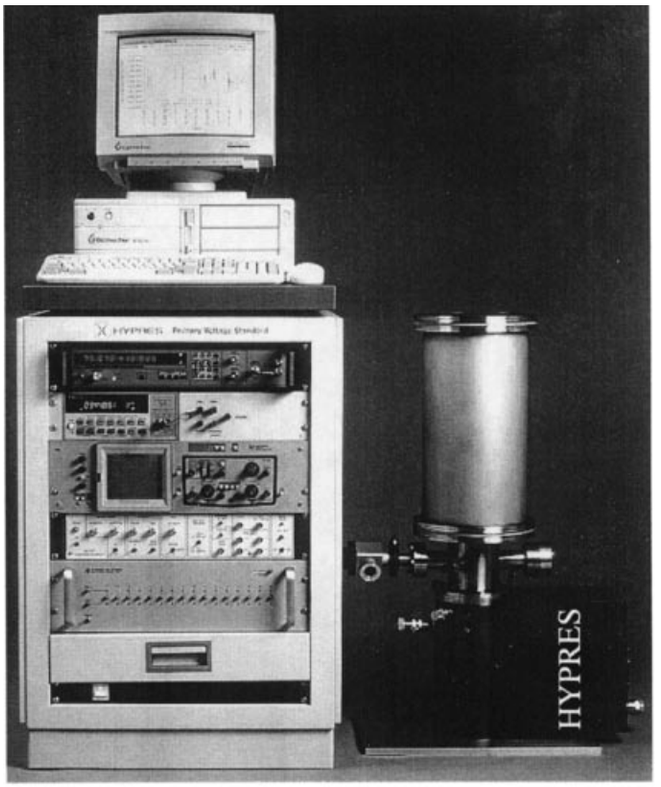
The transmission line parametric amplifier is related to the single junction parametric amplifier, demonstrated in the mid-1980s by TRW and Bell Labs. Applying 36 GHz as a pump, an RF SQUID produced reflection gain for signals near 18 GHz. While producing as much as 32 times (30 dB) reflection gain, the amplifier successfully achieved noise levels at the quantum limit. Parametric amplifiers can therefore have extremely low noise, and degenerate parametric amplifiers in particular can exhibit the novel property of actually "squeezing" the internal noise to less than the amplifier quantum limit (20).

However, by far the most promising electronic application of the Josephson junction is digital circuits. The Josephson junction is the fundamental component of all modern digital superconducting electronics, analogous to a transistor in conventional digital circuits (although the operating principle is completely different). The Josephson junction has the property that it can switch "on" in less than a picosecond (1 ps = 10^{-12} s), and the switching involves very little power dissipation. These properties make Josephson junction circuits ideal candidates for ultrahigh-speed computing applications.

In the last decade low-temperature superconductor microfabrication technology has progressed to the point that superconducting circuits with thousands of Josephson junctions are routinely manufactured. With this level of integration, one can make complex digital circuits, such as analog-to-digital converters (ADC) and small microprocessors that operate at multigigahertz clock speeds (1 GHz = 10^9 cycles/s). As an example Fig. 6(a) shows a digital synthesizer designed by Spooner and co-workers at TRW (21). The circuit consists of approximately 700 logic gates (~3000 Josephson junctions), a read only memory (ROM) that stores a sine wave, and a digital-to-analog converter (DAC).

The circuit in Fig. 6(a) is designed to synthesize waveforms at high speed given a digital program input. Figure 6(b) shows synthesized output for the circuit operating with a 2 GHz internal clock. The power dissipation of the synthesizer is 6 mW, which is approximately 1000 times less power than an equivalent GaAs semiconductor circuit. The low on-chip power consumption of superconducting digital circuits is a fundamental advantage of the technology compared to semiconductor circuits. Therefore, superconducting digital circuits are ideal for low-power applications where large amounts of data must be processed at very high speed. One such application is digital on-board processing in a communications satellite.

Digital superconducting electronic circuits are grouped in two main types: voltage-state logic (22) and rapid single-flux quantum (RSFQ) logic (23). The operating principles and dif-



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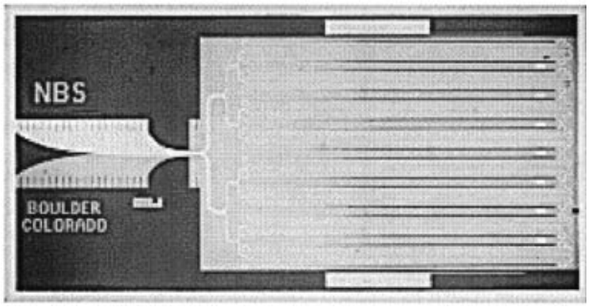
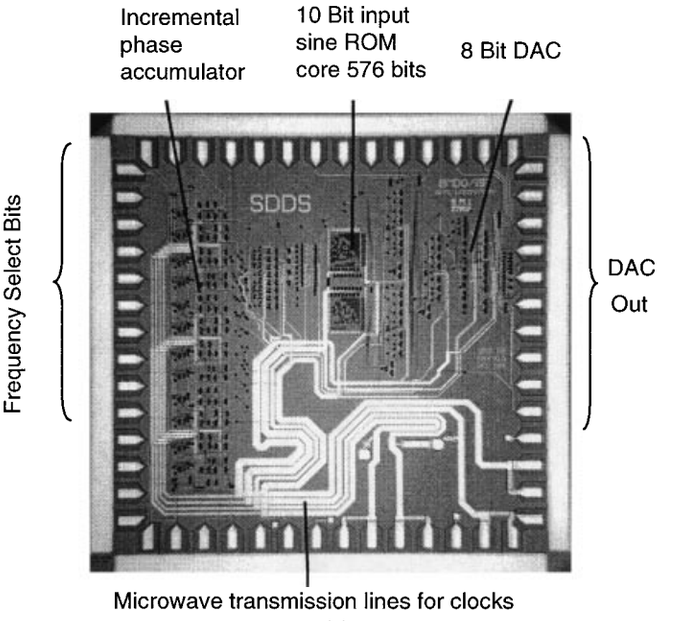


(b)

Figure 5. (a) The HYPRES commercial voltage standard system, including the 4 K Boreas cryocooler cold head, bottom right. The chip is mounted inside the evacuated cylinder on top of the cold head. The compressor is not shown. Photograph courtesy of HYPRES (18). (b) The 19 mm long 10 V voltage-standard chip consisting of over 20,000 Josephson junctions. Photograph courtesy of C. Hamilton and C. Burroughs at the National Institute of Standards and Technology, Boulder, CO (17). Original figure (b) © 1997 IEEE.

ferences between these two types of logic are described in detail in the following sections. Historically, voltage-state logic circuits were the digital circuits used in the IBM computer project of the 1970s and early 1980s (24). This project aimed to build a mainframe computer using superconducting voltage-state logic. The project ended in 1983, and IBM chose not to pursue superconducting digital electronics further. The main reason was that IBM felt that, at that time, superconducting logic was not a significant enough improvement over projected future semiconductor circuits to warrant such a drastic shift in its core mainframe computer technology. Furthermore, the IBM Josephson circuits used a lead alloy technology that degraded over time (especially during thermal cycling), and, while the digital logic met the project specification goals, considerable difficulty was encountered in making high-speed memory suitable for a mainframe computer (24).

However, research in superconducting microprocessors continued in Japan using voltage-state logic. Several successful projects were completed under Ministry of International Trade and Industry (MITI) sponsorship. A series of processor chips were demonstrated at Fujitsu and Hitachi, and a four-chip model computer at the Electrotechnical Laboratory (22). In 1988 Kotani and co-workers at Fujitsu demonstrated a completely operational 4-bit microprocessor consisting of 1841



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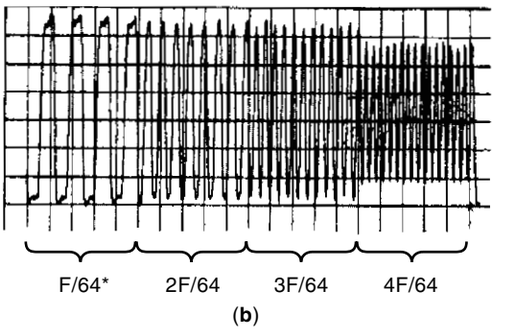


(b)

Figure 6. (a) A superconducting digital synthesizer consisting of an incremental phase accumulator, 10 bit sine ROM, and an 8 bit DAC on a 1 cm × 1 cm chip. (b) Typical synthesized output for clock frequency $f = 2$ GHz. Data and chip photograph courtesy of A. Spooner and co-workers at TRW (21). Original figure © 1997 IEEE.

logic gates operating at 1 GHz with 6 mW of power dissipation (22). This processor used superconducting voltage-state modified variable threshold logic (MVTL) developed by Fujimaki and co-workers (25). MVTL circuits have much higher operating margins than the previous IBM logic circuits, and the MVTL microprocessor chip was fabricated using a more stable niobium trilayer technology. The circuit in Fig. 6 was designed using MVTL voltage-state logic. In 1990 the Fujitsu team designed and fabricated an 8-bit microprocessor consisting of 6300 MVTL gates (23,000 Josephson junctions) on a 5 mm $\times$ 5 mm chip (22). All of the component circuits operated at 1 GHz, and the multiplier had an average loaded gate delay of 5.3 ps. More recently the team led by Tahara at NEC in Japan has demonstrated a 4 kbit superconducting random access memory (RAM) with subnanosecond access times (26).

Voltage-state logic circuits have traditionally been used only for 1 GHz to 2 GHz applications. However Jeffery, Perold, and Vanduzer at UC Berkeley demonstrated a new type of voltage-state logic (27) in simple circuits at 10 GHz to 18 GHz. Therefore, much higher speed operation should be possible with this technology. One reason for the perceived limited speed of voltage-state logic is that the gates are latching. This means that circuits have to be reset to "zero" after a logical "one" operation, and before the next cycle of operation. Furthermore, the information (the logical ones and zeros) cannot be moved from one gate to the next without more than one clock. Typically 2 to 4 overlapping clocks power the gates, and these clocks have to be distributed throughout the circuit. The microwave transmission lines to power the circuit are clearly seen in Fig. 6. Without careful design, the large number of clock lines can cause excessive cross talk that can degrade circuit performance.

In 1985 Likharev, Mukhanov, and Semenov proposed a new type of superconducting logic based upon picosecond voltage pulses (23,28). They called this type of logic rapid single-flux quantum (RSFQ) logic and showed that, in principle, one could make RSFQ circuits that operate at clock frequencies approaching terahertz (10^{12} cycles/s). The operating principle of RSFQ,described in the following section, is fundamentally different from voltage-state logic. Because of the potential ultrahigh-speed operation (greater than 100 GHz), RSFQ is becoming the logic of choice for future digital superconducting applications.

Figure 7 shows a state-of-the-art RSFQ oversampling analog-to-digital converter (ADC) designed and tested by Semenov and co-workers (29) at the State University of New York at Stony Brook, and fabricated using the HYPRES Inc. 3.0 μm niobium process (18). The circuit consists of a single bit sampler and an integrated digital signal processor, called a decimation filter. The circuit is completely operational with a 9 GHz clock and a 10 MHz analog input bandwidth. The circuit comprises 1777 Josephson devices, consumes 0.5 mW of power, and has 11 effective bits. A similar ADC chip designed and fabricated at HYPRES operated in excess of 11 GHz with 11.5 effective bits. Note that these circuits have 10,000 times less on-chip power disipation than an equivalent GaAs ADC.

The circuit in Fig. 7 converts lower speed ($\leq$10 MHz) analog input signals into binary information that can be processed by a computer. Figure 7(b) and (c) show reconstructed sine wave data for the ADC for two different frequency sine wave inputs. The circuit is programmable so that, as the fre-

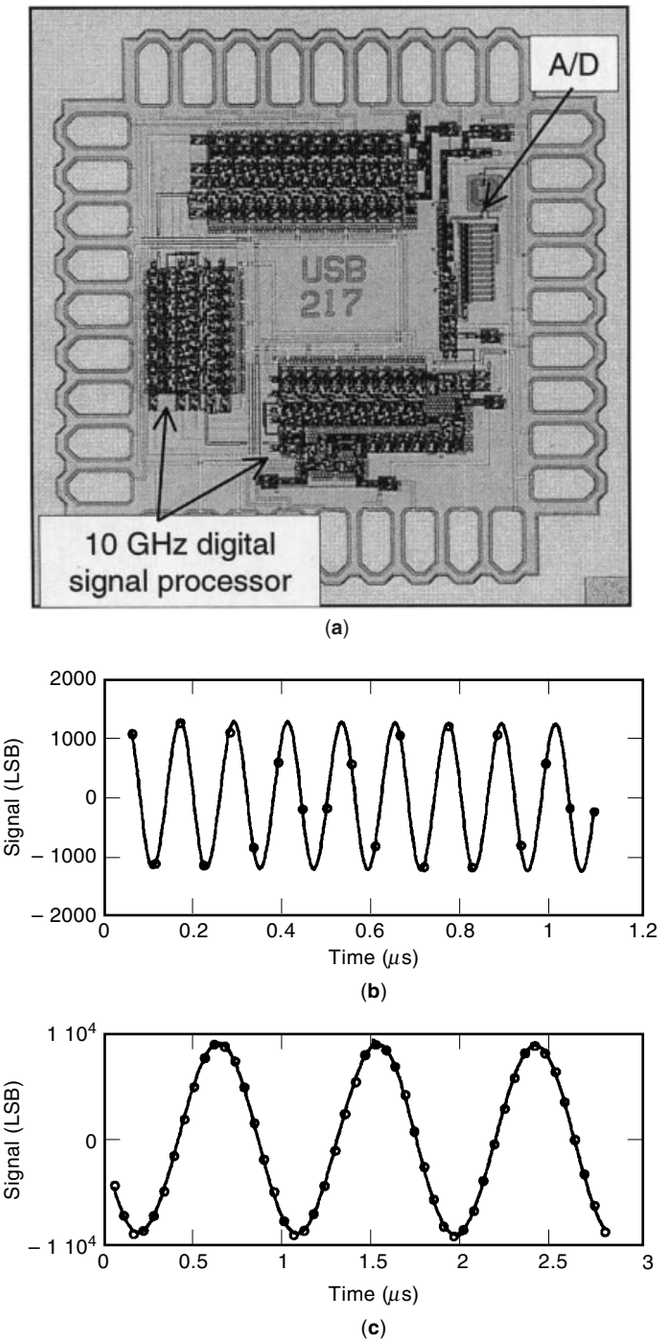


Figure 7. RSFQ oversampling analog-to-digital converter consisting of a 1 bit sampler and an integrated digital signal processor on a 0.5 mm $\times$ 0.5 mm chip. The circuit consists of 1,777 Josephson junctions and is completely operational with a 9 GHz internal clock. (b) 11 bit reconstructed sine wave data for an 8.13 MHz input signal. (c) Reconstructed sine wave for a 1.13 MHz input signal. The circuit is programmable so that for the lower frequency input there are over 14 bits of resolution. Circuit photograph and data provided by V. Semenov, State University of New York at Stony Brook.

quency of the input is reduced, higher resolution digital outputs can be obtained. This circuit performance is as good as the best semiconductor ADC presently available.

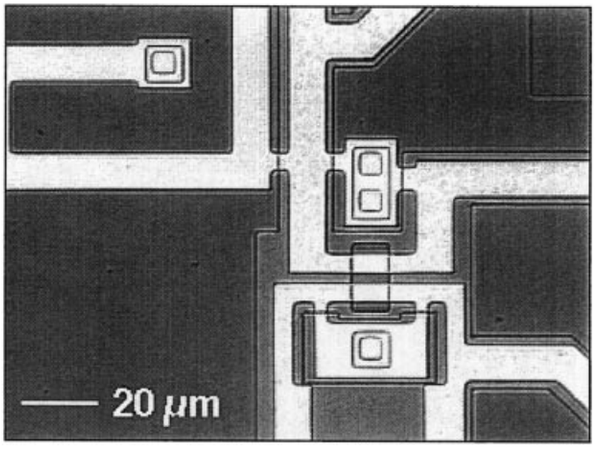
The key advantages of RSFQ circuits are their speed compared to all other digital circuits and that they use a dc power supply. However, the main circuit design challenge is that the gates require clocking. The circuit clock consists of picosecond very low energy voltage pulses with quantized area. The clock pulses are difficult to distribute in complex circuits operating at ultrahigh speeds. Furthermore, the picosecond RSFQ pulses cannot be directly interfaced with room temperature electronics because room-temperature electronics are not fast enough or sensitive enough to detect the low-energy picosecond pulses. Furthermore, RSFQ pulses are easily attenuated by nonsuperconducting cables and by impedance mismatches within superconducting circuits. Researchers are working hard to overcome these engineering design challenges to unlock the full technological potential.

RSFQ and voltage-state are not the only types of superconducting logic, although they are the most widely used today. For example, a type of superconducting logic circuit has been developed in Japan called the quantum flux parametron (QFP) (30), also called the parametric quantron (3). The QFP consists of a two junction loop with parameters chosen so that when an external clock is applied, an input to the loop will cause a quantized current to circulate in either the clockwise or the counterclockwise direction, depending upon the input. The direction of the current flow signifies the logical "1" or "0" in a QFP computer. A team directed by Goto at the RIKEN laboratory has developed innovative pipeline architectures for supercomputers based upon the QFP (30). Unfortunately, QFP circuits are sensitive to noise coupled from the clock lines, and are today not used for complex computing applications. However, the QFP is extremely sensitive to input signals, and is sometimes used as a comparator in analog-to-digital converter applications.

At present all practical superconducting digital circuits are fabricated from low-temperature superconducting materials. For example the circuits in Figs. 6 and 7 were fabricated by a process consisting of layers of patterned and etched thin film niobium and a resistive layer, separated by SiO_2 insulator layers. Niobium is a superconducting metal at temperatures below 9 K. For digital circuits metallic layers are relatively straightforward to pattern and etch into integrated circuits.

Single-flux quantum logic circuits can also be implemented using high-temperature superconductor (HTS) materials. The ultimate advantage of HTS circuits is that they require much smaller refrigerators compared to low-temperature superconducting circuits. In the last few years there has been considerable interest in implementing ultra-high-speed RSFQ circuits using HTS materials. Figure 8 shows one such HTS circuit demonstrated at Northrop Grumman. The circuit uses fundamental properties of superconductivity to quantize a linear input signal and is the basic component of an analog-to-digital converter (ADC). The circuit was cooled to 65 K for the experiment.

High temperature superconductors, such as YBCO, are complex multilayered materials called perovskites, which are related to ceramics. When fabricating integrated circuits, if each layer of YBCO is not planarized, discontinuities of the crystal structure, or grain boundaries, occur at the wire cross-



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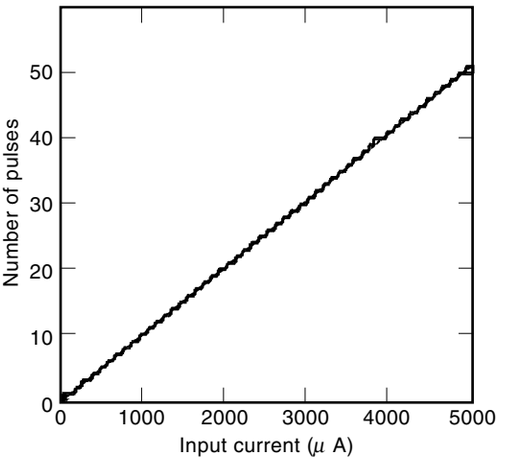


(b)

Figure 8. (a) High-temperature superconducting digital quantizer circuit for an analog-to-digital converter fabricated by a multilayer YBCO process. (c) The measured linearity of the quantizer is better than 5.7 effective bits at 65 K. Photograph and data provided courtesy of M. G. Forrester, D. L. Miller, and J. Przybysz at Northrop Grumman.

overs. These discontinuities can form natural Josephson junctions and open circuits, which can cause circuit failure because they were not originally part of the circuit design. To date only small RSFQ digital circuits, consisting of fewer than 20 Josephson junctions and operating at low speed, have been demonstrated using HTS materials. There are various ways to make HTS Josephson junctions for digital circuits. However, none have thus far demonstrated sufficient process control to allow making junctions in quantity whose characteristics are adequately similar. (See HTS JOSEPHSON JUNCTION DEVELOPMENT.)

Recent Josephson junction fabrication research has also focused on using niobium nitride (NbN) for Josephson circuits (31). NbN is a low-temperature metallic superconductor, and it is much easier to fabricate digital circuits using this material than using HTS YBCO. The advantage of NbN is that its superconducting transition temperature is 16 K so that circuits can operate at 10 K: a 10 K cryocooler is significantly smaller than a 4 K cryocooler.

Since all superconducting electronic components operate at cryogenic temperatures, it is important to briefly discuss cryocooler technology (32). Table 1 lists representative cryocoolers, and temperatures that are important for superconducting electronics applications. The operating temperature of the cryocooler is dependent upon the superconducting electronic application, and in particular on the materials technology being used and the thermal load of the system. For example, present Nb LTS digital circuits require a 5 K cryocooler, whereas NbN digital circuits need a 10 K cooler. HTS circuits can operate at higher temperatures; for example, the wireless filter in Fig. 1 operates at 65 K, and some HTS SQUID systems can operate at 75 K. Note that the power dissipation of superconducting components, except for HTS wireless filter systems, is extremely small. In typical applications the leads connecting from room temperature to the superconducting component are the dominant heat load. If this is minimized, cooling powers of 100 mW to 1 W are adequate for many superconducting electronics applications, and hence the cryocoolers can operate near to their base temperature.

Most cryocoolers use the principle of compressing and then expanding a gas to produce cooling. For a given thermal load, the cryocooler size decreases dramatically as the temperature is increased. Applications at temperatures less than 20 K typically require a Gifford–McMahon or Boreas type cryocooler, shown for the voltage-standard system in Fig. 5(a). The superconducting circuits are attached to the end of a cold head which consists of a capped metal cylinder separating the circuit from the cold helium gas. In Fig. 5(a) the voltage standard circuit is sealed inside an evacuated container around the cold head. Gifford–McMahon/Boreas cryocoolers use an external compressor, and additional pistons behind the cold head. The piston expands the gas from the external compressor, and oscillates at approximately 1 Hz. The cryocooler cold head plus the vacuum jacket is roughly the size of a personal computer tower (~36 kg), and the compressor is the size of a small filing cabinet (~90 kg), not shown in the figure. Two stages of cold head and piston configurations are required to get to 5 K temperatures, with a rare earth regenerator used to extract additional heat from the gas, or with an additional Joule–Thomson cooling stage.

Stirling and pulse-tube cryocoolers generally operate at higher temperatures (although a pulse tube has been demonstrated below 2.5 K), and are often much smaller than the Gifford–McMahon/Boreas. They can be approximately the size of a small coffee can (5 kg to 10 kg total weight) for superconducting electronic applications. The pulse-tube cryocooler, in particular, incorporates a small diaphragm and piston that is oscillated at approximately 60 Hz to compress and expand the gas coolant; this rapid oscillation gives a relatively large cooling power for a small mechanical volume. The focus of commercial R&D for Stirling and pulse-tube refrigerators is now to increase the operating lifetime, for example through the use of compressors with gas bearings to avoid any mechanical wear.

Cryocooler reliability has long been an issue for commercial superconducting electronics applications. However, in recent years vast improvements have been made. For example the 5 K Sumitomo cryocooler requires servicing after 10,000 h of continuous operation, and servicing consists of swapping the regenerator filter. At higher temperatures, the pulse-tube type cryocoolers have impressive reliability records; two TRW pulse-tube cryocoolers are presently in orbit in space satellites, and the reliability of these coolers is estimated at 10 years with zero maintenance. However, it should be noted that such coolers for space applications, including the Stirling machines pioneered at Oxford, are built at enormous cost, many hundreds of thousands of dollars. The challenge is to achieve the same reliability in commercial coolers sold for less than $10,000, that is, manufactured for a few thousand dollars.

In the following sections superconducting electronics is described in more detail. Examples of applications are limited to SQUIDs and digital electronics. Basic design and circuit testing principles are described. Finally, possible future directions for the field of digital superconducting electronics are discussed. For a more in-depth introduction to superconducting electronics, see Refs. 1, 2, and 3.

BASIC PRINCIPLES OF SUPERCONDUCTING ELECTRONICS

Josephson Junctions and the Josephson Effect

At temperatures below the superconducting transition, the electron pairs in a superconductor are correlated with each other. Quantum mechanically this means that all of the Cooper pairs are in the same macroscopic quantum state, so that we can describe the superconductor mathematically by a mac-

Table 1. Representative Cryocoolers and Operating Temperatures for some Superconductive Electronic Applications

Temperature	SC Application	Operating Principle	Cooling Power	Manufacturer
5 K	Nb LTS Digital	2-stage GM with rare earth regenerator or with JT stage	0.5–1.5 W	Sumitomo, Chesapeak/Boreas
10 K	NbN Digital	2-stage GM[a]	1–7 W	Sumitomo, CTI, Leybold
35 K	HTS SQUIDs and HTS Digital	Single-stage Stirling	0.5 W	CTI, Leybold
		Single-stage GM	4 W	CTI, Leybold
		Single-stage pulse-tube	1–10 W	TRW, Lockheed Martin[b]
65 K	HTS filters for cellular phone base stations	Single-stage Stirling	2.5 W	CTI, Leybold
		Single-stage GM	6–90 W	CTI, Leybold
		Single-stage pulse-tube	5–50 W	TRW, Lockheed Martin[b]
		Single-stage pulse-tube	4.5 W	Iwatani
75 K	Some HTS SQUID systems	Mixed gas cooler	1 W	APD CryoTiger

GM = Gifford–McMahon closed cycle, JT = Joule–Thomson.

[a]10 K 2-stage pulse-tube and 2-stage Stirling cycle cryocoolers are presently in development.

[b]Not commercially available, although presently used for satellite applications.

roscopic wave function Ψ:

$$\Psi = \sqrt{\rho}\exp(i\phi) \tag{1}$$

where ρ is the density of the superconducting paired electrons and ϕ is the phase of the wave function. Similar to the single-particle Schrödinger equation, the phase of the wave function Eq. (1) is related to the external magnetic field by $\phi = 2e/\hbar \int \boldsymbol{A}\cdot dl$ where $\boldsymbol{A}$ is the magnetic vector potential ($\boldsymbol{B} = \nabla \times \boldsymbol{A}$).

A Josephson junction is shown schematically in Fig. 9(a). The device is rather simple and consists of two superconductors separated by a thin barrier (such as an insulator, normal metal, or semiconductor) through which quantum tunneling of electron pairs can take place. Mathematically, this is equivalent to coupling the wave functions of the two superconductors through the barrier. Following Feynman (5), one can assume linear coupling across the barrier and that the wavefunctions on both sides obey the single-particle Schrödinger equation. Using Eq. (1) and these coupled equations, one can derive the following famous Josephson equations:

$$I_s = i_c \sin\phi \tag{2}$$

and

$$V = \frac{2e}{\hbar}\frac{d\phi}{dt} \tag{3}$$

where I_s is the supercurrent through the junction, V is the voltage across the junction, ϕ is the phase difference between the wave functions on both sides of the barrier, and i_c is the critical current of the junction.

Equation (2) describes the supercurrent flow through the junction, and Eq. (3) gives the voltage across the junction. For real applications the Josephson junction is modeled by the equivalent circuit in Fig. 9(b). The superconducting Josephson junction is denoted by the cross in the circuit and is in parallel with a resistance and a capacitor. The resistor represents the flow of nonsuperconducting electrons through the junction, and the capacitance exists because the device is a "sandwich" of two superconducting layers separated by a thin dielectric insulator.

From Eqs. (2) and (3) and Kirchhoff's laws (that is, set the bias current equal to the sum of the currents through each component) it is straightforward to show that the general equation governing the Josephson junction in Fig. 9(b) is

$$C_j\frac{d^2\phi}{dt^2} + \frac{1}{R_j}\frac{d\phi}{dt} + \frac{2\pi i_c}{\Phi_0}\sin\phi = \frac{2\pi}{\Phi_0}i_{bias} \tag{4}$$

where R_j is the junction resistance, C_j is the junction capacitance, i_c is the critical current of the junction, i_{bias} is the current applied to the junction, and Φ_0 is the constant $h/2e$. The nonlinear term with sin ϕ, if linearized, has the same form as an inductor in place of the junction. Therefore the nonlinear term is sometimes called the kinetic inductance of the Josephson junction.

Equation (4) is identical to the equation for a pendulum where ϕ is the angle of the pendulum, shown schematically in Fig. 9(b). Therefore one can visualize the pendulum to obtain an intuitive feeling for the dynamic behavior of the Josephson junction. Comparing Eq. (4) to the pendulum mechanical analog, the junction capacitor C_j corresponds to the pendulum moment of inertia (mass m times length l squared), $1/R_j$ to the damping coefficient, $(2\pi/\Phi_0)i_c$ corresponds to mgl (where g is the acceleration due to gravity), and $(2\pi/\Phi_0)i_{bias}$ to an externally applied torque.

Intuitively, an increasing dc current applied to the junction is equivalent to increasing the torque on the pendulum Fig. 9(b). When the current is less than i_c, the pendulum does not spin, and the voltage across the device is zero. However, when the current exceeds a threshold corresponding to the critical current i_c, the pendulum begins to spin because of the torque of the applied current. As the pendulum spins, the angle (junction phase) changes with time, so that by Eq. (3) a voltage appears across the device. The pendulum is nonlinear, and once it starts spinning it has an "angular momentum."

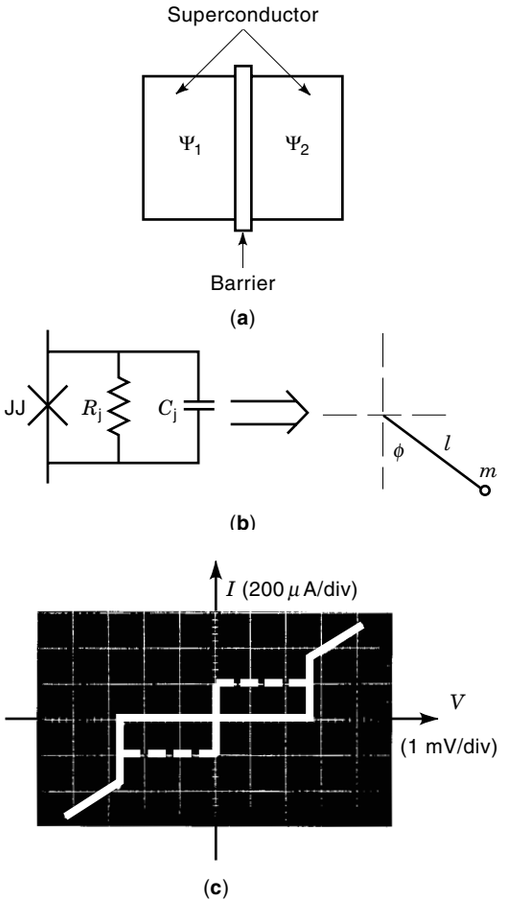


Figure 9. Schematic diagram of a Josephson junction consisting of two superconductors separated by a thin barrier. (b) The equivalent circuit model for a Josephson junction with a parallel normal resistance and a capacitance, sometimes called the *RSJ* model. The circuit model is equivalent to a pendulum mechanical analog where the angle of the pendulum is equal to the phase difference of the wave functions across the barrier. (c) Experimental I–V curve for a typical $NbAlO_xNb$ Josephson junction photographed from an oscilloscope. Note the 2.5 mV gap voltage for the junction and that the I–V curve is hysteretic. The dashed line denotes switching that is too fast to see on the oscilloscope. Data provided courtesy of X. Meng, University of California, Berkeley.

Hence, as the bias current (externally applied torque) is removed, the pendulum continues to spin, so that the junction voltage is nonzero. This corresponds to the fact that the I–V curve of the lightly damped Josephson junction is hysteretic. Adding a resistance of a few ohms in parallel with the junction removes the hysteretic behavior and corresponds to adding damping to the pendulum analog.

The pendulum analog described so far assumes the junction resistance is constant, which is useful for analytic calculations, and describes the general dynamics of the junction. However, the junction resistance is actually a nonlinear function so that when the junction begins to spin (switches on) the resistance sharply increases. The nonlinear resistance of the Josephson junction is included in Josephson SPICE circuit simulators (35). For the specific case of an underdamped superconductor–insulator–superconductor (SIS) tunnel junction, the voltage that appears across the device when it switches on is called the gap voltage of the superconductor. For Josephson junctions in general, the gap voltage physically corresponds to the energy required to break apart Cooper pairs into individual electrons on one side of the Josephson junction, and recombine them as Cooper pairs on the other side. The gap voltage is dependent on the superconducting material and is 2.4 mV to 2.8 mV for Nb, and 4 mV to 5 mV for NbN. The hysteretic I–V curve for an underdamped SIS niobium Josephson junction with a nonlinear resistance is shown in Fig. 9(c).

Superconducting circuits consist of Josephson junctions and inductive loops for SQUIDs, where the SQUIDs and junctions are wired together using superconducting transmission lines. Resistors are used for damping, and to feed currents into the SQUIDs and junctions. In order to make a superconducting circuit one therefore needs multiple layers of superconductor for wires, a layer of resistor, and a superconducting groundplane.

Low-temperature superconductive niobium Josephson circuits are fabricated by using a trilayer process. First, a layer of niobium a few tenths of a micrometer thick is deposited on a silicon wafer. The surface of this layer is coated with a layer of aluminum about 4 nm to 10 nm thick. Then the aluminum is oxidized to a thickness of about 1 nm, and a second layer of niobium (Nb) is deposited on top. The thin aluminum oxide layer is as the tunnel barrier for the $NbAlO_xNb$ Josephson junction. Note that the barrier thickness is approximate, and is only within a factor of two or three of 1 nm. Using photolithography and reactive ion etching, one can pattern circuits from the trilayer with many thousands of Josephson junctions each a few micrometers in size. Additional superconducting wiring and resistor layers are deposited and etched, separated by SiO_2, to make complex circuits. The wiring and resistor layers are connected to each other and the Josephson junctions by vias, or vertical contacts, that are patterned and etched into the SiO_2 insulating layers. For high-speed circuits, a ground plane is usually deposited either as the first or the last step in the process. Note that the actual process is rather simple, that is, all deposition is at 300 K and there is no doping, ion implantation, or high frequency diffusion.

By using a trilayer all of the Josephson junctions are effectively fabricated simultaneously across the wafer, and no processing occurs between depositions of the layers. This means that there are only small variations among the characteristics of each Josephson junction. To make complex circuits the critical current variations across a chip should have a standard deviation less than 3%. At present no trilayer process exists for HTS circuits, and hence the parameter spreads on i_c are rather large (approximately 20 to 100% standard deviation). These large process spreads are the main reason that only small HTS Josephson circuits have been demonstrated thus far. (See HTS JOSEPHSON JUNCTION DEVELOPMENT.)

Finally, note that the switching-on time of the Josephson junction is very fast and can be less than a picosecond. This makes the device useful for ultra-high-speed computing applications. Intuitively, decreasing the junction capacitance corresponds to decreasing the mass of the pendulum, which in turn makes the junction switch (rotate) faster. Mathematically the ultra-fast switching speed is understood by noting that the linearized Eq. (4) (i.e., assuming $\sin \phi \approx \phi$) has a natural angular frequency

$$\omega_c = \sqrt{\frac{2\pi i_c}{\Phi_0 C_j}} \tag{5}$$

where ω_c is called the plasma frequency of the Josephson junction. Similar to the pendulum angular frequency, the plasma frequency relates to how fast the Josephson junction phase (angle) can change. For example, a 300 μA junction with a 0.002 pF capacitance has a Josephson frequency $f_c = \omega_c/2\pi = 1.1$ THz. Since the junction capacitance depends upon the area a of the junction, the switching speed of Josephson circuits can be increased by increasing the critical current density $J_c = i_c/a$, and decreasing the area of the junction to keep i_c constant. With today's fabrication process, typical J_c values are 1 kA/cm^2 to 2.5 kA/cm^2, where the smallest junction linear dimension is 3 μm. The junction switching time with a 3 μm process is a few picoseconds. However, processes with J_c as high as 50 kA/cm^2 have been demonstrated for small circuits. With this high critical current density, and a submicron Junction fabrication process, subpicosecond switching times have been demonstrated (see the section on RSFQ logic).

Flux Quantization

The response of superconducting materials to external magnetic fields divides materials into Type I and Type II superconductors. Type I superconductors remain in the superconducting state and exclude all external magnetic fields until they reach a critical field. At the critical field, the magnetic field enters the material, and it returns completely to the normal nonsuperconducting state. However, this is strictly true only for long thin samples parallel to the magnetic field. Type II superconductors, on the other hand, allow magnetic fields to enter while the material remains in the superconducting state.

The magnetic field that enters in a Type II superconductor has the interesting property that it is quantized, so that the magnetic flux ($\Phi = B \times A$) equals $h/2e$. The quantized magnetic flux corresponds to a circulating current loop in the superconductor. Mathematically, the flux quantization phenomenon is a consequence of single valuedness applied to the macroscopic wave function Eq. (1), that is, the phase change $\Delta\phi$ around any closed superconducting loop must be an integer n times 2π, which is equal to the magnetic action $(2e/\hbar)\boldsymbol{A}$

integrated around the loop:

$$\Delta\phi = \frac{2e}{\hbar}\oint A \cdot dl = \frac{2e}{\hbar}\Phi = 2\pi n \quad \Rightarrow \quad \Phi = n\Phi_0 \qquad (6)$$

where Φ is magnetic flux and the flux quantum $\Phi_0 = h/2e = 20.7\,\mathrm{G} \cdot \mu\mathrm{m}^2$. The third term is derived by Stokes's theorem because the magnetic field is related to the vector potential $\boldsymbol{A}$ by $\boldsymbol{B} = \nabla \times \boldsymbol{A}$. On a microscopic level, the actual structure of a flux quantum in a superconducting film is complicated. However, to a good approximation it corresponds to a small supercurrent loop in the plane of the film, where the film is normal on the inside of the loop. The magnetic field generated by the current loop integrated over the area surrounding the flux quantum corresponds exactly to Eq. (6). The superconductors used for circuit fabrication, YBCO and niobium when deposited as a thin film, are Type II supeconductors.

Because the earth's magnetic field is approximately 650 mG (10^4 G = 1 T), many flux quanta will be trapped in a superconducting thin film if it is cooled in the earth's magnetic field. From Faraday's law $V = d\Phi/dt$, so that thermally induced motion of the flux quanta generate low-frequency voltage noise in superconducting circuits. This noise can limit performance of SQUID magnetometers, and researchers have spent considerable effort devising methods to reduce this noise (see the following section on SQUIDs). Furthermore, if flux quanta trap close to a Josephson junction they can change the junction critical current, and this prevents digital circuits from operating correctly.

Figure 10 is an image of the magnetic field above a superconducting MVTL logic gate. The sample was cooled inside a mumetal magnetic shield in a field of 4.5 mG. Mumetal is a very high permeability material commonly used for magnetic shields. A line drawing of the logic circuit has been superimposed on the image to show its location. The image was obtained by scanning a small (4 μm diameter) SQUID loop across the area of the circuit and measuring the magnetic field. The image measures 400 μm $\times$ 400 μm and the dots clearly show the flux quanta trapped in the film. The Josephson junctions in the circuit can be protected from trapped flux by cutting small "moat" holes in the superconducting ground plane surrounding the circuits. Then the magnetic field traps in the moat holes and not in the circuits (33). The use of moats to protect superconducting digital circuits enables designing complex digital circuits that operate in magnetic fields of several milligauss. Magnetic field values less than 5 mG are easily obtained with mumetal magnetic shields.

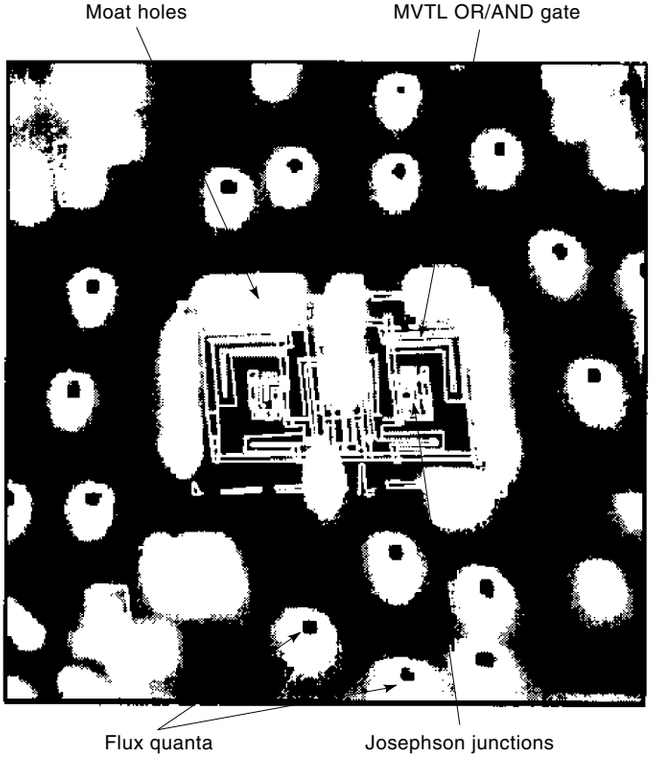


Figure 10. A 400 μm $\times$ 400 μm scanning SQUID microscope image of an MVTL OR-AND logic gate. The magnetic field scale is from 0 (white) to 400 mG (black), and the dots are the flux quanta trapped in the thin film of the superconducting ground plane. Data provided courtesy of M. Jeffery and T. Vanduze, University of California, Berkeley, and J. Kirtley and M. B. Ketchen at IBM.

The dc Superconducting Quantum Interference Device (SQUID) Magnetometer

The basic SQUID circuit is shown schematically in Fig. 3(a). The device consists of two Josephson junctions connected in parallel forming an inductive superconducting loop. For low-temperature superconductor (LTS) SQUIDs normal resistors R are typically connected in parallel with the Josephson junctions to give a nonhysteretic I–V characteristic for the combination. When a dc bias current is applied, the voltage across the resistor is modulated by the magnetic flux ($\Phi = B_{\mathrm{ext}} \times A$) coupled into the SQUID loop. This modulation phenomenon is understood as follows (7).

The total current flowing through the SQUID loop is the sum of currents from the two Josephson junctions given by Eq. (2). Each junction has a phase, and the phase change around the SQUID loop is related to the magnetic field. Specifically, if ϕ_1 and ϕ_2 denote the phase of each junction, then the total phase change around the SQUID loop is given by

$$\phi_1 - \phi_2 = \frac{2e}{\hbar}\oint \mathbf{A} \cdot dl = 2\pi\frac{\Phi}{\Phi_0} \qquad (7)$$

where the last term is derived similarly to Eq. (6).

If a dc current $I > 2i_{\mathrm{c}}$ is applied to the SQUID loop, then the excess current must be carried by the parallel normal resistance, so that $I = I_{\mathrm{s}} + V/2R$ or

$$V = R\left[\frac{I}{2} - i_{\mathrm{c}}(\sin\phi_1 + \sin\phi_2)\right] \qquad (8)$$

Using Eq. (7) and a trigonometric identity,

$$V = R\left[\frac{I}{2} - i_{\mathrm{c}}\cos\left(\pi\frac{\Phi}{\Phi_0}\right)\sin\gamma\right] \qquad (9)$$

where $\gamma = (\phi_1 + \phi_2)/2$. The phase γ evolves rapidly in time by the Josephson Eq. (3), and because $\sin\gamma$ is oscillating, it may appear that the voltage contribution from the Josephson junctions averages to zero. However, the junctions obey the nonlinear Eq. (4), and the oscillation is not a true sinusoid. Therefore, the average of $\sin\gamma$ is nonzero.

Using Eqs. (3) and (4), one can integrate sin γ to find its average value (34). The corresponding average value of V is given by

$$\overline{V} = R\left[\left(\frac{I}{2}\right)^2 - i_c^2 \cos^2\left(\pi\frac{\Phi}{\Phi_0}\right)\right]^{1/2} \tag{10}$$

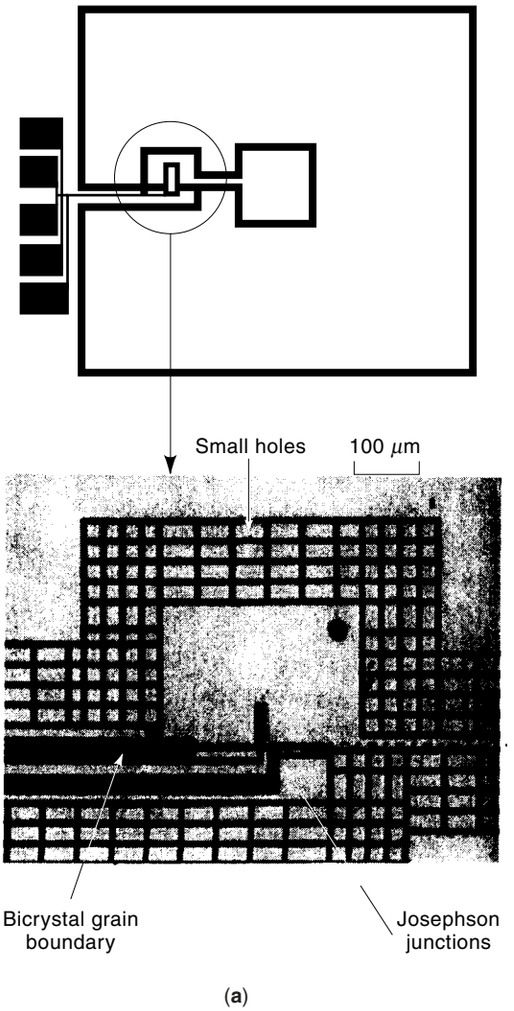
Therefore the average voltage across the dc SQUID, which can be measured with a dc voltmeter, oscillates as a function of Φ with a period $2\Phi_0$. These oscillations are shown for a typical HTS SQUID in Fig. 3(c). One can think of the SQUID as a flux-to-voltage transducer. Using a kilohertz modulator and feedback electronics, called a flux-locked loop, one can use the SQUID characteristic Fig. 3(c) to measure magnetic fields very accurately and with a high dynamic range (13).

For an HTS SQUID, shown in Fig. 3(b), the Josephson junctions are naturally resistively damped by a low normal resistance (of order 1 Ω), so that no external resistors are necessary. In this case the resistance R in Eq. (10) becomes R_j, where R_j is the normal resistance of the HTS junction.

At present, practical YBCO HTS SQUID magnetometers are fabricated using a strontium titanate ($SrTiO_3$) bicrystal. The crystal lattice structure and size of $SrTiO_3$ are similar to those of YBCO. Therefore, when a film of YBCO is deposited on $SrTiO_3$ the crystal growth matches the $SrTiO_3$ substrate lattice. $SrTiO_3$ bicrystals consist of two crystals fabricated and polished with a mismatched grain boundary. When YBCO is deposited on this bicrystal, the YBCO film aligns with the $SrTiO_3$ crystals on each side of the boundary, and the discontinuity forms a long uniform Josephson junction along the boundary. Then the thin film is patterned to form a SQUID structure, such as Fig. 3(b).

The dashed line in Fig. 3(b) shows the location of the bicrystal grain boundary. The two Josephson junctions of the SQUID are too small to be seen on the scale of the photograph. However, the SQUID loop is clearly seen. External magnetic fields are coupled into the SQUID loop by a flux transformer (not shown in the figure). The transformer consists of a thin film of superconductor patterned into a square spiral of several large loops connected to a large pickup loop. It can be fabricated on a separate chip and "flipped" on top of the SQUID. However, today most flux transformers are fabricated on the same chip and direct-coupled to the SQUID loop, similar to Fig. 11.

As described in the previous section, noise from flux trapping is a major problem that limits the performance of HTS



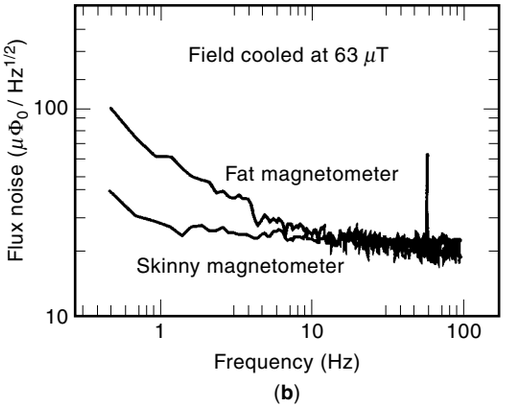


Figure 11. (a) A new type of SQUID consisting of a lattice of thin, 4 μm YBCO wires patterned in a lattice on a $SrTiO_3$ bicrystal substrate. The top picture shows the overall geometry of the device, and the lower photograph shows a portion of the microlattice with the two SQUID Josephson junctions. (b) Flux noise in the SQUID for a conventional "fat" magnetometer and the new "skinny" microlattice type. The flux noise in the skinny magnetometer is significantly less at low frequencies than the conventional magnetometer. Data and photograph provided by R. McDermott, H. M. Cho, B. Oh, K. A. Kouznetsov, A. Kittel, and J. Clarke, University of California, Berkeley.

SQUID magnetometers operating in the earth's magnetic field. Clarke and co-workers at UC Berkeley have spent considerable effort working on this problem. Figure 11 shows a photograph of a new type of magnetometer consisting of a lattice of small (4 μm wide) superconducting lines patterned in YBCO on a $SrTiO_3$ bicrystal. The idea of using a lattice for the body of the magnetometer is similar to using moats to protect superconducting logic circuits (see Fig. 10).

Flux in a superconductor is quantized in units $B \times A = \Phi_0$. For the microlattice design of Fig. 11, the line width is chosen at 4 μm so that $\Phi_0/16\ \mu m^2 \sim 1$ G, which is approximately twice the value of the earth's magnetic field. Therefore, at the transition temperature, flux quanta are unlikely to trap directly in the thin superconducting wires. Instead, they trap in the honeycomb of holes comprising the SQUID body, where they are effectively pinned and cannot easily move around.

Because flux motion is a significant cause of voltage noise in the SQUID, the net result is that the noise floor of the SQUID is considerably reduced. Figure 11(c) shows the flux noise versus frequency of the thin lattice type SQUID and a conventional SQUID magnetometer cooled in 630 mG (63 μT) of applied magnetic field (approximately the earth's magnetic field). Notice that the low frequency $1/f$ noise of the thin magnetometer is much lower than the conventional (fat) dc SQUID.

DIGITAL SUPERCONDUCTING ELECTRONICS

Voltage-State Logic

The basic logical "switch" for voltage-state logic is the hysteretic Josephson junction; see Fig. 9. We can model the hysteretic Josephson junction by the mechanical analog of a pendulum that is free to rotate. The junction phase is analogous to the pendulum angle, and a current bias applied to the junction is equivalent to an external torque applied to the pendulum. When the external torque on the pendulum is increased beyond a critical value, the pendulum begins to spin rapidly. This situation is analogous to the dynamics of the Josephson junction. For a Josephson junction, when the bias current is increased to a value greater than the critical current, the junction phase begins to change rapidly. From Eq. 3 the voltage across the junction is proportional to the rate of change of the phase, so that a voltage appears across the device. The junction is said to have switched to the voltage state. This output voltage is the logical "one" in a computer, and no voltage corresponds to a logical "zero." In order to reset the junction after a logical "one," the bias must be turned off, and for this reason logic using hysteretic junctions is sometimes termed "latching" logic. The switching-on time of the junction can be less than a picosecond. However, because the junction is hysteretic (the pendulum has an angular momentum), it takes a much longer time to switch off when the bias is removed. Therefore, the practical limitation on how fast voltage-state circuits can be clocked in real applications is set by the switch-off time.

As an example of the basic voltage-state logic principle, one could use the switching properties of a single Josephson junction as a logic gate. For an OR gate, the critical current of the junction is chosen so that when the clocked bias and *either* of two inputs A or B is applied, the critical current of the junction is exceeded, and the device switches on; see Gate 1 in Fig. 12(a). For Gate 1 in the figure, note that before the junction JJ_1 switches to the voltage state the Clock 1 bias current has a superconducting path to ground through the junction, so there is no output current from the gate. However, after the junction JJ_1 has switched it becomes a relatively high impedence (since there is now a voltage across the device), and some of the Clock 1 bias current is shunted to the output of the gate. This current will switch Gate 2 when Clock 2 is applied. A logical AND can be constructed similarly by choosing the critical current so that it takes a clocked bias plus both inputs A and B to switch the junction. This is exactly the logical AND of two input signals. The inverse logic function is more complicated but can also be constructed.

The logic gate is on only when the clock is applied. Therefore, for data to propagate between two gates, Gate 1 and Gate 2 in Fig. 12(a), the first gate must be clocked on before the second. Furthermore, Gate 1 must remain on when the clock for Gate 2 is applied. This means that different clocks must be used to move data from one gate to the next. Overlapping clock phases are required for data to propagate through a chain of arbitrary logic gates. Voltage-state logic is often powered by a three-phase clock, whose phases are 120° apart. However, three phases are not always used for voltage-state logic. For example, the original IBM project used a single-phase clock with dc latches after each logical operation, and the circuit Fig. 6 uses a four-phase clock.

The single Josephson junction logic gates described previously are not practical for real applications, since they are very sensitive to parameter variations. Furthermore, there is no isolation between junctions, so that output current from a switched gate can feed back through the gate input and erroneously trigger previous gates. This is clearly seen in Fig. 12(a). Given that Clock 1 is high and there is an input at C, when Clock 2 is applied the Gate 2 junction JJ_2 switches to the voltage state and becomes a relatively high impedance. The current from Clock 2 is then shunted to both the output *and* the input of the gate. This feedback of current through the input may cause the junction JJ_1 in Gate 1 to also switch to the voltage state. Several different voltage-state logic families have been demonstrated that are robust to these problems. Most notably Fujimaki and coworkers have developed modified variable threshold logic (MVTL) (25). MVTL circuits have been demonstrated with thousands of gates at multigigahertz clock rates (see Fig. 5).

The basic building blocks of voltage-state logic circuits are the two- and one-junction SQUIDs shown schematically in Fig. 12(b) and (c). These circuits are similar in structure to the dc SQUID and RF SQUID magnetometers described previously; however, the parameters and modes of operation can be quite different. In order to analyze the underdamped two-junction SQUID in Fig. 12(b) it is useful to make the approximation that the coupling inductors L_c in the SQUID loop are small, so that only the flux Φ_L coupled into the SQUID loop ($\pm\Phi_L/2$ in each SQUID inductor L_c) is important and the voltage across the coupling inductors can be neglected.

Assuming that the Josephson junctions in the two-junction SQUID have identical critical currents, capacitances, and linear resistors, the equation governing the circuit is straightforward to derive from the equivalent circuit Fig. 12(d). This is an ideal two-junction SQUID. Summing the currents in the branches and setting them equal to the input clock current,

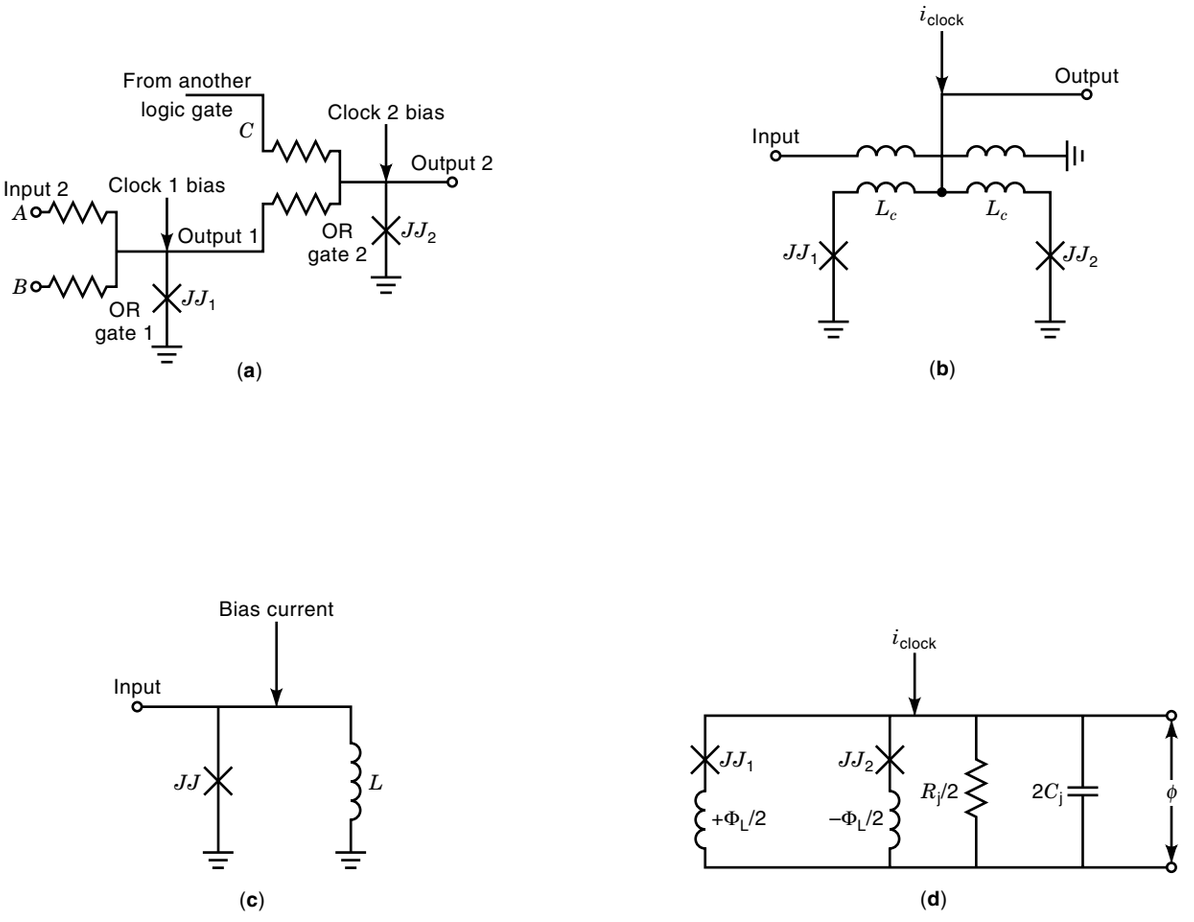


Figure 12. (a) Schematic diagram of a simple voltage-state logic circuit constructed from hysteretic Josephson junctions. (b) Schematic diagram of the two-junction SQUID and (c) the one-junction SQUID used in digital superconducting electronics. (d) Equivalent circuit to (b) assuming the junctions are identical and the SQUID loop inductances L_c are small so their corresponding voltages can be neglected. The Josephson junctions' normal resistances and capacitances are not shown in (a)–(c) and are shown schematically in (d) for the equivalent circuit.

and noting that the phase difference across JJ_1 is $\phi - (\pi/\Phi_0)\Phi_L$ and JJ_2 is $\phi + (\pi/\Phi_0)\Phi_L$, where ϕ is the total phase across the SQUID, and $V = (\Phi_0/2\pi)d\phi/dt$ is the total voltage, we obtain

$$2C_j\frac{d^2\phi}{dt^2} + \frac{2}{F_j}\frac{d\phi}{dt} + \frac{4\pi i_c}{\Phi_0}\cos\left(\frac{\pi\Phi_L}{\Phi_0}\right)\sin\phi = \frac{2\pi}{\Phi_0}i_{clock} \qquad (11)$$

where a trigonometric identity has been used to combine the two sine functions. This equation is similar to the single junction pendulum (4) where the critical current of the junction is $2i_c\cos(\pi\Phi_L/\Phi_0)$, and is modulated by the coupled magnetic flux Φ_L. Hence, a current in the control line varies the switching point of the device.

We can think of the two-junction SQUID circuit as two coupled pendulums with a difference in angle $\Delta\phi = \pi\Phi_L/\Phi_0$. When the applied bias current, or torque on the pendulums, exceeds the critical value $2i_c\cos(\pi\Phi_L/\Phi_0)$, the two pendulums spin and a voltage $V = (\Phi_0/2\pi)d\phi/dt$ appears across the device; the two-junction SQUID has switched to the voltage state. Similar to the single junction, the two-junction SQUID switching is hysteretic. The switching-on time is very fast, but the coupled pendulums have an angular momentum so that they continue to spin when the clock bias is removed. The advantage of this circuit is that the output voltage is isolated from the input control line.

The operation of the one-junction SQUID is understood as follows. For the one-junction SQUID in Fig. 12(b), the input currents (which can be a clock bias and an external bias) must equal the current through the Josephson junction, junction resistance, junction capacitance, and inductor. Because the flux $\Phi = Li$, the current i_L through the inductor adds an additional linear term $i_L = (\Phi_0/2\pi)\phi/L$ to Eq. (4). This linear term adds an effective quadratic term to the potential of the nonlinear pendulum, so that two different modes of operation are possible. Analysis of the one-junction SQUID equation

shows that when the dimensionless parameter $\beta_L = 2\pi L i_c/\Phi_0 \leq 1$ the current in the inductor is a single-valued oscillating function for a linear input current. However, when $\beta_L > 1$ the current in the inductor is no longer a single valued function, and as a linear input current is applied abrupt switching is observed. For $\beta_L > 1$ the circuit operation is hysteretic, so that after switching, if the applied current is reduced the current in the inductor will continue to flow until a different switching point is reached. This hysteretic behavior is shown in Fig. 13(b) for the one-junction SQUID used in the complementary output switching logic (COSL) gate.

As an example of voltage-state logic circuit design, the basic ideas of the COSL family are briefly reviewed (27). COSL was developed for applications from 5 to 20 GHz and was optimized by using a Monte Carlo method in HSPICE (35), so that the basic gates and logic circuits have a high probability of operating at ultrahigh speed despite the process variations of critical current, resistance, and inductance.

Figure 13(a) is a schematic diagram of the COSL OR/AND gate. The XOR function is derived from the OR gate by including a 300 μA Josephson junction in series with the inputs. All of the COSL family of gates consist of a one-junction SQUID input stage and a two-junction SQUID output stage. The two-junction SQUID in the output stage is connected in series with a Josephson junction. The COSL circuits are designed to use a three-phase sinusoidal clocking scheme, and the input and output stages of the gates use two of the clock phases applied through the clock-shaping junctions. These junctions have the effect of clamping the SQUID biases at approximately 2.5 mV when the clocks are applied, independent of the process variations.

The input circuit for the COSL gate is a one-junction SQUID, similar to Fig. 12(c). For this circuit $\beta_L > 1$, so that the SQUID is hysteretic, and when it switches, a relatively large current flows through the inductor. Figure 13(b) shows the relationship between the input current and the inductor current for the one-junction SQUID. For the COSL gate parameters, with an input current of 350 μA, the current in the inductor switches to 250 μA. The output circuit of the COSL gate consists of a hysteretic two-junction SQUID, and is similar to Fig. 12(b).

The operation of the COSL OR gate in Fig. 13 is understood intuitively as follows. When clock 1 is applied, an input to the gate greater than 60 μA is sufficient to fire the one-junction SQUID. Switching the one-junction SQUID causes a relatively large current to flow in the inductor, which is coupled to the output two-junction SQUID loop. By Eq. (11), the one-junction SQUID current suppresses the critical current of the two-junction SQUID so that when clock 2 is applied, the two-junction SQUID switches, giving 1 mV at the output, which produces 200 μA in a 5 Ω load. An AND gate is constructed by increasing the resistor R_b in Fig. 13(a); this reduces the current from the clock so that two inputs are required to switch the gate.

Figure 13(c) is a micrograph of a COSL gate fabricated by the HYPRES Inc. (18) 2.5 kA/cm^2 niobium process. Special care is taken to impedance match all inputs, outputs, and clock lines of the circuit. Specifically, the inputs and outputs to the gate are 5 Ω superconducting transmission lines, and the off-chip driver is a large single Josephson junction designed to switch into a 50 Ω load. The inputs to the circuit from the room temperature electronics are impedance-

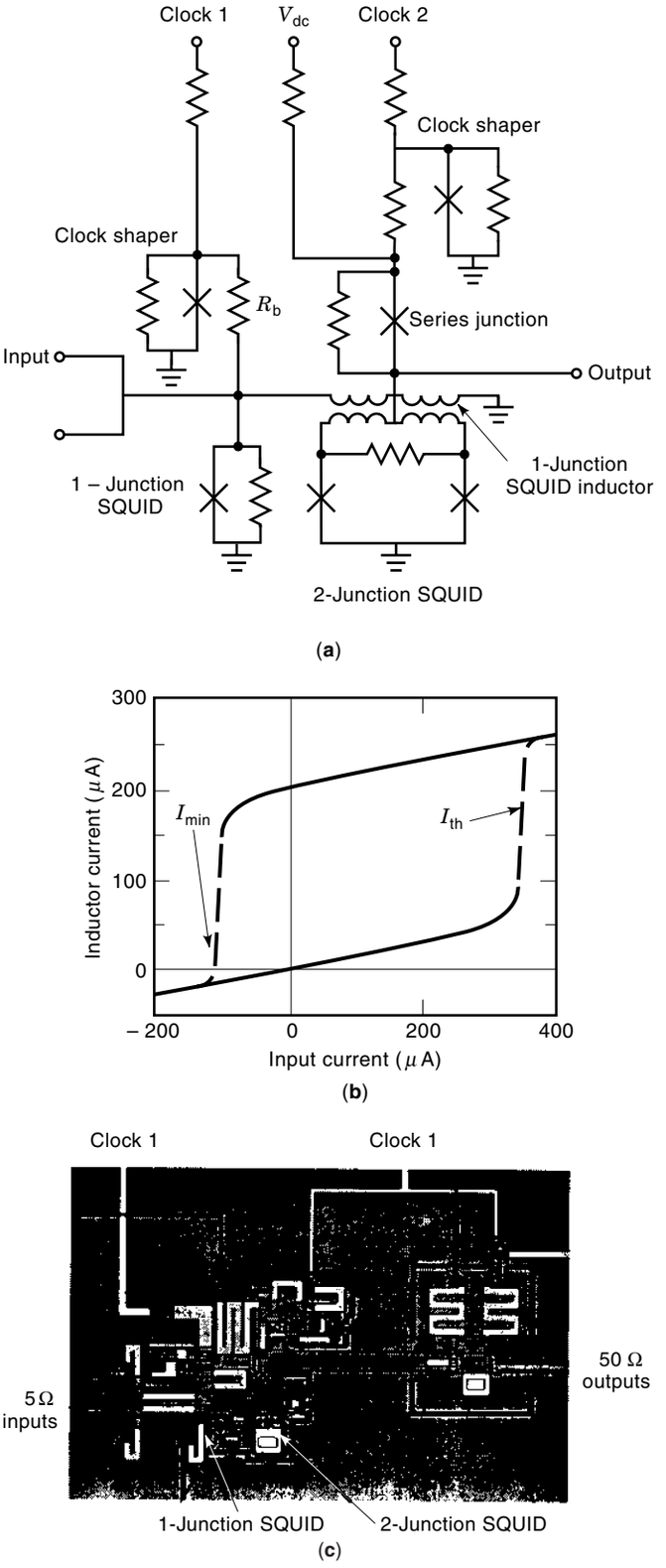


Figure 13. (a) The COSL voltage-state logic gate consists of a one-junction SQUID input stage, and a two-junction SQUID output. (b) The current transfer curve for the COSL one-junction SQUID. (c) Micrograph of the COSL OR/AND gate fabricated using the HYPRES 2.5 μm process. The input and outputs of the circuits are carefully impedance-matched.

matched from 50 Ω to 5 Ω using a simple resistive matching network (not shown in the figure). Impedance matching is essential for circuit operation above a few gigahertz because reflections within the circuit can cause erroneous switching and can make signal detection difficult.

A typical laboratory test setup is shown in Fig. 14. The chip is mounted on the end of a high-bandwidth probe and immersed in a liquid helium dewar. The end of the probe is surrounded by two mumetal magnetic shields. Inputs to the circuit are generated by room temperature multigigabit per second data generators, and the circuit outputs are observed on the sampling oscilloscope. The sinusoidal clock is generated by a signal generator and then split into three phases and amplified by microwave amplifiers. Phase shifters and programmable attenuators vary the phase and amplitudes of the clocks independently. The clock, input signals, and sampling scope must be phase-locked to observe the output of the circuit at high speed.

Figure 15 shows typical test data for the COSL gate in Fig. 13(c) clocked at 15 GHz. The data inputs (top trace) are overlapping low-speed 4 GHz signals. The output, however, is much faster than the input data because the gate is clocked at 15 GHz. For OR operation the COSL gate switches "on" when either of the input signals are high, and switching is observed for AND operation when the two input signals overlap. The oscillation on the background in Fig. 15(b) and (c) is due to feedthrough of the unbalanced clocks, and is sometimes called "ground bounce." The basic COSL gates have been demonstrated at 18 GHz, the maximum speed of the test equipment, and complex COSL encoder circuits for flash ADCs have been demonstrated at 5 to 8 GHz (27).

It is traditionally thought that voltage-state logic operates only in the range of a few gigahertz. This limited speed operation is usually attributed to the "punch-through" problem. There are two types of punch-through, one caused by the plasma oscillations of the junction (36), and another called

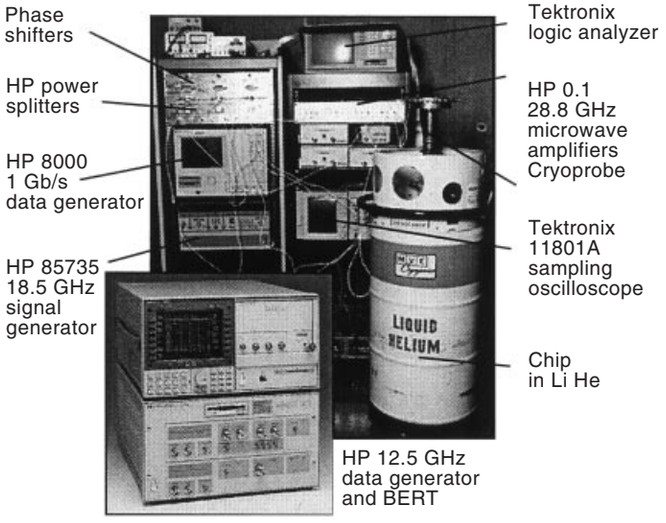


Figure 14. A typical laboratory high-speed test setup. The superconducting chip is mounted on the end of a high-bandwidth probe and is immersed in a liquid helium dewar. Inputs and outputs are via high-speed SMA cables, and the output is detected on the sampling oscilloscope.

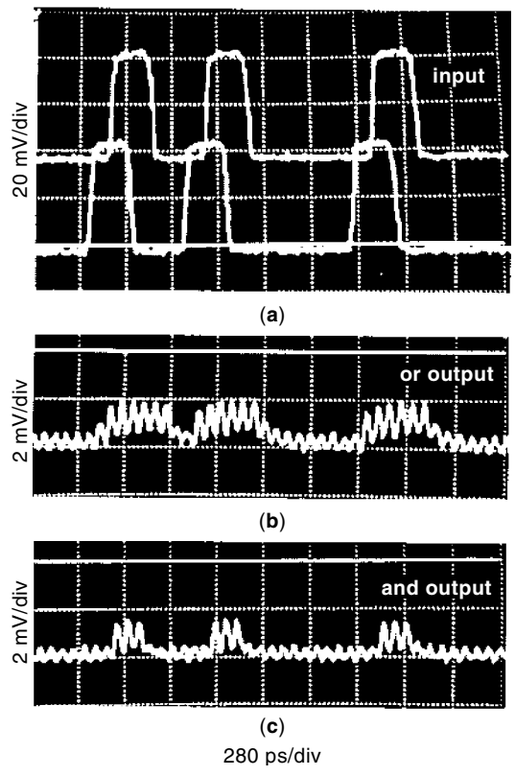


Figure 15. (a) Photograph of 4 GHz input test data taken from a sampling scope. A pulse splitter and a short length of cable were used to make the phase delay of the top trace. (b) Output of the COSL OR gate circuit clocked at 15 GHz. The circuit switching is observed when either of the two lower speed signals is switched "on." (c) The AND gate switching occurs when the two inputs overlap.

low-probability punch-through (37). The first type of punch-through is related to the plasma oscillation of the Josephson junction when it resets. Using the mechanical analog, when the undamped pendulum stops spinning, there are finite oscillations at the bottom of the arc, as the pendulum damps to zero; see Eq. (5). This is analogous to the latching Josephson junction. As the junction resets, voltage oscillations called plasma oscillation are observed at the end of the logical pulse. If the clock is applied before complete damping has taken place, then the junction can misfire. This misfire, caused by nonresetting of the junction, is termed punch-through. However, circuit parameters can be chosen so that for a given clock speed and junction process the damping oscillations never misfire the circuit. Therefore, although the long resetting time of the junction limits the ultimate clocking speed, it will not generate random punch-through errors if the circuits are designed correctly.

To understand the concept of low-probability punch-through, return to the pendulum model of the Josephson junction, Eq. (4). When the undamped spinning pendulum is reset by removing the external tourque (clocked dc bias), there is a small but finite probability that it will stop at the top of the arc rather than at the bottom, that is, there is a small probability that the pendulum will end up balanced at the unstable equilibrium point. If this happens for a Josephson junction, then the Junction is easily switched to the voltage state without any input when the next clock cycle is applied. The device

"punches through" to give an error "one" output even though there may have been a "zero" input. In a process with high Josephson junction initial current, the probability of this type of punch-through is very small, much less than 10^{-12} for COSL. Therefore for applications, such as analog-to-digital conversion, low-probability punch-through is not a significant source of errors. Bit error rate measurements on the COSL gates demonstrate that voltage-state logic can operate with very high clock speeds without significant errors from punch-through.

The design challenge for complex voltage-state logic circuits is the distribution of the multiphase clocks. For large circuits the clock lines have low impedance and will carry all of the power for the circuit (of the order of mW). Considerable cross talk can occur between transmission lines, so that the design and testing of complex voltage-state logic circuits that operate at speeds beyond 10 GHz is challenging. The ultimate application of voltage-state COSL circuits may be as interfaces between rapid single-flux quantum logic (RSFQ) circuits and room temperature electronics. RSFQ circuits can operate at speeds in excess of 100 GHz and are described in detail in the following section.

Rapid Single-Flux-Quantum (RSFQ) Logic

RSFQ logic was proposed by Likharev, Mukhanov, and Semenov (23,28) in 1985, and was based upon the principles proposed by Silver and his collaborators (38) and Sawada and co-workers (39). The basic RSFQ circuit element is shown schematically in Fig. 16(a). The Josephson junctions are resistively damped by parallel resistors and are connected to an inductor. A dc bias is applied to the junction. The value of the critical current, resistor, and the inductor are chosen so that the dimensionless parameter $\beta_c = 2\pi i_c R^2 C_j/\Phi_0 \sim 1$ and $Li_c \sim \Phi_0$.

For the simple case where the inductor in Fig. 16(a) is connected to ground, Eq. (4) is applicable to the circuit where the inductance adds just a linear term in ϕ. Returning to the pendulum mechanical analog for the Josephson junction, the junction (pendulum) cannot "spin" freely because of the damping resistor. Recall that a dc bias applied to the junction is equivalent to a torque on the pendulum. For a bias current approximately 80% of the critical current value, the pendulum is rotated close to the horizontal unstable equilibrium point. If the pendulum is kicked over the unstable equilibrium point, it flips in a circle. One can imagine that with gravity the pendulum moves slowly over the top, rapidly picks up speed toward the bottom of the arc, and then moves back to the original position. From Eq. (3) the rate of change of the pendulum angle (junction phase) is equivalent to the voltage across the device. Hence, as the junction flips, a voltage pulse is produced; see Fig. 16(b).

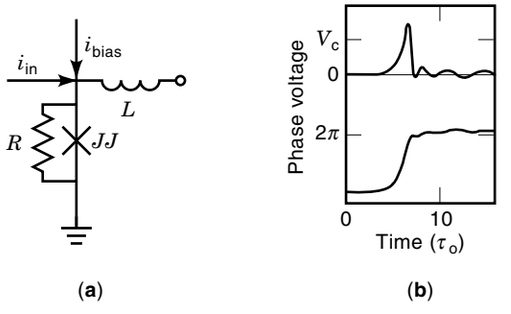


Figure 16. (a) The basic RSFQ circuit element. The junction is shunted by a resistor that is typically 1 Ω to 2 Ω. (b) A single flux quantum pulse generated by flipping a damped Josephson junction in parallel with an inductor. The width of the pulse is a few picoseconds. The original part (b) is from Likharev and Semenov (23), © 1991 IEEE.

The junction switching is very fast, and the corresponding voltage pulse is typically a few picoseconds in width. These picosecond voltage pulses comprise the logical "ones" in an RSFQ digital circuit. Logical "zero" is the absence of a picosecond pulse within a clock period. As a junction flips, the phase (pendulum angle) changes by exactly 2π radians. From Eq. (6) the junction phase can be related to the magnetic field in the inductor by $\phi = 2\pi\Phi/\Phi_0$, so that a 2π phase change corresponds exactly to the transfer of a single quantum of magnetic flux. Equivalently, the integral of the voltage pulse "area" is quantized,

$$\int V(t)\,dt = \Phi_0 = 2.07\,\text{mV ps} \tag{12}$$

so that the total RSFQ voltage pulse integrated over time equals a quantum of magnetic flux given by Eq. (6). Hence the name single-flux-quantum logic. Also note from Eq. (12) that if the pulse is a few picoseconds wide the amplitude will be much less than 1 mV.

The simplest RSFQ circuit, called the Josephson transmission line (JTL) and shown schematically in Fig. 17(a), consists of the basic RSFQ component in Fig. 16(a) connected in series. The series junction and the inductor at the input convert a dc signal to single-flux quanta (dc-SFQ converter). Intuitively one can image the circuit as a series of pendula connected together by torsion springs (the inductors). The dc bias currents torque the pendulums close to the unstable equilibrium point. When a single-flux quantum pulse is fed in at the left end of the line, it flips the first junction (pendulum). Because this junction is connected to the adjacent junction by an inductor (a spring), when the first junction flips, it makes a current in the inductor which in turn flips the adjacent junction (the next pendulum). Hence in a JTL, a flux quantum input at the left "hops" down the line, flipping adjacent junctions until reaching the output. Figure 17(b) shows a WRspice (35) simulation of the input and output voltage of the JTL with a 10 GHz input.

The clock signals for RSFQ circuits are single-flux-quantum pulses. The logical convention is that a "one" corresponds to an RSFQ pulse within a clock period, and a logical "zero" is the absence of a pulse in a clock period. JTLs are used for clock distribution. However one does not have to use JTLs for all data and clock distribution. For example, the digital signal processor in the ADC in Fig. 7 is broken into three components. The RSFQ and data pulses are transferred between modules by superconducting microstrip lines. Because the transmission lines are superconducting, they have low loss and low dispersion. With superconducting transmission lines one can transport RSFQ pulses for relatively large distances on a chip.

The switching speed of the damped junction is a function of the device capacitance. Reducing the junction area corre-

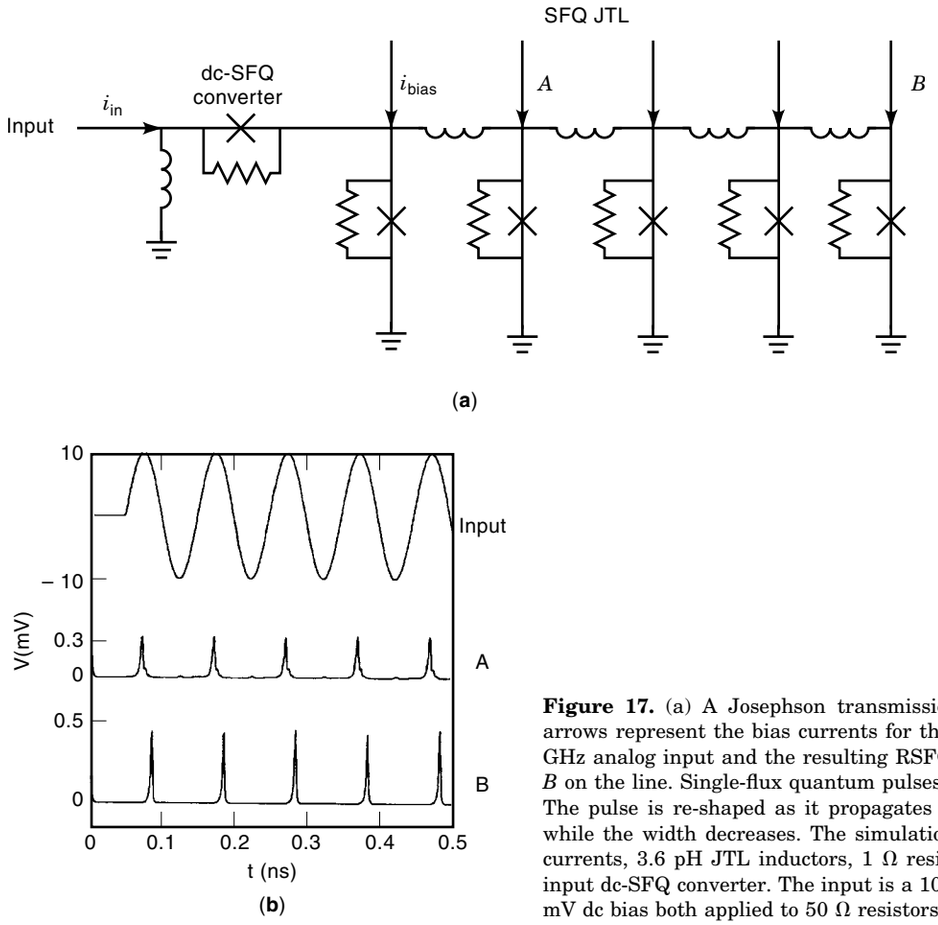


Figure 17. (a) A Josephson transmission line with a dc-SFQ input circuit. The arrows represent the bias currents for the JTL. (b) WRspice simulation with the 10 GHz analog input and the resulting RSFQ voltage pulses measured at points *A* and *B* on the line. Single-flux quantum pulses propagate from *A* to *B* with a 10 ps delay. The pulse is re-shaped as it propagates from *A* to *B*, and the amplitude increases while the width decreases. The simulation assumes 200 μA junctions, 175 μA bias currents, 3.6 pH JTL inductors, 1 Ω resistors, and a 5 pH parallel inductor in the input dc-SFQ converter. The input is a 10 GHz 10 mV amplitude sine wave and a 10 mV dc bias both applied to 50 Ω resistors.

spondingly decreases the junction capacitance and enables the junction (pendulum) to flip faster. Hence smaller junctions make faster RSFQ circuits, providing one scales the other parameters accordingly. For example, a 100 μA critical current Josephson junction with a 2.5 μm linear size corresponds to a 3 ps RSFQ pulse. A 1.25 μm junction corresponds to a 2 ps pulse, and a 0.7 μm junction corresponds to a 1 ps pulse. Lukens and co-workers at the State University of New York at Stony Brook have used e-beam lithography to fabricate simple RSFQ frequency divider circuits with 0.5 μm $\times$ 0.5 μm junctions and 50 kA/cm^2 critical current density.

Figure 18(a) shows a micrograph of an RSFQ T flip-flop circuit, and Fig. 18(b) shows experimental test data with a schematic of the circuit inset on the graph. The circuit consists of a Josephson transmission line connected to the RSFQ flip-flop, consisting of four Josephson junctions. A dc bias applied to the first junction in the JTL generates a high frequency SFQ pulse train which is input to the flip-flop circuit. The parameters of the SQUID loop are chosen so that a single-flux quantum can circulate in the loop. When the input pulses are injected into the loop, they have the effect of flipping the direction of the circulating flux quanta. Furthermore, if the current is circulating in the clockwise direction, a single flux quantum pulse is also produced at the output, V_{out}; see Fig. 18(b). Therefore, the input flips the circulating current, and a half-frequency RSFQ pulse train is produced.

The diagonal plot on Fig. 18(b) is an overlay of the average voltage of the clock and twice the average voltage of the output. Increasing the input bias current increases the frequency of the input clock. Because the output is half the frequency of the input, we expect that, on average, the input voltage should equal twice the output voltage. The two measured quantities are indeed equal, and from the fundamental Josephson Eq. (3) one can calculate that the speed corresponds to 750 GHz.

The experimental data in Fig. 18(b) are dc average value measurements. The circuit operation is too fast to observe the digital outputs directly by room temperature electronics. Therefore, it is not clear how many errors the circuit makes at 750 GHz. The lower trace in Fig. 18(b) is the subtraction of the two curves and gives the error in the experiment. It corresponds very roughly to a limit on the maximum bit error rate in this experiment. The error is less than one part in 10,000 which is the limit of the test equipment, and the true bit error rate should be significantly less.

Therefore, RSFQ circuits have the potential of operating at hundreds of gigahertz clock rates. So far we have described the JTL, which can be used to transport RSFQ pulses, and the T flip-flop which is the basic memory storage element. To make a complete logic family, Likharev, Mukhanov, and Semenov demonstrated OR, AND, and inversion functions for RSFQ (28). As one example, Fig. 19 shows the RSFQ 2-input OR gate.

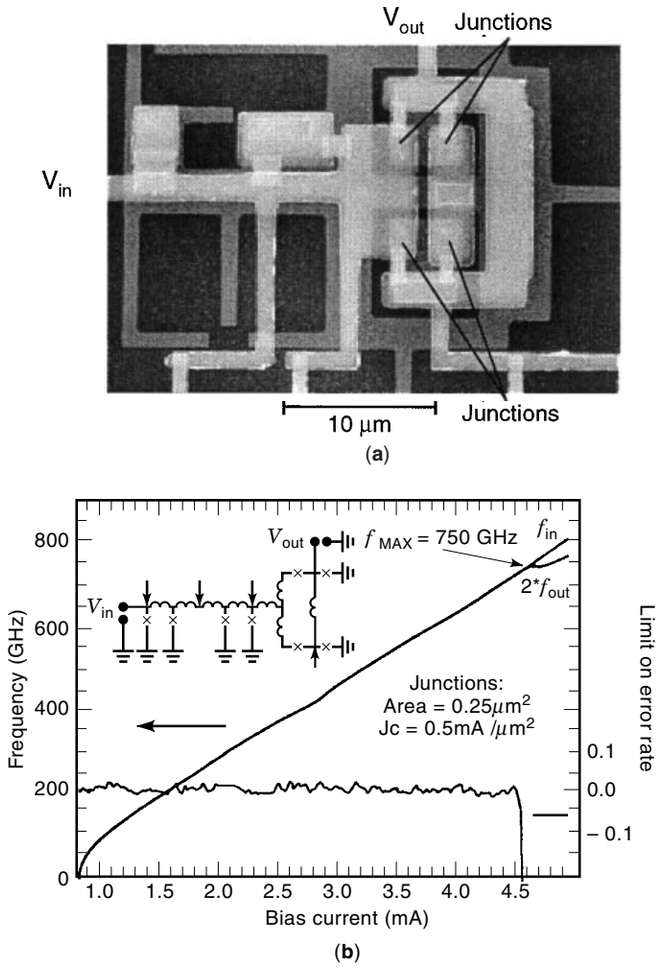


Figure 18. (a) Micrograph of an RSFQ T flip-flop fabricated using e-beam lithography. (b) Test data for a T flip-flop fabricated with 0.5 μm $\times$ 0.5 μm Josephson junctions. The circuit operates correctly up to a speed corresponding to 750 GHz. Photograph and data courtesy of W. Chen, A. V. Rylyakov, V. Patel, and J. E. Lukens at State University of New York at Stony Brook.

The OR gate consists of two Josephson junctions J2 and J4 at the input connected to the inductor L3 and the junction J5. The junctions J1 and J3 are for isolation and stop feedback of RSFQ pulses to the input. Parameters are chosen so that an input RSFQ pulse at either *A* or *B* flips the junction J6. This junction is connected to a flip-flop circuit (J6, L, J7) which is a SQUID loop with an RSFQ readout. When junction J6 is switched by the input at either *A* or *B*, a single-flux quantum is held in the SQUID loop J6, L, and J7. The SQUID loop acts as a latch until the clock is applied. Quanta stored in the SQUID loop are read out by a clock pulse applied to the junction pairs J7 and J8. Parameters are chosen so that the clock pulse resets the SQUID loop and produces a flux quantum at *F* if there has been an input at *A* or *B*. This is the timed OR function. For more detailed information on the complete RSFQ logic family, see Ref. 23.

Figure 20 is a schematic of a simple RSFQ circuit designed by Herr and Feldman at the University of Rochester to test bit error rates (40). The circuit consists of a 10 GHz RSFQ

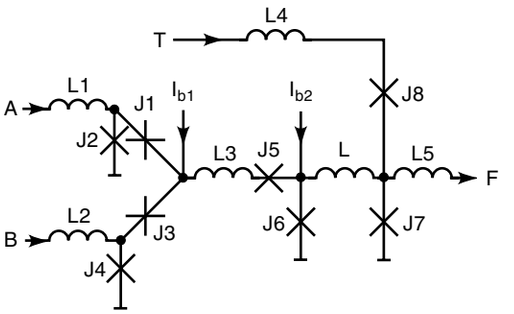


Figure 19. The basic RSFQ OR gate. The picosecond RSFQ pulses race through the circuit and are held in the SQUID loop J6, L, and J7 "latch." A clock RSFQ pulse is applied to the junction pair J8 and J7 to read out the latch. Original figure from Likharev and Semenov (23), © 1991 IEEE.

ring oscillator, which generates the clock, and two JTL stages connected to an XOR gate. Identical pulse trains from the clock propagate down the JTL stages, so that the XOR function should be logical "zero" for all correct outputs. Any error in the JTL stages produces an RSFQ pulse at the output of the XOR gate. The Rochester team measured the continuous operation of the circuit for nine days and measured a bit error rate of 5×10^{-17}. This error rate corresponds to 4 errors in 150 h ($5\frac{1}{2}$ days). These results matched well with thermal noise analysis of errors for a single junction. Therefore, RSFQ circuits have the potential for ultrahigh-speed operation with very low bit error rates.

Ruck and coworkers in Jülich have done the same experiment with a circuit fabricated using high temperature superconductors, and have measured bit error rates less than 10^{-11} at 39 K (41). However, note that in these experiments the circuit under test is rather simple and the bit error rates may increase for complex RSFQ circuits.

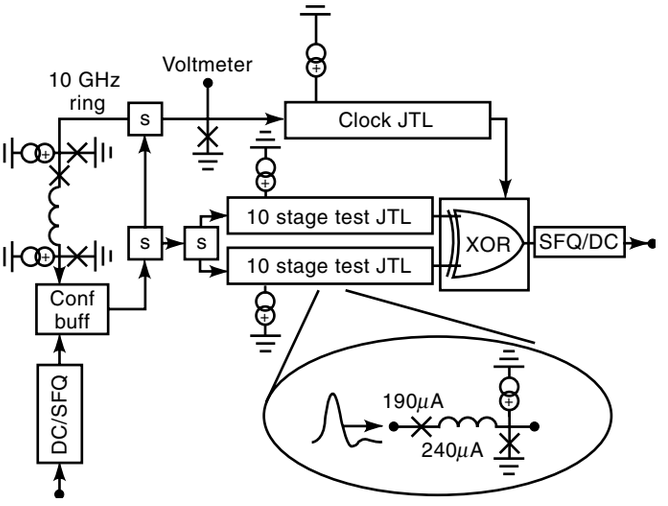


Figure 20. Schematic diagram of the test circuit to measure RSFQ bit error rates. Figure reproduced courtesy of Q. Herr and M. Feldman, University of Rochester, and *Applied Physics Letters* (41).

Picosecond RSFQ voltage pulses cannot be transferred between chips or to room temperature electronics with existing packaging. This is because they are easily attenuated or reflected by impedance mismatches and conventional room temperature electronics is simply neither fast enough nor sensitive enough to detect small picosecond signals. Therefore, the RSFQ pulses must be converted to lower frequency voltages at the output (23). Recently, researchers at HYPRES and Conductus have developed asynchronous amplifier circuits, so that one can interface RSFQ pulses directly to room temperature electronics at clock rates up to 8 GHz (42). High-speed testing has been performed on-chip at 20 GHz to 40 GHz by loading shift registers with data at low speed. Then these data are clocked through an RSFQ circuit at high speed, and the outputs are collected at high speed in shift registers. Finally, the output data are read out from the shift registers at low speed to verify the correct operation of the circuit.

One advantage of RSFQ over voltage-state logic is that it requires only dc power. The power dissipation of RSFQ circuits is approximately 10,000 times lower than GaAs room temperature electronics and approximately 50 times less than voltage-state logic. Therefore, thermal management is significantly easier for superconducting RSFQ digital circuits than for other room temperature technologies such as GaAs. The main challenge for RSFQ circuits and indeed any circuit operating above 10 GHz is clock distribution. For example, at 100 GHz there is only 10 ps between clock pulses. Assuming propagation at the speed of light, 10 ps corresponds to 3 mm. Because typical complex circuits are larger than 3 mm, global clock distribution is not possible at this speed. Researchers at UC Berkeley and elsewhere have been working to develop new types of asynchronous timing schemes to enable complex circuit operation at ultrahigh gigahertz clock rates (23,43).

ADVANCED APPLICATIONS AND FUTURE DIRECTIONS FOR DIGITAL SUPERCONDUCTING ELECTRONICS

We are at an exciting point in the development of superconducting electronics. Fabrication techniques and design tools are enabling the development of the first real systems. For example Conductus, TRW, Stanford University, and UC Berkeley, funded through the US Department of Commerce Advanced Technology Program (ATP), collaborated to demonstrate a superconducting cross-bar packet switch. The system was packaged in a 4 K closed cycle refrigerator, all components were operational at 10 Gb/s, and the complete integrated system was demonstrated at 4 Gb/s (44). Although this system is not a final commercial product, it demonstrates the possibility of integrating and packaging superconducting circuits.

A significant accomplishment of the ATP project was the development of a superconducting multichip module (MCM) technology by TRW. Figure 21 shows a superconducting MCM with two chips used in the cross-bar demonstration flipped on top. Using reflow solder bumping and superconducting transmission lines between chips, researchers at TRW and Conductus demonstrated 10 Gb/s data transfer rates between chips and room temperature electronics. This MCM technology will facilitate the development of complex superconducting digital circuits from smaller components.

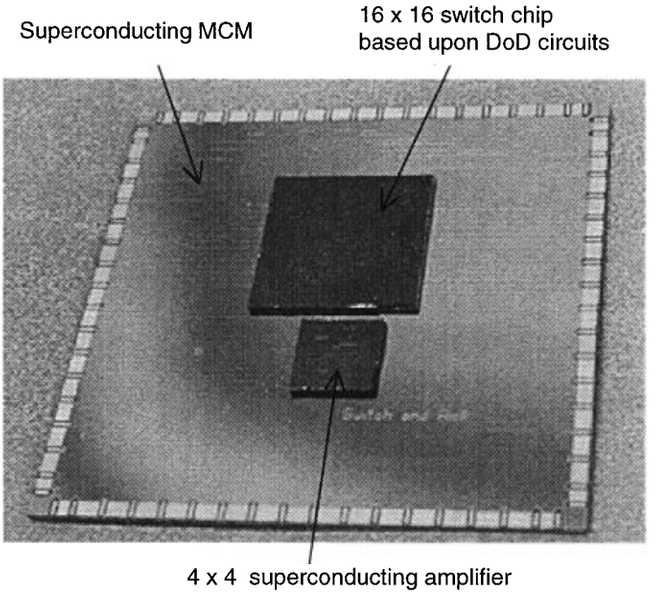


Figure 21. MCM module used in the ATP demonstration of a superconducting packet switch by Conductus, TRW, Stanford University and University of California, Berkeley. Both chips were fabricated using a 2 μm, 2 kA/cm^2 Nb Josephson fabrication technology. Photograph courtesy of G. Akerling, A. Smith, K. Yokoyama, and J. Spargo at TRW Space and Electronics.

Japanese industrial laboratories, such as Hitachi and NEC, continue to work on digital superconducting electronics. Recently completed projects at Hitachi include the development of a 4 $\times$ 4 packet switch using voltage-state logic (45). NEC researchers have demonstrated a system consisting of three computers connected by a superconducting parallel-pipelined ring (26,46). Components of these sytems, consisting of several hundred logic gates, have been demonstrated at multigigahertz data rates. The complete NEC system operated at 100 MHz, with an estimated ultimate throughput of 10 Gbit/s (46). NEC is working to develop micron size Josephson fabrication technologies in order to increase speed and integration density of their superconducting RAM. In 1998 the Japan Science and Technology Agency (STA) initiated a three year program for NEC, Hitachi, ETL, Fujitsu, Tokyo University, and Nagoya University. The goal of this program is to develop the core technology in Japan for ultrahigh-speed RSFQ logic circuits using both low-temperature and high-temperature superconductors.

Perhaps the most promising applications are in analog-to-digital conversion using RSFQ logic (see Fig. 7). Analog-to-digital converters (ADCs) are ideal candidates for superconducting electronics applications because all of the high-speed operations are internal to the circuit, and the outputs to room temperature electronics are relatively low speed. Furthermore, ADC circuits do not require frequent access to cache memory, which is at present difficult to implement in superconducting circuits. HYPRES Inc. in Elmsford, NY (18) has done considerable research to develop advanced ADC circuits.

Figure 22(a) is a 6-bit (2^6 level) flash type ADC developed at HYPRES Inc. The circuit consists of six comparators. The analog input signal is applied to a resistor divider network which feeds a one-junction SQUID at the input of each com-

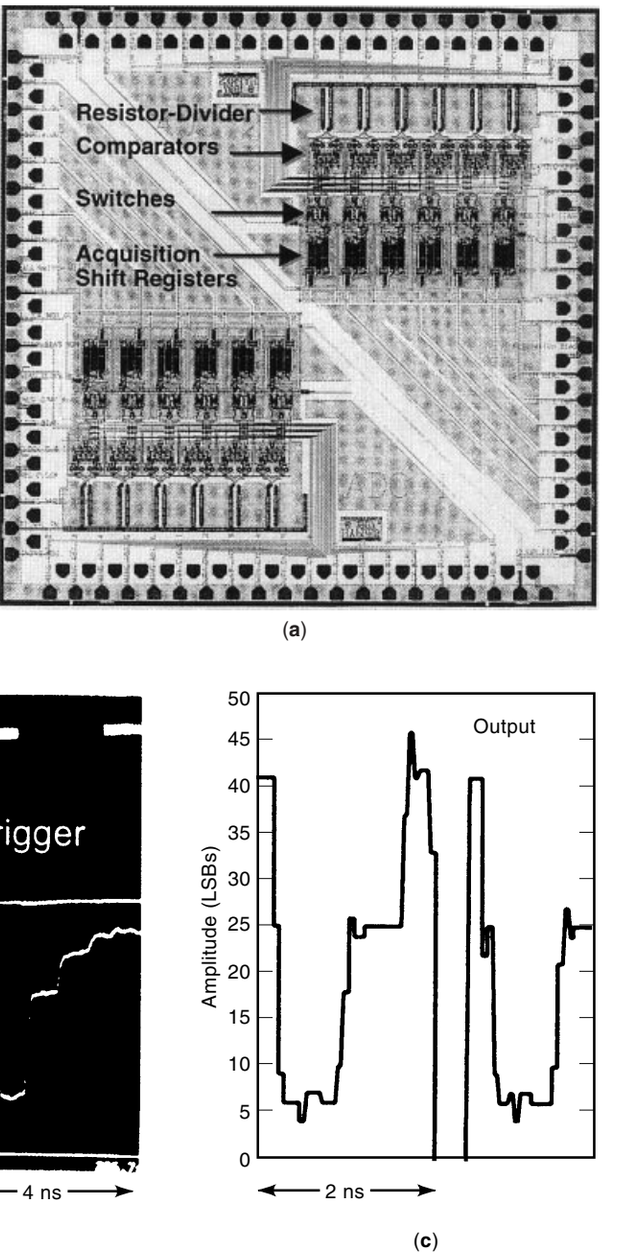


Figure 22. (a) HYPRES six-bit flash analog-to-digital converter fabricated on a 1 cm $\times$ 1 cm chip. Experimental test data (b) input to the circuit, and (c) collected in real time at 16 Gs/s. Photograph and data provided courtesy of S. Kaplan, S. Rylov, D. Gaidarenko, W. Li, and P. Bradley at HYPRES Inc. (18).

parator. RSFQ circuits are used for ultrafast sampling of the one-junction SQUID current. With certain parameters (that is, $\beta_L \leq 1$), the output current of the one-junction SQUID is periodic in the input current. Hence by using a resistor divider network, the one-junction SQUID currents make an interference pattern gray code for the input signal. Picosecond RSFQ sampling of this gray code gives a binary representation of the input analog signal. The circuit is compact, and requires only one comparator for each bit because the unique properties of the one-junction SQUID. To store the digitized data, a 32-word shift register memory is integrated within the ADC.

Figure 22(b) shows test data for the flash ADC for a 16 GHz sampling rate. The input signal (inverted by the amplifier) was acquired in real time, and the binary data were stored in a 32 bit shift register for low speed output to room temperature electronics. Research is in progress to directly interface this ADC to room temperature electronics, so that the performance specifications (spurfree dynamic range, effective number of bits, etc.) can be measured.

A fundamental advantage of superconducting electronics is low on-chip power dissipation compared to room temperature electronics, such as GaAs. Therefore, thermal management on-chip is significantly easier than with GaAs. Furthermore, compared to all other room temperature technologies, RSFQ has a raw speed advantage because digital operation is possible in excess of 100 GHz. These advantages make superconducting electronics a candidate for ultrahigh-speed supercomputer applications of the future. In fact, recent research has indicated the feasibility of a 10^{12} floating-point operations per

second (petaFLOP) RSFQ-based supercomputer. The peta FLOPs computer project, presently funded by the US Defence Advanced Projects Agency (DARPA), is studying the possibility of incorporating thousands of 100 GHz superconducting RSFQ vector processors (47).

The challenge for future digital superconducting technology is to unambiguously demonstrate circuits operating in excess of 100 GHz. These circuits will require small area ($\sim$0.8 μm linear size), higher current density ($J_c \approx 10$ kA/cm^2) junctions, and one must first demonstrate that a fabrication process can make hundreds of 0.8 μm 10 kA/cm^2 Josephson devices with small parameter spreads. In addition exact clocking of the ultrafast circuits needs to be achieved. At 100 GHz there is only a 10 ps window for a clock period, and at 200 GHz this window shrinks to 5 ps. Parameter variations and propagative time delays can easily introduce timing errors which will significantly limit the speed of complex circuits. Finally, the circuits must be tested unambiguously at ultrahigh speed. This is no easy task, since demultiplexer (DEMUX) circuits are needed to interface with room temperature electronics, which increases the complexity of even the simplest 100 GHz RSFQ circuit.

In the near future all systems based on digital superconducting circuits are expected to use conventional 4 K niobium superconductor technology that requires a relatively large refrigerator. For applications requiring low power and a small form factor, niobium nitride (NbN), $T_c = 17$ K, will most probably become the processing technology of choice for digital superconducting circuits. NbN circuits operate at 10 K and use small pulse-tube or Stirling coolers described in the introduction. However, research and development is required for NbN fabrication technology to reach its full potential.

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