SILICON-ON-INSULATOR DEVICES

TRENDS IN MICROELECTRONICS

Silicon is the leading semiconductor in the electronics industry. More than 95% of the integrated circuits are fabricated with Si-based devices. The basic component which is currently used for very large scale integrated (VLSI) circuits, such as microprocessors and memories, is the silicon metal–oxide–semiconductor field-effect transistor (MOSFET). The first structure with a thermally oxidized silicon was proposed and fabricated in the 1960s (1) and hugely developed during the past 30 years. The main advantage of this device, compared with many others using the field effect principle, is the quality of the Si/SiO_2 system. This silicon/dioxide interface has been improved over these years, leading to high-performance transistors with a very low defect density. Compared with their bipolar counterparts, in which both types of carriers are involved, the virtues of MOS transistors are low cost and high density. However, bipolar devices are also used for some applications needing high speed and/or low noise.

Complementary MOS (CMOS) has become the dominant MOS technology and uses both *n*-channel (electrons) and *p*-channel (holes) MOSFETs (Fig. 1). This structure has been chosen historically owing to its low-power consumption property compared with other ones (NMOS, etc.). More than 80% of the recent VLSI circuits are fabricated with the CMOS technology. The general trends in microelectronics are the reduction of device geometry which allows one to obtain an improvement of device performance and integration density. Other priorities in this field are the decrease of power consumption, the enhancement of reliability, and the reduction of the cost of electronic systems.

However, the device scaling down to deep submicron dimension faces formidable challenges. After 30 years of technology development, MOSFETs are pushed toward their fundamental and technological limits. Indeed, the scaling scenario put forth in widely accepted industry roadmaps calls for sub-0.1 μm gate length MOSFETs in the first decade of the twenty-first century. In this channel length range, the optimization of the transistors need in particular very thin source/drain junction depths and a good control of the electrostatic potential and charge in the active silicon layer in order to reduce parasitic effects (for instance, short channel effects and leakage currents) and to improve device performance (for example, drain current and transconductance). All these aspects, together with other advantages, which will be presented in the next section, are afforded by another Si-based device type, the silicon on insulator (SOI) structure.

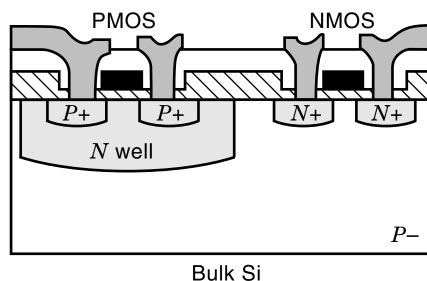

Figure 1. Bulk silicon CMOS structure.

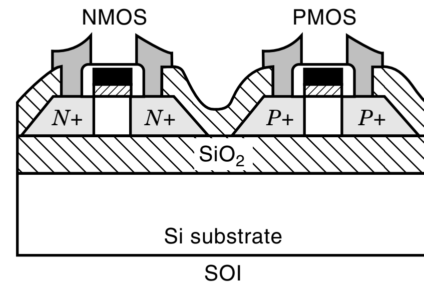

Figure 2. Silicon on insulator (SOI) CMOS structure.

THE SOI STRUCTURE

The SOI CMOS is shown in Fig. 2. A buried insulator, which is typically an oxide layer, is fabricated in the silicon substrate using various methods (see next section). A number of advantages, suitable for many applications, are obtained with the SOI structure, which allows us to push back the technological and physical limits intrinsic to the bulk Si structure (2,3):

1. The latch-up, a parasitic *n*-*p*-*n*-*p* structure (thyristor) which can be triggered in bulk silicon CMOS structures, is suppressed by the dielectric isolation of the SOI technology.
2. Ultrathin SOI films, inducing a full depletion of the active silicon layer, can easily be fabricated and have been shown to lead to very interesting behaviors. In this respect, a low-threshold voltage together with small leakage currents can be obtained which is of major importance for low-power–low-voltage integrated circuits used in portable electronic systems. Another advantage of such thin films is related to higher drain current and device speed.
3. The parasitic source/drain junction capacitances are substantially reduced using thin film SOI, leading to high-frequency operation (several tens of gigahertz have been demonstrated).
4. The leakage currents are significantly smaller in SOI than that of bulk Si devices (2–3 orders of magnitude) due to the reduction of the drain junction area. The exponential enhancement of the leakage current with temperature is the main limitation of the circuit functionality in conventional CMOS operation at high temperature. SOI devices are fully functional up to over 300°C and can be used in analog and digital circuits for automotive and aircraft applications.
5. In the DRAM field, the SOI structure also lead to improved performances. In particular, a better soft error immunity and a reduction of the cell capacitor can be obtained; 16 Mb, 64 Mb and 1 Gb memory chips have already been fabricated.
6. SOI MOSFETs are of great interest for niche applications, especially in the field of radiation hardness [advantage in transient ionizing and single-event upset (SEU)] for both space and nuclear radiation environments, owing to the small active volume. This was the first application of the SOI technology. Another example is low-temperature electronics for which the SOI

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structure prevents some harmful parasitic effects (for instance, the absence of the kink effect for thin-film SOI) observed in bulk transistors.

7. The dielectric isolation afforded by the buried insulator opens the way to integrate into a state-of-the-art CMOS process complementary bipolar transistors, power switches, or sensors (flow sensor, magnetic sensor, pressure sensor, etc.). The SOI technology leads to new "system on chip" concepts.
8. The special SOI structure can be advantageously used for developing new devices, like the volume-inversion MOSFET (with two gates or a gate all around the active Si layer), the voltage-controlled bipolar MOS device (with gate and body connected), and quantum devices (extremely thin Si film, quantum wires, single electron transistors, etc.).
9. Some process simplification are induced by the SOI technology, mainly in the isolation and high-energy implantation.
10. Short channel and hot carrier effects, which are detrimental to device reliability, can be reduced in SOI MOSFETs.
11. Three-dimensional ICs can also be realized on SOI materials, allowing a further potential enhancement of the level of circuit integration.

However, some parasitic effects can also be observed in SOI devices. In this respect, floating body effects and self-heating effects are the main drawbacks of the SOI technology. These phenomena and possible improvements will also be discussed in the following sections together with the previous advantages.

In view of the huge amount of work recently carried out by many companies, it seems that the SOI CMOS technology is really taking off. Various circuits have been realized in SOI technology: DRAM and SRAM (Hyundai—64 MB and 1 GB DRAM; Samsung—16 MB DRAM; TI—1 MB SRAM; IBM—512 kB SRAM, Sony—256 kB SRAM, Mitsubishi—64 kB DRAM; LETI—16 kB SRAM; Harris—4 kB SRAM; NTT—1 kB SRAM), frequency divider—prescaler—PLL (NTT), μcontroller CPU (Motorola), 16 × 16B multiplier (Toshiba), and so on. The first large-volume commercial market for SOI technology will certainly be low-voltage applications. In this respect, the capability of SOI has been demonstrated for a power supply reduction in the sub-1 V range, down to 0.5 V, with respectable performances. SOI devices will thus be part of the wireless electronic revolution.

A relevant question is the availability of SOI wafers in large number. Various approaches have been used for fabricating SOI materials. Among all the techniques proposed to perform the SOI structure, only three are still competing and are the only serious challengers of standard silicon: SIMOX (separation by implanted oxygen), WB (wafer bonding, or BESOI—bond and etch back SOI), and the Smart Cut technology (material called UNIBOND) which combined both hydrogen implantation and bonding. These last two techniques have a much higher throughput potential and are available in Europe, the United States, and Japan. The next section will discuss the various SOI material approaches.

SOI MATERIALS

SOI materials can be divided into two groups. In the first group, the silicon film is deposited directly on an insulating substrate, as in the case of silicon on sapphire (SOS), which was the first SOI technology proposed in the 1960s, and silicon on zirconia (SOZ). In the second group, a thin insulating layer is used to separate the active silicon layer from the Si substrate. Methods of forming these structures include zone melting recrystallization (ZMR) of polysilicon, epitaxial lateral overgrowth (ELO), and full isolation by porous oxidized silicon (FIPOS), as well as SIMOX, WB, and Smart Cut discussed previously. Only the last three techniques, which are the main ones, will be briefly presented below.

SIMOX

The SIMOX material formation uses the following key processes (4–6) (Fig. 3):

1. An oxygen implantation step at high dose (O^+ doses around 1.8×10^{18} cm^{-2} are commonly used, which is several hundred times higher than the heaviest doses of conventional dopants used for the formation of the channel and source/drain in microelectronics processing), along with high energy (≥150 keV) to locate underneath the initial silicon substrate a high concentration of oxygen. A buried oxide 0.2–0.4 μm thick is formed with this process.
2. A high-temperature anneal (1250–1405°C) to regenerate the crystalline quality of the silicon layer remaining over the oxide; this anneal drives or obstructs the chemical reaction which forms the stoichiometric oxide buried in the silicon wafer, which depends on the ambient temperature.

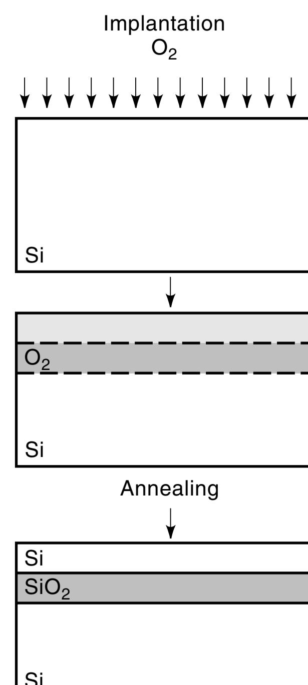

Figure 3. SIMOX material formation.

The new trend in SIMOX development is the use of low-dose (a few 10^{17} O^+/cm^2) and low-energy oxygen implantation to obtain a low-cost SOI material, since the production cost is proportional to the dose and the energy used for the implantation. Thin buried oxides (≤100 nm) and silicon overlayers with low defect density are obtained with this method. The main disadvantages of the SIMOX technology are the use of nonstandard equipment and the need for very high temperature annealing, which could be a limitation for 300 mm wafer size. SIMOX is also limited to thin-film applications.

Wafer Bonding

The wafer bonding technique can be used for manufacturing thick film of both oxide and silicon. There are three basic steps which are required for the bonding process (7) (Fig. 4):

1. Starting with two silicon wafers, at least one with an oxide layer on top, these two wafers are bonded together using van der Waals forces.
2. Subsequent annealing of the bonded wafers at temperature above 800°C for several hours increases the bonding strength.
3. Then one of the substrates is thinned down to a proper thickness by grinding and polishing and/or etching (a chemical etch stop, for instance a boron-doped layer, can also be used to ensure a better uniformity).

The main drawback of wafer bonding technique is its difficulty in producing extremely thin uniform Si film. However, new techniques have recently been proposed for the production of thin SOI films with a good uniformity (8).

Smart Cut

This is the most recent technique for the fabrication of SOI material. Smart Cut is based both on ion implantation and on wafer bonding technologies (Fig. 5). The ion implantation step ensures uniformity of the SOI film, and the bonding step allows the use of a thermally grown buried oxide and the perfect crystalline quality of the top silicon film. Standard equipment can be used for the fabrication of these structures.

Smart Cut needs the following main steps (9):

1. Starting with two wafers, at least one is oxidized to form what will become the buried oxide layer of the SOI structure.
2. Ion implantation (H^+) through the oxide forms the Smart Cut layer. The dose is in the range of $5 \times 10^{16}/cm^2$.
3. The two wafers are bonded together using van der Waals forces.
4. The top wafer is then cut away using 500°C thermal activation to form in the hydrogen implanted region a cleavage plane by merging all the microcavities created after H^+ implantation.
5. The SOI wafer is then annealed at 1100°C. Finally a touch polishing step is used to bring the surface roughness to a suitable value.
6. The remaining wafer is used as the support wafer in the next process flow, which is interesting for the cost reduction.

The type of SOI materials, the thickness of the Si film inducing a full or partial depletion of the SOI MOSFETs fabricated on the top of these materials, the buried oxide thickness, and the operation mode (inversion or accumulation) are relevant issues which may depend on the application. The electrical properties of these various SOI devices will be discussed in the following sections. In particular, the potential of the SOI structure for optimizing device and circuit operation and

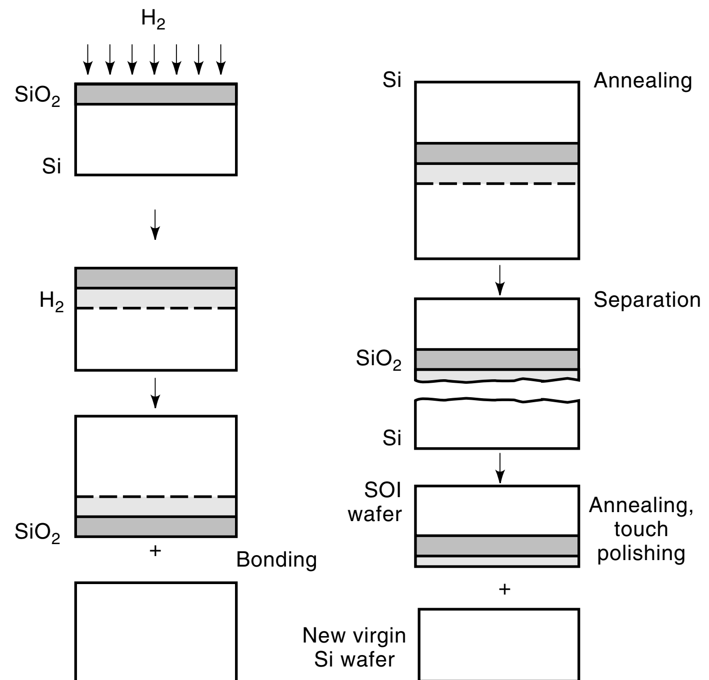

Figure 5. Processing sequence for Smart Cut (UNIBOND material).

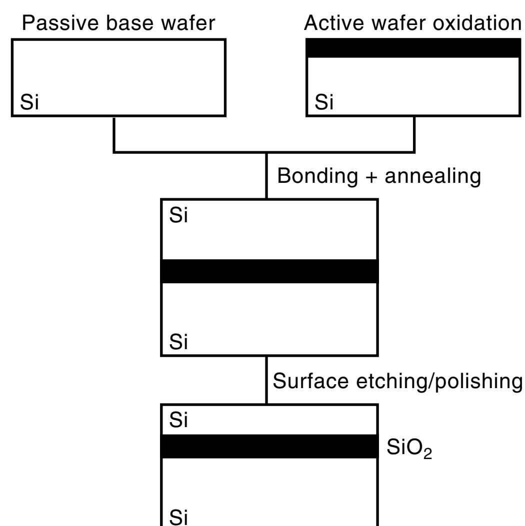

Figure 4. Material formation by the wafer bonding technique.

reaching the main goals of MOSFET operation (high drain current and transconductance, minimum subthreshold swing, low short channel and hot carrier effects, reduced electrical noise, minimal leakage currents, and parasitic phenomena) will be thoroughly investigated.

SUBTHRESHOLD SWING AND THRESHOLD VOLTAGE OF THE SOI MOSFET

MOSFET operation is governed by the electrons or holes transport between the source and the drain of the devices which leads to the drain current. The inversion (N^+PN^+ or P^+NP^+ structures) or accumulation (N^+NN^+ or P^+PP^+ structures) channel of electrons or holes can be formed at the silicon/oxide interface by biasing the gate of the transistors. The threshold of the MOSFET is reached when a high density of free carriers (equivalent to the doping density) is created at the Si surface (for a surface potential equal to $2\Phi_F$, Φ_F being the Fermi potential depending on the Si doping). The gate voltage for which this situation appears is called the threshold voltage of the MOS transistor. Above the threshold voltage V_t, the drain current I_d presents a linear or sublinear variation with the gate bias V_g (strong inversion or accumulation region). Below V_t, the drain current varies exponentially with V_g (weak inversion or accumulation region). The slope of the transfer $I_d(V_g)$ characteristic in a logarithmic scale is called the subthreshold slope (the term "subthreshold swing" is also used and is proportional to the inverse of the slope). This is a key parameter because it determines the switching characteristics between the off (very small current) and on (high current) state of the device (see Fig. 6).

Two types of SOI MOSFETs can be obtained according to the thickness and the doping of the active silicon layer. When the depletion layer under the gate oxide, obtained by biasing the gate of the MOSFET, extends throughout the whole silicon film thickness, the device is called "fully depleted (FD)." If the maximum depletion width given by

$$x_{\mathrm{d\,max}} = \sqrt{\frac{4\epsilon_{\mathrm{Si}}\phi_{\mathrm{F}}}{qN_{\mathrm{a}}}} \quad (1)$$

(which is observed for $V_g \geq V_t$) is smaller than the Si film thickness, the transistor is called "partially depleted (PD)"

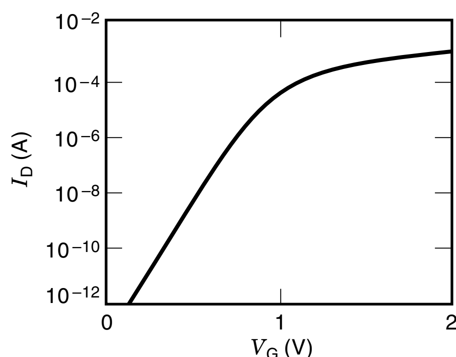

Figure 6. Typical drain-current–gate-voltage transfer characteristic of a MOSFET.

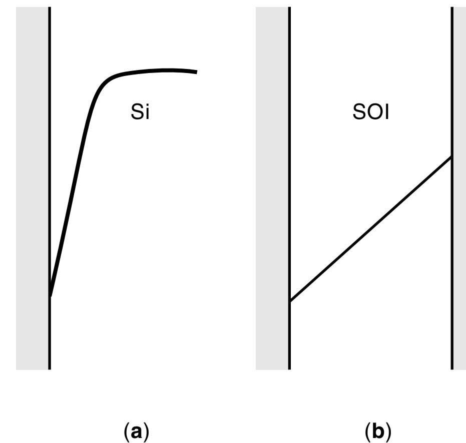

Figure 7. Typical potential variation in the active silicon layer for (a) a bulk-like SOI MOSFET and (b) a fully depleted SOI MOSFET; a linearly varying potential is a good approximation for $V_g \leq V_t$ in thin-film fully depleted SOI devices (13).

(Fig. 7) (ϵ_{SI} is the Si permittivity, Φ_F the Fermi potential, N_a the Si film doping, and q the electron charge). Fully depleted SOI MOSFETs have been fabricated on SOS materials (10), but an Si film of poor quality was obtained with this technology. SOI MOSFETs with full or partial depletion present very different electrical properties. A prominent advantage of fully depleted SOI MOSFETs formed on good-quality thin film (with SIMOX, WB, or Smart Cut) is due to the possible improvement of the subthreshold swing as compared to partially depleted Si film or bulk silicon transistors (11). The equivalent circuits in weak inversion of a bulk-like MOSFET (bulk or partially depleted SOI transistor) and a fully depleted SOI MOSFET (12,13) are shown in Figs. 8 and 9, respectively. For a fully depleted device (Fig. 9), the depletion capacitance C_d ($= dQ_d/d\Phi_s$, Q_d being the depletion charge and Φ_S the potential at the Si/SiO_2 interface) is suppressed because the depletion charge is limited by the thickness of the Si film and thereby does not vary with the gate voltage or the surface potential. C_d is replaced by a series of capacitances. If the FD SOI MOSFET is fabricated with a thick buried oxide and/or a low doping density in the silicon substrate (under the buried oxide) leading to small buried oxide and substrate (depletion) capacitances, the subthreshold swing S can be substantially lower than that observed in bulk devices. For small interface state densities at the various Si/SiO_2 interfaces, which is usually the case for present technologies, the swing can reach the minimum theoretical limit of about 60 mV/dec at 300 K (11,14). This offers the opportunity to achieve both a low threshold voltage and a small leakage current. These fully depleted SOI devices are very interesting for high-performances, low-voltage, low-power integrated circuits.

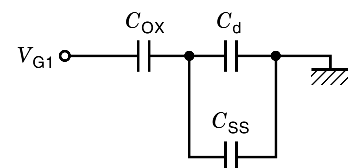

Figure 8. Equivalent circuit in weak inversion of a bulk MOSFET.

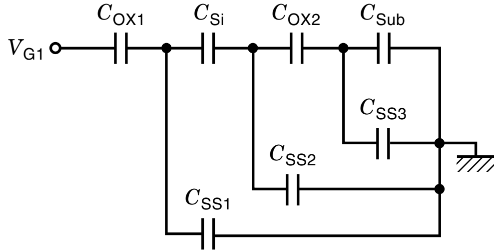

Figure 9. Equivalent circuit in weak inversion of a fully depleted SOI MOSFET.

The swing S for bulk-like [Eq. (2)] and FD SOI [Eq. (3)] MOSFETs (13) can be described by

$$S_{\text{bulk}} = \frac{kT}{q}\ln(10)\left(1 + \frac{C_{\text{d}} + C_{\text{ss}}}{C_{\text{ox}}}\right) \tag{2}$$

$$S_{\text{soi}} = \frac{kT}{q}\ln(10)\,\frac{(C_{\text{ox1}} + C_{\text{ss1}})[(C_{\text{si}} + C_{\text{ss2}})C + C_{\text{ox2}}(C_{\text{sub}} + C_{\text{ss3}})] + C_{\text{si}}[C_{\text{ss2}}C + C_{\text{ox2}}(C_{\text{sub}} + C_{\text{ss3}})]}{C_{\text{ox1}}[(C_{\text{si}} + C_{\text{ss2}})C + C_{\text{ox2}}(C_{\text{sub}} + C_{\text{ss3}})]} \tag{3}$$

where kT is the thermal energy, q is the electron charge, C_d ($= \epsilon_{si}/x_d$, ϵ_{si} being the silicon permittivity and x_d the width of the depletion charge under the gate) is the depletion capacitance, C_{ss} ($= qN_{ss}$, N_{ss} being the interface state density) and C_{ox} are the interface state and gate oxide capacitances for bulk structures, C_{si} ($= \epsilon_{si}/t_{si}$, t_{si} being the Si film thickness) is the thin Si film capacitance for SOI devices, C_{ox1} and C_{ox2} are the gate oxide and buried oxide capacitances, C_{ss1}, C_{ss2}, and C_{ss3} are the interface state capacitances at the gate oxide/Si film, Si film/buried oxide, and buried oxide/Si substrate interfaces, respectively, C_{sub} is the substrate capacitance associated with the charge under the buried oxide, and $C = C_{ox2} + C_{ss3} + C_{sub}$.

Figure 10 presents the simulated variations of S as a function of Si film thickness t_{si}. A significant improvement of the swing is observed when the SOI device becomes fully depleted ($t_{si} \leq 100$ nm) (11). The influence of the buried oxide thickness in a fully depleted SOI MOSFET is simulated in Fig. 11 (13). In the case of a thick buried insulator ($t_{ox2} \geq 300$ nm), the swing is slightly reduced with decreasing the film thickness. In contrast, the swing shows a substantial increase when we reduce the Si layer thickness in the case of a thin buried insulator (<100 nm). This behavior is observed for a high doping in the Si substrate inducing an accumulated buried oxide/silicon substrate interface (Figs. 11 and 12). When the bottom surface of the buried oxide is depleted (for a low Si substrate doping), the substrate capacitance is significantly reduced. Therefore, the swing is improved when we decrease the film thickness whatever the buried oxide thickness is (Fig. 12), but the decrease of t_{ox2} always degrades the swing (Fig. 13).

The back interface state density may also play a remarkable role. This is why for an Si film/buried oxide interface of

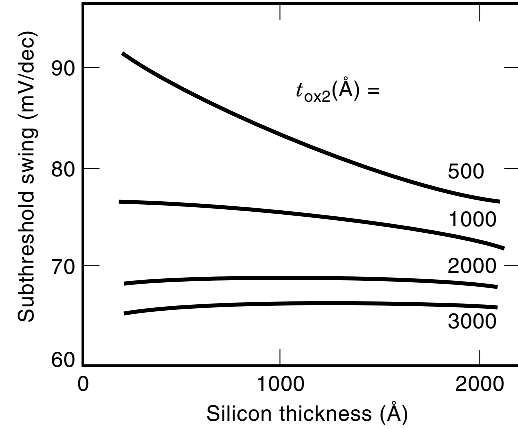

Figure 11. Simulation of the subthreshold swing as a function of the Si film thickness for various back insulator thicknesses (gate oxide thickness t_{ox1} = 27 nm, 10^{15} cm^{-3} Si film doping, $N_{ss2} = C_{ss2}/q = 0$, $N_{ss3} = C_{ss3}/q = 0$, accumulation at the buried oxide/Si substrate interface).

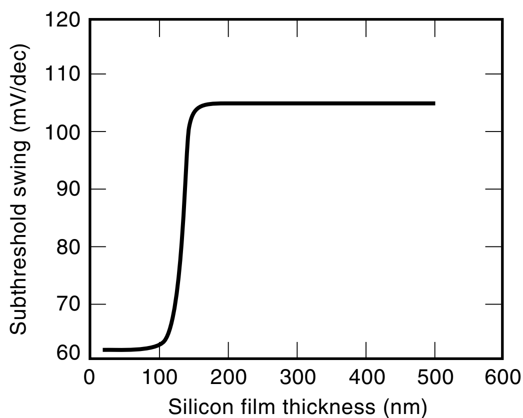

Figure 10. Subthreshold swing (proportional to the inverse of the subthreshold slope) of SOI MOSFETs showing the transition between partial and full depletion of the silicon layer; the Si film thickness for which this transition is obtained decreases with increasing the Si doping.

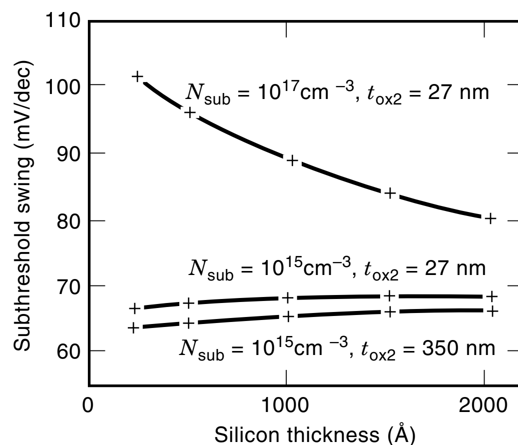

Figure 12. Simulation of the subthreshold swing as a function of the Si film thickness for various back insulator thicknesses t_{ox2} and substrate doping N_{sub} (t_{ox1} = 27 nm, 10^{15} cm^{-3} Si film doping, $N_{ss2} = 0$, $N_{ss3} = 0$).

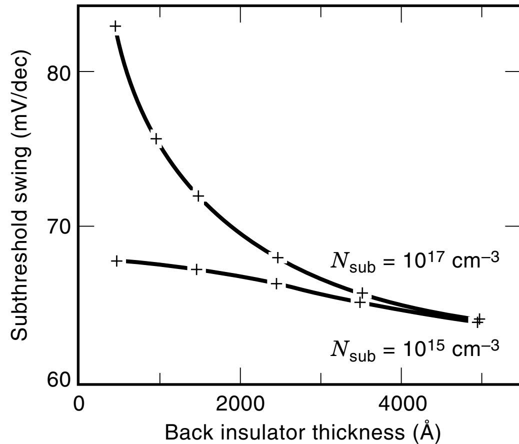

Figure 13. Simulation of the subthreshold swing as a function of the buried oxide thickness for various substrate dopings (t_{ox1} = 27 nm, 10^{15} cm^{-3} Si film doping, $N_{ss2} = N_{ss3} = 0$) showing the degradation of the swing for thin buried oxides.

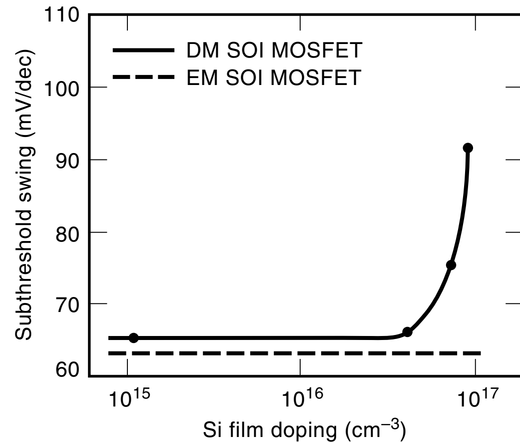

Figure 15. Simulation of the subthreshold swing for a depletion- or accumulation-mode (DM or AM) SOI MOSFET compared with an enhancement-mode (EM) device (t_{si} = 100 nm).

poor quality ($N_{ss2} > 10^{11}$ cm^{-2} eV^{-1}), the reduction of the silicon layer thickness does not lead to an improvement of the subthreshold swing [Fig. 14 (13)]. These results imply that the optimization of the device characteristics needs high-quality SOI wafers as well as a careful design of the MOSFET parameters.

The behavior of thin-film depletion (or accumulation)-mode (DM or AM) SOI MOSFETs (N^+NN^+ or P^+PP^+ types) is very different from that of enhancement-mode (EM) transistors (N^+PN^+ or P^+NP^+ structures) (15,16). Indeed, the subthreshold swings of AM devices can be larger than those of EM SOI MOS transistors due to an additional Si film charge capacitance (Fig. 15). This behavior of AM MOSFETs is attributed to the additional front channel capacitance when the back channel is in weak accumulation. Indeed, the front surface can be in strong inversion, depending on the doping and the thickness of the thin Si film, which induces a substantial degradation of the swing for AM devices (15).

The subthreshold swing and the threshold voltage of thin-film fully depleted SOI transistors also depend on the applied substrate voltage (or back gate). The swing is a minimum for a depleted back surface (upper buried oxide interface), with a back surface potential around $\Phi_F/2$ when the front surface is in weak inversion (17). The threshold voltage is significantly reduced when the substrate bias V_{g2} is positive (for N-channel devices), and it increases when V_{g2} is negative (Fig. 16). For $V_{g2} \ll 0$, the back surface is strongly accumulated, and for $V_{g2} \gg 0$ the back surface is in strong inversion. In these operation modes, the threshold voltages becomes almost independent of the back gate bias (18). If the third interface (buried oxide/Si substrate) is neglected, the threshold voltage of fully depleted enhancement-mode SOI MOSFETs (18), obtained for a potential of $2\Phi_F$ at the upper Si film interface, can be expressed as

1. Back interface accumulated (with a back surface potential $\Phi_{s2} = 0$):

$$V_{t1}^{acc} = V_{FB1} + \left(1 + \frac{C_{si} + C_{ss1}}{C_{ox1}}\right) 2\phi_F + \frac{qN_a t_{si}}{2C_{ox1}} \quad (4)$$

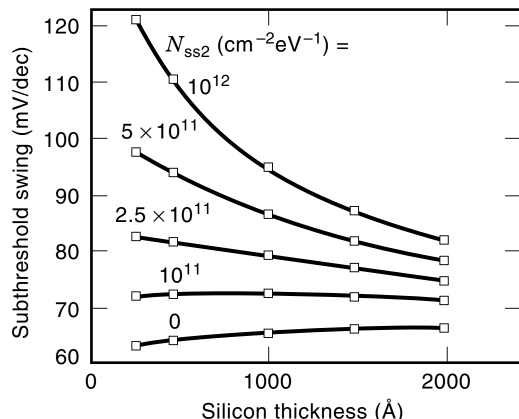

Figure 14. Simulation of the subthreshold swing as a function of the Si film thickness for various back interface state densities (t_{ox1} = 27 nm, t_{ox2} = 350 nm, 10^{15} cm^{-3} Si film doping, 10^{15} cm^{-3} substrate doping, $N_{ss3} = 0$).

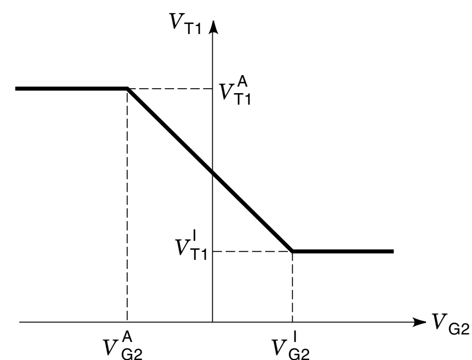

Figure 16. Variation of the front threshold voltage V_{T1} versus the back gate bias V_{G2}; V_{T1}^{A} is the maximal threshold voltage with the back Si film/buried oxide interface accumulated ($V_{G2} < V_{G2}^{A}$), and V_{T1}^{I} is the minimum threshold voltage for an inverted back surface ($V_{G2} > V_{G2}^{I}$).

2. Back interface inverted ($\Phi_{s2} = 2\Phi_F$):

$$V_{t1}^{inv} = V_{FB1} + \left(1 + \frac{C_{ss1}}{C_{ox1}}\right) 2\phi_F + \frac{qN_a t_{si}}{2C_{ox1}} \tag{5}$$

3. Back interface depleted ($0 < \Phi_{s2} < 2\Phi_F$):

$$V_{t1}^{dep} = V_{t1\,acc} - \frac{C_{s1}C_{ox2}}{C_{ox1}(C_{ox2} + C_{si} + C_{ss2})} \left(V_{g2} - V_{FB2} + \frac{C_{si}}{C_{ox2}} 2\phi_F - \frac{qN_a t_{si}}{2C_{ox2}}\right) \tag{6}$$

where V_{FB1} and V_{FB2} are the flat-band voltages of the front and back gates of the SOI structure, respectively.

Another important issue in SOI devices is the edge effects. The lateral edges of the Si islands in SOI MOSFETs represent a potential parasitic conduction between source and drain. This sidewall transistor operates in parallel with the main transistor. A hump in the subthreshold current of the transistor owing to this effect can be observed if the threshold voltage of the edges is lower than that of the main part of the device. This can lead to large leakage currents. Possible solutions to mask the parasitic transistor include (1) overdoping the sidewall causing a shift in its threshold voltage, (2) accumulating the back interface, or (3) using edgeless devices.

DRIVING CURRENT

Typical output drain-current–drain-voltage $I_d(V_d)$ characteristics are shown in Fig. 17. The curves present various operation regimes: the ohmic (or linear) operation for low V_d, the saturation for high V_d, and the beginning of the breakdown regime for the largest drain biases. The value of the driving current I_d in saturation (I_{dsat}) and the associated transconductance ($g_m = dI_{dsat}/dV_g$) are key electrical parameters for optimizing the performances of the MOSFETs.

In a fully depleted thin-film SOI MOSFET, the transverse electric field is reduced as compared with a partially depleted film (for a given surface potential). This decrease is accentuated for thinner layers, and the electric field has a quasilinear variation with the Si film thickness. Therefore, the carrier profile extends deeper in the silicon film leading to higher carrier mobility μ owing to lower surface roughness and coulomb carrier scattering associated with the Si/SiO_2 interface. This interesting feature induces a substantial increase in drain current as compared to long-channel bulk-like devices operated at the same ($V_g - V_t$) bias [$I_{dsat} \propto W/L\, C_{ox}\, \mu\, (V_g - V_t)^2$; W and L are the gate width and length, and C_{ox} is the gate oxide capacitance]. Therefore, this is also an advantage for low-voltage applications. However, carrier velocity saturation driven by a high longitudinal electric field (the velocity maximum being v_{sat}) limits the current enhancement when the devices are scaled down in the deep submicron range [$I_{dsat} \propto WC_{ox}v_{sat}\,(V_g - V_t)$]. The simulations presented in Fig. 18, fully supported by device measurements, show that the benefit of drain current, relative to bulk Si or PD SOI, is partially lost as the channel length is reduced and carrier velocity saturation occurs (19). However, in an extremely thin Si layer (<10 nm), a substantial increase of the driving current with scaling down the devices has been pointed out in the deep submicron range. This effect is due to carrier velocity overshoot occurring in sub-0.1 μm ultrathin SOI devices (20).

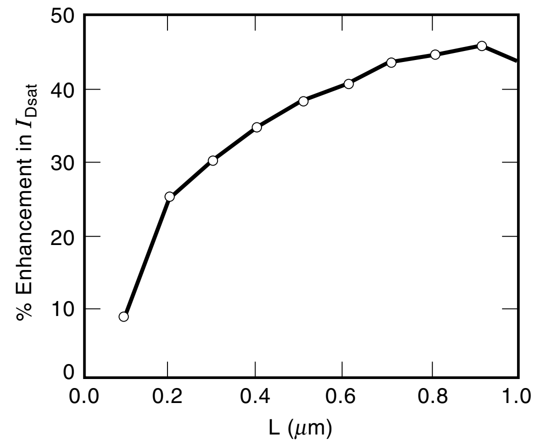

Figure 18. Simulated relative (to bulk counterparts) enhancements of drain current in saturation versus channel length of fully depleted n-channel SOI MOSFETs at V_d = 3.3 V and $V_g - V_t$ = 1.7 V. (© 1992 IEEE)

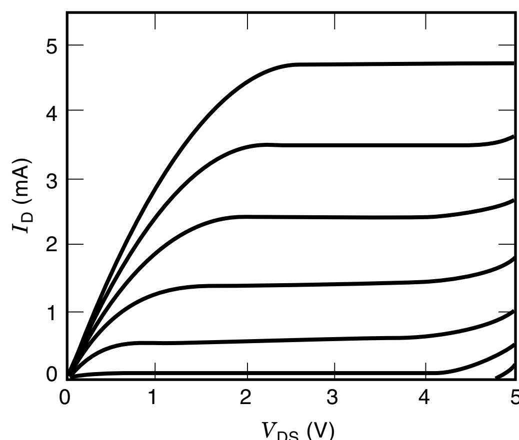

Figure 17. Typical drain-current–drain-voltage output characteristics of a MOSFET.

KINK EFFECT

The buried insulator of the SOI structure leads to floating body effects. Indeed, contrary to the case of bulk silicon device, there is usually no substrate (or body) contact to determine the potential of the active Si layer and to collect free carriers induced by various mechanisms (for instance, carriers created by impact ionization). When a body contact is available, the efficiency of this contact depends on the thickness of the Si film and on device architecture, owing to possible series resistance effect and/or potential barrier between the active silicon layer and the body contact.

The kink effect is one of the main floating body effects that are triggered by the impact ionization charging of the film body. It is observed in partially depleted SOI MOSFET, and it leads to excess drain current in saturation. The impact ionization in the high lateral electric field region close to the

drain induces electron–hole pairs creation, with the electrons flowing toward the drain and the hole forming the substrate current for a *N*-channel device. A reduction of the threshold voltage is obtained via the substrate current, which leads to a forward bias of the source/Si layer diode and a body potential increase (Fig. 19) (21). This phenomenon is also observed at low temperature in bulk silicon devices owing to impurity freeze-out in the Si substrate (22). It has been shown that this parasitic behavior can be suppressed by using fully depleted devices (23).

The excess drain current ΔI_d and the shift of the threshold voltage ΔV_t (24) are given by

$$\Delta I_d = g_b V_b \quad (7)$$

where

$$g_b = \frac{C_d}{C_{ox}} g_m \quad (8)$$

$$\Delta V_t = -\frac{C_d}{C_{ox}} V_b \quad (9)$$

where g_b ($= dI_d/dV_b$) is the body transconductance, V_b is the internal body potential induced by impact ionization, C_d and C_{ox} are the depletion and gate oxide capacitances, respectively, and g_m ($= dI_d/dV_g$) is the gate transconductance.

For a fully depleted SOI MOSFET, the depletion capacitance C_d vanishes, which suppresses the shift of the threshold voltage, the excess drain current, and, thereby, the kink effect.

Thin-film SOI transistors are subject to another harmful effect: the parasitic bipolar transistor. This last effect is enhanced with a reduction of the silicon film thickness (higher lateral electric field), especially for inversion-mode MOSFETs. An interesting tradeoff could be the use of an intermediate Si layer thickness in order to suppress the kink effect and to alleviate the parasitic bipolar transistor action. Thin but undepleted SOI films were also proposed as an optimum substrate for low-voltage CMOS (25). However, it has been recently shown that a moderate kink effect can still be obtained for fully depleted SOI MOSFETs with intermediate Si film thickness [Fig. 20(a) (26)]. This effect can be modulated by connecting the body terminal [Fig. 20(a)], if available. This kink is due to the substantial barrier height of the source/thin film diode in moderately fully depleted transistors.

Figures 20(b) and 20(c) illustrate the transfer $I_d(V_g)$ characteristics for various applied body biases V_B. It is clear that the variation of the threshold voltage V_t from $V_B = 0$ to $V_B = -1$ V, for a zero substrate voltage [(Fig. 20(b)], is very small because the silicon film is already fully depleted for $V_B = 0$, and therefore the depletion region cannot be extended any deeper. On the other hand, with a small positive bias applied to the body terminal (up to 0.5 V) a significant shift of V_t is obtained. In this case, the potential barrier between the source and the thin Si film can be reduced, due to the additional forward bias, because of its large initial value for this moderate full depletion. When a small positive substrate bias is applied (10 V), the strong full depletion case is reached with a small potential barrier at the source/silicon film junction, which almost suppresses the variation of the threshold voltage for body voltages up to 0.5 V. Finally, for a negative substrate bias, a large shift of V_t can be obtained for negative values of body voltages [Fig. 20(c)]. This case corresponds to partially depleted SOI MOSFETs.

In moderately fully depleted devices, the depletion charge can be modulated for sufficiently large V_d, because of the possible change of the potential barrier at the source/substrate junction. The additional forward bias associated with the impact ionization current induces a reduction of the potential barrier and depletion charge; as C_d becomes different from zero [see Eqs. (7)–(9)], it gives rise to a small kink effect (which is in fact proportional to the reduced variation of the internal potential V_b close to the back interface). This reduced V_t shift has to be taken into account in order to obtain an accurate modeling of moderately fully depleted MOSFETs (26). These device types also show subthreshold kinks in the transfer Id(Vg) characteristics (27).

This means that these SOI MOSFETs are fully depleted for low drain biases, but for large drain biases the devices become partially depleted, due to a reduction of the depletion charge. The physical difference between various devices is associated with the potential barrier at the source/substrate junction for small drain biases. The barrier is maximum for partial depletion, minimum for strong full depletion, and between these two extreme cases for a moderate full depletion which gives rise to a moderate kink. This kink effect can in fact be modulated by the degree of depletion of the Si film.

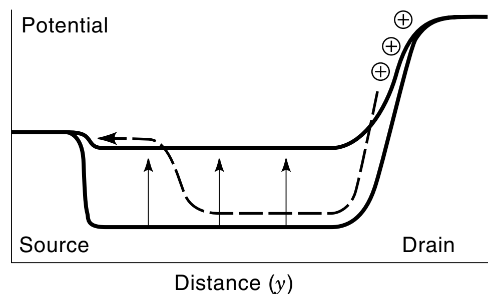

Figure 19. Band diagram between source and drain before (large barrier height at the source/Si film junction) and after (small barrier height) the kink effect triggered by the impact ionization charging of the film body; the hole transport between drain and source is also shown.

LATCH AND BREAKDOWN PHENOMENA

Another floating body effect is the parasitic bipolar transistor (PBT) action which can be observed for SOI MOSFETs in a certain voltage range. This PBT induces latch and premature breakdown as compared to bulk Si devices (Fig. 21) (28). As the kink effect, this parasitic phenomenon is triggered by the impact ionization current which leads to an internal forward bias of the (floating) base/emitter (thin Si film/source) junction of the PBT. A large collector (drain) current is thus created, giving a substantial enhancement of the drain current. This PBT action portends power-consumption problems in SOI CMOS, hysteresis in the subthreshold characteristics, and eventually the loss of gate control.

Breakdown and latch phenomena have been reported for both *N*- and *P*-channel enhancement- and depletion-mode de-

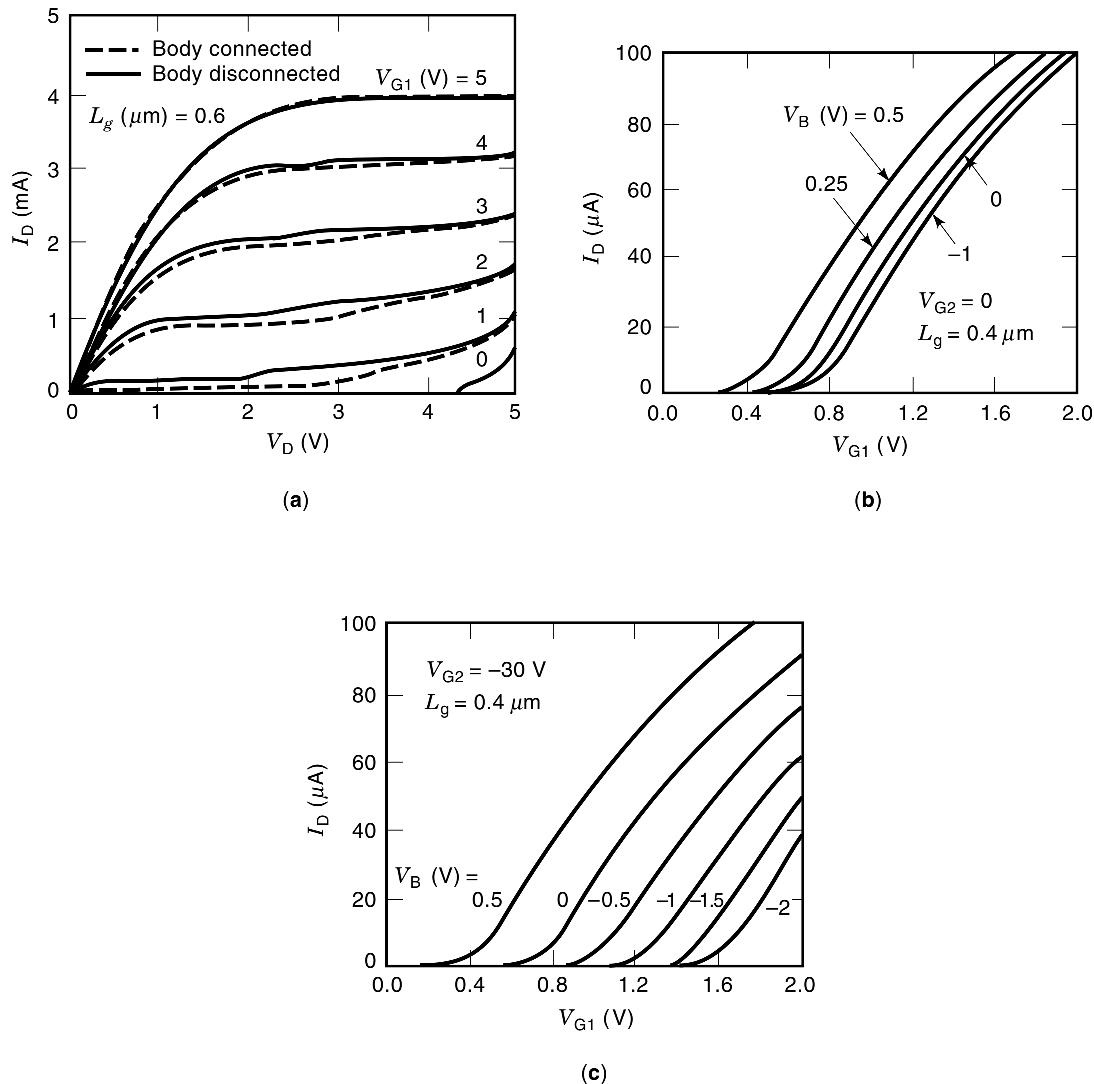

Figure 20. (a) Output $I_d(V_d)$ characteristics of n-channel thin-film SIMOX MOSFET showing influence of body connection. (b, c) Transfer $I_d(V_g)$ characteristics showing influence of body bias V_B for various substrate voltages V_{g2}.

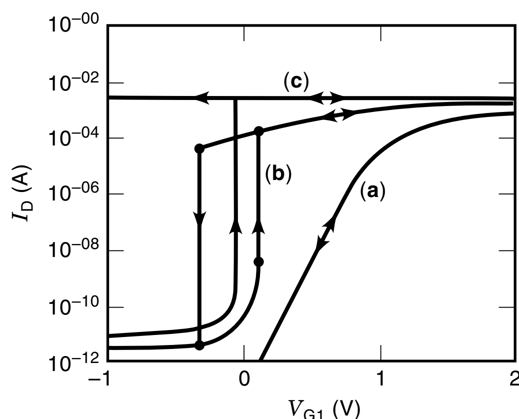

Figure 21. Drain-current–gate-voltage characteristics showing the latch effect owing to the parasitic bipolar action. (a) Small drain bias, (b) medium drain bias with hysteresis, and (c) high drain bias with a reverse-V_g-scan latch.

vices (29–32). For P-channel transistors, these effects are attenuated by the lower impact ionization rate of holes.

The breakdown voltage V_{bd} is evaluated for gate voltages near threshold (where V_{bd} is the lowest). The measured V_{bd} as a function of channel length and Si film thickness is shown in Fig. 22 for an enhancement mode (N^+PN^+ structure) SOI MOSFET. In long channels, V_{bd} is reduced for thinner films due to the increase of the lateral electric field (33). V_{bd} is further degraded with decreasing channel length (higher lateral electric field and bipolar transistor gain). However, for channel lengths below 0.5 μm, short-channel effects lead to an increase of V_{bd} in thinner Si films.

By contrast to the case of enhancement-mode devices, the breakdown voltage of depletion (or accumulation)-mode SOI MOSFETs (N^+NN^+) is remarkably improved by thinning the silicon layer [even for long channel transistors, L = 1 μm, Fig. 23 (34)].

The latch and breakdown phenomena can also be improved by optimization of the device structure. For instance, lightly doped drain and source regions are useful in order to reduce

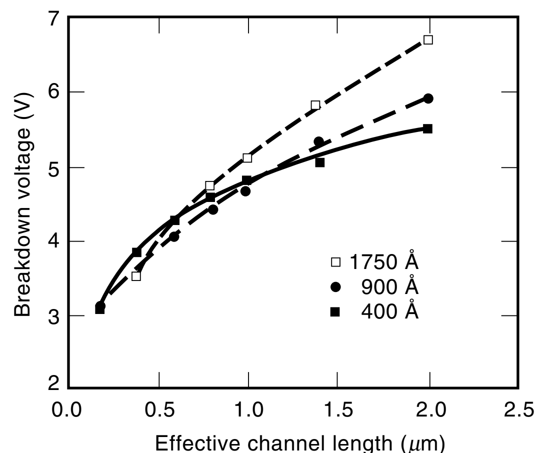

Figure 22. Measured breakdown voltage due to the parasitic bipolar transistor action versus effective channel length for an enhancement-mode SOI MOSFET. (© 1992 IEEE)

the impact ionization near the drain (lower lateral electric field) and the gain of the PBT by maximizing the recombination in the source (emitter) region (30). Another possibility is to fabricate a dual source SOI MOSFET (35), where the source region is an n^+ over p^+ structure (for N-channel), both regions being contacted by the same spiked aluminum electrode. In this transistor, the buried p^+ region collects the holes created by impact ionization near the drain, thus eliminating the PBT. In fact, this structure acts as a body contact without increasing device area. Other possibilities are the silicidation of the source region in order to decrease the gain of the PBT (36), bandgap engineering using a SiGe source (37), localized lifetime killing (away from the source and drain regions) (38), and reduction of the supply voltage if allowed by system constraints.

SELF-HEATING EFFECTS

SOI MOSFETs suffer from self-heating effects conveyed by the low thermal conductivity of the buried oxide. At high power dissipation levels, one observes the onset of negative output conductance in the saturation region (39). This behavior is mainly attributed to the reduction of the mobility with increasing channel temperature by self-heating. However, other device parameters (threshold voltage, saturation velocity, etc.), have to be taken into account for accurate modeling. Self-heating also leads to an increase of the interconnect temperature, which is critical for electromigration considerations. The excess temperature in the Si film can be expressed as

$$\Delta T = R_{\text{th}} I_{\text{d}} V_{\text{d}} \tag{10}$$

where R_{th} is the thermal resistance and $I_{\text{d}}V_{\text{d}}$ is the device power.

Figure 24 shows the measured channel temperature versus device power for varying film thickness (40). The temperature rise is proportional to the power, and it is much larger in an SOI device than in a bulk Si transistor. As the silicon layer is thinner, the channel temperature substantially increases. The channel temperature is also raised by increasing the buried oxide thickness and the channel–metal contact distance (40). The reduction of this important parasitic effect in SOI technology may require that the device structure as well as the film and buried oxide thicknesses be optimized. Fortunately, reduced self-heating effects are obtained under dynamic operation.

TRANSIENT EFFECTS

The isolation of the floating body is also responsible for the occurrence of parasitic current transients. If no body contact is available, there is no substrate current to promptly adjust the majority carrier density. This behavior can lead to a drain current overshoot in partially depleted SOI MOSFETs when the gate is switched from accumulation to inversion. In good-quality, high-lifetime SOI, the adjustment of the carrier density requires a long transient period which may affect the switching performance of integrated circuits before a steady-state regime is achieved. During the transient, the current at the turn-on stage may exceed twice the steady-state value. Time-domain simulations have shown that the holes (for a N-channel device), expelled from the surface when the depletion region forms, have no way to escape and temporarily keep up

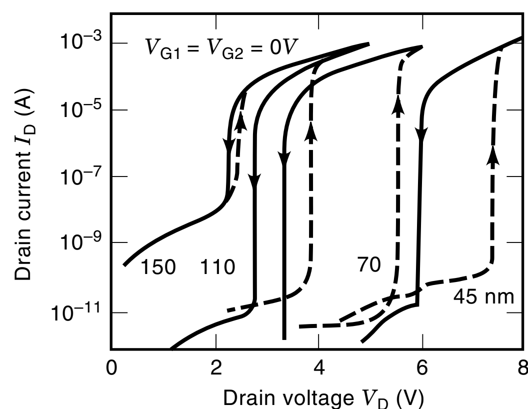

Figure 23. Improvement of off-state $I_d(V_d)$ characteristics when we reduce the Si film thickness in accumulation-mode SIMOX transistors (L = 1 μm).

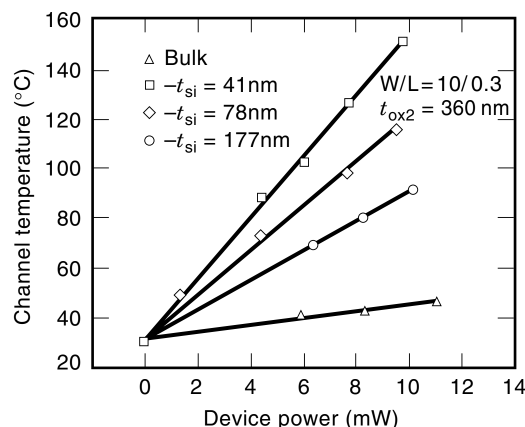

Figure 24. Enhancement of channel temperature with increasing device power for SOI devices with varying Si film thickness. (© 1992 IEEE)

the body potential. Since the inversion charge and drain current respond very rapidly to any potential variation, the overshoot transient reflects the time needed for excess holes to recombine within the body or in the source region. At turn-off, the potential recovery is a function of the thermal carrier generation. If the off-time period is too short for equilibrium to be recovered, the overshoot induced by the following pulse is attenuated. Both the transient current and decay-time are reduced when the drain is biased in the saturation region, since the forward biasing of the body-to-source junction makes the collection of excess holes easier.

As a general rule, it can be inferred that the transient magnitude is proportional to the difference between the final and initial body charges, and the time constant depends on the hole generation or recombination process. Drain current undershoot, memory effect, and dynamic instabilities have also been observed in partially depleted devices.

These parasitic effects are suppressed in fully depleted SOI MOSFETs where the source potential barrier is lower and the threshold voltage is not sensitive to a small amount of excess holes (41–43).

SHORT-CHANNEL EFFECTS

Short-channel effects can become severe in the deep submicron range. In this respect, two phenomena have to be optimized in order to obtain a reliable device and circuit operation. The charge-sharing effect is due to the increased influence of the depletion region at the source and drain junctions with scaling down the MOSFETs. This leads to a reduction of the depletion charge controlled by the gate and thereby a decrease of the threshold voltage of the transistor which can induce substantial leakage currents. The drain-induced barrier lowering (DIBL) is due to the electrostatic influence of the drain potential on the source/Si film barrier height at high V_d. This phenomenon has been shown to jeopardize deep submicron device operation with, in particular, a significant drain leakage current.

SOI structures offer unique options for the reduction of short-channel effects. However, a careful adjustment of the SOI parameters is necessary to improve the performance of deep submicron devices. Figure 25 presents the simulated variations of the threshold voltage in SOI MOSFETs due to charge-sharing effects (44). The roll-off of the threshold voltage between long (1 μm) and ultrashort (0.1 μm) channel devices is a strong function of film thickness and doping. The worst-case condition (i.e., peak in the characteristics) is obtained for an intermediate silicon layer thickness, which roughly corresponds to the transition between full and partial depletion. In this region, short-channel effects are aggravated for fully depleted devices as compared to partially depleted SOI and bulk Si transistors. The silicon layer thickness must be far from the transition between partial and full depletion and substantially smaller than the junction depth of a comparable bulk MOSFET in order to improve short-channel effects in fully depleted SOI devices. A similar condition is obtained for attenuating the DIBL effect in deep submicron SOI MOSFETs (44).

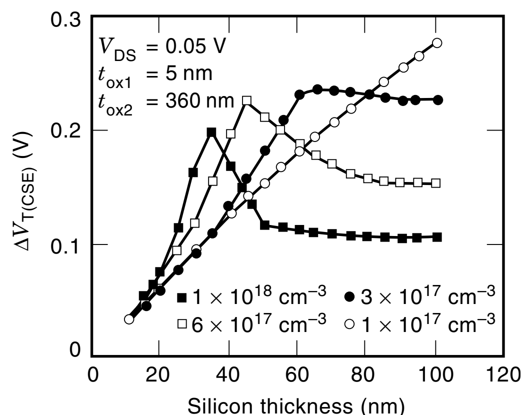

Figure 25. Charge-sharing effect versus silicon layer thickness for various dopings. $\Delta V_t(\text{CSE}) = V_t(L_{eff} = 1\ \mu m) - V_t(L_{eff} = 0.1\ \mu m)$. (© 1993 IEEE)

The buried oxide thickness is another important parameter for alleviating short-channel effects. A significant attenuation of the threshold voltage shift is observed for ultrashort SOI devices when we reduce the buried oxide thickness below 100 nm (45).

HOT-CARRIER EFFECTS

Hot-carrier effects (HCE) are created by the large lateral electric field observed at high V_d close to the drain/Si film junction inducing high-energy carriers in the conduction channel. These electrons or holes give the substrate current by impact ionization and the gate current for carriers which can overcome the Si/SiO_2 energy barrier, as well as photon emission. The high-energy carriers can also be injected in the gate oxide, thereby creating interface or oxide defects (positive or negative fixed charges and interface states). This gate oxide degradation usually leads to a reduction in the transconductance and drain current of the MOSFETs as well as a shift in the threshold voltage which is very harmful for long-term device reliability.

Therefore, HCE in SOI devices are investigated by monitoring the substrate current, gate current or photon emission spectra, as well as hot-carrier-induced device degradation. The measurements of the substrate current with a body contact (not always available) can lead to underestimated hot-carrier effects due to a poor efficiency for collecting the majority carriers. The efficiency of the body contact depends on the SOI structure and is reduced with decreasing the silicon film thickness (46). The gate current or the number of emitted photons can be used for a reliable analysis of hot carrier effects in thin film fully depleted SOI MOSFETs. A substantial reduction of the normalized gate current is found for decreasing the Si film thickness. 2-D simulations (including the energy balance equation) show that the inversion layer thickness increases with reducing the film thickness in fully depleted SOI transistors, which results in a decrease in the maximum electron temperature [Fig. 26(a)] (47). The study of the aging processes of SOI MOSFETs is rather complex due to the multi-interface SOI structure. Distinct aging signatures have been found for (1) fully and partially depleted MOSFETs and (2) thick (i.e., bulk-like), thin and ultrathin film transistors. Interface coupling allows the back interface defects to be responsible for an "apparent" degradation of the front channel properties. Because the buried oxide is more

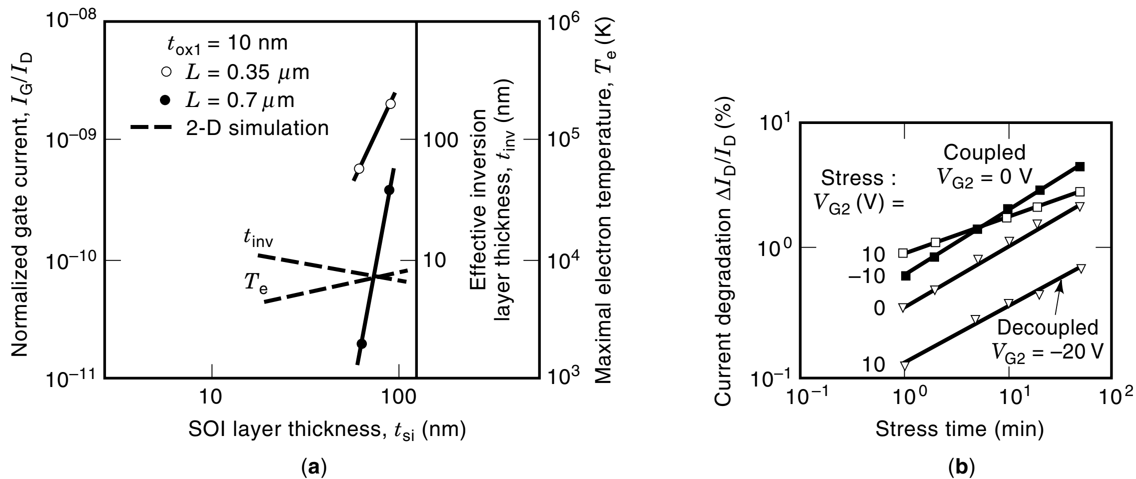

Figure 26. (a) Variation of the experimental normalized gate current as a function of Si layer thickness compared with simulated inversion layer thickness and maximum electron temperature. (© 1995 IEEE) (b) Influence of the back-gate (or substrate) bias during the stress (V_{g2} = −10 V, 0, 10 V) and the test (V_{g2} = 0, −20 V) of a fully depleted thin-film SOI MOSFET (t_{si} = 100 nm, L_{eff} = 0.7 μm, stress: $V_g - V_t$ = 0.15 V and V_d = 3.8 V, test: $V_g - V_t$ = 1 V and V_d = 0.05 V for various back-gate biases).

subject to degradation than the gate oxide (especially for SIMOX devices), its defects may jeopardize, via coupling effects, the performance of SOI/CMOS circuits. For simplicity of analysis, the stressing and testing conditions should be carefully checked in order to avoid misleading conclusions due to interface coupling. The assessment must be aimed to a segregation of the defects generated at each interface. For instance, Fig. 26(b) shows the role of the back gate during front-channel stress for an n-channel fully depleted thin film SOI MOSFET (3,48). When the aging is evaluated with a zero substrate bias, different slopes are obtained. However, when the aging is assessed with the back interface accumulated, similar degradation slopes are found. These results show that the amount of degradation is lower in the case of an inversion at the back interface. Therefore, the choice of V_{g2} is quite relevant during the stress and for the evaluation of the damage location.

Photon emission measurements have shown that a number of hot carriers are also created in the parasitic bipolar regime for small gate biases ($0 \leq V_g \leq V_t$) and high V_d (49). Substantial degradation has been pointed out in this gate voltage range.

It should be mentioned that the buried oxide degradation in wafer bonding or UNIBOND material could be substantially lower than that observed in SIMOX devices owing to the different buried oxide formation mechanisms.

VOLUME INVERSION

The inversion channel induced by the gate of a MOSFET is located at the Si/SiO_2 interface with a typical length of a few nanometers. The double-gate control of an SOI MOSFET allows forcing the whole silicon film (interface layers and volume) in strong inversion and gives rise to the “volume inversion (VI)” concept (Fig. 27) (50). The fact that the current drive of the VI-MOSFET is governed by two gates and that carriers are no longer confined at one interface presents remarkable advantages: enhancement of the number of minority carriers, increase in carrier mobility and velocity due to reduced influence of scattering associated with oxide charges and surface roughness, increase in drain current and transconductance, and ideal subthreshold slope (50,51). The subthreshold slope S_{vi} and threshold voltage V_t of the VI-MOSFET are calculated using a constant potential in the whole silicon layer (12,52) which is a very good approximation for $V_g \leq V_t$.

$$S_{vi} = \frac{kT}{q}\ln(10)\left(\frac{C_{ox} + C_{ss}}{C_{ox}}\right) \tag{11}$$

$$V_t = V_{fb} + 2\phi_F + \frac{qt_{si}N_a}{C_{ox}} - \frac{Q_{ss}(2\phi_F)}{C_{ox}} \tag{12}$$

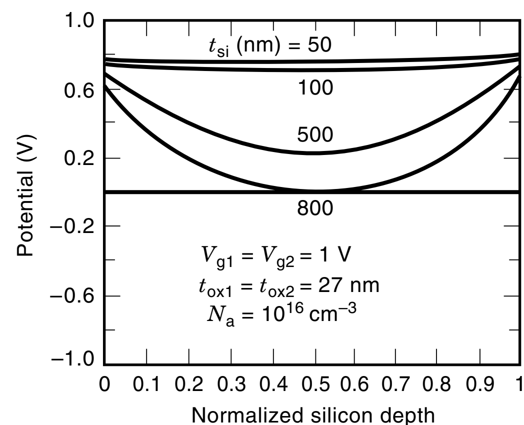

Figure 27. Potential profile inside the silicon layer showing the volume inversion regime for thin-film (≤100 nm) double-gate SOI MOSFETs; the occurrence of a volume inversion (with a quasi-constant potential larger than $2\phi_F$ in the whole Si layer) depends on the Si film thickness and doping.

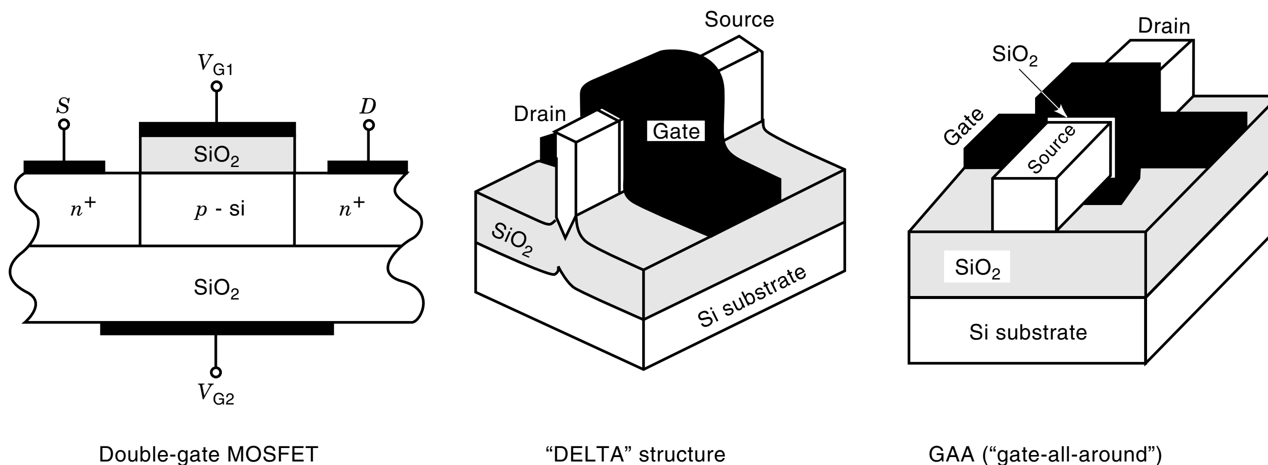

Figure 28. Various SOI structures using the concept of volume inversion.

where C_{ss} $(= qN_{ss})$ is the interface state capacitance, C_{ox} is the gate oxide capacitance (similar interface state densities N_{ss} and oxide thickness are assumed at the upper and lower Si film interface), V_{fb} is the flat-band voltage for both front and back gate, N_a is the silicon layer doping, Φ_F is the Fermi potential, and $Q_{ss}(2\Phi_F)$ is the interface state charge for a surface potential of $2\Phi_F$.

It is worthwhile noting that, in the threshold expression, the inversion charge Q_i is usually neglected with regard to the depletion charge Q_d. However, this is not possible in the case of volume inversion as, at threshold, $Q_i = Q_d$.

A dramatic reduction of hot carrier effects (substrate current, photon emission, and hot-carrier-induced degradation) has also been reported in SOI MOSFETs with volume inversion operation (46,53,54). Various SOI structures [double-gate (55), DELTA (56), GAA (gate-all-around) (57)] have been proposed in order to take advantage of this original feature (Fig. 28). Figure 29 shows an example of the performance improvement during volume inversion operation as compared to a conventional single-gate SOI operation (57): The GAA device exhibits a transconductance up to three times larger. The VI-MOSFET seems to be an ideal device for alleviating short-channel effects in ultimate ultra-short-channel MOS transistors (58). For instance, a substantial reduction of the DIBL phenomenon in volume inversion operation has been observed (59).

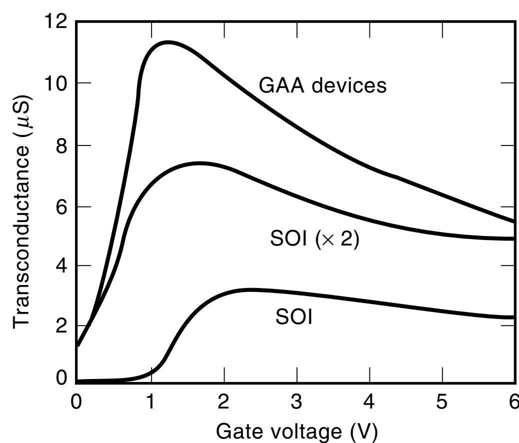

Figure 29. Transconductance in a conventional SOI MOSFET, a double-gate transistor without volume inversion, and a GAA device with volume inversion (W/L = 3 μm/3 μm, V_d = 100 mV). (© 1990 IEEE)

NOISE

Flicker noise in microelectronics devices, observed at low frequency with a variation inversely proportional to the frequency ($1/f$), is very harmful for analog applications. It is attributed to carrier mobility or carrier number fluctuations. When the drain current noise is proportional to the transconductance squared or inversely proportional to the drain current, it is concluded that the carrier number fluctuation model (60–62) or the Hooge mobility fluctuation model (63), respectively, is valid. In MOS transistors, the main fluctuations are due to dynamic exchange of channel carriers with interface or oxide traps (carrier number fluctuations). The normalized drain current spectral density in the carrier number fluctuation model is given by

$$\frac{SI_d}{I_d^2} = \frac{g_m^2}{I_d^2} S_{Vg} \tag{13}$$

where g_m $(= dI_d/dV_g)$ is the gate transconductance and S_{Vg} is the equivalent input gate voltage spectral density.

In SOI MOSFETs, supplementary fluctuations are obtained owing to floating body effects. For a thin-film fully depleted transistor, a conventional drain current noise (bulk-like) is obtained as a function of V_d (Fig. 30). However, when a negative bias is applied to the substrate (back gate), the device becomes partially depleted (accumulation of the back interface) and a kink effect is obtained, leading to an excess noise around the kink (Fig. 30 with $V_{g2} = -10$ V) (64,65). This excess noise can be attributed to the dynamic trapping of carriers created by impact ionization in the Si layer or at the interfaces of the SOI structure.

Another floating body effect, the parasitic bipolar transistor action which can be observed in both partially and fully depleted SOI MOS transistors, also leads to an original low-frequency noise behavior. The noise measurements are shown

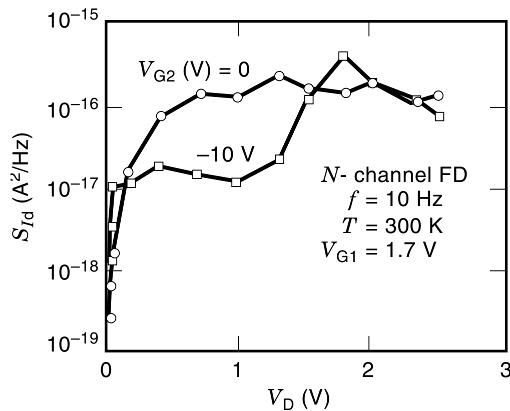

Figure 30. Experimental drain current noise as a function of drain voltage, for various back gate biases (N-channel thin film (80 nm) enhancement-mode SOI MOSFET); a kink effect and an excess noise is obtained when the device is partially depleted ($V_{g2} = -10$ V).

in Fig. 31. For small drain current, below the threshold of the parasitic bipolar transistor, similar noise magnitudes are obtained for the various V_d values. However, for large I_d, the PBT regime is reached for a sufficiently high drain bias ($V_d \geq$ 3.3 V), leading to a significant increase of the noise. Similar results for the drain current noise are obtained in the case of forward (V_d = 3.35V)- and reverse (V_d = 3.3 V) − V_g-scan latch (66).

This excess noise is attributed to supplementary fluctuations associated with the impact ionization (generation) and carrier capture in the SOI layer (recombination). Note also that the impact-ionization current leads to a biasing of the base of the parasitic bipolar transistor, and further fluctuations can be caused by the PBT carrier transport between emitter (source) and collector (drain).

On the other hand, an interesting behavior in the low-frequency noise has been observed in volume inversion. In this case, an important part of the carrier transport is carried out in the Si volume far from the interfaces, inducing a reduction of the dynamic exchange of carriers with the oxide traps and a screening of the oxide charge fluctuations, thus enabling a significant reduction of the noise of the MOS transistors (65).

QUANTUM EFFECTS

We have already noted how promising ultrathin Si films are for reducing short-channel and hot-carrier effects and for improving high-speed performance and parasitic phenomena. It is worth mentioning that 2 nm thick silicon film has recently been realized (67). However, quantum mechanical effects (energy quantization) can appear in ultrathin layers due to the transition from a 3-D to a 2-D electron system. Figure 32 presents the impact of this transition on the variation of the threshold voltage V_t (68). The calculated classical behavior consists of a reduction of V_t with decreasing film thickness (in fully depleted MOSFETs) as a consequence of the reduction of the depletion charge. The quantum mechanical calculation leads to an increase of V_t for Si film thickness below 10 nm. This is explained by the formation of a 2-D-subband system, with a ground state located above the bottom of the conduction band E_c. In SOI MOSFETs, the difference between the ground-state energy level and E_c becomes larger as the layer thickness decreases, which induces such an increase of V_t in ultrathin films. Quantum mechanical influences have also been shown to enhance short-channel effects in extremely thin SOI layers (<10 nm), especially at low temperature (69). The quantum effects have to be taken into consideration for the design of advanced SOI devices. On the other hand, SOI devices can also be fabricated with very small surfaces and volumes leading to ultrasmall capacitances. For these structures, the charge quantization regime can be reached, and conductance oscillations due to Coulomb blockade effect have been observed even at room temperature (70).

INFLUENCE OF TEMPERATURE

The low- or high-temperature properties of SOI transistors are rather different from those of bulk devices as a consequence of the specific mechanisms existing in SOI structures. The variation of the threshold voltage as a function of temperature is illustrated in Fig. 33 (71). Two slopes can be clearly seen in this characteristic. The device is partially depleted in the high temperature range and becomes fully depleted in the low temperature range. The reduction of the $V_t(T)$ slope at low temperature occurs when the full depletion of the silicon

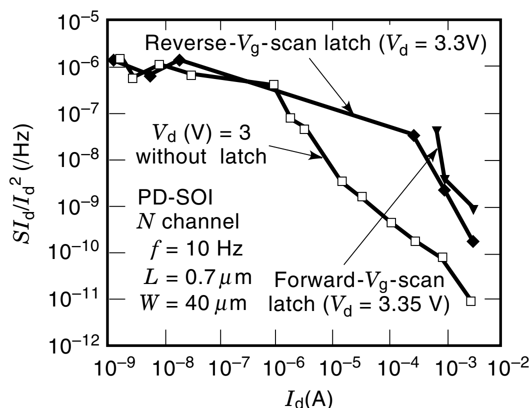

Figure 31. Normalized drain current noise versus drain current for N-channel partially depleted SOI MOSFET (t_{si} = 100 nm, t_{ox1} = 4.5 nm, t_{ox2} = 80 nm); an excess noise is observed in the presence of both forward- and reverse-V_g-scan latch.

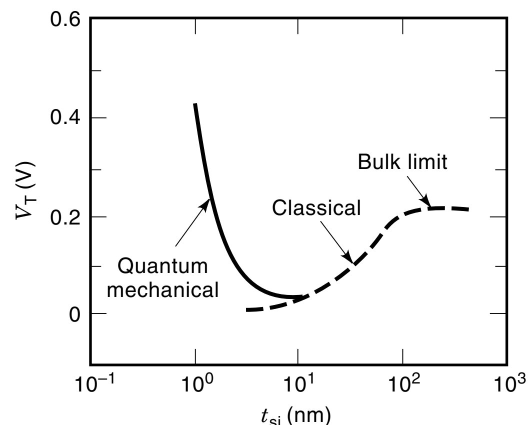

Figure 32. Theoretical threshold voltage variation versus Si layer thickness showing the occurrence of quantum effects for ultrathin Si film (t_{ox1} = 7 nm, t_{ox2} = 80 nm, Na = 10^{17} cm^{-3}, N_{sub} = 10^{17} cm^{-3}, T = 300 K). (© 1993 IEEE)

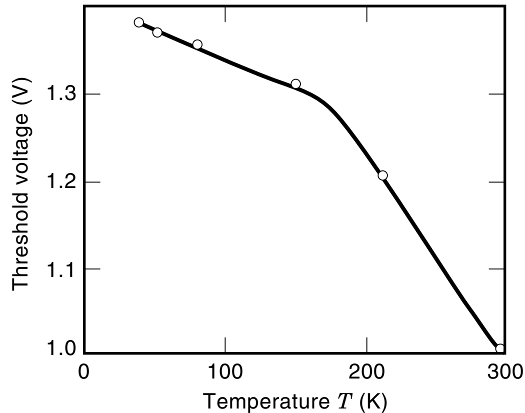

Figure 33. Threshold voltage against temperature for a partially depleted (at 300 K) SIMOX MOSFET becoming fully depleted at low temperature ($L = 2\ \mu$m, $V_d = 30$ mV).

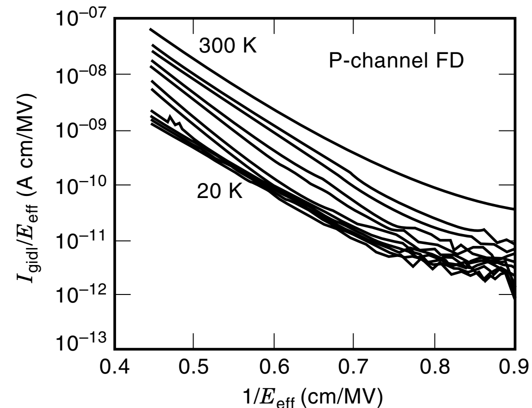

Figure 35. Variations of the GIDL current characteristics as a function of inverse of transverse electric field for various temperatures (from the top to the bottom: 300, 250, 230, 200, 180, 160, 140, 120, 100, 80, 50, 20 K) for a p-channel fully depleted ($t_{si} = 80$ nm) LDD SIMOX MOSFET.

film prevents the further extension of the depletion region under the gate by decreasing the temperature (71,72). The variation of the threshold voltage with temperature can be expressed as

$$\frac{dV_t}{dT} = \frac{d\phi_F}{dT}\left[\alpha\left(\frac{q\epsilon_{si}N_a}{\phi_F C_{ox}^2}\right)^{1/2} + 2 + \frac{qN_{ss}}{C_{ox}}\right] \quad (14)$$

where $\alpha = 1$ for a partially depleted film and $\alpha = 0$ for a fully depleted film, Φ_F is the Fermi potential, N_a is the Si film doping, C_{ox} is the gate oxide capacitance and N_{ss} is the interface state density.

Therefore, a substantial reduction of the variation of V_t versus temperature can be achieved in fully depleted SOI MOSFET because of the suppression of the variation of the depletion charge with temperature. This behavior is very attractive for device operation in a large temperature range.

The latch and breakdown phenomena associated with the parasitic bipolar transistor (PBT) action are temperature-dependent. Figure 34 presents a typical off-state ($V_g = 0$) breakdown for a thin-film (80 nm) LDD SOI n-MOSFET as a function of temperature (32). At 300 K, a conventional breakdown is observed at low drain bias (<4 V), unlike at liquid nitrogen temperature where breakdown is avoided for V_d below 6 V. Similar improvements are obtained for the latch phenomenon in the $I_d(V_g)$ characteristics. These considerable advantages at low temperature are attributed to various mechanisms. First, the PBT gain β decreases quasi-exponentially by reducing the temperature ($\beta \propto \exp(-\Delta E_g/kT)$), due the difference in bandgap ΔE_g between emitter (source) and base (thin Si film). In addition, the lightly doped regions at the source and drain freeze-out at low temperature. Since the lightly doped drain is useful to reduce the impact ionization by lowering the lateral field, the freeze-out of the LDD region induces a further decrease of the ionization. The benefit of the lightly doped source is to reduce the PBT gain by maximizing the carrier recombination in the source (emitter) region; the freeze-out of this region produces a further decrease in gain.

These low-temperature mechanisms are responsible for the reduction of the gate-induced drain leakage (GIDL) current in thin film SOI MOSFETs. The variations of the normalized GIDL characteristics with temperature are shown in Fig. 35 (I_{gidl}/E_{eff} = A $\exp(-B/E_{eff})$, E_{eff} is the effective surface electric field and where A and B are constant parameters) for a p-channel thin-film (80 nm) SIMOX MOSFET as a function of

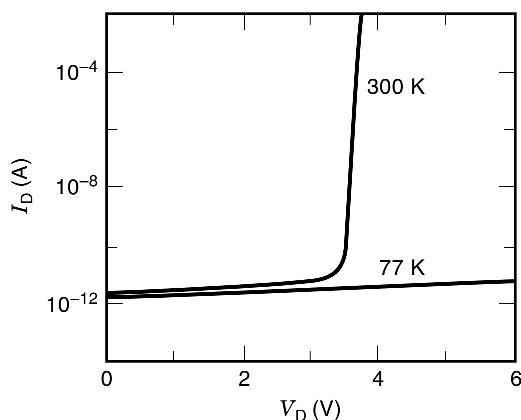

Figure 34. Off-state breakdown ($V_g = 0$) at 300 and 77 K for an n-channel thin-film depletion-mode SIMOX MOSFET ($t_{si} = 80$ nm, $W = 40\ \mu$m, $L_g = 0.8\ \mu$m).

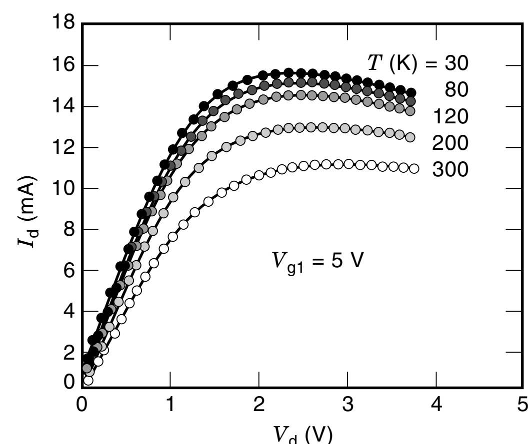

Figure 36. Typical variations of $I_d(V_d)$ characteristics for a SIMOX MOSFET showing increased self-heating effects at low temperature.

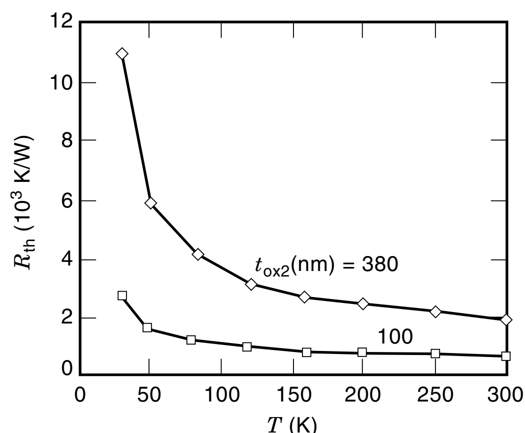

Figure 37. Simulated variations of the thermal resistance versus temperature with various buried oxide thicknesses for SIMOX MOSFETs.

the inverse of the surface field (73). A strong reduction of the leakage current, much larger than in bulk Si MOSFETs (74), is obtained at low temperature. This considerable improvement is attributed to the reduction of the PBT gain and to impurity freeze-out in the LDDs. Indeed, it has been shown that the GIDL current is enhanced in short-channel SOI MOSFETs due to the influence of PBT (75). The GIDL current is known to originate from a high electric field in the gate/drain overlap region which causes electron tunneling from valence band to conduction band. Note that the increase in the bandgap due to energy quantization leads to a reduction in this band-to-band tunneling current in ultrathin SOI films ($<$5 nm) (76). In an SOI n-MOSFET the GIDL current is in fact the base current of the PBT; and the collector current is enhanced by the PBT gain, which is exponentially dependent on temperature. This feature causes the GIDL current to substantially decrease at low temperature. Similar effects have been shown for both n- and p-channel transistors. It should also be mentioned that these improvements are obtained together with a strong increase of the drain current in saturation for thin-film SOI MOSFETs.

Finally, it is worth noting that the self-heating effects also strongly depend on temperature (77). An increase in self-heating for SIMOX MOSFETs has been observed when decreasing the temperature (Fig. 36), and is explained by the reduction of the thermal conductivity of the buried oxide. Indeed, the thermal resistance, which presents a substantial variation with the buried oxide thickness, is significantly enhanced at low temperature (Fig. 37). However, this behavior is associated with the buried oxide quality and thereby will not be similar for other SOI materials.

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F. BALESTRA
ENSERG

SIMULATED ANNEALING. See STOCHASTIC OPTIMIZATION, STOCHASTIC APPROXIMATION AND SIMULATED ANNEALING.

SIMULATION. See CIRCUIT ANALYSIS COMPUTING; MONTE CARLO ANALYSIS.

SIMULATION, AEROSPACE. See AEROSPACE SIMULATION.

SIMULATION BY WAVEFORM RELAXATION. See CIRCUIT ANALYSIS COMPUTING BY WAVEFORM RELAXATION.

SIMULATION, CFD. See FLOW VISUALIZATION.

SIMULATION, CIRCUITS. See CIRCUIT ANALYSIS COMPUTING.

SIMULATION, MODELING. See MODELING AND SIMULATION.

SIMULATION OF NONLINEAR NETWORKS. See NONLINEAR NETWORK ELEMENTS.

SIMULATION OF SEMICONDUCTOR PACKAGES AND SYSTEMS. See CIRCUIT ANALYSIS COMPUTING OF SEMICONDUCTOR PACKAGES AND SYSTEMS.

SIMULATORS. See ANALOG COMPUTERS.