MODULATION DOPED FETS

To some extent, the modulation doped field effect transistor (MODFET) is the compound semiconductor analog of the ubiquitous MOSFET which utilizes a pseudo-two-dimensional carrier gas, the concentration of which is modulated by a gate potential. In a MODFET, a larger bandgap material with a high doping concentration (assumed to be *n*-type in this discussion) is grown on a lower bandgap intrinsic material (1). In practice, growth of a thin intrinsic layer of the high bandgap material, known as the intrinsic layer, setback layer or spacer, precedes growth of the rest of the high bandgap material. Electrons diffuse from the doped larger bandgap material to the lower bandgap material where they are confined and form a conducting sheet, a two-dimensional electron gas (2DEG). When the gate voltage is adequately high so that the source-drain channel is no longer depleted, the 2DEG is free to conduct in the intrinsic material. Because the undoped low bandgap material has no donor atoms cluttered about, impurity scattering no longer inhibits the carrier mobility and saturation velocity. The spacer mentioned above serves to increase the channel mobility further by shielding the 2DEG from ionized impurities, although at the cost of decreased sheet carrier density.

Major refinements of the MODFET following its introduction have concentrated on improving the electron concentration through increased band discontinuity, DE_C, by increasing the LnAs mole fraction in the channel. The conventional MODFET uses AlGaAs and GaAs for the high bandgap and low bandgap materials, respectively, denoted as AlGaAs/GaAs, on a GaAs buffer. Carrier and its confinement in the GaAs improves with increasing ΔE_C, which corresponds to a larger aluminum mole fraction in $Al_xGa_{1-x}As$. Unfortunately, increased AlAs composition exacerbates the DX center problem. Typically, DX-center are mitigated by choosing an aluminum mole fraction less than 22% at the expense of reducing the conduction band discontinuity and thus the sheet electron concentration (2).

The pseudomorphic MODFET (PMODFET) alleviates the DX center problem as well as providing a channel in InGaN with superior transport properties over GaAs. The structure is achieved by inserting a thin InGaAs layer between the GaAs buffer and the AlGaAs setback layer in otherwise conventional MODFET. The more favorable carrier transport properties of InAs mean that the higher the indium mole fraction in $In_xGa_{1-x}As$, the higher the electron mobility and velocity within the 2DEG. Additionally, greater carrier confinement can be achieved with pseudomorphic systems, because large conduction band discontinuities can be obtained between InGaAs and low AlAs mole fraction AlGaAs. However, the thickness of the lattice mismatched InGaAs must be below the critical thickness beyond which misfit dislocations occur. The lattice constant, lattice mismatch, and the critical thickness are functions of the indium mole fraction of the strained InGaAs layer; this limits the indium mole fraction content to approximately 30% on GaAs. There is also the lattice matched and pseudomorphic MODFETs based on InP substrates, which take advantage of the superior mobility and

confinement properties of the AlInAs/InGaAs system; this is out of the scope of this discussion. Devices based on InP have exhibited the lowest noise figures yet achieved.

ANALYTICAL DESCRIPTION OF MODULATION DOPED FIELD EFFECT TRANSISTORS

In MODFETs the carriers form the channel in the smaller bandgap material which are donated by the larger bandgap material and/or provided by metal contacts. Since the mobile carriers and their parent donors are spatially separated, ionized impurity scattering is nearly eliminated, which leads to mobilities that are characteristic of nearly pure semiconductors. A Schottky barrier is then used to modulate the mobile charge, which in turn causes a change in the drain current. By virtue of the heterolayer construction, the gate can be placed very close to the conducting channel, which results in large transconductances (1). In what follows, a simplified analytical description of MODFET operation shows quantitatively the effect of charge stored at the heterointerface on mobility and carrier velocity. For its simplicity, while making the important points, the model of Drummond et al. (3) is utilized. Simultaneous solutions of Poisson's and Schrödinger's expressions in the presence of bias must be numerically solved for a more complete description.

The treatment will begin by imposing that the amount of charge depleted from the barrier donor layer is equal to the charge accumulated at the interface while the Fermi level is kept constant across the heterointerface. For a visual description refer to Fig. 1. The electron charge (or hole charge in the case of *p*-channel MODFET) depleted from the barrier layer is given by

$$n_s = \sqrt{\frac{2eN_d}{q}(\Delta E_c - E_{F2} - E_{Fi}) + N_d^2 d_i^2} - N_d d_i \qquad (1)$$

where E_{F2} is the separation between the conduction band in the barrier layer and the Fermi level. N_d is the donor concentration in the barrier layer, ϵ is the dielectric permissivity of the barrier layer, ΔE_c is the conduction band discontinuity, E_{Fi} is the Fermi level with respect to the conduction band edge in the channel layer, and d_i is the thickness of the undoped layer in the barrier layer at the heterointerface. The electron charge stored at the heterointerface is given by

$$n_s = \frac{\rho kT}{q} \ln[(1 + e^{q/kT(E_{Fi} - E_0)})(1 + e^{q/kT(E_{Fi} - E_1)})] \qquad (2)$$

where $E_0 = \gamma_0 n_s^{2/3}$ and $E_1 = \gamma_1 n_s^{2/3}$ are the positions of the first and the second quantum states at the interface, a triangular well formed by the interfacial stored charge. The energy reference is the bottom of the conduction band edge in the smaller bandgap material.

We are assuming here that these lowest energy states are the only ones that are either filled or partially filled. The constants γ_0 and γ_1, which are dependent on the effective mass of the channel material used, and ρ (density of states = $qm^*/\pi h^2$) are derived in the triangular well. Depending on the value of the voltage applied, the gate on the surface of the barrier layer depletes some or all the stored charge at the interface. Simultaneously solving Eq. (1) and (2) results in the determination of the Fermi level in case the interface sheet charge concentration is known or the determination of the sheet charge concentration when the Fermi level is known. With a gate present, Eq. (1), which depicts the equilibrium situation, must be replaced with

$$n_s = \frac{\epsilon}{qd}[V_g - (q\phi_b - qV_{p2} + E_{Fi} - \Delta E_c)] \qquad (3)$$

where ϕ_b is the Schottky barrier height of the gate metal deposited on the barrier layer, V_g is the gate to channel bias voltage, and $V_{p2} = qN_d d_d^2/2\epsilon$. Here d_d is the thickness of the doped barrier layer, and $d = d_d + d_i$. Simultaneous solutions of Eqs. (2) and (3) give the interface charge concentration in the presence of a gate bias. Equation (3) can be conveniently reduced and expressed as

$$n_s = \frac{\epsilon}{q(d + \Delta d)}(V_g - V_{off}) \qquad (4)$$

with $V_{off} = \phi_b - \Delta E_c - V_{p2} + \Delta E_{F0}$ and $\Delta d = \epsilon a/q$ (= 80 Å for GaAs). Here the terms ΔE_{F0} and a are determined from the extrapolations. For example, ΔE_{F0}, which is a temperature-dependent quantity, is the residual value of the Fermi level and can be obtained by extrapolating the calculated Fermi level values from the interface sheet charge and zero sheet charge.

The term a is the slope of the curve, which is reasonably linear for a wide range of sheet charge except near the vanishing values, relating the Fermi level to the sheet charge, $E_{Fi} = \Delta E_{F0}(T) + an_s$. For example, for the GaAs/AlGaAs case, $a \approx 0.125 \times 10^{-16}$ V · m^{-2}, and $\Delta E_{F0} \approx 0$ at 300 K and 0.025 meV at $T \leq 77$ K.

In a field effect transistor, the drain bias produces a lateral field. In long-channel devices and/or for very small drain biases one normally makes the assumption that the channel voltage, which varies along the channel between the source and the drain and finally reaches a value equal to the drain voltage, is added to the gate potential. Doing so reduces Eq. (4) to

$$n_s = \frac{\epsilon}{q(d + \Delta d)}[V_g - V_{off} - V(x)] \qquad (5)$$

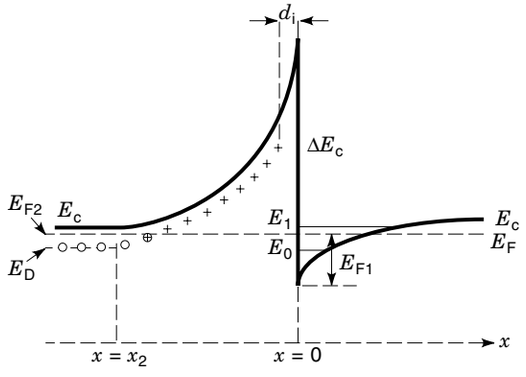

Figure 1. Equilibrium band diagram of a modulation doped structure with Fermi level, quantum states, and the band discontinuity indicated.

where $V(x)$ is the channel potential. For small values of $V(x)$ or when the electric field is the channel, we can assume that the constant mobility regime is in effect and that

$$I_d = qn_s\mu Z\frac{dV(x)}{dx} = \mu Z\frac{\epsilon}{(d+\Delta d)}[V_g - V_{off} - V(x)]\frac{dV(x)}{dx} \quad (6)$$

where μ is the charge mobility and Z is the width of the gate. By integrating Eq. (6) from the source to the drain while keeping in mind that the drain current remains constant throughout the channel, one obtains

$$I_d = \beta(V'_g V_{ds} - \tfrac{1}{2}V_{ds}^2) \quad (7)$$

where $V'_g = (V_g - V_{off})$ and $\beta = \mu Z[\epsilon/(d + \Delta d)L]$ (L is the intrinsic channel length or more popularly the gate length). The current reaches saturation when the drain voltage is increased so that the field in the channel exceeds its critical value thereby causing the velocity to saturate. In that case the drain current is expressed as

$$I_{ds} = Z\frac{\epsilon}{(d+\Delta d)}(V'g - V_{ds})v_s \quad (8)$$

where V_{ds} is the saturation drain voltage, I_{ds} is the saturation current, and v_s is the saturation velocity.

The treatment above is called the two-piece model, meaning an abrupt transition from the constant mobility regime to the constant velocity regime. A more accurate picture is one in which this transition is smoother. In that case a phenomenological velocity field relationship can be used to more accurately describe the MODFET operation. The simplest of all these expressions is one that neglects the peak in the velocity field curve and assumes a silicon-like velocity field characteristic (see Fig. 7). One such expression is

$$v = \frac{\mu F(x)}{1 + \mu F(x)/v_s} \quad (9)$$

where $F(x)$ represents the electric field in the channel that is equal to $dV(x)/dx$. We must also point out that the field is not constant throughout the channel. To calculate the drain current one must write the drain current as

$$\begin{aligned} I_d &= vZ\frac{\epsilon}{(d+\Delta d)}[V_g - V_{off} - V(x)] \\ &= \frac{\mu dV(x)/dx}{1 + \{[\mu dV(x)/dx]/v_s\}}\frac{\epsilon Z}{(d+\Delta d)}[V_g - V_{off} - V(x)] \end{aligned} \quad (10)$$

where $v_s = \mu F_{cr}$, F_{cr} being the field where the velocity assumes its saturation value. By integrating Eq. (10) from the source end of the channel to the drain end, while keeping in mind that the drain current must be constant throughout, one can obtain an expression for the drain current following the mathematical steps of Ref. 4.

Integrating Eq. (10) from the source end of the gate to the drain end of the gate while keeping in mind that the current must remain constant throughout the channel, one obtains

$$I_d = \frac{\frac{\epsilon Z}{d+\Delta d}(V_g V_d - \frac{1}{2}V_d^2)}{L + \frac{\mu}{v_s}V_{ds}} \quad (11)$$

Note that if v_s, the saturation velocity, approaches infinity, Eq. (11) reduces to Eq. (7), which is applicable for the constant mobility case or the long channel case. Following the procedure of Lehovec and Zuleeg (4). The drain saturation current, I_{ds}, can be found by the mutual use of Eqs. (10) and (11) and assuming velocity saturation, as

$$I_{ds} = 2(V_g - V_{off})^2\frac{\epsilon Z}{L(d+\Delta d)}\frac{1}{\left\{1 + \left[\frac{2\mu(V_g - V_{off})}{v_s L}\right]^{1/2}\right\}^2} \quad (12)$$

The transconductance is an important parameter in FETs and is defined as

$$g_m = \left.\frac{\delta I_d}{\delta V_g}\right|_{V_d = \text{constant}}$$

In the saturation regime, the transconductance is expressed as

$$\begin{aligned} g_m^{sat} &= \left.\frac{\delta I_{ds}}{\delta V_g}\right|_{V_d = \text{constant}} \\ &= \mu Z\frac{\epsilon}{(d+\Delta d)L}(V_g - V_{off})\left[1 + \left(\frac{V_g - V_{off}}{v_s}\right)^2\right]^{-1/2} \end{aligned} \quad (13)$$

The maximum transconductance is obtained when the sheet charge density is fully undepleted under the gate that leads to

$$g_m^{max} = \frac{q\mu Z n_s}{L}\left[1 + \left(\frac{q\mu n_s(d+\Delta d)}{\epsilon v_s L}\right)^2\right]^{-1/2} \quad (14)$$

For very short gate lengths, which represent all of modern MODFETs, Eq. (14) reduces to

$$g_m^{max} = \frac{\epsilon v_s Z}{d+\Delta d} \quad (15)$$

The measured transconductance is actually smaller than that given in Eq. (15) in that the source resistance, which will be defined shortly, acts as a negative feedback. Through circuit considerations, the measured, extrinsic transconductance is given by

$$\left.g_m^{max}\right|_{ext} = \frac{g_m^{max}}{1 + R_s g_m^{max}} \quad (16)$$

High-speed devices are commonly analyzed by two-port scattering measurements which are performed generally in the range of 2 GHz to 26 GHz on the wafer by an on-wafer microwave probe station, although 60 GHz is possible, and this figure is constantly moving upward. From the scattering measurements, one can obtain an equivalent circuit for diagnosis and circuit design. From the s parameters one deduces the y parameters, from which an equivalent circuit can be generated.

The transit time under the gate of a submicron MODFET is on the order of a few picoseconds. This being the case, the charging time of the input and the feedback capacitance

through the input resistance R_i in the equivalent circuit is substantial. Generally, two parameters, the current gain cut-off frequency and the maximum oscillation frequency, are figures of merit to gauge the expected high-frequency performance of an FET.

The current gain cut-off frequency, defined as the frequency at which the current gain goes to unity, is given by

$$f_T = \frac{g_m}{2pC_{gs}} = \frac{v_s}{2pL} \tag{17}$$

since the feedback capacitance is negligible compared to the input capacitance. As was mentioned previously, the higher the saturation velocity and the smaller the gate length, the higher the f_T.

The maximum oscillation frequency (5), defined as the frequency at which the power gain goes to unity is given by

$$f_{max} = \frac{f_T}{2\sqrt{r_1 + f_T\tau_3}} \tag{18}$$

where $r_1 = (R_g + R_i + R_s)\, G_d$ and the feedback time constant $\tau_3 = 2pR_gC_{dg}$.

Having derived the simple analytical expressions, it is clear that with strained layers, one can increase the band discontinuities and thus the interface sheet carrier densities [Eq. (1)]. This, in turn, leads to larger current levels [Eq. (6)], as compared to the lattice matched cases. Coupled with large sheet carrier concentrations, higher velocities and mobilities offered by the InGaAs alloy are exploited by the strained layer concept. A larger mobility through reduced source resistance leads to a larger transconductance [Eq. (15)] which in turn leads to larger current gains [Eq. (17)] at high frequencies and larger power gains [Eq. (18)]. Better carrier confinement at the heterointerface also aids in confining the carriers there, which has experimentally been shown to reduce the output conductance, G_d. Therefore, the r_1 term discussed above can be reduced, leading to larger f_{max} values.

To analyze the carrier confinement effect, albeit under equilibrium conditions only, Ballingall et al. (6) solved Schrodinger's and Poisson's equations simultaneously for GaAs/AlGaAs, $In_xGa_{1-x}As$/AlGaAs pseudomorphic, and lattice $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ MODFETs. As expected, the results clearly show that the larger the conduction band discontinuity on the donor barrier side as well as on the buffer side is, the tighter the electron distribution is. On GaAs substrates, the strained-channel MODFET fares better. The confinement gets even better in the structure on InP substrates. If the InGaAs channel on InP contained more InAs than the lattice-matched composition, the confinement as well as the sheet carrier concentration would have been better.

Power gain is also aided by the reduction of parasitic resistances and the time constant, τ_3, which to a large extent depends on the geometry of the device. We begin our discussion of experimental results by discussing the *p*-channel MODFETs first, followed by *n*-channel MODFETs.

POWER MODELING

An accurate modeling of device power performance in emerging semiconductor technologies is very useful in understanding how they stack up against more established semiconductor technologies and in determining in which applications they will have the largest impact. In high-power semiconductor devices, it is imperative that the effect of temperature on device performance is accounted for accurately because power devices typically operate at elevated temperatures. As in small-signal modeling, the first step in power modeling is to establish the basic device geometrical factors needed to calculate the current voltage characteristics. Once these are known, the output characteristics superimposed with the load line can be used to get an estimate of the power level that can be obtained from the device, provided that it is not limited by the input drive as shown in Fig. 2. In class A operation, the maximum power that can be expected from the drain circuit of a device is given by

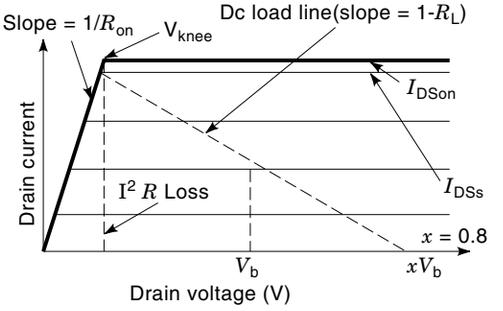

Figure 2. Output characteristics superimposed with the load line that can be used to get an estimate of the power level that can be obtained from the device provided that it is not limited by the input drive.

$$P_{max} = \frac{I_{DSon}(V_b - V_{knee})}{8} \tag{19}$$

where I_{DSon} is the maximum drain current, V_b is the drain breakdown voltage, and V_{knee} is the knee voltage as shown in Fig. 2. I_{DSon} is the drain current with a small positive voltage on the gate electrode. The allowable positive gate voltage ($\approx$1 V) will depend on the channel doping and the work function of the gate metal. The positive gate voltage is limited by the onset of forward Schottky diode current. Although Eq. (19) applies specifically to pentode-like devices such as FETs, the same approach would apply equally well to electronic devices with triode-like devices such as static induction transistors (SIT) operated in the SIT mode, the pentode-like FET mode, or a mixed mode. The dc load line shown in Fig. 2 would be used in a Class A radio frequency amplifier with the drain voltage $V_d = (V_b + V_{knee})/2$. The slope of the load line is $-1/R_L$, where R_L is the value of the load resistance at the output of the FET.

To be of some value, the effect of junction temperature on the output characteristics must be taken into consideration. Temperature-dependent materials parameters, if known, can be used to calculate the output characteristics with respect to temperature. However, a more pragmatic approach, particularly when the aforementioned parameters and or models required are not available, can be taken in which one measures the output characteristics of the device under consideration as a function of temperature. The junction temperature is critically dependent on the substrate thermal conductivity that is available for various substrates including GaN (7). The

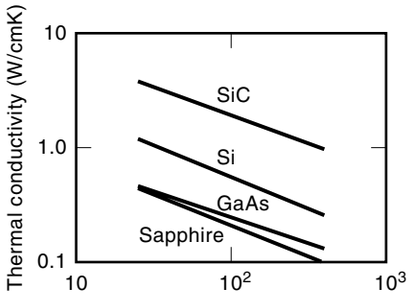

Figure 3. Plot of the thermal conductivity versus temperature (K) of sapphire which is used for GaN devices, SiC which is used for some GN devices, GaAs which is used for GaAs based MODFETs, and silicon for comparison.

functional dependence of thermal conductivity on temperature is

$$\chi(T) = \chi(T_0)(T/T_0)^{-r} \tag{20}$$

where the coefficient r is 0.559, 0.443, 0.524, and 0.544 for Si, GaAs, SiC, and sapphire, respectively (8). In Fig. 3, $\chi(T_0)$ has also been appropriately reduced to account for the doping of the substrate material.

PROCESSING

Increasingly, processing has become a central issue in device design and development. MODFETs represent a case of a buried channel device and requires special attention to be paid. The short gate lengths that generally accompany MODFETs necessitate unique approaches for the gate metal in an effort to keep the gate resistance from getting too large.

Gate Profile

High-performance devices require short gate lengths while keeping the gate resistance to a minimum. As shown in Fig. 4 in conjunction with a cross-sectional diagram of a MODFET structure, the T-shaped gate has proven highly beneficial, because it combines low gate resistance with low gate capacitance. The upper, wide part of the T serves to reduce the gate resistance by virtue of its wide area, and the lower, narrow part of the T correspondingly reduces the gate capacitance through its narrow profile. e-Beam lithography has been the favored method of fabrication, capable of submicron T-gate lengths (9). More recently, deep ultraviolet lithography of submicron T-shaped gates has been developed, overcoming the primary e-beam disadvantages of insufficient throughput and high cost (10). The resistance combines polymethylmethacrylate (PMMA) and polymethylisopropenylketone (PMIPK) in a trilayer resistance structure of PMMA/PMIPK/PMMA. Reliability studies with high-temperature accelerated failure tests have shown that the recess depth of the T-shaped gate plays a decisive role in device failure (11). An unnecessarily deep gate recess in time contributes to a sharp rise in the gate forward resistance due to the excess distance between the wide part of the T and its base. To avoid the consequent degradation of the gain and minimum noise figure, a gate recess depth less than 125 nm is sufficient. A single etch gate recess method utilizes e-beam lithography followed by reactive ion etching or electron cyclotron resonance plasma etching of the GaAs cap (12). This represents an advance in simplicity over the more traditional double gate recess process (13).

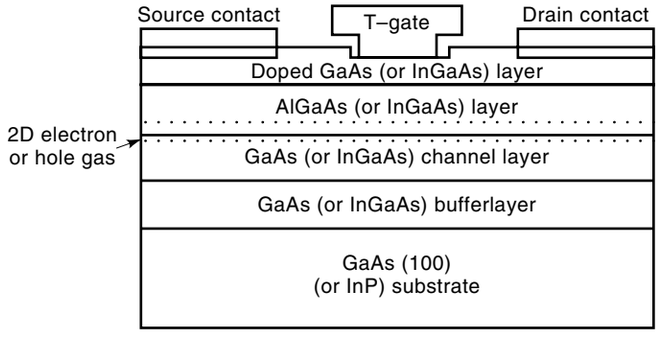

Figure 4. A cross-sectional representation of MODFET structures with the prominent T gate. Those within parenthesis indicate the materials used when the MODFET structure is on InP substrate. Other materials depict the case for GaAs substrates.

The Schottky barrier related processes for GaN-based devices are nascent, but rapid progress is being made. Until recently, it has been difficult to fabricate good quality single-crystal films on which a Schottky metal could be deposited, and properties of Schottky barrier could be studied. However, considerable progress has been made with Pt-GaN Schottky barriers (14,15) that have been successfully implemented in GaN based MODFETs (16–21).

Recent successes in growing good-quality single-crystal III-V GaN layers prompted the fundamental electrical property studies of metal-semiconductor barriers on GaN. The formation of metal-semiconductor barriers is an essential element of a variety of semiconductor devices, particularly MODFETs. To get a large Schottky barrier height, metals with large workfunctions have been explored for rectifying metal contacts on GaN, among which are gold (22) and platinum (14). Hacke et al. (22) obtained gold Schottky barriers on unintentionally doped n-GaN grown by hydride vapor-phase epitaxy. The forward current ideality factor was $n_{idl} \sim 1.03$ and the reverse bias leakage current was $<10^{-10}$ A at a reverse bias of -10 V. While the current–voltage measurement indicated the barrier height to be 0.844 eV, the capacitance measurements led to a value of 0.94 eV.

Recently, Suzue et al. (14) have studied the platinum Schottky barriers on unintentionally doped n-GaN. Dependence of both current–voltage and capacitance–voltage characteristics on temperature was studied in the range of -195°C and 42°C in an effort to gain insight about the current conduction mechanism. The excess current observed for small gate biases pointed to parasitic processes besides the thermionic emission over the Schottky barrier. This excess current is traditionally attributed to defects (generation recombination centers) and surface leakage current. The ensuing current is called the Shockley–Read–Hall (SRH) recombination current resulting from the midgap states. Preliminary investigations indicate that this excess current can be modeled very well with SRH current. Further experiments must be conducted to unravel the exact nature of the underlying processes involved. If one neglects this excess current, a bar-

rier height of approximately 0.8 eV is deduced as opposed to approximately 1 eV deduced from the C–V measurements. Because of the excess current affecting the slope of the I–V curve, the C–V measurement in this particular case is a closer representation of the metal barrier height. An examination of the C–V plots however indicated that under reverse bias condition, the capacitance depended insignificantly on the density of traps. The curves corresponding to all temperatures were largely linear, which yielded barrier heights ranging between 0.95 eV and 1.05 eV. Reduced capacitance with decreasing temperature is consistent with relatively deep donors.

Binari et al. (23) studied titanium Schottky barriers on unintentionally doped n-GaN. The Schottky barrier heights estimated from the current–voltage and capacitance measurements were 0.58 eV and 0.59 eV, respectively. The ideality factor n_{idl} was approximately 1.28, and the diode series resistance R_s = 100 W. The ternary $Al_xGa_{1-x}N$ is an essential component of nitride-based $Al_xGa_{1-x}N$/GaN heterostructure MODFET devices. In fact, the Schottky barriers are deposited on $Al_xGa_{1-x}N$, which makes it imperative to investigate metal $Al_xGa_{1-x}N$; so far such investigations have been lagging behind those on GaN in part due to the lack of good quality layers. Khan et al. (24) reported the fabrication of chromium–gold Schottky barrier on n-AlGaN. Moreover, Khan et al. (25) studied the Schottky barrier characteristics of the $AuAl_xGa_{1-x}N$ system. A typical current–voltage characteristics of $Al_{0.14}Ga_{0.86}N$ Schottky diode had an ideality factor of 1.56 under reverse bias, and a threshold voltage of about 0.9 V at 0.1 A. The reverse bias leakage current was recorded to be marginally low (10^{-10} A) for a reverse bias of -10 V. Employing the current–voltage method the barrier height and the electron affinity were determined to be 0.94 eV and 4.16 eV, respectively. From the C^{-2}/V plot, the same barrier height and electron affinity were deduced to be 1.3 $\pm$ 0.05 eV and 3.8 eV, respectively.

In short, the current conduction mechanism in metal-semiconductor structures is strongly affected by surface and bulk states. Deviations from an ideal ideality factor, as in the case here, are indicative of such states. The situation gets more complicated with AlGaN and gets worse as the AlN mole fraction is increased. Likewise capacitance–voltage measurements also are affected by states that are charged, whether interface state or bulk state charge. As is the case in many facets of research and development, insights into the metal–nitride contacts will be a gain in an evolutionary manner hinging upon the developments in nitride layers.

Ohmic Contacts

Ohmic contact formation to the source and drain of a MODFET is complex because of the necessity that the ohmic contact somehow penetrate the high bandgap barrier layer. In case the contact metal does not penetrate through the barrier, ohmic conduction is realized by tunneling of electrons through the remaining AlGaAs barrier, models for which have been developed (26). On the other hand, a contact with too large a lateral penetration causes shorting to the gate. Several requirements should be fulfilled by a good ohmic contact. These requirements should include not only the short ohmic contact length mentioned above, but also robust thermal stability, and of course, low contact resistance. A clear understanding and control of the alloying reactions that occur at the metal–semiconductor interface and the effect of the wide bandgap semiconductor on contact penetration are essential elements for optimizing the device and the ohmic contact process. Achieving all of these properties is not trivial. Also, different MODFET structures (e.g., AlGaAs/GaAs, AlGaAs/InGaAs, AlIn As/InGaAs) may interact distinctly with the metallization. Consequently, investigators have been forced to adjust their metallurgical mixes for ohmic contacts.

Alloyed ohmic contacts are the traditional ohmic contacts used for a MODFET's source and drain, and certainly are the MODFET ohmic contacts with the longest history of research behind them. Although AuGe/Ni/Au metallization has enjoyed favor as the typical ohmic contact on GaAs-type MODFETs, other similar metallizations under investigation which address problems evident with AuGe/Ni/Au may supplant it.

Nonalloyed ohmic contacts to the source and drain of the MODFET promise to become the ohmic contacts of choice for high-density integration. A short ohmic length with low parasitic source series resistance is a great advantage of nonalloyed ohmic contacts in high-density VLSI. Furthermore, nonalloyed ohmic contacts suffer marginally from the orientation dependence of the specific contact resistance. The difference between the (011) and (00$\bar{1}$) directions is very small, with insignificant variation. In contrast, alloyed ohmic contacts demonstrate a rather large difference in the specific contact resistance between the (011) and (00$\bar{1}$) directions, as evidenced by electron microscope observations of the formation of the alloying region and the alloyed grain fluctuations in size (27,28). The nonalloyed ohmic contact has been prescribed from the actual use in a MODFET structure because of the necessarily high doping concentrations. Electron concentrations in the range of 10^{19} cm^{-3} are needed to enable electron tunneling (or sufficient lowering of the Schottky barrier at the metal–semiconductor interface) with the result that the resistance offered by the heterojunction appears larger. The addition of a capping contact layer, typically a thin, heavily doped n-type InAs or InGaAs layer, is a common solution to enable nonalloyed ohmic contacts. This cap layer approach does have the drawback of requiring its removal for the subsequent gate metallization, however. A heavily tin-doped GaAs contact layer can also be used, obviating the need for additional growth (29).

Contacts to III–V Nitrides Notably Gallium Nitride. Ohmic contacts constitute a major obstacle in large bandgap semiconductors and thus to successful realization of GaN MODFETs. Early results for GaN indicate that ohmic contacts can be formed to both n- and p-type material. The contact resistances to n-type GaN using aluminum and gold metallizations (30) were in the range of 10^{-4} and 10^{-3} Ω/cm^2. The current–voltage measurement revealed that while the as-deposited aluminum contacts were ohmic, the as-deposited gold contacts were rectifying, which became ohmic after annealing at 575°C. Using Ti/Au (31) and TiAl (32), specific contact resistivities of 7.8×10^{-5} Ω/cm^2, and 8×10^{-6} Ω/cm^2 were obtained, respectively. Nakamura et al. (33,34) used gold (and later Au/Ni) and Ti/Al as p- and n-type contacts, respectively, in their LED structures. Although no contact resistances were reported, an operating voltage of 4 V at 20 mA forward bias in a p–n junction device clearly demonstrates that reasonable contact resistances were obtained. Carrying the TiAl contact

work one step further, Wu et al. (35) confirmed that, except at very high annealing temperatures, the ohmic contact suggested by Lin et al. (32) functions very effectively. At very high temperatures, the aluminum of the metal contact melts and tends to ball up, resulting in rough surfaces and increased ohmic contact resistances as pointed out already by Lin et al. (32). In an attempt to circumvent this difficulty, Wu et al. (35) designed a separate layer metallization method where a realignment and deposition of a second thin titanium layer, and a 2000 Å gold overlayer was carried out. Specific contact resistivities were in the range of 3.0×10^{-6} Ω/cm^2 and 5.5×10^{-6} Ω/cm^2 depending on the doping concentration in the semiconductor.

In an attempt to obtain an improved ohmic contact, Fan et al. (36) have designed a multilayer ohmic contact method. Utilizing a composite metal layer of Ti/Al/Ni/Au (150 Å/2200 Å/400 Å/500 Å), very low contact resistivities were obtained. Specifically, for n-GaN with doping levels between 2×10^{17} cm^{-3} and 4×10^{17} cm^{-3}, specific contact resistivities in the range of $\rho_s = 1.19 \times 10^{-7}$ Ω/cm^2 and 8.9×10^{-8} Ω/cm^2, respectively, were obtained. The calculation of the contact resistivity was based on the assumption that the semiconductor sheet resistance underneath the contacts remains unchanged, which is not true for nonalloyed contacts. As for the current conduction mechanism in these ohmic contacts, the large metal-semiconductor barriers diminish the possibility of thermionic emission governed ohmic contacts to GaN. The alternative mechanism is naturally some form of tunneling, which may take place if GaN is so heavily doped to cause a very thin depletion region. Tunneling is possible if, due to annealing, for example, at 900°C for 30 s, aluminum and titanium along with nickel undergo substantial interaction with each other and GaN. A cursory look would imply that titanium receives nitrogen from GaN forming a metallic layer, whereas the lack of nitrogen on GaN provides the desired benefit of increased electron concentration through nitrogen vacancy formation. Aluminum acts to passivate the surface and also possibly react with titanium-forming TiAl. For details, the reader is referred to Ref. 7.

CHANNEL DESIGN

Low-field mobilities in heterostructures rise and parasitic resistances decrease with decreasing temperature. However, the conventional AlGaAs/GaAs MODFET exhibits the well-known collapse of the I–V characteristics and a strong threshold voltage shift (37). The low-temperature behavior of the device is affected also by the altered behavior of the n-AlGaAs layer. As long as the aluminum mole fraction and the doping level are low, the activation energy of the donors is shallow. However, as the aluminum content exceeds 25% and the doping level exceeds 5×10^{17} cm^{-3}, both of which are necessary for obtaining higher 2DEG and a better electron confinement in the channel, a large number of donors become deep, resulting in a freeze-out of carriers, I–V collapse, and persistent photoconductivity at low temperatures. Replacing the doped n-AlGaAs layer with an n-GaAs/AlAs superlattice reduces these low-temperature effects (38). Another novel improvement of the MODFET involves striping of the active channel. A striped channel MODFET (SC-MODFET) is essentially the same as the conventional MODFET except that the source-to-drain region is divided into a number of narrow conducting channels referred to as wires. Thus an active AlGaAs/InGaAs layer grown on a GaAs substrate exhibits well-defined square well properties, providing good confinement of the 2DEG even at low sheet carrier density. In SC-MODFETs the 2DEG can be controlled in both vertical and lateral directions by the Schottky gate, and the enhancement in transconductance is consistent with gate capacitance increase (39).

MODFET PERFORMANCE

To reiterate, MODFETs good performance is due to the conduction channel which eliminates impurity scattering and unique capacitance voltage relationship. The PMODFET alleviates the DX center problem while using an InGaN channel with superior transport properties over GaAs (40). There is also the lattice matched and pseudomorphic MODFETs based on InP substrates utilizing higher mole fraction InGaAs.

In the conventional III–V semiconductors, three types of MODFETs have been explored: those with GaAs channels on GaAs substrates, $In_xGa_{1-x}As$ channels on GaAs substrates, and the high InAs mole fraction InGaAs channels on InP substrates. The exploration has allowed the goals set, for example, for the W-band (approximately 5 dB for gain and 4 dB for noise figures) to be well exceeded. With 0.15 μm gate devices (41) a 12.6 dB gain and minimum noise figure of 1.4 dB have been obtained at around 95 GHz. The associated gain at the bias point producing this extremely low noise figure is 6.6 dB. This value is remarkable and indicates the suitability of the InGaAs/InAlAs MODFET structure for operation near 100 GHz and beyond. Peng et al. (42) showed that the increase in the InAs mole fraction leads to an improvement in the high-frequency performance. The results indicate that, as the InAs mole fraction is increased, for example, from zero to 65%, the current gain cut-off frequency increases by more than a factor of two, from approximately 110 to 260 GHz (43–52). The current gain cut-off frequency corresponding to unity current gain, is an important parameter in logic gates. The maximum oscillation frequency (f_{max}), for which the maximum available gain of the device goes to unity, is also an important factor for determining the electrical and microwave performance. This figure too shows that an increase in the InAs mole fraction leads f_{max} values, for example, for GaAs channel device to increase by approximately 30%, to approximately 350 GHz. With a 53% mole fraction and a 0.15 μm gate length, it increases to a remarkable 405 GHz. The minimum noise levels from MODFETs based on GaAs and InP obtained at Lockheed Martin are shown in Fig. 5.

Devices based on InP hold the highest f_t and f_{max} (53). The promise held by PMODFETs was demonstrated with the development of the 0.25 μm gate length (54). The results obtained since show that f_t increases by more than a factor of two, from 110 to 260 GHz, as the InAs mole fraction is increased from zero to 65% (55–58). With the pseudomorphic approach, the f_{max} for a GaAs channel device is increased by 30%, to 350 GHz (59). With a 53% mole fraction, a remarkable 405 GHz was obtained with 0.15 μm gate devices (60). Performance above 100 GHz has been measured by Tan et al. (61). Using a 0.1 μm gate length pseudomorphic $In_{0.52}Al_{0.48}As/In_{0.6}Ga_{0.4}As/InP$ structure, a noise figure of 1.3 dB and an associated gain of 8.2 dB at 95 GHz have been obtained. At

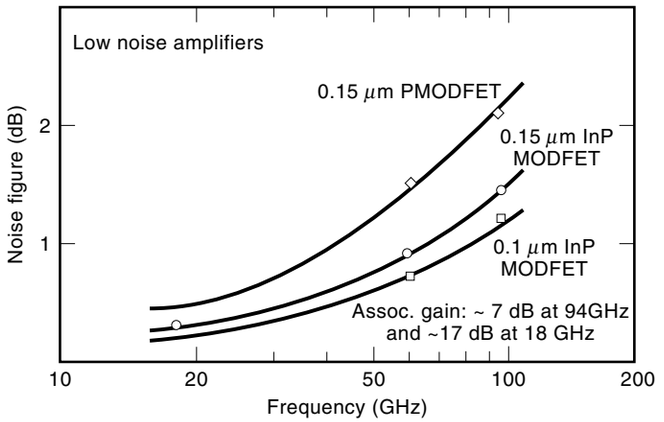

Figure 5. Minimum noise figure of pseudomorphic AlGaAs/InGaAs and InAlAs/InGaAs MODFETs with 0.15 μm for GaAs-based and 0.1 μm for InP-based gate lengths. Courtesy of P. M. Smith, Lockheed Martin.

141.5 GHz, a D band frequency, the device exhibited a gain of 7.3 dB.

The current gain cut-off frequency along with the maximum oscillation frequency f_{max}, the maximum transconductance g_m, and the maximum channel current I_{max} for some representative MODFETs are listed in Table 1.

Low-Noise Amplifiers

Low-noise amplifiers (LNAs) are required in a number of millimeter wave and microwave applications including radar, satellite communications, seekers, and munitions. They are key components in the receiving portion of these systems. Recent advances in low-noise MODFET technology have significantly improved their performance, particularly for those at W-band frequency. Coplanar waveguides (CPW) and conductor-backed coplanar waveguides (CBCPW) are important alternatives to microstrip transmission lines for MMICs. These millimeter wave monolithic CPW and CBCPW LNAs have been developed in a variety of forms including a two-stage single-ended Q-band LNA, a 5 to 100 GHz distributed amplifier, a W-band cascade amplifier, and a W-band four-stage single-ended CBCPW amplifier. These LNAs are particularly attractive for MMIC design because their properties of minimizing active device source inductance, increase line-to-line isolation, improving on-wafer probe testing, and simplifying MMIC processes. One major advantage of CPW LNA structures is that they can be fabricated together with microstrip line and slot-line components.

Fabrication of LNAs is performed primarily by making use of conventional n-AlGaAs/GaAs MODFETs. However, LNAs with these MODFETs suffer from performance degradation. The latter stems from the degradation of the performance of the conventional MODFETs with uniformly doped n-AlGaAs layer and the channel length lower than 0.25 μm due to short-channel effects. To circumvent the degradation resulting from short-channel effects, the aspect ratio L/t, where L is the gate length and t is the thickness of the electron supply layer, is usually increased. This is achieved by lowering t, because a thin electron supply layer confines the 2DEG very effectively at the interface. The InGaP-based MODFETs are particularly useful in this respect. The Schottky barrier height for this system is low and the charged DX centers practically absent. All these allow the thickness of the n-InGaP layer to be substantially reduced. Good carrier confinement thus achieved in the pseudomorphic quantum well channel contributes to reducing short-channel effects. Because of this, InGaP/InGaAs/GaAs MODFETs may be improved alternatives to conventional AlGaAs/GaAs MODFETs. InP-based InAlAs/InGaAs/InP MODFETs may satisfy the same purpose. Recently, these MODFETs have demonstrated the lowest noise figures among all three-terminal solid-state devices. The lowest noise figures F_{min} from various GaAs- and InP-based MODFETs are depicted in Table 2 (85–94). From this figure, it may be noted that InP-based T-gate technology with noise figures below 1.0 dB has been realized.

Power Amplifiers

Power applications present another useful area in which the benefits of MODFETs can be exploited. A tabulation of power performance of some representative MODFETs, MESFETs, and HBTs are shown in Table 3. From this table it may be noted that MODFETs demonstrate power performance better than those of MESFETs and HBTs.

High-power amplifications are necessary for achieving maximum reliability, minimum size and weight, high volume, low cost, and high performance of phased-array systems such as radar, satellite communications transmitters, electronic warfare, seekers, and smart munitions. An efficient MODFET power amplifier should be not only cost-effective, but also yield superior power added efficiencies (PAE) and gain for phased array systems applications. Chen et al. developed chip PMODFET K-band power modules that deliver 3.2 W with a power added efficiency (PAE) of 35% at 3 dB compression, 10 dB saturated gain at 20 GHz, a 1 dB bandwidth of 1.7 GHz, and power density of 500 mW/mm (116). Such high-power modules are specially suited for spacecraft on-board applications. A 0.15 μm double heterostructure InGaAs/AlGaAs/GaAs PMODFET has displayed a maximum transconductance over 500 mS/mm, a maximum current density over 600 mA/mm, a cutoff frequency of 90 GHz, and a maximum oscillation frequency of 200 GHz (117). This particular MODFET has been utilized in a V-band monolithic power amplifier with an output power of 313 mW (0.39 W/mm) with 8.95 dB power gain and 19.9% PAE at 59.5 GHz (118).

There is no doubt that AlGaAs/InGaAs/GaAs PMODFETs have demonstrated great potential as the microwave and millimeter wave device for high-gain low-noise applications. However, there is still for improvement. To further optimize the transmitter modules, the output power should be increased, which necessitates the improvement of the power performance of PMODFETs. To this end, both the current drivability and the breakdown voltage must be increased. The breakdown voltage can be increased without deteriorating high-speed performance if the double-recess approach is employed (119) or if high bandgap AlGaAs layers with lower mobility are used; perhaps a combination of both approaches may be viable. Alternatively, a highly p-doped, very thin surface layer in combination with GaInP as the wide bandgap material can be used. Such a modification of device structure can lead to a distinct advantage over more typical AlGaAs/InGaAs PMODFETs (120). Remarkably, a device with 1.8 μm

Table 1. The Full Channel Current I_{max}, Cutoff Frequency f_T, Maximum Oscillation Frequency f_{max}, and Maximum Transconductance g_m for Various MODFETs[a]

MODFET Type	I_{max} (mA/mm)	f_T (GHz)	f_{max} (GHz)	g_m (mS/mm)	Comments	Ref.
GaAs-based MODFETs						
AlGaAs/GaAs MODFET		100	9	15	p-channel, L = 0.25 μm 115	62
AlGaAs/InGaAs/GaAs PMODFET		250	5	4	Vertically integrated with GRINSCHSQS laser, A = 2 μm × 500 μm	63
Unstrained InGaAs/InAlAs MODFET		250	15	56	VGB3523.5V. A = 1 μm × 10 μm	64
AlGaAs/GaAs MODFET		275	72	144	CPE330 = 0.2 μm × 150 μm	63
AlGaAs/InGaAs MODFET		300	15	59	V_{Br}224 = 10 V, L = 1.8 μm	66
GaInP/InGaAs MODFET		400	12	42	V_{Br}208 = 14 V, L = 1.8 μm	
AlGaAs/InGaAs PMODFET		400	100	200	A = 530–0.17 μm × 75 μm	67
AlGaAs/InGaAs PMODFET		400	100	200	7 dB50 ln at 90 GHz, L = 0.2 μm	68
InAlAs/InGaAs		400	45	115	Metamorphic on GaAs, triangular gate, A = 0.4 μm × 150 μm	69, 70
GaAs/InGaAs PMODFET		500 (77K) 690			δ-doped, graded channel, 45 × 100 μm	71
DR PMODFET		525	50	100	VDS366V V_{BR}DG = 11 V, L = 0.25 μm	72
AlGaAs/InGAAs PMODFET		550	122	80–90	12n55SQW, A = 0.2 μm × 140 μm	73
AlGaAs/InGaAs PMODFET		550	100	200	12nSSS QW, A = 0.2 μm × 50 μm	
DR PMODFET		580	39	170	L = 0.545 m	74
2 Heterostructure MODFET		600	90	200	VBr500 10 V, A = 0.15 μm × 80 μm	75
AlGaAs/InGaAs PMODFET		630	110	230	A = 0655 μm × 50 μm	76
AlGaAs/InGaAs PMODFET			152	150	A = 0.15 μm × 150 μm	
AlGaAs/InGaAs PMODFET			66	75	Enhancement mode, L = 0.3 μm	77
			66	75	Depletion mode	
GaInP/GaAs PMODFET			17.8	23.5	A = 11 × 200 μm (77K) 213	78, 79
N-InGaP/InGaAs/GaAs			76	191	A = 0.42 μm × 200 μm	80
InP-based MODFETs						
AlInAs/GaInAs/InP MODFET		350	22	75	Junction modulation device, A = 1 μm × 150 μm	81
GaInAs/AlInAs/InP PMODFET		700	80	—	V_g = 50 V, A = 0.25 μm × 50 μm, Power MODFET, BV_{gd} = 6.8 V	82
InAlP/InGaAs/InP PMODFET		800	86	>20	A = 0380 μm × 50 μm, Al mole fraction in InAlP = 0.25, BV_{gd} = 12 V	83
InP/InGaAs/InP MODFET		—	27	89	In most fraction in InGaAs = 0.74, Quantum well MODFET, V_g = 5 V, A = 1 μm × 50 μm	84

[a] In the table A is the cross-sectional area of the channel, L is the channel length, V_G is the gate voltage, and BV_{gd} is the breakdown voltage. PMODFET is an abbreviation of pseudomorphic MODFET.

gate length designed in this experiment shows a breakdown voltage of 4 V or higher, with all other parameters almost unchanged.

The main weakness of the InGaAs-based MODFETs is the impact ionization in the channel by hot electrons injected from the gate and that the weak Schottky barrier height on InAlAs allows large reverse bias gate leakage current to flow reducing the gate-diode breakdown. This prevents the $In_{0.53}Ga_{0.47}As$-channel MODFETs from demonstrating high-power performance. To address this issue, various modifications to both the gate and channel regions have been investigated. These modifications include variations in the gate contact layers, channel material, and doping strategy of the 2DEG. Three different approaches are undertaken to improve the gate barrier and the gate-drain breakdown voltage: incorporation of a junction to modulate the 2DEG, incorporation of an AlInP Schottky barrier, and increasing of barrier height by increasing the aluminum mole fraction in the AlInAs Schottky barrier layer.

To realize the junction-modulated MODFETs a heavily doped p-type AlInAs layer is incorporated on the top of the conventional MODFET structures. This results in high turn-on voltage, low leakage current, and high reverse breakdown voltage. The increase in the barrier height by increasing the aluminum mole fraction of the AlGaAs, for example, from 48% to 70%, and a proper tailoring of the dopant concentration lead also to an increase in the turn-on voltage from 0.5 to approximately 1.0 V.

The concept of regrown contacts (121) to a 2DEG has been tested in an InAlAs/InGaAs-InPMODFET (122). It was noted that the improvement in barrier height that results from incorporating a junction between a surface p^+ layer and the

Table 2. Frequency, Noise Figure and Gain of Various MODFETs

MODFET-type	Frequency (GHz)	Noise Figure (dB).	Gain (dB)	Comments[a]	Ref.
		InP-based MODFETs			
AlInAs-GaInAs-InP	2.0	0.5	35.0	2-stage MMIC	95
AlInAs-GaInAs/InP	7–11	1.2	22.0	—	96
AlInAs-GaInAs-InP	12.0	0.8	12.0	—	97
AlInAs-GaInAs-InP	18.0	0.7	—	L = 0.1 μm, planar doped	98
AlInAs-GaInAs-InP	36	1.6	17		99
AlInAs-GaInAs-InP	40–45	0.2	33.0	L = 0.1 μm	100
AlInAs-GaInAs-InP	56–64	3.0	24	L = 0.1 μm	101
AlInAs-GaInAs-InP	60	1.9	13.0		87
AlInAs-GaInAs-InP	60	0.8	8.9	L = 0.1 μm	102
AlInAs-GaInAs-InP	60	0.9	—	L = 0.1, 0.2 μm	103
AlInAs-GaInAs-InP	92	—	9.2		87
AlInAs-GaInAs-InP	94	1.2	7.2		89
AlInAs-GaInAs-InP	95	1.3	8.2	L = 0.1 μm	104
AlInAs-GaInAs-InP	141.5	—	7.3	L = 0.1 μm	104
		GaAs-based MODFETs			
AlGaAs-InGaAs-GaAs	41–45	3.0	22	x = 0.25, L = 0.15 μm	103
AlGaAs-InGaAs-GaAs	112–115	6.3	12	2-stage LNA, L = 0.1 μm planar, T-gate	106
AlGaAs-InGaAs-GaAs	113	5.3	10	—	106
AlGaAs-InGaAs-GaAs	110	3.9	19.6	—	106
AlGaAs-InGaAs-GaAs	113	3.4	15.6	—	106
AlGaAs-InGaAs-GaAs	2–20	>3.0	13	L = 0.25 μm, mushroom profile	107
AlGaAs-InGaAs-GaAs	91	3.4	8.7	2-stage, 0.15 × 60 μm^2	108
AlGaAs-InGaAs-GaAs	10	0.6	13	T-gate, L = 0.3 μm	109
n-$In_{0.25}Ga_{0.75}P$-$In_{0.48}Ga_{0.52}As$-GaAs	12	0.41	13	(0.15 × 200) μm^2	110
n-$In_{0.25}Ga_{0.75}P$-$In_{0.48}Ga_{0.52}As$-GaAs	50	1.2	5.8	—	135
AlGaAs-InGaAs-GaAs	93–95	4.5–5.5	17	L = 0.1 μm, single side band noise	111
AlGaAs-InGaAs-GaAs	113	3.4	15.6	L = 0.1 μm	112
AlGaAs-InGaAs-GaAs	110	3.9	19.6	—	112
AlGaAs-InGaAs-GaAs	41–45	3.0	22	L = 0.15 μm T-gate	113

[a] L is the channel length.

2DEG leads to increase in the two-terminal gate-drain and the three-terminal off-state breakdown voltages. Furthermore, the formation of a stable nonalloyed contact to the 2DEG by using selection regrowth of the source and the drain regions causes a reduction in the drain fields. Interestingly, all these improvements are achieved without sacrificing the full-channel current and transconductance. The replacement of the InGaAs channel by the InP channel also provides a significantly large microwave power of 30 GHz or so, and a three-terminal on-state breakdown voltage of 10 V. However, the same replacement accompanies a deterioration in carrier mobility in the channel (123). The formation of a composite bilayer channel, for which both doped and undoped InP along with a thin GaInAs layer are utilized, brings about improved microwave power up to approximately 60 GHz. One notable advantage of a composite channel over a conventional channel is that it enjoys the effect of high electron mobility of InGaAs and of high breakdown field and velocity of InP (124). The effect of the indium mole fraction alternation of the InGaAs channel material on the electrical performance of the MODFETs has been carefully explored. This investigation points to the expected reduction in the electron effectiveness mass in the channel as the indium mole fraction is increased to about 60% or more. Thus the gain at submillimeter frequencies is increased substantially (125). The power performance and related properties of some representative MODFETs are presented in Table 4.

Table 3. A Comparison of Power Performance of GaAs-Based MODFETs, MESFETs, and HBTs

Device	Power (W)	Gain (dB)	PAE (%)	Frequency (GHz)	Ref.
HBT	0.5	11	60	10	114
MESFET	8.0	9	40	10	114
PMODFET	10	13.5	63	2.45	115

The expected frequency band of operation of low noise GaAs and InP-based MODFET technologies is approaching 100 GHz. The lower frequency end, particularly that in the wireless communication arena, is challenged by MOSFET and SiGe technologies. Although the digital telephone operation band is currently slated to be near 2 GHz, with the almost certain video transmission over the wireless systems in the future, this frequency is expected to be pushed upward. Burgeoning Personal Communication System (PCS) technology provides excellent opportunities for the devices discussed here.

Table 4. Power Performance and Related Properties of Various MODFETs

MODFET Type	Frequency (GHz)	Gain (dB)	Power (mW)	PAE (%)	Comments[a]	Ref.
			GaAs-based MODFETs			
0.32 μm × 48 μm 2 × pulse doped AlGaAs/GaAs MODFET	0.5–50	6.5	16 at 40 GHz		6-stage distributed, VDS = 4 V, ft = 45 GHz, fmax = 110 G Hz, NF = 4.8 dB at 0.5–26.5 GHz	126
0.2 μm × 50 μm recessed AlGaAs/GaAs MODFET	2–52	9	2.5 max 12.6		Matrix distributed, 2-stage 4-section VDS = 3 V	127
	2.45	13.5	10 W	63		128
0.25 μm × 8 mm DR MODFET	4	15.4	4.3 W	66	g_{mmax} = 430 mS/mm, I_{max} = 450 mA/mm, VDS = 8 V	129
	4	12.6	5.7 W	57	VDS = 11 V	129
	4	16.6	3 W	63		129
	4		4.1 W	72	VDS = 7 V	129
0.25 μm × 400 μm DR PMODFET	4.5	17.2	330	63	VDS = 8 V, g_{mmax} = 510 mS/mm, I_{max} = 540-mA/mm	130
0.25 μm × 400 μm DR PMODFET	4.5		505	40	VDS = 14 V	130
0.25 μm × 400 μm DR PMODFET	10	11	326	62	VDS = 8 V	130
0.7 μm × 3 mm 2 × HJ SL AlGaAs/GaAs IMODFET	5.5	8.3	1.3 W	55	g_m = 180 mS/mm	131
0.25 μm × 1.12 mm recessed PMODFET	9	9.25	850	50	VDS = 5 V, g_m = 428 mS/mm f_T = 50 GHz, I_{max} = 545 mA/mm	132
0.35 μm PMODFET DR 2 × pulse doped	10	10.4	870	59	V_{DS} = 7 V	133
0.25 μm PMODFET DR	10	10	970	70	Dry first recess etching, VDS = 8 V	134
	18	6.8		48		135
0.25 μm × 1.6 mm 2 × HJ PMODFET	12	14	2.2 W	39	2-stage	135
	12	14	2.75 W	36	2-stage, power tuning	136
	15	10.8	600	51	Single device	136
0.25 μm × 8 mm DR PMODFET, QW planar- and pulse-doped	12	10.8	6 W	52	V_{DS} = 9 V, 420 mS/mm I_{max} = 420 mA/mm	136
	12	10.3	5.4 W	53	V_{DS} = 8 V	137
	12	10.8	6.0 W	52	V_{DS} = 7 V	137
	12	10	3.9 W	55.6	V_{DS} = 6 V	137
GaAs/InGaAs/GaAs PMODFET	14.25	5	4.7 W	25	V_{Br} = 20 V, g_m = 224 mS/mm	137
10.5 mm-wide GaAs/InGaAs/GaAs MODFET	14.25	lin. 8	4.7 W	25	V_{DS} = 10 V V_{Br} = 25.7 V	138
PMODFET	15	12	575	50		139
0.25 μm PMODFET	18	6.3	776	53	I_{max} = 550 mA/mm, V_{DS} = 7 V g_m = 350 mS/mm, 2 × pulse doped	140
0.25 μm PMODFET	10	10.2	955	66	V_{DS} = 8 V	140
0.25 μm × 50 μm PMODFET	18	8	20	59	g_m = 554 mS/mm, monolithic integration w/MODFET LNA	141
0.33 μ × 120 μm PMODFET	25	12.9	680	45	$n+$ GaAs supply layer I_{max} 530 mA/mm, V_{DS} = 5 V	142
	25	10.9	810	59		142
0.25 μm PMODFET	30	8.5	500	40	2-stage cascaded	143
	31	11	141	40.3	2-stage cascaded	
0.2 μm DR PMODFET	32	6	500	35		144
	44	4.3	494	30		
0.15 μm PMODFET	34–36	9	1 W	20	V_{DS} = 5 V	145
	34–36	17	3 W	15	2-stage	
0.25 μm × 900 μm PMODFET	35	3.2	658	24		146
0.15 μm × 50 μm PMODFET	35	9.0	32	51		147, 148
	35	8.5	42	37		147, 148
0.15 μm × 150 μm PMODFET	35	8.0	95	50		147, 148

(*Continued*)

Table 4. *(Continued)*

MODFET Type	Frequency (GHz)	Gain (dB)	Power (mW)	PAE (%)	Comments[a]	Ref.
			GaAs-based MODFETs			
	35	7.6	137	40		147, 148
0.2 μm × 80 μm/150 μm PMODFET	40	19.1	41		3-stage	149
0.2 μm × 600 μm DR 2 × pulse doped PMODFET	40–45	10–11	500–725	10–17	First pass, 3-stage, V_{DS} = 5 V	150
0.25 μm × 400 μm PMODFET	55	4.6	184	25	g_m = 500 mS/mm T_{max} = 540 mA/mm	151
0.25 μm × 320 μm PMODFET	55	4.9	153	25		151
0.25 μm × 240 μm PMODFET	55	4.9	105	22		151
0.2 μm × 50 μm PMODFET	55	3.3	42	22.1	g_m = 760 mS/mm T_{max} = 800 mA/mm	152
0.3 μm × 800 μm PMODFET	55	4.1	219	18	f_t = 50 GHz, f_{max} = 92 GHz I_{max} = 420 mA, G_m = 360 mS	153
PMODFET 2 × heterostructure	59.5	8.95	313	19.9	2-stage, V_{DS} = 5 V	154
0.15 μm × 320 μm DR PMODFET	59.5–63.5	7	370	11	V = 5 V, I_{max} = 500 mA/mm f_T > 75 GHz	155
0.15 μm × 320 μm DR PMODFET	59.5–63.5	11.7	740	8	1 amp drives 3 amps, V = 5 V	155
0.15 μm × 50 μm PMODFET	60	6.0	32	41	NF = 1.8 dB, Ass. Gain = 6.4 dB	147, 148
	60	5.9	42	37		
0.15 μm × 150 μm PMODFET	60	4.7	82	38		
	60	4.5	125	32		
0.15 μm × 400 μm PMODFET 2 × heterostructure	60	4.5	225	25.4	V_D = 5 V	156
0.15 μm × 400 μm	60	4.4	174	28.8	V_{DS} = 4.5 V	156
0.15 μm × 320 μm	60	5.3	170	31.1	V_{DS} = 4.5 V	156
0.15 μm × 320 μm	60	5.1	191	28.7	V_{DS} = 5 V	156
0.15 μm × 100 μm PMODFET	77	21	12		3-stage, V_D = 3.5 V, f_r = 110 GHz, f_{max} = 200 GHz	157
0.1 μm × 160 μm PMODFET	93.5	5.9	100	6.6	2-stage, V_{DS} = 3.5 V	158
0.1 μm × 40 μm PMODFET	94	7.3	10.6	14.3	f_{max} = 290 GHz	159
0.15 μm × 50 μm PMODFET	94	3.3	18	23		147, 148
0.15 μm × 50 μm PMODFET	94	3.2	22	19		147, 148
0.15 μm × 150 μm PMODFET	94	3.0	45	16		147, 148
0.15 μm × 50 μm PMODFET	94	2.0	57	16		147, 148
0.25 μm InGaAs/IniP PMODFET	4	15	560	63	Composite channel	160
AlInAs/GaInAs/InP PMODFET	12	11.1	110	50	Double-doped channel	161
	12	11.0	288	40		
AlInAs/GaInAs/InP PMODFET	20	7.1	516	47	Double-doped channel	162
AlInAs/GaInAs/InP PMODFET	20	10.5	20.5	52	$In_{0.47}Ga_{0.53}As$ channel	163
	20	10.2	39.0	44		
0.30 μm PMODFET	30		145	13	InP-channel	164
	30	5.2	120	23		

(*Continued*)

Table 4. *(Continued)*

MODFET Type	Frequency (GHz)	Gain (dB)	Power (mW)	PAE (%)	Comments[a]	Ref.
			InP-base MODFETs			
0.15 μm AlInAs/GaInAs/InP PMODFET	60	4.9	155	30	δ-doped channel	165
0.15 μm AlInAs/GaInAs/InP PMODFET	60	3.6	288	20.4	δ-doped channel	
0.20 μmAlInAs/GaInAs/InP PMODFET	60	4.2	145	24	double-doped channel	
0.15 μm GaInAs/InP PMODFET	60	—	170	30	composite channel	166
0.15 InAlAs/InGaAs/InP MODFET	60	7.2	18.5 W	41	$Ga_{0.31}In_{0.69}As$ channel	163
0.15 InAlAs/InGaAs/InP MODFET	60	5.9	26 W	33	$Ga_{0.31}In_{0.69}As$ channel	163
0.15 InAlAs/InGaAs/InP MODFET	94	4.9	10 W	26	$Ga_{0.31}In_{0.69}As$ channel	163
0.25 μm $\times$ 400 μm AlGaAs/InGaAs/GaAs PMODFET	34–36	12	500	32	2$\times$ sided delta-doped 2-stage	167

[a] V_{DS} is the drain-source voltage, and V_{Br} is the breakdown voltage.

Expected frequency bands of operation of low noise GaAs- and InP-based MODFET technologies are shown in Fig. 6 for 0.25, 0.15 and 0.1 μm gate lengths. In a more applications specific format, Fig. 7 shows the possible applications of MODFET along with competing technologies, MESFET and HBT. As Fig. 7 indicates, the bulk of the applications can be satisfied by the GaAs-based pseudomorphic MODFETs (PMODFETs), particularly so for power applications. For any device to be considered for any application at all, the longevity requirements must be met. Results of accelerated lifetime investigations are shown in Figs. 8 and 9 for low noise and power amplifiers. Clearly, even the InP devices, while not as good as those on GaAs substrates in terms of longevity, exhibit reasonable operating lifetimes and meet the requirements.

The lower frequency end, particularly that in wireless communication arena, is challenged by MOSFET, and SiGe technologies. Recently, burgeoning PCS technology provides excellent opportunities for electronic devices and in particular for the devices discussed here. The digital telephone operation band is currently slated to be near 2 GHz, with the almost certain video transmission over the wireless systems in the future but this frequency is certain to be pushed upward. At present, digital telephone components for which compound semiconductors are being considered are power amplifiers (PA), drivers, LNAs, mixers, and switches as shown in Fig. 10 which shows the radio frequency section of such a telephone. Conflicting pressures are in effect in that on one hand integration is emphasized to simplify system assembly and reduce cost. On the other hand, more integration imposes application-specific designs and manufacture. Suppliers at the moments lean in the direction of less integration for a wider range of applications for each part. Cost considerations and manufacturing simplicity have favored the use of MESFETs more so among the compound semiconductors for the wireless. However, the ever-increasing demands on performance and power amplifier efficiency to extend the battery operation coupled with advanced epitaxial technology in regard to production issues are paving the way for MODFETs. Already, companies such as Hewlett Packard produce large quantities of low noise amplifiers and mixers on the same chip.

AlGaN/GaN MODFETS

Semiconductor GaN-based field-effect transistors (FETs) are projected to be highly useful for amplification and switching

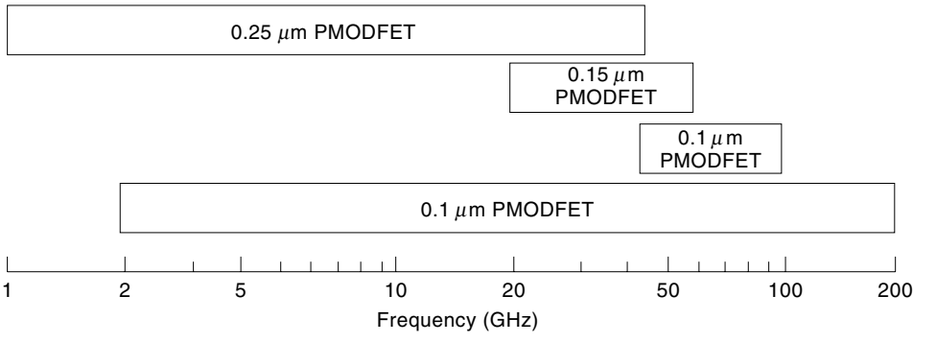

Figure 6. Frequency band of applications for MODFETs. Courtesy of P. M. Smith of Lockheed Martin.

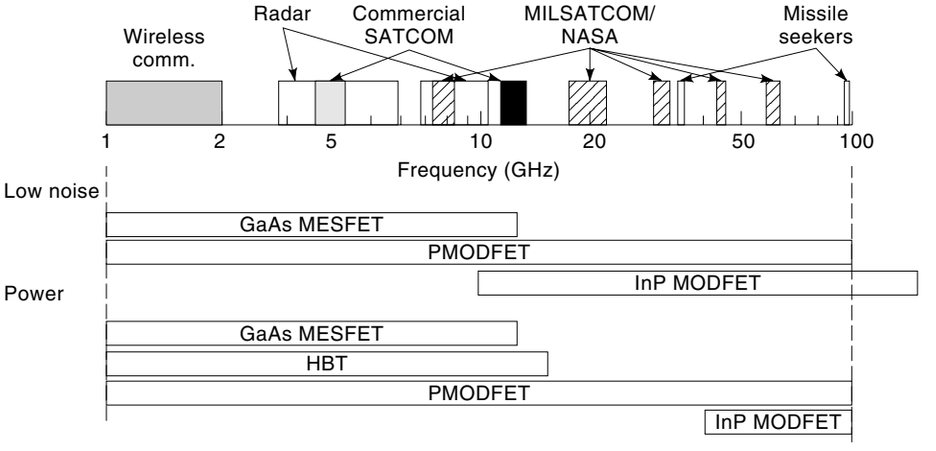

Figure 7. Possible applications of MESFET, MODFET, and HBT technologies categorized by frequency of operation. Courtesy of S. Komiak of Lockheed Martin.

in a high-power and/or high-temperature environment. The optimism is justifiably fueled by the calculated large electron velocity and the robustness of the material. Other pertinent parameters include, but not limited to, large thermal conductivity of GaN, type 1 heterojunctions, large-band discontinuities with resultant large interface carrier concentrations, and large breakdown voltage, albeit requires high-quality films (168,169). Consequently, there has been a flurry of activity in GaN based MODFETs (17–19,21,170–174). The results are extraordinarily encouraging and needless to say that the activity is on a rapid rise. These devices are receiving increased attention as the crystal growth techniques and processing methods advance to the point where the performance predicted by the material characteristics are beginning to be approached. The large conduction band offset between A1GaN/GaN (175,176) possibly in conjunction with the strain-induced piezoelectric effect as alluded to by Smith (177), Bykhovski (178), and Martin (179), enable large measured carrier concentrations to be realizable.

Electronic properties of modulation-doped structures based on the III-nitride semiconductor system have recently been theoretically treated by Stengel et al. (180). The structure considered for this particular study was a wurtzitic $Al_xGa_{1-x}N/GaN$ layered normal MODFET structure. For source and drain contacts, a scheme where the metal contact is deposited on $Al_xGa_{1-x}N$ was considered with the well-justified assumption that contact metal penetrates down to the GaN layer, which hosts the two-dimensional electron gas. Because of conduction band discontinuity, the electrons diffusing from the larger bandgap AlGaN into the smaller bandgap GaN form a triangular quantum well at the $Al_xGa_{1-x}N/GaN$ interface.

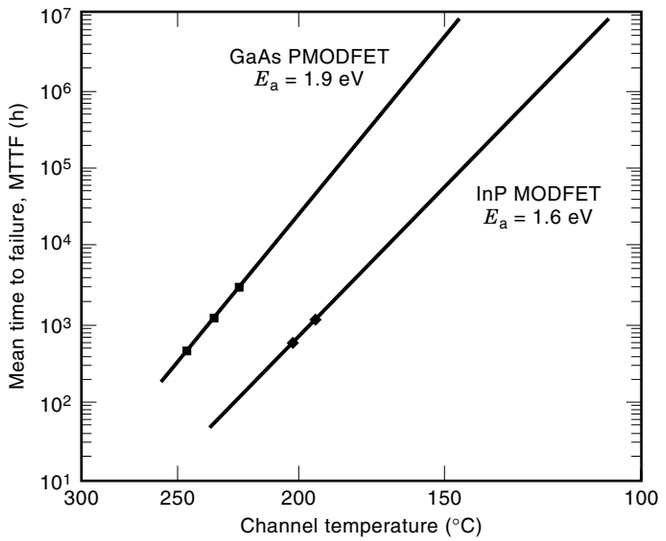

Figure 8. Accelerated lifetime tests for low noise GaAs- and InP-based MODFETs. Activation energies of 1.9 eV and 1.6 eV are apparent for GaAs- and InP-based devices, respectively. Courtesy of P. M. Smith of Lockheed Martin.

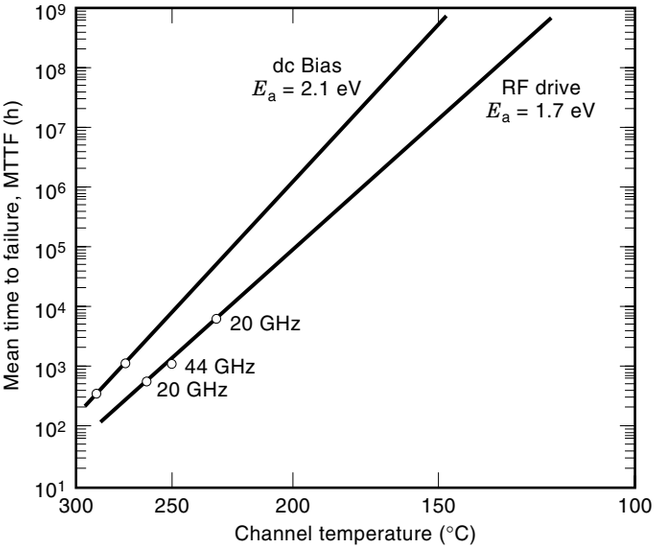

Figure 9. Accelerated lifetime tests for power GaAs-based PMODFETs. Activation energies of 2.1 eV and 1.7 eV are apparent for dc and radio frequency biases, respectively. Courtesy of P. M. Smith of Lockheed Martin.

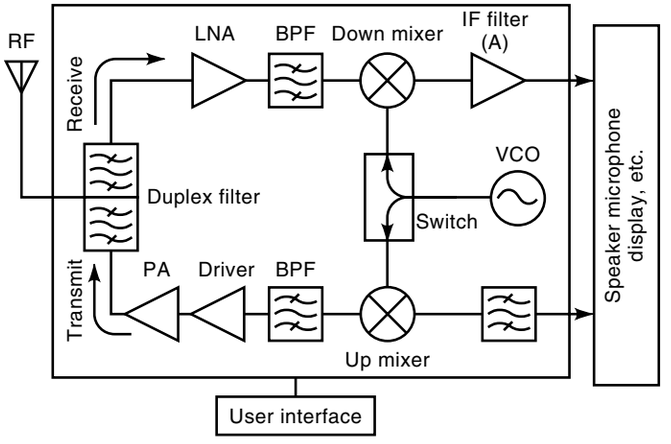

Figure 10. Mobile telephone cell phone radio frequency section with areas of opportunity for compound semiconductor devices shown in bold lines. After M. Golio of Motorola (190).

Band Diagram for AlGaN/GaN MODFETs

For illustrative purposes, the energy band diagram for a normally on (N-ON) MODFET, ignoring polarization effect, as calculated by Stengel et al. (180) are shown in Fig. 11 for AlN mole fraction, $x = 0.25$, donor concentration in AlGaN, $N_d = 10^{19}$ cm^{-3}, and the undoped layer thickness (spacer layer) in AlGaN, $W_{sp} = 20$ Å. Also shown is the electron gas concentration at the heterointerface. For the calculations for N-ON MODFET, a gate bias of $V_G = 0.04$ V, and doped AlGaN layer thickness of $d = 200$ Å were used. The 2DEG does not extend to the AlGaN region due to a high $Al_xGa_{1-x}N$/GaN conduction band discontinuity (more than 500 meV as compared to 142 meV for $Al_xGa_{1-x}As$/GaAs at $x = 0.3$). Because of this, and the fact that the amplitude of electron wave functions extending

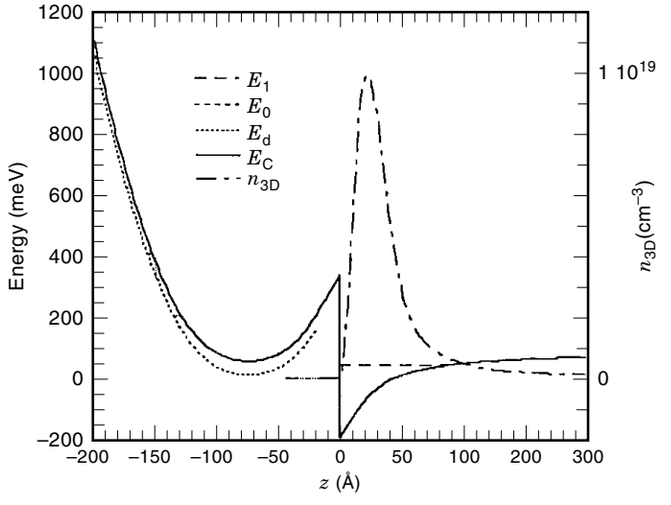

Figure 11. Band diagram for a normally on MODFET. The origin of energy for these band diagrams is the Fermi level. The left side of $z = 0$ line corresponds to the AlGaN region, and the right side to the GaN. The donor level in AlGaN is represented by E_d, the quantum energy levels in GaN by E_0 and E_1. The term E_c represents the conduction band edge in AlGaN and GaN.

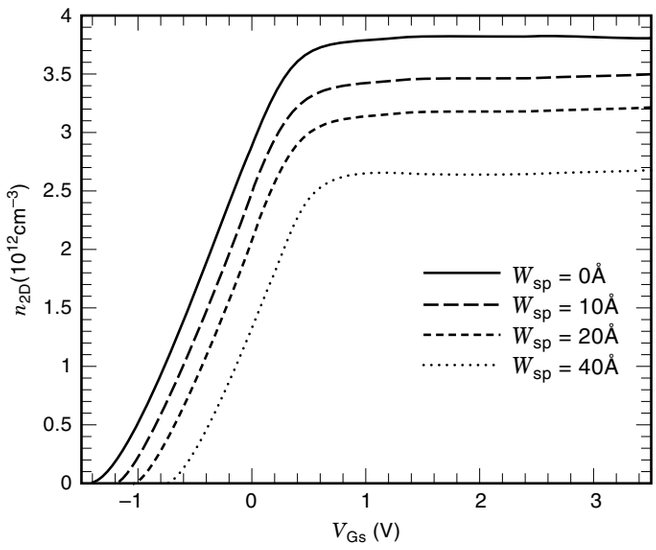

Figure 12. Plots of the 2DEG concentration as a function of the gate-source bias V_G for various values of the spacer layer thickness in $Al_xGa_{1-x}N$.

to the $Al_xGa_{1-x}N$ is very low, a thinner spacer would be needed to achieve the optimal mobility in the 2DEG due to a lower alloy scattering (181). In spite of this, the effect of Coulombic scattering could presumably be opposite, especially because of the lower dielectric constant of GaN and AlGaN which leads to a higher scattering potential. Very precise calculations or experiments would be needed to resolve this matter. For the MODFET of Fig. 11, the quasi-Fermi-level in GaN is far above the lowest energy level, and the peak concentration of electron in the 2DEG is 10^{19} cm^{-3}. Also, some of the donor atoms (for z between -100 Å and -50 Å) are now neutralized, and some electrons start to appear in the $Al_xGa_{1-x}N$ region. Because of these, a further rise of the gate bias causes not only an increase in the donor neutralization, but also an increase in the electron concentration in $Al_xGa_{1-x}N$. However, the 2DEG concentration remains unaltered.

Calculations employing typical parameters (7) for GaN and AlGaN indicate that the peak value of 2DEG concentration for $Al_xGa_{1-x}N$/GaN MODFETs is around 2 to 5×10^{12} cm^{-2}. However, much larger values of n_{2D} have been measured, which is most likely due to ionization and redistribution of shallow charges caused by the piezoelectric effect. Figure 12 shows n_{2D} versus V_G plots for various spacer thicknesses. As long as the unintentional doping level in the spacer layer is low, the effects of varying the AlN mole fraction, x, and W_{sp} on n_{2D} are essentially equivalent, because at the end of the spacer layer the value of $E_c - E_F$ is very close to E_c (interface) $- W_{sp}(dE_c/dz)$ (interface). Experimental data describing the effect of the spacer layer thickness on the mobility of the electrons in the 2DEG are needed to evaluate optimized values for this spacer layer. One may, however, predict that these values for the $Al_xGa_{1-x}N$/GaN system would be smaller than those for the $Al_xGa_{1-x}As$/GaAs system, because the $Al_xGa_{1-x}N$/GaN system provides a deeper confinement, and the wave function of the 2DEG over a shorter range in $Al_xGa_{1-x}N$ is nonzero.

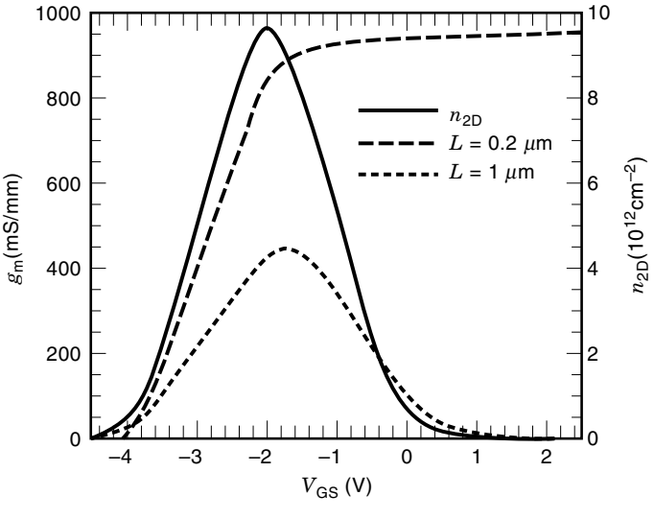

Figure 13. Variation of the transconductance g_m of MODFETs as a function of the gate-source bias V_{GS} at the optimal value of the drain-source bias V_{DS} (optimum value of V_{DS} is defined to be the value at which transconductance peak reaches its maximum value) for each of the plot, for various values of the channel length, L, values of 1 and 0.2 μm. The parameters used for the 2DEG are d = 130 Å, N_d = 10^{19} cm^{-3}, W_{sp} = 20 Å, x = 0.25, and E_d = 45 meV.

Stengel et al. (180) calculated the variation of transconductance with gate bias for various channel lengths as shown in Fig. 13. When the channel length was decreased from 1 to 0.2 μm, the peak transconductance increased from 420 to above 900 mS/mm. These very large values of transconductances are made possible when the values of both V_G and V_D were chosen to be small to avert the velocity saturation of the carriers. This was indeed very encouraging considering the fact that, for all practical purposes, MODFETs with reduced channel length are very desirable, and have lower leakage current at the operating point. Notably the peak transconductance of these MODFETs is obtained for lower gate biases.

The drain current can also be obtained from the model of Stengel et al. (180) as shown in Fig. 14. For a relatively relaxed geometry device, L = 2 μm. The pinch-off depends on the relative values of the gate-source and the drain-source voltages. Although the gate-source voltage tends to keep channel electrons stuck to the $Al_xGa_{1-x}N$/GaN surface, the drain-source voltage tends to drag them away to the drain. This competition between the gate-source and the drain-source voltage becomes increasingly imbalanced as the difference between them increases. Consequently, the length of the pinch-off region and hence the leakage become larger when the drain-source voltage becomes much larger than the gate-source voltage. This causes a slight decrease in drain saturation current with increasing drain-source voltage V_D.

Performance of GaN MODFETs

As stated earlier, modulation doped field effect transistors utilize a two-dimensional carrier gas confined at an interface between two layers with an interfacial energy barrier such as AlGaAs/GaAs and AlGaAs/InGaAs. A GaN MODFET taking advantage of the background donors in the AlGaN layer, which is not controllable to say the least, was reported. Congruent with the early stages of development and the defect laden nature of the early GaN and AlGaN layers, the MODFETs exhibited a low-resistance and a high-resistance state before and after the application of a high drain voltage (20 V). As in the case of GaAs/AlGaAs MODFETs, hot electron trapping in the larger bandgap material at the drain-side of the gate is primarily responsible for the current collapse. The negative electron charge accumulated due to this trapping causes a significant depletion of the channel layer, more probably a pinch-off, leading to a drastic reduction of the channel conductance and the decrease of the drain current. This continues to be effective until the drain-source bias is substantially increased leading to a space-charge injection and giving rise to an increased drain-source current.

Single Heterostructures. The dc drain characteristics of MODFETs with a gate length of 2 μm, gate width of 40 μm, and the drain-source separation of 4 μm are presented in Fig. 15. The maximum drain-source current I_{DS} corresponding to a drain-source voltage V_{DS} = 3 V and strong forward gate bias (~3 V) is approximately 500 mA/mm. The linear characteristics of the I–V curves demonstrate that the source and drain contacts of the MODFETs are highly ohmic. Good ohmic characteristics of the source and drain contacts probably led the present MODFETs to exhibit a substantial higher drain-source current. These MODFET with 2 μm gate lengths have room temperature extrinsic transconductances of approximately g_{em} = 185 mS/mm. The peak value in the g_{em} versus V_{GS} curve occurs at the gate-source voltage V_{GS} = 1 V, and the drain-source voltage V_{DS} = 4 V. With increase in V_{GS}, there occurs higher accumulation of electrons in the active channel, and a higher variation of I_{DS} with respect to V_{GS} at a certain value of V_{DS}. Consequently, the transconductance increases with V_{GS}. However, when V_{GS} exceeds a certain limit (viz. 4 V), the accumulation of electrons in the active channel no longer increases at the previous rate with increasing V_{GS}, and the voltage drop in the extrinsic circuit increases. As a result, the transconductance decreases with V_{GS}. The drain-source

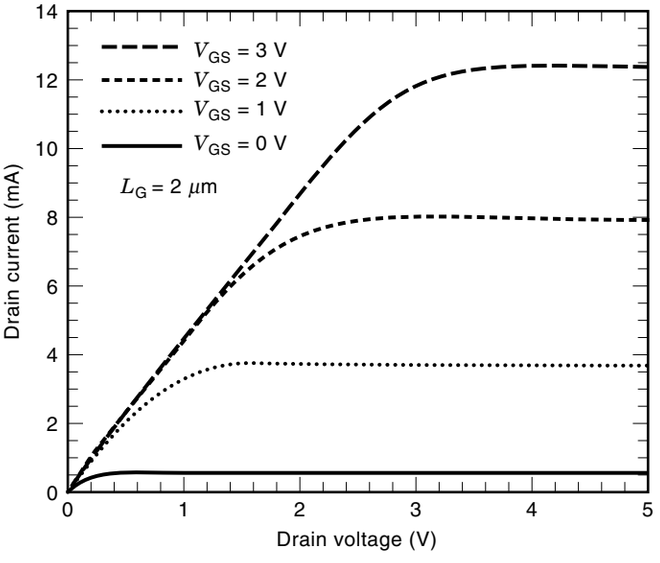

Figure 14. Calculated drain-source current I_{DS} for AlGaN/GaN MODFETs under various gate-source bias conditions (0, 1, 2, and 3 V).

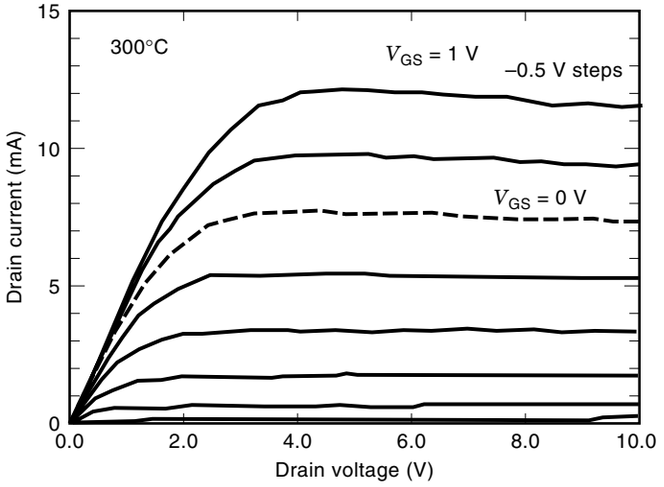

Figure 15. Direct current drain characteristics of a single heterostructure MODFET with a gate length of 2 μm, gate width of 40 μm, and drain-source separation of 4 μm.

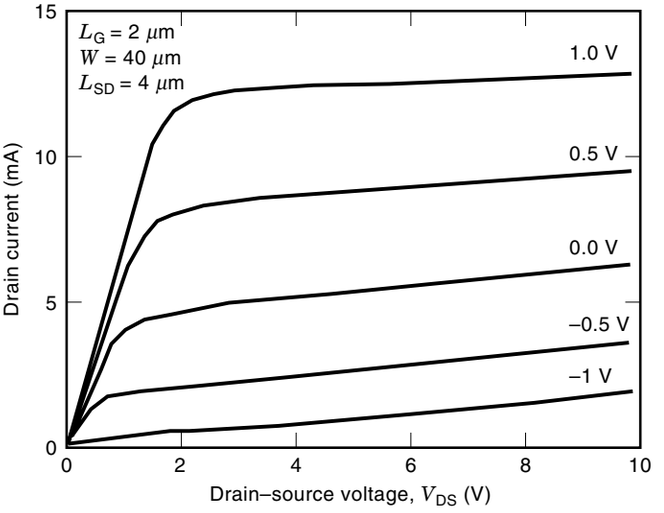

Figure 16. Direct current drain characteristics at room temperature of a DHCMODFET with gate a length of 1.5 μm, gate width of 40 μm, and drain source separation of 3 μm.

breakdown voltages are in the range of 100 V per 1 μm spacing, the exact value depending on the layer design and quality of the layered structure.

Double Heterostructures. To increase the current capability of MODFETs, multi-2DEG structures are employed. In this case, the GaN layer is straddled by two doped AlGaN that donate electrons to the channel increasing the number of electron available for current conduction. By Hall-effect measurement, the mobility and sheet carriers density in the two-dimensional electron gas (2DEG) were approximately 304 $cm^2/V \cdot s^{-1}$ and 3.7×10^{13} cm^{-2}, respectively, at room temperature. The sheet carrier concentration may have been affected by the piezoelectric effect. A number of double heterochannel MODFETs (DHCMODFETs) with gate lengths of 1.5 μm to 1.75 μm and a gate width of 40 μm have been reported. The dc drain characteristics at room temperature of the DHCMODFET device with gate length of 1.5 μm, gate width of 40 μm, and drain source separation of 3 μm are presented in Fig. 16. The maximum drain source current I_{DS} corresponding to a drain-source voltage V_{DS} = 7 V, V_{GS} = 3.5 V is approximately 1100 mA/mm, which is important as in high-power devices the input is momentarily forward biased. The HDCMODFET has a room temperature extrinsic transconductance g_m = 270 mS/mm. The value of the total resistance R_T extracted from the linear region of the I–V curves is 4 Ω/mm. Near pinch-off, the drain breakdown voltage is approximately 80 V, indicating the excellent power potential of the device. The I–V characteristics of the HDCMODFET at 300°C is shown in Fig. 3. These measurements were made in a nitrogen pressurized container to avoid possible oxidation of the contacts and probes. The maximum drain-source current and extrinsic transconductance of the DHCMODFET are 500 mA/mm and 120 mS/mm, respectively. These devices maintain reasonable output characteristics at temperatures as high as 500°C with maximum drain current and extrinsic transconductance values of 380 mA/mm and 70 mS/mm, respectively. Cooling down to room temperature restored the characteristics that are indicative of the robustness of this material system and metallization employed.

Interface Roughness

The mobility in AlGaN/GaN structures ranges from approximately 500 cm^2/Vs to over 2000 cm^2/Vs which is higher than what can be obtained in bulk GaN, but may still be lower than that eventually expected. The charge state of defects in GaN and AlGaN are near the interface, geometrical effects such as interface roughness may not be negligible. The AFM measurements indicate the presence of a three-dimensional roughness on the surface of these samples. This roughness combined with polarization effects is likely to have a strong effect also on the mobility because it reduces the effective electric field on the electrons and the effective speed of electrons across the channel. As may be noted from Fig. 17 albeit somewhat exaggerated for the purpose of making the point, the effective field on the electrons in the channel is $E_{ch}\cos(\theta)$, and the effective velocity $V_{QW}\cos(\theta)$. The extent of the mobility reduction due to this effect may be calculated by taking an average over the surface, which would be difficult to perform analytically. However, for a qualitative understanding of this, we may consider the mean values of the measured roughness, which would yield $\theta = 60°$ and the effective value of the mobility μ 0.25 times the original value, which may be considered to be a significant reduction in the mobility.

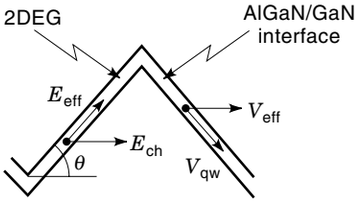

Figure 17. Schematic diagram showing three-dimensional surface and the reduction in electric field and velocity of the carriers in the channel.

The value of the total resistance, $R_T = R_s + R_{ch} + R_D$, where R_s is the source area resistance, R_{ch} is the channel area resistance, and R_D is the drain area resistance, is extracted from the linear region of the I–V curves after accounting for the leakage from the gate. Using these values, we may calculate the intrinsic transconductance as a function of temperature. Assuming a long channel operation, it would allow us to extract the μn_s product of the mobility μ and the sheet carrier concentration n_s from the intrinsic transconductance values. The same product μn_s may be extracted also from the values for R_T by assuming that the drain and source resistances are negligible. The analysis shows that the ohmic contacts do not really play any significant role in decreasing the transconductance at all temperatures. Therefore, the increase in these resistances should be mostly due to a decrease in the mobility-sheet carrier density product. Probably because of higher ionization of dopant atoms in n-AlGaN, the 2DEG concentration increases slowly with increasing temperature. Because of this, the observed decrease in transconductance and increase in the channel resistance is actually due to the decrease in the low field mobility and the saturation velocity. The mobility degradation caused by three-dimensional surface roughness is not expected to have a temperature dependence. Therefore, the decrease in transconductance by an increase in temperature may be an intrinsic mechanism, most likely by polar optical phonon scattering which is very effective at high temperatures.

Radio Frequency Results

MODFETs have progressed to a point where microwave measurements have been performed on a variety of devices with gate length as wide as 2 μm and as narrow as 0.2 μm. A typical MODFET structure with 2 μm gate lengths have been tested at small-signal S-parameter measurements were performed at bias conditions used for the power measurements, that is, 15 V, −2.5 V, and 20 mA for the drain voltage, gate voltage, and drain current. Short circuited current gain, maximum available power gain and the unilateral gain calculated from the small-signal S-parameters are shown in Fig. 18.

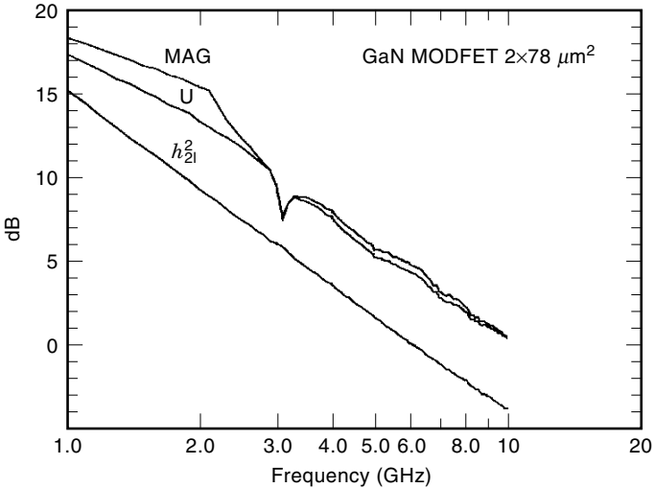

Figure 18. Short circuited current gain, maximum available gain, and unilateral gain as a function of frequency under bias conditions of V_{DS} = 15 V and V_{GS} = −2.5 V. The I_{DS} at this bias was approximately 20 mA which corresponds to 260 mA/mm.

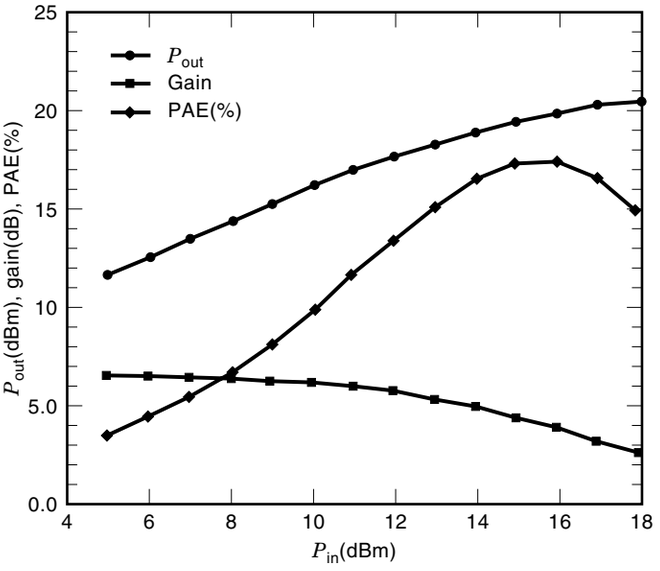

Figure 19. CW output power, power gain, and the power added efficiency vs. input power level.

Short-circuited current gain, maximum available gain, and unilateral gain as a function of frequency under bias conditions of V_{DS} = 15 V and V_{GS} = −2.5 V are presented. The I_{DS} at this bias was approximately 20 mA, which corresponds to 260 mA/mm. The unity current gain cut-off frequency (f_t) and maximum frequency of oscillation were 6 GHz and 11 GHz, respectively, at both 15 and 30 V bias. Values in excess of 50 GHz and 100 GHz have been reported for short channel devices respectively, i.e., approximately 0.2 μm. The CW microwave power measurement results are presented in Fig. 19. The measurements were taken at 4 GHz with the input power swept from 5 dBm to 18 dBm in 14 steps. The input and output matches, which were used during the power sweep, were determined by iterating between source and load pulls. The output match was selected to optimize the output power, and the input match was selected to maximize the delivered power. The devices were biased to V_{DS} = 15 V and V_{GS} = −2.5 V. The I_{ds} at this bias was approximately 20 mA, which corresponds to 260 mA/mm. From the figure, we see that the devices exhibited 6 dB gain for various input levels. The maximum output power was 20.6 dBm, and the peak PAE was 17.5%. This corresponds to a normalized output power density of 1.5 W/mm. Improved devices with shorter gate lengths have demonstrated normalized power levels of approximately 2.56 W/mm at X band, extrapolated from small gate width devices that sidesteps the thermal limitations imposed by sapphire substrates (174).

Inclusion of thermal limitations leads to results shown in Fig. 20 for devices that compete in the high-power device arena (8). Because new device developments do in general compete with existing and alternative technologies, a brief account of competing technologies for power arena will be given below. The silicon MESFET analytical curve, modeled for its simplicity, is slightly above the SiC analytical curve and indicates a maximum power density of 0.35 W/mm at V_{dS} = 7 V, which is slightly lower than 0.39 W/mm. Since silicon radio frequency (RF) MESFETs are unavailable, commercial silicon

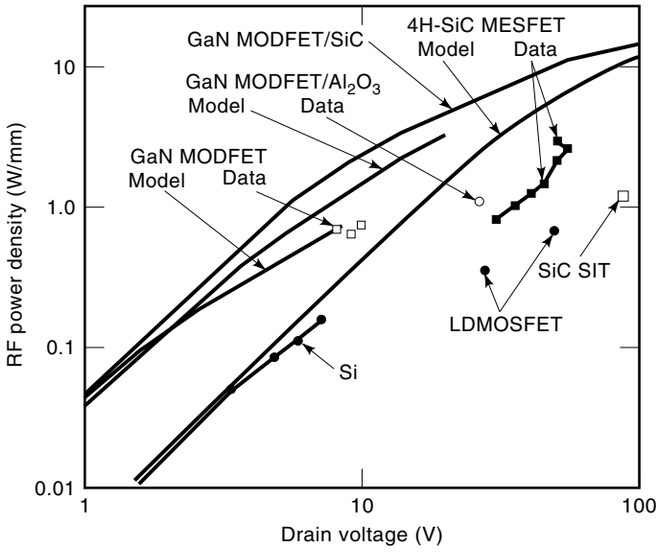

Figure 20. Simulated and experimental RF power density data for Si, GaAs, SiC, and GaN FETs. After C. Weitzel (8).

RF MOSFET results have been used for comparison instead. At low voltages the silicon MOSFET data parallel the analytical curve, suggesting the validity of the functional dependence of power density on drain voltage. Also shown are two higher power density data points 0.4 W/mm, V_{dS} = 28 V and 0.87 W/mm, V_{dS} = 48 V. These higher power densities were obtained with specially designed RF power MOSFETs that incorporate lightly doped drains and field plates that significantly increase the breakdown voltage. The GaAs analytical curve shows the highest power density of all of the devices at the lowest voltages, primarily because of the higher electron mobility of GaAs. However, the low breakdown field limits the GaAs MESFETs drain voltage to approximately 8 V and power density to 0.63 W/mm including thermal effects. Typical commercially available GaAs MESFET power densities are below 1 W/mm. However, high-performance GaAs FETs with more complex device cross sections have achieved power densities as high as 1.4 W/mm at 18 V. The SiC MESFET has a calculated maximum power densities at 100 V with and without thermal effects being taken into account of 7.96 W/mm and 9.7 W/mm, respectively. The highest demonstrated continuous wave power density 3.3 W/mm (V_{ds} = 50 V) for a SiC MESFET (182) is also shown for comparison. Additional SiC data again illustrates the functional dependence of power density on drain voltage. The GaN analytical results are highly dependent on the thermal conductivity of the substrate. With a sapphire substrate, the device is severely thermally limited to 2.24 W/mm at 30 V with a resulting channel temperature over 400°C. However with a SiC substrate the analysis predicts that a GaN HFET could achieve 15.5 W/mm at 100 V with a channel temperature of approximately 300°C. To date, the highest power density achieved for a GaN HFET is 2.56 W/mm at 25 V (174), which is also shown in Fig. 20. This experimental data point is actually higher than the simulated result because of the very small size, 100 μm device width, of the experimental device.

The GaN results of analytical models are highly dependent on the thermal conductivity of the substrate. With a sapphire substrate, the device is severely thermally limited to 2.24 W/mm at 30 V with a resulting channel temperature over 400°C. However with a SiC substrate, the analysis predicts that a GaN MODFET could achieve 15.5 W/mm at 100 V while keeping the channel temperature at approximately 300°C (8).

Piezoelectric Effect

III-V nitride semiconductors possess highly pronounced piezoelectric properties. As such, any strain present in these crystals causes a distortion in atomic orbitals which leads to large polarization effects and must be taken into consideration, particularly in dealing with strained heterostructures. Piezoelectric effect has recently become the focus of attention with many claims including achievement of MODFET channels with no intentional doping anywhere in the entire heterostructure. It should be made clear that the resultant polarization field causes to redistribute the free and weakly bound charge which could be mistakenly interpreted as bonus carriers (7). The treatment must also include the charge redistribution in the presence of metal semiconductor contacts such as gate Schottky barriers. In positive strain (tensile strain), the direction of the polarization is from the anion, B face, to the cation. A face, sites. As can be easily imagined, if the growing nitride surface contains both polarities, the direction of the polarization vector would follow suit and would point in an up direction and down direction depending on the spot. The polarity of the growing surface is somewhat controversial at the time of writing, which is in part fueled by the lack of commercial GaN substrates. It appears that low-quality films may contain both polarities. Borrowing from the II–VI wide bandgap semiconductor field that the anion surface is more conducive to high-quality layer growth with uniform polarity, one could predict that high-quality GaN films can be grown on the N face of GaN (0001) in which case the strain polarization vector would be toward the surface under compressive strain. If the strain is tensile, then the polarization vector would be from the surface toward the substrate.

$Si_{1-x}Ge_x$ MODFET STRUCTURES

The advent of high quality SiGe layers on silicon substrates has paved the way to the exploration and exploitation of heterostructure devices in a silicon environment. Capitalizing on the favorable band discontinuities outlined by Abstreiter et al. (183), Ismail et al. (184) reported encouraging values of electron mobility in a modulation doped strained $Si_{0.7}Ge_{0.3}$ channel surrounded by $Si_{0.86}Ge_{0.14}$ donor layers. The cross-sectional view of this particular structure imbedded into an FET structure is shown in Fig. 21. The electron mobilities measured were 1800 $cm^2/V \cdot s^{-1}$ 9000 $cm^2/V \cdot s^{-1}$ and 19,000 $cm^2/V \cdot s^{-1}$ at room temperature, 77 K and 1.4 K, respectively. The corresponding sheet electron densities are 1.2×10^{12} cm^{-2}, 8.3×10^{11} cm^{-2}, and 7.5×10^{11} cm^{-2}, respectively. The layers were grown using UHV/CVD, which offered a very low background impurity concentration in the intrinsic layers. As will be briefly mentioned below, the layered structures of this kind have been exploited for high transconductance modulation-doped FETs. Mii et al. (185) used a SiGe layer graded from 0% to 30% followed by a $Si_{0.7}Ge_{0.3}$ buffer layer, both of which were relaxed. A strained silicon channel was grown on the $Si_{0.7}Ge_{0.3}$ buffer and capped with a doped $Si_{0.7}Ge_{0.3}$ layer. A

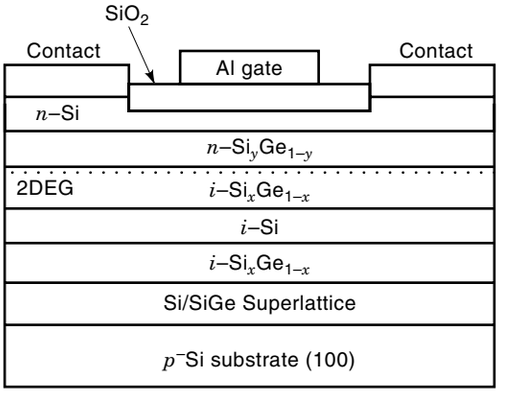

Figure 21. Schematic cross-sectional diagram of a strained layer SiGe/Si structure in conjunction with a MODFET device.

maximum Hall mobility at 4 K of 125,000 $cm^2/V \cdot s^{-1}$ has been obtained. The sheet electron concentrations that the heterostructure can sustain were 1.2×10^{12} at 300 K, to 7.8×10^{11} at 77 K and below. Informal results indicate that mobilities close to 300,000 $cm^2/V \cdot s^{-1}$ can be obtained, which compares with the approximate 30,000 $cm^2/V \cdot s^{-1}$ attainable in the Si/SiO_2 system. MODFETs with current gain cut off and maximum oscillation frequency of about 32 GHz and 40 GHz, respectively, have been reported in 0.5 μm gate length devices (186). High-quality $Si/Si_{1-x}Ge_x/Si$ p-type modulation-doped double heterostructures with $x = 0.12$ and $x = 0.15$ have been grown using UHV/CVD by Wang et al. (187). In this heterostructure, hole mobilities as high as 3700 $cm^2/V \cdot s^{-1}$ at 14 K have been obtained with $x = 0.12$ and a silicon spacer of 60 Å for a sheet carrier concentration of $\sim 8 \times 10^{11}$ cm^{-2}. The values of hole mobility is roughly an order of magnitude higher than the highest values reported in p-type silicon inversion layers and are most probably limited by remote ionized impurity scattering from the heavily doped silicon layer, and/or the interfacial quality at the Si/SiGe heterointerface. Murakami et al. (188) utilized an MBE-grown modulation-doped heterostructure where the strain at the heterointerface (p-$Si_{0.5}Ge_{0.5}$/Ge layers) is controlled by the silicon composition $(1 - x)$ of the $Si_{1-x}Ge_x$ buffer layer. When the silicon composition is 25%, a hole mobility of 9000 $cm^2/V \cdot s^{-1}$ at LN_2 temperature was achieved. Very recently Arafa et al. (189) have reported p-channel Si/SiGe MODFETs with extrinsic transconductances of 150 mS/mm and 250 mS/mm for 1 μm and 0.25 μm gate devices, respectively. As the gate length was reduced from 1 μm to 0.25 μm; the current gain cut-off frequency increased from 5 GHz to 40 GHz. Preliminary devices with 0.1 μm gate lengths appear to show current gain cut-off frequencies of approximately 70 GHz.

CONCLUSION

In less than two decades, the MODFET has evolved dramatically, from an interesting research innovation to an extremely formidable and yet practical device with numerous areas of applications including wireless, low-power communications, direct satellite broadcasting systems, millimeter-wave systems, and digital electronic systems. As is evident from the tables and figures presented in this article the MODFET has progressed to the point where the performance barriers thought to be insurmountable by three-terminal devices not long ago have been overcome with amazing dispatch. Although the GaAs channel MODFETs formed the genesis of this unique device, the pseudomorphic MODFET with InGaAs channels has become the device of choice. Strained channel MODFETs with 80% InAs in their channel layers have shown current gain cut-off frequencies above 300 GHz. Again strained channel MODFETs with 60% InAs in their channel exhibited measured power gain at 140 GHz. The data clearly indicate that the pseudomorphic MODFET has demonstrated increasingly enhanced electronic properties without compromising the breakdown voltage afforded by GaAs. Strained channel InGaAs MODFETs on GaAs substrates currently hold the power record. In concert with the gain and power performance, strained layer MODFETs on GaAs have shown a noise performance of 1.4 dB in the 90 GHz range. Despite the enhanced hole mobilities measured in compressively strained InGaAs, the p-channel MODFETs do not appear to have gained remarkably better performances. The bulklike properties away from the zone center and band mixing, which is very likely at high electric fields, are thought to be responsible for such a lack of enhanced performance.

Due to their large bandgaps, large high-field electron velocity, large breakdown fields, large thermal conductivity, and robustness, wide bandgap nitride semiconductors have gained considerable attention. The ensuing materials developments paved the way to AIGaN/GaN MODFETs with superior power performance in that when normalized from small devices to 1 mm of gate periphery, the X band CW power levels of approximately 2.56 W/mm have been obtained at drain biases of around 25 V. The current and power gain cut-off frequencies for devices having about 0.2 to 0.25 μm gate lengths are approximately 50 and 100 GHz, respectively. Drain breakdown voltages in the vicinity of 100 V/μm gate to drain spacing have been reported, which is very essential for power applications.

Relatively recent introduction of SiGe alloys propelled the silicon technology into the realm of the heterojunction world. The new Si/SiGe system has provided a laboratory in which to study quantum phenomena and has led to an exploration into commercially important devices such as MODFETs. SiGe channel MODFETs with 0.2-μm gate lengths challenge the 100 GHz cut-off frequency benchmark. More recently, the MODFET phenomenon has expanded to include the emerging wide bandgap GaN/AIGaN semiconductor system which already is beginning to demonstrate high frequency (current and power gain cut-off frequencies of about 50 and 100 GHz, respectively) and high-power operation.

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