## LITHOGRAPHY

The explosive growth of the semiconductor industry is spurred on by the relentless drive toward the miniaturization of electronic devices. Year after year, the size of the transistors, resistors, and capacitors that form the ubiquitous integrated circuits is made smaller. At the same time the area available for making the circuit is increased, so that the final circuit will contain more devices and hence will be able to process a larger amount of information: Because of miniaturization, microprocessors become more powerful and memory chips become larger. Central to the miniaturization process is a technique called *lithography*. For a detailed and up-to-date discussion on the various techniques used in lithography, see, for instance, Ref. 1.

Lithography is an imaging process; that is, it is used to form and imprint an image on an electronic device during its fabrication. An electronic semiconductor device functions by way of the nonuniform electric fields built into the material; these fields are established by suitably modifying the silicon by selectively doping adjacent areas of the crystal. An integrated circuit is thus formed by a sequence of several hundred steps, beginning with a pristine silicon wafer that is progressively modified by adding, removing, and modifying materials. Thus, an "electrically active" device is made by controlling the spatial distribution of materials such as dopants atoms, oxide insulating layers, and metal connectors.

Controlled material topologies are obtained by the combination of batch processing and of lithography. Batch processes are nonselective, and they affect uniformly the areas exposed to the particular process. Thus, a semiconductor structure built with a sequence of processes appears as a layered structure (planar process). Spatial differentiation is obtained either by selectively removing (etching away) part of the current topmost layer or by preetching the topmost layer before exposing the wafer to the next processing step. For instance, a local oxidation process is based on first depositing a uniform silicon nitride film 50 nm to 100 nm thick on the wafer and then creating some unprotected areas in the film by etching the nitride away. Thus, the surface of the wafer will have regions of nitride and of bare silicon. When the wafer is put in an oxidation furnace, only the areas where the silicon is exposed will oxidize, thus leading to isolated islands of nitride inlaid in the oxide film. A subsequent etch can be used to remove the nitride, thus leaving islands of bare silicon wafer where transistors can be fabricated with further processing; these transistors will be isolated by the "sea" of oxide.

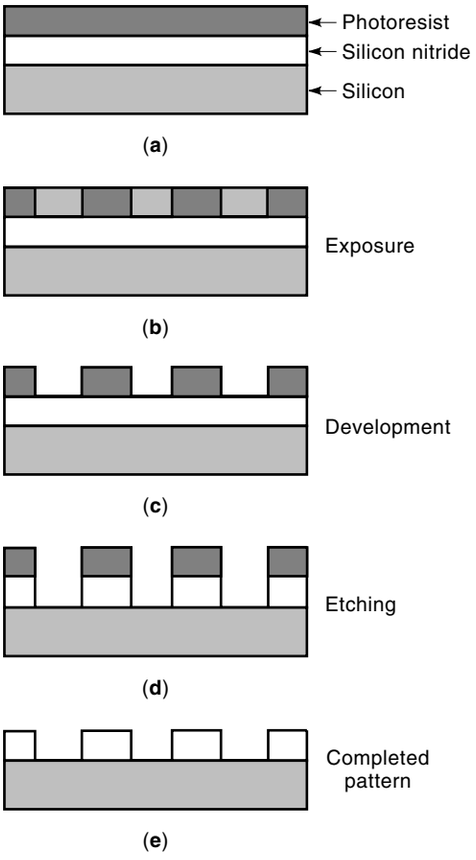


**Figure 1.** Lithographic process.

The process of creating the "islands" of nitride is based on lithography. As shown in Fig. 1(a), a photosensitive polymer is coated on the surface of the wafer to a thickness of 400 nm to 1000 nm. This material, called *photoresist,* changes chemical properties where it is exposed to actinic (ultraviolet) or other ionizing radiation. Thus, after projecting an image on the resist [exposure, Fig. 1(b)] we can selectively remove the exposed fraction [development, Fig. 1(c)], making the underlying layer available for subsequent processing. Finally, the remaining photoresist is removed, and the *patterned* wafer is ready for the next step. We note that resists are temporary layers applied onto the workpiece for imaging purposes only. After pattern transferring onto the active layer (insulator or semiconductor material), the resist is removed (stripped) in a solvent or a water solution. The most common resists are organic solutions applied on the workpiece (wafer) by spinning and dried by baking at a suitable temperature, referred to as "prebake temperature." The thickness of the dried resist layer depends largely on the concentration of solids in the solution and on the spinning speed.

In general, resists undergo chemical changes when exposed to the appropriate radiation, which renders them soluble (positive resists) or insoluble (negative resists) in the exposed area relative to the unexposed area. Many different formulations exist, so that the detailed photochemistry can be quite complex. Most resists, with some recent exceptions, are developed in a solution which could be a mixture of organic solvents or an inorganic water solution. Measures of quality in resists include the following:

- Sensitivity, which refers to the minimum incident exposure dose required to adequately differentiate between exposed and unexposed regions.
- Resolution, referring to the ability of the resist to reproduce faithfully the size of the image that the lithographic tool can expose on it.
- Compatibility with the pattern transfer process, which includes resist adhesion to the substrate, temperature stability resistance to wet or dry etching processes, and so on.

For a resist to be acceptable in a manufacturing process, it must satisfy all of these conditions. That is, its sensitivity must be adequate so that it does not impose a throughput limitation on the lithographic tool. Its resolution must also exceed that of the lithographic tool and it must be compatible with all the manufacturing processes.

A typical circuit pattern is shown in Fig. 2. The whole surface of the integrated circuit (of the order of $25 \times 25$ mm$^2$ for a modern circuit) is covered with these patterns. The finest dimension of the device (for instance, the length of the gate) is called the *critical dimension* (CD). This is a key parameter in the performance of the circuit.

In Fig. 3 we show the evolution of the silicon-based metal oxide semiconductor (MOS) electronic devices as predicted by the Semiconductor Industry Association (SIA). These devices are the base of all modern electronics, with the exception of photonics and some high-speed communication systems. In

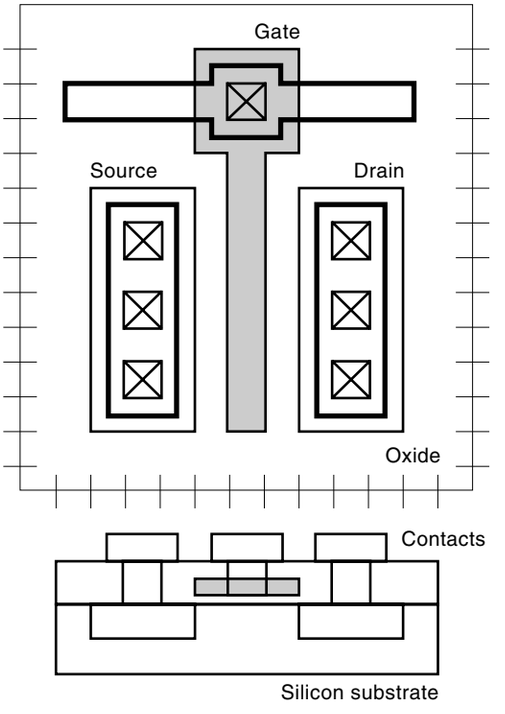


**Figure 2.** Typical layout of a MOS transistor. The design is laid out in a multiple of basic unit $\lambda$, equal to the CD. The various levels must overlay precisely.

the year 2001, devices with CD as small as 0.18 $\mu$m are expected to have entered large-scale manufacturing. The decrease in the device dimensions is expected to continue unabated until at least 50 nm, and very likely to 30 nm. At each generation the cost per bit has continuously decreased.

In parallel to the decrease in dimensions the physical size of the circuits (the chip size) increases, so that at each generation the fourfold increase of functionality (for instance, from the 64 Mbit to the 256 Mbit DRAM) is due to both factors in equal measure. Economy of scale dictates the use of large silicon wafers, increasing from the current 200 mm to 300 mm in the very near future. It is impossible to form the high-resolution pattern on a wafer that size in a single imaging step; full wafer lithography was abandoned in the early 1980s in favor of step-and-repeat systems, where only a field is patterned at a time.

Optical lithography has made the electronic revolution possible. At the simplest level, a "mask" is projected by an optical system on the wafer, and the image is recorded in the photoresist material. The mask is a glass or quartz slide ($100 \times 100$ or $150 \times 150$ mm$^2$) with the pattern to be printed etched in a thin film of chromium (400 Å to 500 Å). The pattern is four to five times the final size to be printed, so that the lithographic camera reduces the size of the image; in essence, this is the same as using a photographic microscope in reverse—that is, putting an exposed slide at the film position and imaging it, demagnified, on the sample.

High-volume lithography, as used in manufacturing, relies on the use of the *masks* whose image is projected on the wafer. To understand the importance of masks in lithography, we have to consider the amount of information that is typically contained in a lithographic pattern. In a field of $25 \times 32 = 800$ mm$^2$ there are approximately $10^{12}$ pixels of size 25 nm ($\frac{1}{10}$ of a 250 nm critical dimension). This is a huge amount of information (1 terabit). Using lithographic (or photographic) methods, this information is printed in 1 s or less with a flash of ultraviolet (UV) light or other radiation through the mask. With a system writing the field only a few pixels at a time, the writing time becomes quickly prohibitively long. Hence, today all manufacturing lithographies are based on the use of masks.

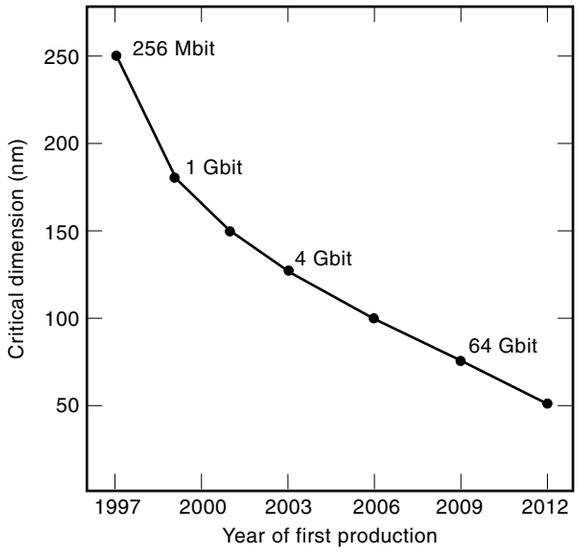


**Figure 3.** SIA roadmap for MOS devices system. This roadmap is published by the SIA and can be found on-line at http://www.sematech.org.

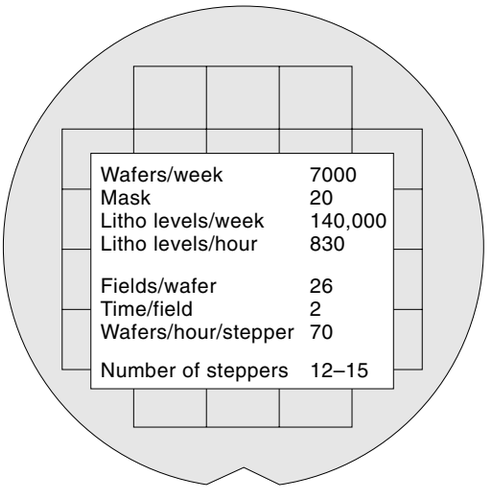


**Figure 4.** Lithographic throughput analysis.

Masks are fabricated using electron-beam or laser-based pattern generators, where a fine beam of radiation (electrons or UV) is rastered over the mask, precoated with photoresist. Writing a complex mask may take several hours. After exposure, the mask is developed and the chrome is etched, leaving the final pattern of (absorbing) metal to be projected on the wafer.

From a manufacturing point of view, lithography must be capable of imaging the required pattern on the wafer within the tolerances required by the device performances. These tolerances are expressed as a fraction of the CD, typically 10% for the accuracy in dimension (i.e., 25 nm for a nominal 250 nm gate) and 30% for the positioning accuracy. Since an actual circuit is built using as many as 20 to 25 lithographic steps, the need for accurate registration between the layers is readily apparent. In addition to the requirements of pattern accuracy, the technology must also be capable of large volume manufacturing—that is, of high volume throughput. Figure 4 illustrates a typical lithographic case, that of a large DRAM manufacturing plant that can produce upward of 7000 wafers a week. Each field may accommodate two circuits (chips).

## LITHOGRAPHIC TECHNOLOGIES

There are several lithographic techniques, based on different methods of defining an image. At first, UV light from a mercury lamp was used to define the patterns; today, shorter wavelengths from excimer lasers are used for advanced manufacturing. Fine beams of electrons and ions are also used. Table 1 lists the main techniques in use today.

By far the most commonly used technique is UV lithography, often simply called *optical lithography* (OL). Manufacturing is currently dominated by it, with steppers operating at the mercury I-line (365 nm) for the largest fraction of production, while deep UV (248 nm) is used for the most advanced levels. Deep ultraviolet (DUV) tools are much more expensive

**Table 1. Comparison of Lithographic Techniques Capabilities as of 1998**

| Technology | Description | Wavelength (Energy) | Application | Volume | Status |
|---|---|---|---|---|---|
| Optical | I-line | 365 nm | 350 nm | High | Production |
| | DUV I | 248 nm | 250–180 nm | High | Advanced production |
| | DUV II | 193 nm | 150 nm | High | Development |
| | EUV | 13 nm | 100–80 nm | High | Research |
| X-ray | Proximity | 1 nm | 150–50 nm | High | Development |
| E-beam | Focused | 30–100 kV | 500–50 | Low | Production |
| | Cell Projection | 50–100 kV | 100 nm | Medium | Development |
| | SCALPEL | 100 kV | 150–100 nm | Medium | Research |
| Ion beam | Focused | 30–100 kV | 500–50 | Low | Production |
| | Projection | 100 kV | 500–50 | Medium | Research |

than I-line and have a lower throughput; thus, a plant will deploy both types of tools for noncritical (I-line) and critical (DUV) levels.

The evolution of integrated circuits (ICs)—that is, the doubling of functionality every 18 months—mandates the deployment of successive generations of lithographic technologies. A manufacturing plant is built with the expectation to last for two generations of devices—that is, approximately 6 years. After that time it is not economically effective to completely refit and update the processing line, and new factories are built and brought in line. Hence a lithographic technology is expected to "live" at least two generations, and this expectation clocks the development of new steppers, sources, and resist materials.

The cost of manufacturing integrated circuits has been analyzed by many authors (1); exact information is not available because of its sensitive nature, but most estimates give to lithography about 40% of the cost of fabricating a finished chip. Interestingly enough, the high initial costs of the steppers (a modern tool costs easily upward of $10 million) is not the main contributor; rather, masks and photoresist (i.e., consumable materials) carry the largest fraction of lithographic costs. Lithography costs keep rising with the development of more complicated steppers, masks, and processes, and the trend is not expected to reverse itself soon. Indeed, it is arguable that the real limit to miniaturization will come not from physical or process limits but rather from the economics of manufacturing.

Optical lithography will not be able to support manufacturing to the smallest projected dimensions, and alternative technologies based on more energetic radiation are being readied. The main limitation to the extension of the imaging capabilities of optical is the lack of sources and optical materials. At wavelengths shorter than 150 nm, all materials are strongly absorbing, so that not only glasses become unusable but the whole optical system must be kept in vacuum.

*Extreme ultraviolet* (EUV) uses radiation of a 13 nm wavelength to expose the image on the resist. Special reflective optics coated with interference reflectors are used. The technology is under development at major US national laboratories.

*Proximity X ray* is based on X rays of 1 nm wavelength. The mask is held in close proximity (10 $\mu$m to 20 $\mu$m) to the wafer, and X rays are used to project the image. The technology is under active development in the United States and Japan.

*Electron beam* refers to the exposure by means of a fine pencil of energetic electrons (100 kV) or by projection of a mask; in the last case the technology is similar, conceptually, to optical lithography and is called SCALPEL. The development is carried out in the United States.

*Ion beam* is similar to electron beam, but ions are used instead of electrons. Both direct write [focused ion beams (FIB)] and projection [ion projection lithography (IPL)] are being developed in the United States and in Europe.

Among the new technologies, the most advanced is proximity *X-ray lithography* (XRL). Since the wavelength of radiation is the ultimate determinant of the resolution, it is obvious that moving from 248 nm or 193 nm to 1 nm should solve the resolution problem once and for all. While this is true, other problems are generated by the need to use 1× systems (no projection optics are possible). All in all, XRL could see introduction in manufacturing for the 130 nm to 100 nm generation (4 Gbit to 16 Gbit DRAM type of devices).

Lithography is thus likely to remain the core of the electronic device industry, supporting the evolution of the technology well into the sub-50 nm domain.

## BIBLIOGRAPHY

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**LITHOGRAPHY, ELECTRON BEAM.** See ELECTRON BEAM LITHOGRAPHY.

**LITHOGRAPHY, PHOTO-.** See PHOTOLITHOGRAPHY.

**LITHOGRAPHY, X-RAY.** See X-RAY LITHOGRAPHY.

**LOAD-COMMUTATED CONVERTERS.** See SYNCHRONOUS MOTOR DRIVES.

**LOAD FLOW ANALYSIS.** See POWER TRANSMISSION LINES.

**LOAD FLOW OF ELECTRIC POWER.** See POWER FLOW.

**LOAD FORECASTING, SHORT-TERM.** See SHORT-TERM LOAD FORECASTING.