JUNCTION GATE FIELD EFFECT TRANSISTORS

The transfer resistor, or transistor, has, through its incorporation in integrated circuits, revolutionized modern technology. In particular, computers and microprocessors, which are composed of millions of transistors, are prevalent in nearly every aspects of our lives. This chapter deals with one type of transistor—the junction field effect transistor (JFET)—which is based on a *pn* junction gate as opposed to a metal-semiconductor or metal-oxide-semiconductor gate as used in other field effect transistors [e.g., metal-semiconductor field effect transistors (MESFETs) or metal-oxide-semiconductor field effect transistors (MOSFETs)].

JFET OPERATION

Basic Diode Theory

To understand the operation of a JFET one first must understand the basic operation of a semiconductor *pn* diode. Figure 1 shows a simple schematic of a *pn* diode under equilibrium, forward bias, and reverse bias. Under equilibrium a built-in potential (V_{bi}) develops at the metallurgical junction between the *p*-type and the *n*-type semiconductor. This potential is created by the ionized fixed impurities (acceptors and donors) on each side of the junction. These ionized acceptors and donors create a depletion region, *W*, where free carriers are swept out by a drift mechanism. The extent of *W* is determined by the concentration of acceptor (N_A) and donor (N_D) impurities on each side of the junction, the built-in potential (V_{bi}), the dielectric constant of the semiconductor (ϵ_s), and the charge on an electron (q) (see Ref. 1):

$$W = \sqrt{\frac{2\epsilon_s}{q}\frac{N_A + N_D}{N_A N_D}V_{bi}} \tag{1}$$

Under forward bias [Fig. 1(b)] the built-in potential is reduced by the applied voltage (V_f) and the depletion width is decreased. For a sufficiently large forward bias, typically on the order of two-thirds of the semiconductors bandgap, appreciable current flows through the diode. Under reverse bias [Fig. 1(c)] the built-in potential is increased by the applied voltage (V_r), and the depletion width is increased as more free carriers are stripped from dopant atoms to form additional ionized impurities. This increases the barrier to current flow in the diode. With this background the operation of a JFET is now presented.

JFET DC Operation

First consider a simple block of *n*-type semiconductor with ohmic (linear) contacts on each end as in Fig. 2 (2). When a bias is applied between these two contacts, a current flows through the semiconductor. This current flow is defined by

$$I = \frac{q\mu_e ntw}{l}V \tag{2}$$

where q is the charge on an electron, μ_e is the electron mobility, n is the free electron concentration, V is the applied volt-

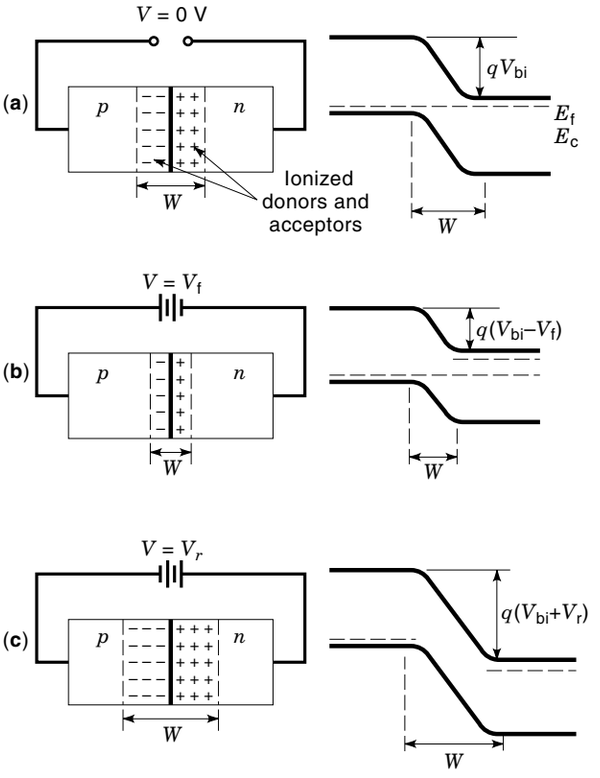

Figure 1. Schematic and energy band diagram of a *pn* junction under (a) equilibrium ($V = 0$), (b) forward bias ($V = V_f$), and (c) reverse bias ($V = V_r$).

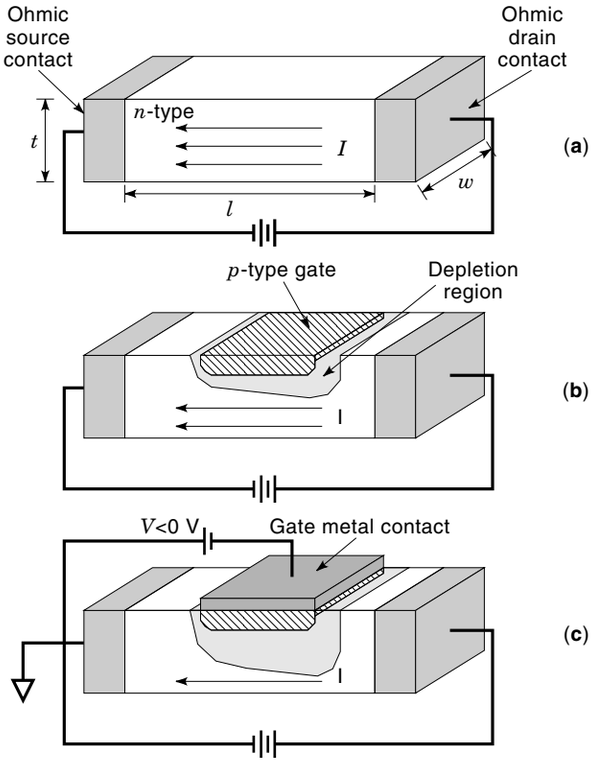

Figure 2. Schematic illustration of (a) condition in *n*-type semiconductor, (b) addition of *p*-type gate region with associated depletion region, (c) application of reverse bias to the gate contact that increases the depletion region and reduces the current flow from source to drain.

age, and the other quantities are the dimensions of the block as shown in Fig. 2(a). The current through this block can be changed by varying any of the terms on the right-hand side of Eq. (2). In practice, the doping level and mobility are set once the semiconductor material is prepared. However, if a *p*-type region is placed in the middle of the block as in Fig. 2(b), a depletion region is formed in the *n*-type material that effectively reduced the thickness t through which the current can flow through the block. If an electrode is now placed on the *p*-type region [Fig. 2(c)], the depletion region thickness can be varied by applying either a forward or reverse bias on the *p* electrode as with the diode in Fig. 1 and Eq. (1). Figure 2(c) shows the case of an applied reverse gate bias where the depletion width is increased and the current flow is reduced. This *pn* junction region forms the basis of the JFET and gives it its name, *junction field effect transistor.*

The operation of the JFET can be summarized by three bias conditions as shown in Fig. 3(a–c). With the gate held at zero voltage bias (and assuming that the built-in potential is insufficient to limit current flow from source to drain completely) the current from source to drain follows a linear relationship with respect to the source-to-drain bias V_{DS}, as shown in Fig. 3(a). As V_{DS} is increased, a reverse bias develops between the drain and the gate, acting to reverse-bias the gate junction. This in turn increases the junction depletion width and reduces the region through which current can flow from the source to the drain. Under this condition, the current no longer increases linearly, as seen in Fig. 3(b). As V_{DS} is increased further and the gate junction reverse bias is increased, the depletion width extends completely across the *n*-type channel at the drain end. At this point the channel is said to be *pinched off.* Current still flows through the channel by carrier injection from the applied V_{DS} across the depletion region. The current does not increase with increasing V_{DS}, however, since this only acts to increase the extent of the depletion region along the length of the channel as seen in Fig. 3(c). The current in this region is referred to as a *saturation current,* since it remains constant with increased applied bias.

If the bias to the gate, V_{GS}, is now varied, a family of curves is generated as in Fig. 4. Figure 4 is typical of any unipolar transistor (e.g. a MOSFET or MESFET). The circuit symbol for a JFET is shown in the inset of Fig. 4. Typically the value of V_{GS} is maintained below the junction turn-on voltage to limit the flow of gate current and to minimize the effect of minority carrier injection from the gate into the channel. Limiting the gate current is critical for low-power operation of the device, whereas minority carrier injection will degrade its high-frequency performance.

An alternative way to plot the relationship between gate bias V_{GS} and drain-to-source current I_{DS} is in a transfer curve such as the ideal curve of Fig. 5. The transfer characteristic can be expressed by Shockley's equation (3):

$$I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_{TH}}\right)^2 \tag{3}$$

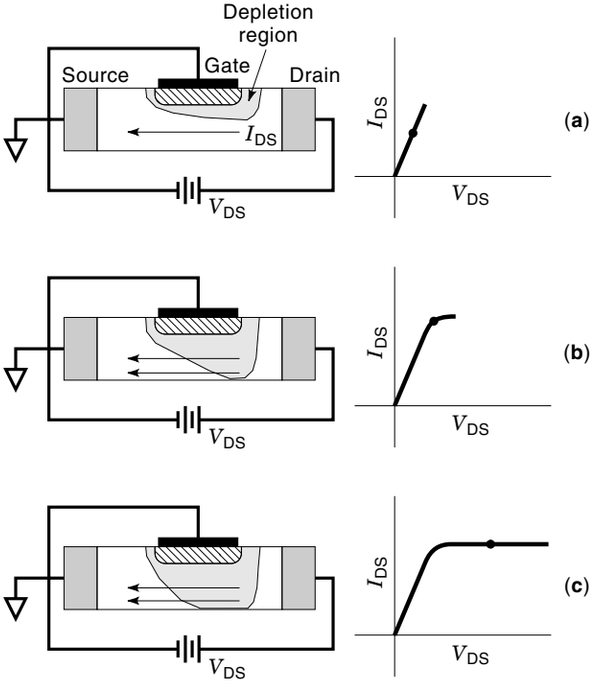

Figure 3. Schematic of a cross section of a JFET under three different source-to-drain bias (V_{DS}) conditions with the corresponding current versus voltage characteristics: (a) linear region, (b) transition or knee region at pinchoff, (c) saturation region.

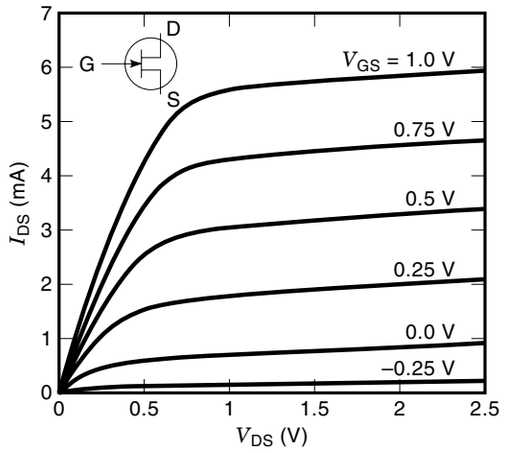

Figure 4. I_{DS} versus V_{DS} for the gate bias (V_{GS}) conditions shown for a GaAs JFET with a ~1 μm gate length.

where I_{DSS} is the saturation current for $V_{GS} = 0$ V and V_{TH} is the threshold voltage, the gate voltage where channel conduction first occurs. V_{TH} is defined as the x-axis intercept of a plot of $I_{DS}^{1/2}$ versus V_{GS}. In practice, V_{TH} is often reported at some defined value of channel current, say $I_{DS} = 1$ mA/mm. Equation (3) strictly holds only for an ideal device with no current flowing through the gate and for $V_{GS} > V_{TH}$.

Ac (Small Signal) Operation

With an understanding of the dc operation of a JFET we can now turn to its ac (small signal) characteristics. To do this, one needs the ratio between changes in V_{GS} and in I_{DS} for a set value of V_{DS}. This is referred to as the transconductance g_m, defined as

$$g_m = \frac{\Delta I_{DS}}{\Delta V_{GS}} \tag{4}$$

for which the unit is the siemens (S), or ampere per volt. g_m is often reported normalized to gate width (e.g. in millisiemens per millimeter). In the small-signal limit, Eq. (4) reduces to the derivative dI_{DS}/dV_{GS}, and gives

$$g_m = \frac{-2I_{DSS}}{V_{TH}}\left(1 - \frac{V_{GS}}{V_{TH}}\right) \tag{5}$$

The transconductance for the ideal transfer curve is also shown in Fig. 5. In the ideal case, the transconductance increases monotonically with increasing V_{GS}; however, in practice g_m saturates at some value of V_{GS} before decreasing as the gate diode becomes forward biased and significant gate current start to flow. Figure 6 shows the transfer curve and transconductance for an actual gallium arsenide (GaAs) JFET and shows the rolloff in g_m and I_{DS} caused by the onset of gate current. This device has a gate turn-on voltage, V_{GS}(on), of 0.95 V, defined at 1 mA/mm of gate current (4).

The high-frequency performance of a transistor (JFET or other type) is typically characterized by two metrics, the unity current gain cutoff frequency (f_t) and the maximum oscillation frequency (f_{max}). Of these, f_t is the point where the transistor current gain with the output short-circuited (h_{21}) goes to one; it can be expressed as (5,6)

$$f_t = \frac{g_m}{2\pi(C_{GS} + C_{GD})} \tag{6}$$

where C_{GS} and C_{GD} are the gate-to-source and gate-to-drain capacitances, respectively. f_{max} is the point where the unilateral power gain (U, the gain that exists when the input and output impedances of the transistor are ideally matched) goes to one, and can be approximated by

$$f_{max} \approx \frac{f_t}{2[g_{DS}(R_G + R_S) + 2\pi f_t C_{GD} R_G]^{1/2}} \tag{7}$$

where R_G and R_S are the gate and source resistances, respectively. g_{DS} is the output conductance (in siemens or millisiemens), defined as dI_{DS}/dV_{DS} for a set value of V_{GS}. From Eq. (6) we see that to maximize f_t, g_m should be maximized while C_{GS} and C_{GD} should be minimized. For maximizing f_{max}, the quantities g_{DS}, R_G, and R_S should be reduced along with C_{GD} (5,6).

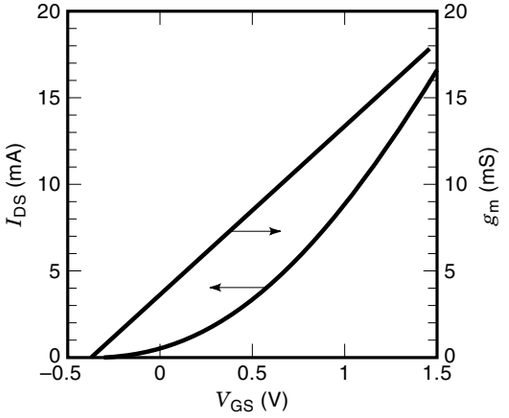

Figure 5. Transfer curve (I_{DS}, left axis) for a fixed value of V_{DS} and transconductance (g_m, right axis) versus V_{GS} for an ideal JFET with no gate leakage.

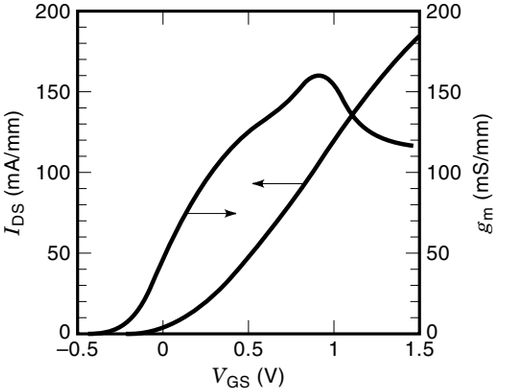

Figure 6. Transfer curve (I_{DS}, left axis) and transconductance (g_m, right axis) versus V_{GS} for $V_{DS} = 1.5$ V for a GaAs JFET with a gate length of ~1 μm that shows the saturation of g_m due to the onset of gate leakage.

A potential disadvantage of a JFET is the added gate capacitance resulting from the gate junction as compared to a MESFET or MOSFET structure. Details of the origin of this capacitance, and approaches to minimizing it, are addressed in the next section on JFET fabrication.

A further issue for high-frequency operation is the effect of minority carrier injection from the p^+-gate region into the channel if the gate is forward biased above the gate diode turn-on voltage [$V_{GS} > V_{GS}(\text{on})$]. If this occurs, the transistor cannot be switched off until the injected minority carriers are eliminated from the channel. This introduces an additional time constant, the minority carrier lifetime, into the switching process. Therefore, for maximum frequency performance, the bias on the junction gate should be at most equal to the gate turn-on voltage [$V_{GS} \leq V_{GS}(\text{on})$]. This is not typically a problem when using a JFET for a low-power technology operating on a low-voltage power supply, but can limit the applicability of a JFET for some higher-voltage logic circuit families.

Fabrication

Figure 7 shows a schematic of a simplified process for fabricating an n-channel JFET. First [Fig. 7(a)], the n-channel is formed in a selective area by diffusion or ion implantation though an opening in a masking material, typically photoresist or a dielectric mask. Second [Fig. 7(b)], a new opening is defined and the highly doped p-gate region is formed, again by diffusion or ion implantation. Third [Fig. 7(c)], an additional pair of openings are defined for the source and drain regions and high n-type doping is introduced. If the doping has been done by implantation, an implant activation anneal is performed at this stage. Fourth [Fig. 7(d)], the metal ohmic gate contact is deposited and patterned. Finally [Fig. 7(e)], the metal ohmic source and drain contacts are similarly deposited and patterned. Typically the metallization is dropped onto the semiconductor through an opening in an insulating dielectric such as silicon dioxide or silicon nitride.

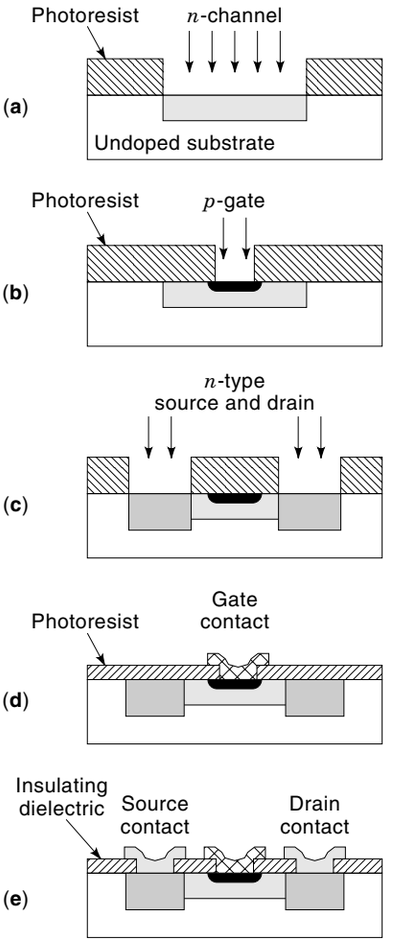

Figure 7. Schematic of a simplified process for fabricating an n-channel JFET. (a) The n-channel is formed in a selective area by diffusion or ion implantation through an opening in a masking material, typically photoresist or a dielectric mask. (b) A new opening is defined, and the highly doped p-gate region is formed, again by diffusion or ion implantation. (c) An additional pair of openings are defined for the source and drain regions and high n-type doping is introduced. If the doping has been done by implantation, an implant activation anneal is performed at this stage. (d) The metal ohmic gate contact is deposited and patterned. (e) The metal ohmic source and drain contacts are similarly deposited and patterned.

By examining the doping and metal profile of the JFET formed in Fig. 7, the causes of additional gate capacitance in the JFET are clear. The first is the fringing capacitance from the p-type region that extends laterally beyond the opening in the mask. This is compounded by the overlap of the gate contact metal that is created in realigning this metal with the original opening. The capacitance can cause a significant reduction in the high-frequency performance of the transistor.

An alternative processing sequence developed for a JFET that minimizes C_{GS} by self-aligning the gate contact metal with the p-type region is shown in Fig. 8 (see Ref. 4). This process is based on ion implantation doping and has been applied to gallium arsenide (GaAs) JFETs for high-speed operation (7). The process starts with selective area implantation of the n-channel and the p-type gate regions [Fig. 8(a)]. Second [Fig. 8(b)], a refractory gate contact (e.g. tungsten) is deposited and patterned. Third [Fig. 8(c)], a well-controlled etch of the p-type semiconductor is performed in the regions not protected by the gate contact metal. This etch effectively self-aligns the gate contact with the p-type gate region. Fourth [Fig. 8(d)], an n-type implantation is done with the gate contact metal acting as a mask to self-align the source and drain regions with the gate contact. At this point an anneal is performed to activate all the implanted dopants. Finally [Fig. 8(e)], the source and drain ohmic contact metal is deposited, patterned, and alloyed. Since the gate contact closely coincides with the p-type gate region, no additional fringing capacitance is incurred in this structure. In fact, this approach has been used to produce JFETs with the same high-frequency performance as a MESFET with the same gate length and achieved an f_t of 50 GHz for a 0.3 μm gate length (8).

JFETs in Advanced Materials

All the discussion to this point can generally be applied to JFETs based on silicon or mature compound semiconductors (e.g., GaAs). However, some of the most recent use of the JFET structure is based on less mature, but very promising, materials such as silicon carbide (SiC) and gallium nitride

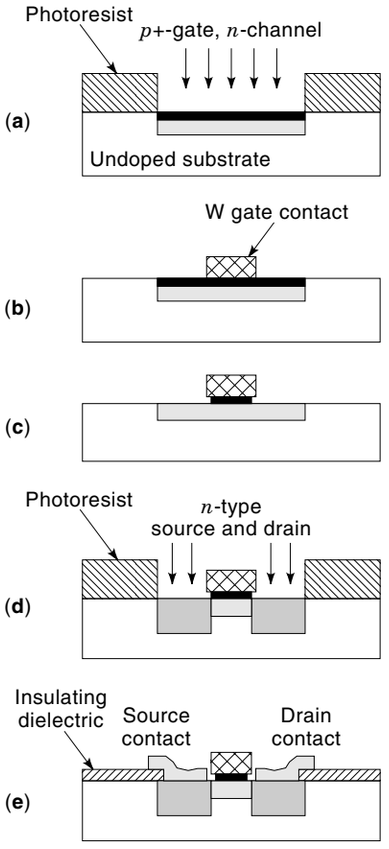

Figure 8. Schematic of self-aligned JFET process flow. (a) Selective area implantation of the *n*-channel and the *p*-type gate regions. (b) A refractory gate contact (e.g. tungsten) is deposited and patterned. (c) A well-controlled etch of the *p*-type semiconductor is performed in the regions not protected by the gate contact metal. This etch effectively self-aligns the gate contact with the *p*-type gate region. (d) An *n*-type implantation is done with the gate contact metal acting as a mask to self-align the source and drain regions with the gate contact. At this point an anneal is performed to activate all the implanted dopants. (e) The source and drain ohmic contact metal is deposited, patterned, and alloyed.

(GaN). These materials have much larger bandgaps (2.5 eV to 3.5 eV) and high electron saturation velocities, which make them ideal for high-power, high-frequency transistors. In addition, the large bandgaps make transistors based on these materials able to operate at temperatures where materials with smaller bandgaps, such as silicon (1.1 eV), are limited by thermal carrier generation. Furthermore, JFETs are attractive for high-temperature operation in that transistors based on metal-semiconductor gates (e.g., MESFETs) may fail at elevated temperatures due to degradation of the metal-semiconductor interface. In fact, one of the highest reported operating temperatures of a transistor is for a SiC JFET at 600°C (9). A GaN JFET has also been demonstrated with frequency performance comparable to a similar-gate-length epitaxial GaN MESFET (10). Further developments of JFETs in these material systems should result in robust high-temperature, high-power, high-speed electronics.

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JUNCTION ISOLATION. See ISOLATION TECHNOLOGY.