J. Webster (ed.), *Wiley Encyclopedia of Electrical and Electronics Engineering*

HOT CARRIERS

Charged carriers in semiconductor materials that have a higher energy than they have when in thermal equilibrium with the host material's lattice temperature T_L are called *hot carriers*. Both hot electrons and hot holes can exist. The average energy for a carrier in thermal equilibrium is $3kT/2$, where k is Boltzmann's constant (1.381×10^{-23} J/K) and T is the thermal equilibrium temperature in absolute temperature units of Kelvin. At room temperature ($T = 300$ K) the average energy of each carrier in thermal equilibrium is 6.21×10^{-21} J. For nonequilibrium the carrier temperature, either T_e for electron temperature or T_h for hole temperature, is defined. The energy of hot carriers can be ten to a few hundred times higher than that of thermal equilibrium.

In thermal equilibrium at normal semiconductor device operating temperatures, the equilibrium is maintained by continuous exchange of energy between the carriers and the lattice via phonons. The carriers both absorb phonons (lattice vibration energy) and emit phonons. If the carriers have more energy (higher temperature), there is more emission of phonons than absorption, causing the carriers to cool. Conversely, if the carriers have a smaller energy (lower temperature), there is more absorption of phonons and the carriers heat up to the lattice temperature.

Hot carriers are most often created by electric fields that produce a force F on the charged carrier of magnitude $F = qE$ where q is the charge of the carrier and E is the electric field. In the presence of the electric field, the carriers are accelerated and they gain energy. If the carriers were in a vacuum, the energy would rise indefinitely; but in a solid, various scattering or collision events dissipate the energy. As shown in Fig. 1 for silicon semiconductor material (1), if the applied electric field is low (below 10^4 V/cm) the scattering events primarily involved are impurity scattering and acoustical phonon scattering. The average energy (temperature) of the carriers shown in Fig. 2 (2) increases only slightly above the lattice temperature in this electric field range. The energy of the electrons in this figure is in electron volt (eV) units. The conversion to joules is 1.602×10^{-19} J $= 1.0$ eV. Once the electric field exceeds 10^4 V/cm the carrier drift velocity saturates and the energy of the carriers starts to increase substantially. As the energy increases, the dominant mechanism for loss of energy is emission of optical phonons. As the electric field increases even higher to 10^5 V/cm, the average electron and hole energies in silicon approach values of 0.5 eV. Also, at this electric field strength and higher, another scattering mechanism called *impact ionization* becomes important. Impact ionization is the collision of an energetic carrier with the lattice, resulting in the excitation of an electron from the valence band to the conduction band. This results in a reduction of the initial colliding carrier energy and the generation of a new conduction band electron and a new valence band hole. The threshold energy for the impact ionization process to occur is the bandgap of the semiconductor, which is approximately 1.14 eV for silicon. It is important to note that, even though the majority of the electrons in a 0.5 eV average energy distribution have less energy than needed for impact ionization, some of the electrons in the higher energy tail of the carrier energy distribution have sufficient energy to cause impact ionization.

Hot carrier effects can occur in any semiconductor device which has sufficiently high electric fields. Figure 3 shows a cross-section of a MOSFET transistor. The region of high electric field during normal transistor operation is where the channel region meets the drain region. The presence of the high electric field produces

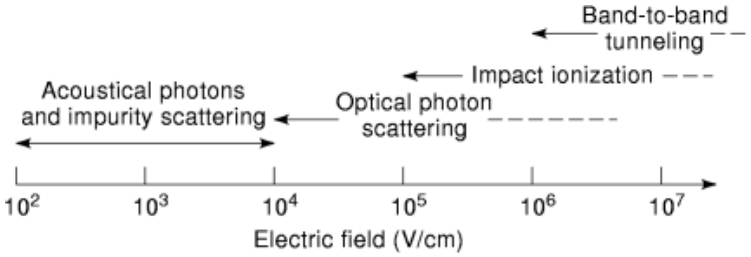

Fig. 1. Semiconductor phenomena occurring in silicon at various electric field strengths.

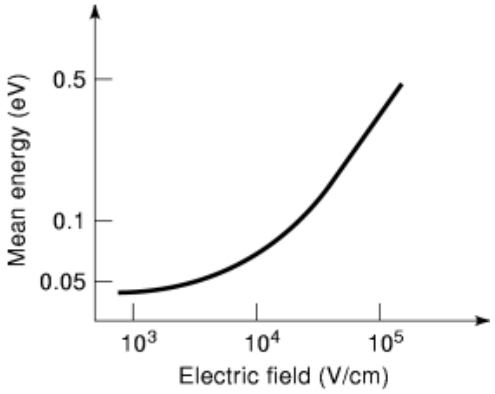

Fig. 2. Mean electron energy in silicon increases with the electric field (2). Reprinted from (2) with permission from Elsevier Science.

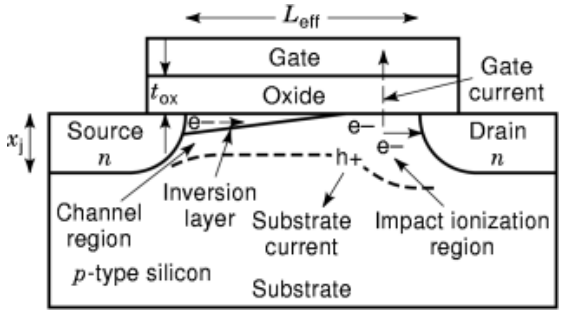

Fig. 3. Hot carrier effects occur in MOSFET transistors at the high electric field region located at the channel-drain junction.

hot carriers, which leads to a number of effects including substrate current, gate current, trapping of carriers in the oxide, generation of interface states, and the generation of photons that produce leakage current at other points in the circuit (3). These effects can degrade the performance of the device, resulting in circuit performance degradation or even circuit failure.

Substrate currents occur when the electrons moving from the source to the drain gain enough energy from the high electric field near the drain to produce impact ionization. The new electrons produced by the impact ionization in a n-MOSFET primarily move to the drain region. The holes, because of the electric field present between the drain and the substrate, move to the substrate. These holes produce the substrate current, which,

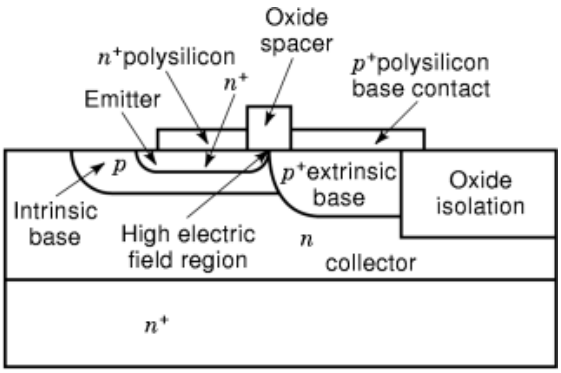

Fig. 4. Bipolar transistors show high electric fields at the emitter-base junction when this junction is reverse biased.

if large enough, can overload the substrate-biasing circuit, and can produce CMOS latchup, giving wrong circuit operation.

The energetic carriers at the drain end of the channel can also gain enough energy to be injected into the oxide layer. The energy needed for the injection of electrons over the silicon/silicon dioxide barrier is 3.2 eV. The electrons, once in the oxide, can flow to the gate, creating a gate current. Associated effects of hot carriers interacting with the silicon dioxide and the oxide/silicon interface are the generation of interface states and the trapping of carriers (holes or electrons) in the oxide. The interface states and/or trapped carriers produce a degradation in the transistor operating characteristics, including changes in threshold voltage and reduction in transconductance. If the degradation is severe enough, the device will cause a fault or failure in the circuit operation.

The hot carrier degradation mechanisms are of importance because a circuit may be tested as good immediately after it is manufactured, but then, at a later time (possibly years later), the circuit starts to function erroneously, due to the accumulated degradation effects. An area of hot carrier investigations is predicting the lifetime of devices that are experiencing degradation. These investigations are based on doing accelerated hot carrier degradation aging of a device until the device fails. This establishes its lifetime for a given operating condition. This operating condition is selected to be more severe than that occuring during normal operation, so the device will fail in a short period of time. This accelerated failure testing is repeated at a number of different operating conditions, until an empirical model is established for the lifetime as a function of operating conditions. Once the model is established, an extrapolation is performed to predict the lifetime for normal device operating conditions. The targeted minimum lifetime of semiconductor devices is often 10 years.

Another important area of hot carrier investigations is the redesign of semiconductor device structures to reduce the electric field magnitude in regions of the device where high electric fields and hot carrier effects occur. One example of this is the development of the lightly doped drain (*LDD*) structure for MOSFET devices. The LDD structure consists of a lighter doped drain region being formed at the junction of the channel and drain. The lower doping reduces the electric field in the portion of the MOSFET where the highest electric fields generally occur. As is often the case, a penalty is incurred in using the LDD structure. Specifically, the drain resistance increases.

Figure 4 shows a bipolar transistor structure experiencing hot carrier effects. The presence of high electric fields at the reverse-biased base-emitter junction produces hot carrier effects, including impact ionization (avalanching), interface state generation, and carrier trapping in the oxide. The major degradation effect for the bipolar transistor is the generation of interface states at the oxide interface, which form sites for surface recombination/generation. The interface states increases the emitter–base junction nonideal current and reduces the transistor gain.

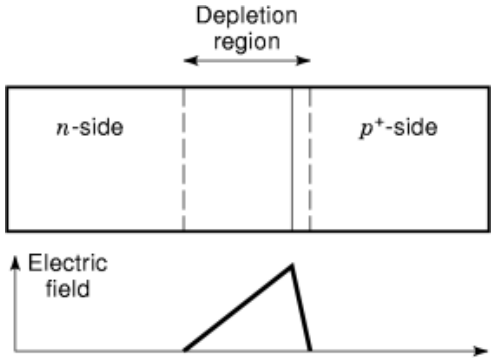

Fig. 5. Electric field present in a *pn* junction.

This entry is divided into several sections. First, the origination of hot electrons via high electric fields is described. Next, the microscopic picture of hot carrier phenomenon is presented. Then the hot carrier effects in both MOSFET and bipolar transistors are detailed. Last, the use of accelerated testing to predict the cumulative effects of hot carrier damage and the prediction of semiconductor lifetime is presented.

Hot Carrier Generation

This section discusses the location and magnitude of high electric fields in semiconductor devices, and it discusses the electron heating and hot carrier energies produced by these electric fields.

High Electric Field Regions. High electric field regions in several common semiconductor devices, including MOSFETs, bipolar transistors, and *pn* junctions, are displayed in Figs. 3, 4, and 5. The device shown in Fig. 5 is an idealized p^+n junction, where one side (p-side) is heavily doped and the other side (n-side) has a smaller doping density. The determination of the electric field strength for this device is found by starting with Poisson's equation. For this one-sided *pn* junction, the width of the depletion region is primarily on the lighter doped n-side, and it is given by

$$W = \left(\frac{2\epsilon_s[V_{bi} - V]}{qN}\right)^{1/2}$$

and the maximum electric field is given as

$$|E_m| = \frac{qNW}{\epsilon_s}$$

where ε_s is the semiconductor permittivity, for example, silicon $\varepsilon_s = 11.9\ \varepsilon_o$ with $\varepsilon_o = 8.85 \times 10^{-12}$ F/m, N is the n-side doping density, V_{bi} is the built-in junction potential, and V is the applied bias across the junction (negative for reverse bias).

An example calculation of the maximum electric field for a p^+n junction with $V_{bi} = 0.8$ V, V $= -5$ volts, and $N_D = 10^{18}$ cm^{-3} gives a depletion width of W $= 0.28\ \mu$m and maximum electric field of 4.2×10^5 V/cm.

The hot carrier region in bipolar transistors as seen in Fig. 4 occurs at the emitter-base junction when this junction is reversed biased. The region with the highest electric field is the emitter-base junction near the top of the silicon. The base region is typically formed first by either diffusion or ion implantation of the

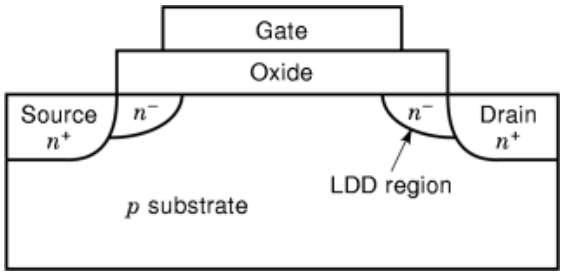

Fig. 6. The lightly doped drain (LDD) structure is used to reduce the electric field in region where the channel and the drain meet in the MOSFET.

impurity dopants from the silicon surface. Then the emitter is formed. For both the emitter and the base, the dopant concentration is usually highest near the silicon surface and decreases with depth into the silicon. The impurities from the emitter also have a distribution that decreases parallel to the silicon surface at the edge of the emitter opening. The result of the fabrication process is that the highest doped region that forms a *pn* junction occurs at the emitter edges near the silicon surface.

The high electric fields in MOSFET devices occur under normal operating conditions where the channel region meets the drain region, as seen in Fig. 3. The electric field in this region is not as easy to predict as that in the one-dimensional *pn* junction already discussed above. The electric field for the MOSFET is a function of gate voltage, drain voltage, oxide thickness, substrate doping, and drain region doping and junction profile. The work by Chan et al. (4) describes an approximate model for the maximum electric field. In this model a region is defined at the drain end of the channel, where the voltage in the channel varies from V_{DSAT} to V_{D}. V_{DSAT} is defined as the potential at the pinch-off, or saturation point in the channel and V_{D} is the drain voltage. The electric field in this approximate model is estimated as

$$E_{\mathrm{m}} = \frac{V_{\mathrm{ds}} - V_{\mathrm{DSAT}}}{l}$$

where l is the effective length of the velocity saturation region. This model requires that the value of l be estimated.

Empirical formulas of E_{m} and l in MOSFET devices with channel lengths in the range from 1 μm to 5 μm have been developed (5). One such model estimates the electric field using

$$l = 0.22(t_{\mathrm{ox}})^{1/3}(x_{\mathrm{j}})^{1/2}$$

where t_{ox} is the gate oxide thickness and x_{j} is the drain junction depth, both in centimeters. This expression is an empirical fit to two-dimensional device simulations, which solved Poisson's equation for the value of l. The MOSFETs described by this model had channel lengths of 1 μm to 5 μm, drain junction depths of 0.3 μm to 0.45 μm, and oxide thicknesses of 12 nm to 100 nm. The equation for l is likely different for new technologies with shorter channel lengths. For shorter length devices, the electric field and, hence, hot carrier effects are often reduced by using a lightly doped drain structure, as shown in Fig. 6. The LDD structure has a two-part drain region, with the section that touches the channel region having a lower doping density. Accurate solution of the electric field requires two- and sometimes three-dimensional numerical solutions of the MOSFET structure with realistic doping profiles.

Carrier Heating Models. Carrier heating models discussed below divide into two types. First are the electric field models, which describe hot carrier effects such as impact ionization as a function of the local electric

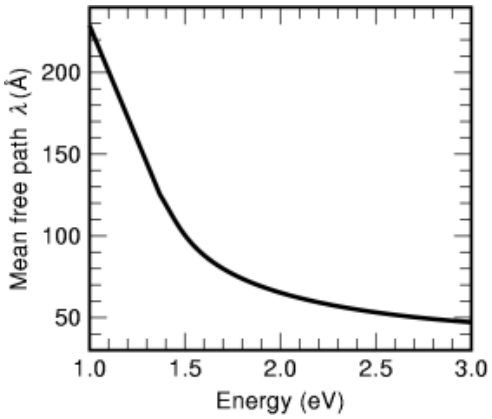

Fig. 7. Hot electron mean free path in silicon decreases versus electron energy (7). (© 1990 IEEE)

field. Second are the models that describe the carrier energy distribution based on various assumptions. The carrier energy-based models are used to calculate the number of carriers with an energy above some threshold energy ϕ_a. These various models may be classified as: (1) lucky electron model, (2) carrier temperature model, and (3) full carrier energy distrubution model.

Electric Field Dependent Model. In this model the various parameters, such as carrier drift velocity and impact ionization, are treated as functions of the electric field. The values reported are the steady-state values of the parameter assuming the carriers have moved through a long distance of the semiconductor at the electric field magnitude of interest. This type of model is also called the *local electric field model,* since it predicts various phenomena based only on the electric field at a given position.

Lucky Electron Model. The lucky electron (6) model is based on the concept of the scattering mean free path, λ, of hot carriers. The probability that a carrier travels a distance d if the mean free path between collisions is λ, is given by $\exp(-d/\lambda)$. For an electric field of strength E, the potential that the carrier moves through is given by $\phi = qEd$. Therefore the probability that the "lucky" carrier acquires the energy ϕ is given by $\exp(-\phi/qE\lambda)$ (3). The underlying assumption in this model is that a mean free path for hot carriers can be defined. A commonly used value at $T = 300$ K is $\lambda = 7.3$ nm in silicon. The utility of the lucky electron model is that, if a certain hot electron effect has a threshold energy of occurrence such as ϕ_a, then the rate at which the effect occurs is given by $\exp(-\phi_a/qE\lambda)$. The physical picture assumed by the lucky electron model is that the electrons move ballistically until a collision occurs. One consequence of this assumption is that no electron gets an energy greater than the potential energy difference through which the carrier moves. For the example of the MOSFET, the hot carriers, according to this model, have a maximum energy given by the carrier falling through the potential energy difference between the source and the drain, V_{ds}.

The mean free path between collisions is only a rough approximate model. Work by Goldsman, Henrickson, and Frey (7) did a more accurate determination of the mean-free path λ in silicon at room temperature as a function of electron energy, as shown in Fig. 7. They calculated the full electron energy distribution function using the Monte Carlo method. The mean free path is seen to decrease to a value of $\lambda = 5.0$ nm as the electron energy increases to an energy of 3.0 eV.

The lucky electron model can also be applied to the prediction of the number of hot holes. For hot holes in silicon, the mean free path at room temperature is taken as $\lambda = 3.7$ nm.

Hot Carrier Temperature Model. In this model, the distribution of carrier energies is modeled based on a single temperature. The carrier energy distribution assumed is a Maxwellian given by

$$f(\phi) \sim \exp(-\phi/kT) \qquad (1)$$

where T is T_e for electrons and T_h for holes. In this model, the carriers can acquire an energy greater than the value of potential through which the carrier moves, due to collisional exchange of energy between carriers. The carrier temperature is typically solved from the energy conservation equation, which balances the energy gained from the electric field, and the energy exchange and loss produced by collision and diffusion processes. In this model, the phenomenon of interest is quantified as a function of the carrier temperature. An example of using the carrier temperature model is the thermionic emission of a heated electron gas over an energy barrier. The Richardson's expression for thermionic current J over an energy barrier of height ϕ_b is given by

$$J = qn\left(\frac{kT_e}{2\pi m^*}\right)^{1/2} \exp\left(\frac{-\phi_b}{kT}\right)$$

where T is the carrier temperature, $m*$ is the electron effective mass, and n is the electron density. Such a method has been used to predict the emission of electrons over the silicon dioxide barrier to the gate in n-MOSFETs (3).

Full Carrier Energy Distribution Models. The behavior of hot carriers in semiconductor devices is more complex than the above models suggest. The first discrepancy is that the distribution function is not Maxwellian for hot carriers. Second, the electric field changes value quickly versus position, hence the carriers never reach steady state at a given electric field value. The more accurate descriptions of hot carriers in both MOSFET and bipolar devices have been developed using full-band structure models (specifically local empirical pseudopotential models) and Monte Carlo simulation techniques (8). A sample of the results obtained from these models for a short-channel MOSFET is shown in Figs. 8 and 9. The MOSFET simulated has an effective channel length of 0.15 μm. Figure 8 shows the average electron energy and the electron potential energy in the region where the channel meets the drain. For the applied bias of $V_g = 1.0$ V and $V_{ds} = 3.4$ V, the average electron energy exceeds 1.0 eV and the electron distribution function at the various positions A–G, as shown in Fig. 8, are given in Fig. 9. The electron energy distribution is significantly different from the exponential variation versus energy expected by a Maxwellian distribution of Eq. (1). This is particularly true at positions A and B. In this example, the electric field at the position $x = 0.34$ μm has a value of 500 kV/cm.

One concept that has been more fully understood using these more complex models is the presence of hot carrier effects, even when the applied bias is less than the threshold for the particular effect. Specifically, substrate currents produced by impact ionization in MOSFETs have been observed at V_D values that produced a potential energy difference between the source and drain that is less than the threshold for impact ionization (9,10). These full-bandstructure models, which include electron–electron scattering, show a "thermalization" of the high-energy carriers, with some carriers gaining energy from the scattering events (11). Hence the carriers do not need to gain all their energy from a ballisticlike motion through a potential energy difference; rather, some of their energy can be gained through collisional events.

Microscopic Hot Electron Effects

Impact Ionization. Impact ionization occurs when a carrier (either an electron or a hole) undergoes a scattering event that excites another electron from the valence to the conduction band. The overall effect is the production of one new electron in the conduction band and one new hole in the valence band. The minimum

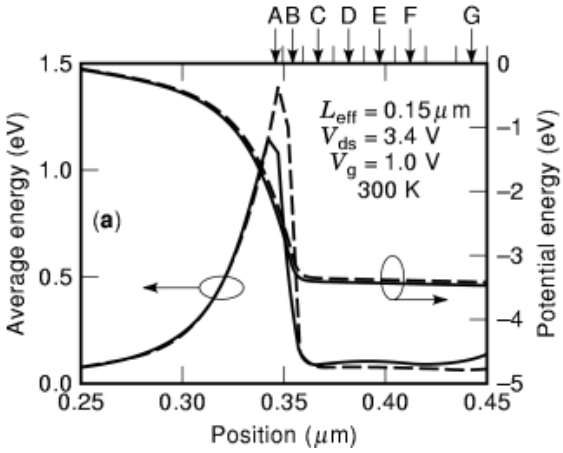

Fig. 8. The potential energy and average electron energy versus position at the junction of the channel and the drain for a MOSFET (8).

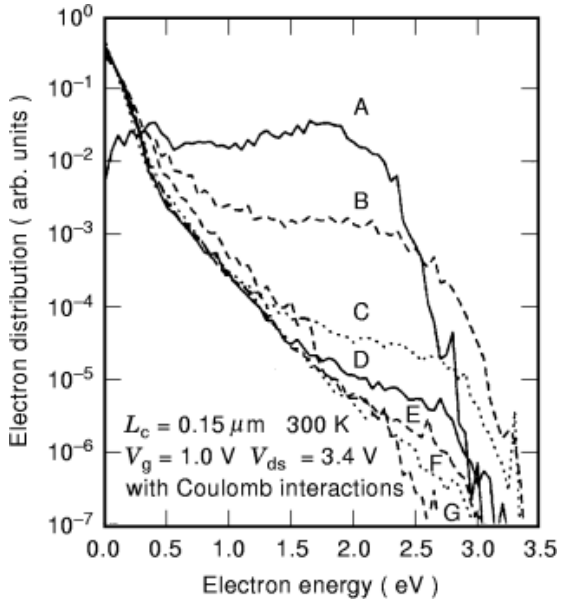

Fig. 9. The electron energy distribution at the seven positions (A–G) indicated in Fig. 8 (8).

threshold energy for the initial electron to produce an impact ionization event is the bandgap energy. Impact ionization can be understood by two different models. The more traditional approach is to describe the ionization coefficent α as a function of the electric field. The impact ionization coefficient is the number of ionization events produced by one carrier per unit length of carrier movement. This model assumes a homogeneous electric field. The data (12) for silicon are shown in Fig. 10. The typical model used is $\alpha = A_i \exp(-B_i/E)$. For silicon, the impact ionization parameters (3) for electrons are $A_i = 2.0 \times 10^6$ cm^{-1} and $B_i = 1.7 \times 10^6$ V/cm, and for holes the parameters are $A_i = 8.1 \times 10^6$ cm^{-1} and $B_i = 3.7 \times 10^6$ V/cm.

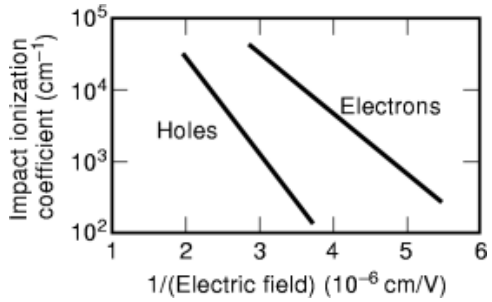

Fig. 10. Impact ionization coefficient for holes and electrons in silicon as a function of the electric field strength.

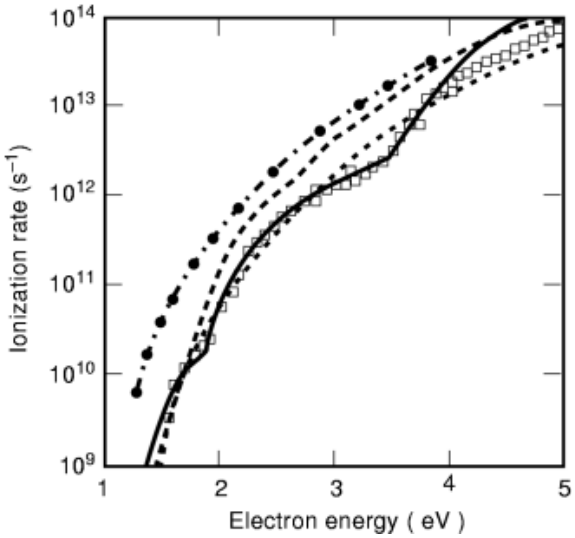

Fig. 11. Ionization rate of electrons in silicon increases with electron energy (8).

An alternative model describes either ionization rate or quantum yield as a function of the electron energy. The data for this second approach are shown in Figs. 11 and 12. Figure 11 shows the ionization rate of an electron in silicon versus the energy of the electron (8). An ionization rate of 10^{12} s^{-1}, for example, means that 10^{12} impact ionization events occur per second for each electron. Viewed differently, on average, each electron with an ionization rate of 10^{12} s^{-1} will have an impact ionization event each picosecond. A model of the ionization rate shown in Fig. 11 was developed by Cartier et al. (13). This model describes the ionization rate as the sum of the processes each with a different threshold energies, which are consistent with impact ionization between different valleys of the conduction band and different valance bands (light and heavy hole) in silicon. The threshold energies for this silicon model are 1.2 eV, 1.8 eV, and 3.45 eV, respectively. Figure 12 contains a quantum yield description of the impact ionization process (14). Quantum yield is the ratio of the impact ionization rate to the total rate of all types of collisions. Worded differently, it is the number of new electrons generated per scattering event. At higher electron energies of 4 eV, most of the scattering is of the impact ionization variety.

Photon Generation. The presence of hot carriers in semiconductors generates light. In the case of silicon, the photons are generated by direct and indirect (phonon-assisted) conduction–conduction band spontaneous emission. In work by Selmi et al. (15) the light emission intensity as a function of photon energy was

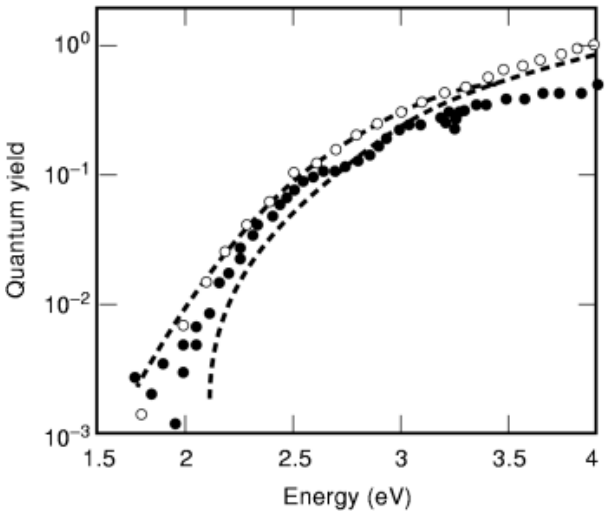

Fig. 12. Quantum yield for the number of electron-hole pairs created by impact ionization for each electron scattering event (14).

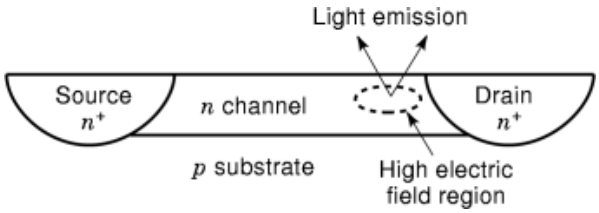

Fig. 13. $n+$–n–$n+$ structure used to measure the light emission from hot carriers (15). (© 1995 IEEE)

measured in a silicon $n+$–n–$n+$ device as shown in Fig. 13. The device, which had a length between the source and drain regions of 0.4 μm, showed the experimental light emission given in Fig. 14. The increase of the drain voltage from 3.5 V to 6.0 V produced large increases in the number of photons emitted at a given photon energy. Other researchers (16,17) have approximately described the spectrum of the light generated by an electron gas with a temperature T_e given by the relation

$$I(\nu) = \exp(-h\nu/kT_e) \qquad (2)$$

where I is the emitted light intensity and ν is the light frequency. This relation permits the extraction of the electron temperature from the emitted light characteristics.

Emission of Carriers over Barriers. Hot electrons and hot holes can acquire enough energy to surmount the silicon–silicon dioxide barrier. The barrier height for an electron to go from the silicon conduction band to the oxide conduction band is 3.2 eV. The barrier height for holes to go from the silicon to the oxide is 4.7 eV.

Once an electron or hole is in the silicon dioxide, one of three outcomes can occur. First, the carrier can experience an electric field such that the electron or hole is simply pushed back into the silicon, resulting in no observable effects. Second, the carrier can have enough energy to move to a different conducting region or it can be forced by an electric field to a different conducting region. In either case, it produces a hot-carrier-generated current. An example of this second outcome is the gate current observed in MOSFETs. The third possible

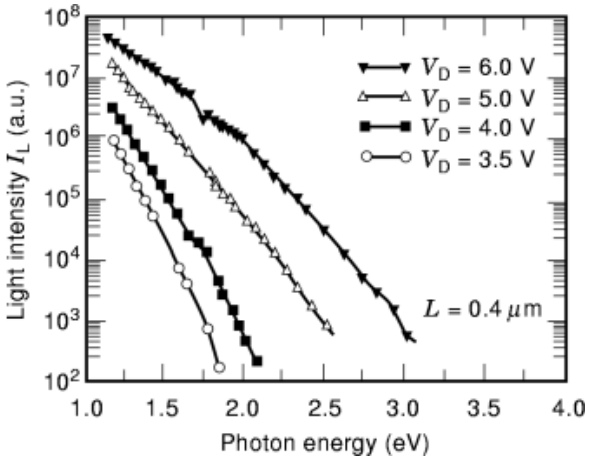

Fig. 14. Larger drain biases produce more intense and higher photon energy light via hot carriers (15). (© 1995 IEEE)

outcome is the capture of the electron or hole into a trap in the silicon dioxide. The trapped charge appears as a fixed charge in the oxide. In the case of MOS structures, the trapped charge produces a shift in the threshold voltage.

Traps in the oxide can be either hole or electron traps. The traps occur when not all the silicon and oxygen atoms are bonded as shown in Fig. 15, with each silicon atom bonded to four oxygen atoms and each oxygen atom bonded to two silicon atoms. These trap locations provide sites for the capture of electrons or holes that have energies located within the bandgap of the silicon dioxide. These energies are far enough below the conduction band that electrons once trapped cannot easily escape back to the conduction band. Likewise, the hole traps are above the valence band energy far enough that the holes are not released by normal thermal processes. Many of these trap sites are made electrically inactive by the presence of hydrogen, which neutralizes the traps. In fact, infrared measurements have shown the existence of sizable numbers of Si–H groups in silicon dioxide of semiconductor devices (12).

One consequence of hole trapping has been shown to be electron trap generation and interface state creation (18,19,20). The process is believed to begin as a hole being captured into a hole trap of the silicon dioxide. Subsequently, the hole in the trap recombines with a conduction band electron in the oxide. The excess energy of the recombination is large enough that a hydogen bond in the oxide is broken, producing a new electron trap and an atomic hydrogen, which can diffuse in the oxide and break another silicon–hydrogen bond, producing more traps or states, either in the oxide or at the silicon/silicon-dioxide interface. The importance of trapping and the generation of new traps or interface states depends on the oxide quality.

Interface State Generation. Another effect of hot carriers is the generation of interface states. Interface states are traps for either electrons or holes that exist at the silicon/silicon dioxide interface, with energies located in the bandgap of the silicon. These traps can serve as locations for surface recombination and/or surface charging. An understanding of the degradation process begins by noting that the Si/SiO_2 interface can and does have a number of dangling bonds. The dangling bonds are present because not every silicon atom on the silicon surface bonds to the amorphous SiO_2 material. The dangling bonds are silicon atoms, which have only three bonds to adjacent silicon atoms. Silicon likes to have a full valence shell, which requires eight electrons. This occurs when the silicon is bonded to four other silicon. Many of the silicon atoms at the surface form the fourth bond with the oxide, but the SiO_2 is amorphous and not all the silicon atoms on the surface have an oxide atom with which to bond. This dangling bond then acts as an electron trap, with an energy located in the

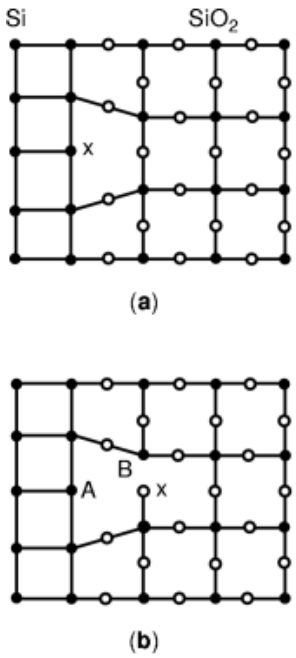

Fig. 15. Silicon–silicon dioxide interface showing a Si–H bond (*x* for hydrogen), electron trap (a) and hole trap (b). The filled dots are silicon and the open circles are oxygen atoms (22).

energy gap of silicon. Reduction in the number of dangling bonds occurs by hydrogen bonding to the dangling bonds of the silicon atoms. This makes the silicon atom electrically inactive, so that electrons are not trapped.

The first mechanism of degradation of the silicon/SiO_2 interface occurs when hot carriers directly break the SiH bond at the interface (12,21,22). The energy needed by the hot electrons is the energy to exceed the potential barrier of the silicon/silicon dioxide interface (3.2 eV), plus the energy to dissociate the Si–H bond (0.3 eV). The atomic hydrogen is then believed to either bond with another H atom, forming H_2, which is either trapped in the silicon dioxide or released to the atmosphere (23). Alternatively, it is also believed possible for H to break an existing Si–O bond, forming a silanol Si–OH bond. This process also forms a surface hole trap, with a silicon in the SiO_2, short one bond to an oxygen.

A second mechanism for the generation of interface states is the trapping of a hole followed by its recombination with an electron, as described in the previous section on carriers being injected into the oxide. The energy involved in the recombination breaks an Si–H bond, creating either a interface state, or a hydrogen that diffuses to the surface, breaking a Si–H bond, leading to an interface state. Even though the barrier for holes to surmount the oxide barrier is quite large (4.7 eV), suggesting that hole injection into the oxide is difficult to achieve, holes can also enter the hole trap sites near the interface by tunneling into the hole traps. Once in the hole trap, the subsequent recombination of the hole with an electron can occur, driving this second mechanism for the creation of interface states.

n-Mosfet Hot Electron Effects

An ideal *n*-MOSFET device has current flow between the source and drain, which is controlled by the voltage applied to the gate, source, drain, and substrate. This ideal MOSFET has no gate current or substrate current,

and it has current-voltage and capacitance-voltage charateristics that do not change as the device is operated over its lifetime. The presence of hot carriers produce nonideal effects, including substrate currents, gate currents, and changes in the device's operating performance as the device is utilized.

Hot carriers are generated in the channel region as the electrons move from the source to the drain. Near the drain end of the channel the electric field is largest. A number of phenomena occur in this region of high electric field. First the electron drift velocity saturates as optical phonon generation becomes significant. At even higher electric fields, the carrier energies become large enough that impact ionization occurs. The ionization produces both electrons and holes. The holes are generally forced by the electric field to the flow to the substrate, which produces the substrate current. Also at these higher electric fields, hot carriers can be injected into the oxide, producing gate current, trapping of carriers in the oxide, and interface state generation.

The understanding and the prediction of the various hot carrier effects in n-MOSFET has been developed using three approaches. Approach 1 looks at the correlation of the various effects including substrate current, gate current, leakage current, interface state generation, and shifts in device characteristics (3). Approach 2 develops a semiquantitative model of the electric field and proceeds to model the various hot carrier effects based on the electric field strength (3). This second approach is based on predicting the hot carrier behavior using the steady-state electric field model, the lucky electron model, and/or the carrier temperature model. The third approach is a numerical approach, which solves for the electron energy distribution using a full-band structure model and realistic doping profile (8). With this approach, the population of hot carriers capable of producing various hot carrier effects is simulated and this population is used to model the various phenomena.

Substrate Current. The presence of hot electrons at the drain end of the channel produces impact ionization, which yields holes that flow to the substrate contributing to the substrate current. A typical plot (3,24) of the substrate current that is produced by the hot electrons is shown in Fig. 16, for a MOSFET with a channel length of 1.1 μm and a gate oxide thickness of 20 nm. The presence of larger drain voltage values produces larger electric fields, more impact ionization, and larger substrate currents. Another phenomenon also observed is that the substrate current peaks at a gate voltage of $V_G - V_T \sim V_D/2$. It is at this gate voltage and drain voltage that both the drain current is large and the electric field is large. Both of these conditions are needed to have substantial substrate currents. The substrate current has been modeled using a lucky electron model (3,4) of the form

$$I_{sub} = C_1 I_d \exp\left(\frac{-\phi_i}{q\lambda E_m}\right) \qquad (3)$$

where E_m is the maximum electric field, λ is the hot carrier mean free path, I_d is the drain current, and C_1 is a proportionality constant. ϕ_i is the threshold energy for impact ionization, which, in silicon, is often taken as 1.3 eV. According to this model, the substrate current is determined by the electron flow I_D and by the number of hot electrons in this electron flow with energy greater than ϕ_i.

The substrate current by itself is not a problem, as long as it is small enough. If the substrate current is too large, the substrate-bias generator may not be able to maintain a constant substrate voltage. This can result in forward biasing of the source–substrate junction, giving electron injection into the substrate, which can contribute to CMOS latchup.

Gate Current. The gate current is produced by carriers gaining enough energy to surmount the silicon/silicon dioxide barrier and flowing across the oxide to the gate. This produces a gate current. An example plot of the gate current (3,24) in an n-MOSFET is shown in Fig. 16. The data given in Fig. 16 are for a MOSFET with an oxide thickness of 20 nm and an effective channel length of 1.1 μm. The gate current typically has a maximum value when the gate voltage is equal to the V_D voltage. The gate current is typically much smaller than the substrate current. The mechanism of gate current is one where the electrons gain a large kinetic energy from the electric field, such that they can surmount the oxide potential energy barrier of 3.2 eV. Since

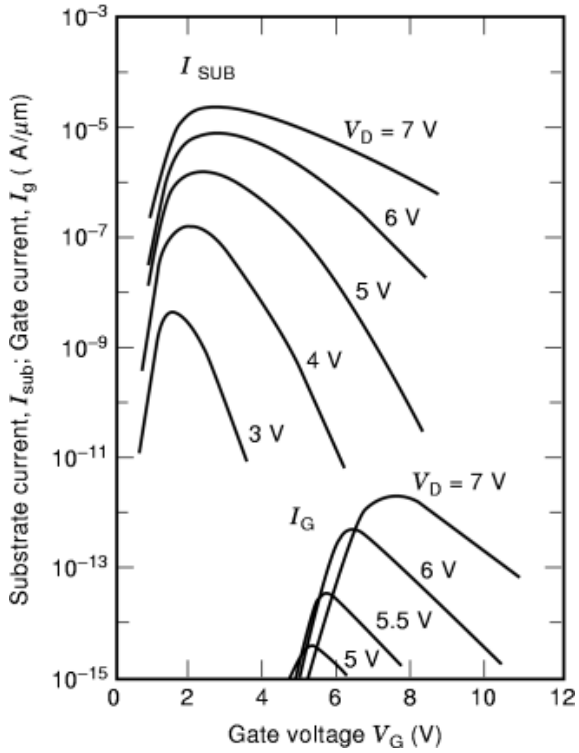

Fig. 16. Hot carrier generated substrate and gate current in an n-MOSFET (24). (© 1982 IEEE)

the largest electric field is typically directed from the channel to the drain, the hot electrons must undergo a scattering event (with minimal energy loss) so that the momentum is redirected toward the oxide layer. A model for the gate current based on the lucky electron model is

$$I_G = C_1 I_D \exp\left(\frac{-\phi_b}{q\lambda E_m}\right)$$

where ϕ_b is the barrier height for the carriers to surmount the silicon/silicon dioxide barrier and C_2 is a fitting constant.

Leakage Current. Another effect of hot electrons is the generation of light as described in the above section on microscopic hot carrier effects. The detrimental effect of this light is shown in Fig. 17, where, once the light is created, it can be reabsorbed again into another region of the semiconductor, creating an electron hole-pair. If this pair is created near a reverse bias junction, as shown in Fig. 17, the minority carrier crosses the reverse bias junction, creating a leakage current, I_{coll}. An example (17) of measured currents, including the drain current, substrate current, and photon-generated leakage current, are shown in Fig. 18, for a 1.2 μm channel length n-MOSFET with a channel width of 100 μm and an oxide thickness of 82.1 nm. The leakage current I_{COLL} is proportional to the substrate current generated by the impact ionization.

The simple model for the light generated by the hot carriers was given above in Eq. (2). The photons that can both travel some significant distance in the semiconductor ($h\nu \sim E_g$) and can be absorbed ($h\nu > E_g$), give that the photons contributing to the leakage current are those whose energy is $h\nu = E_g$. The amplitude of the

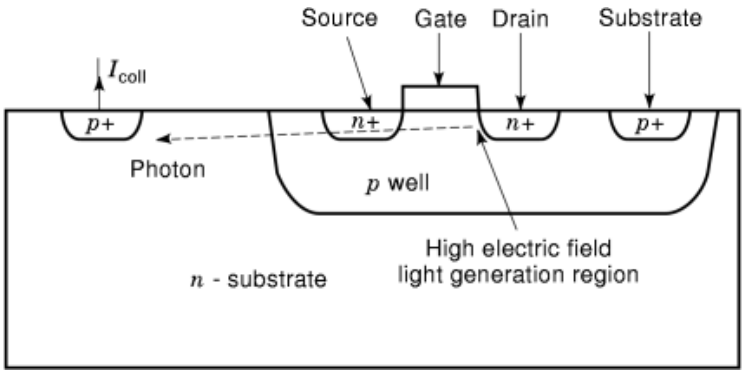

Fig. 17. Light generated by hot carriers in one n-MOSFET is absorbed at another location affecting a distance device with a current I_{coll} (17). (© 1984 IEEE)

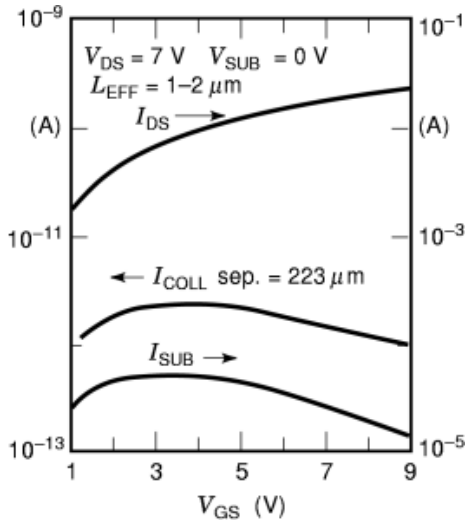

Fig. 18. Measured drain, substrate, and I_{COLL} current versus V_G for the structure shown in Fig. 17 (17). (© 1984 IEEE)

leakage current I_{coll} is written as

$$I_{COLL} = C_3 I_d \exp\left(\frac{-h\nu}{q\lambda E_m}\right)$$

where ν is the light frequency and C_3 is a fitting parameter.

Degradation Effects. The stressing of n-MOSFETs produces two types of degradation. First, interface states can be created at the silicon/silicon dioxide region where the channel meets the drain. A second mechanism is the trapping of charged carriers (either electrons or holes) in the gate oxide. These two damage mechanisms produce permanent changes in the MOSFET characteristics, including the threshold voltage and drain current. The type and magnitude of the stress depends on the device structure and the applied voltage. Three general stressing conditions are defined, including hot hole stress, where the gate voltage is negative,

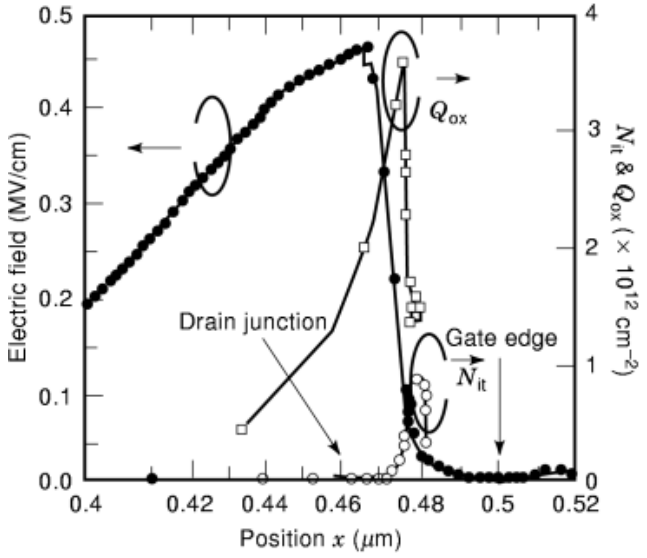

Fig. 19. Negative charge trapped and density of interface states generated versus position as the result of maximum gate current stressing of an n-MOSFET (25). (© 1997 IEEE)

maximum substrate current stress, where the impact ionization producing the substrate current is maximum, and maximum gate current, which occurs when the gate voltage is large.

Experimental characterization studies of n-MOSFET degradation have permitted detailed mappings of the interface state density and trapped charged density. Figures 19, 20, and 21 show the interface state charge density N_{it} and trapped charge density Q_{ox} distributions from the work by Cheng et al. (25). In this work, they utilized experimental measurements to quantify the lateral distribution of the trapped oxide change and interface state density created by stressing 0.5 μm channel length n-MOSFETs. The gate oxide thickness for the MOSFETs was 7 nm. In Fig. 19 is plotted both Q_{ox} and N_{it} versus lateral position. Also plotted is the calculated electric field versus position. The gate extends in the geometry of the figure from $x = 0$ μm to $x = 0.50$ μm and drain junction extends under the gate to $x = 0.458$ μm. The data in this figure are for a maximum gate current stress condition of $V_D = 5$ V and $V_G = 5.5$ V. The trapped charge (which is negative) and the interface states are created for this stress condition in the gate-drain overlap area between $x = 0.458$ and 0.50 μm.

Figure 20 shows the distribution of the interface state density for the maximum substrate current stress condition. This stress condition corresponds to the bias which creates the most impact ionization at the channel–drain junction region. The bias voltage for this stress condition was $V_D = 5$ V and $V_G = 2$ V. At this stress condition, oxide charging is small and insignificant. Therefore, the dominant degradation is due to interface state generation. The interface state generation occurs at the region where the gate and the drain overlap.

Figure 21 shows the distribution of the trapped oxide charge and the interface state density for the hot-hole stress condition. This stress condtion was at $V_D = 5$ V and $V_G = -4$ V for 5000 s. The MOSFET is in the off state with no current flow from the source to the drain for this stress condition. Positive charge (holes) are injected from the silicon to the oxide with this large negative bias on the gate. Some holes are trapped in the oxide, resulting in a positive oxide charge. Note that the location of the trapping is shifted away from the drain region and further into the channel region, as compared with the data in Fig. 19 for the maximum gate current stress condition.

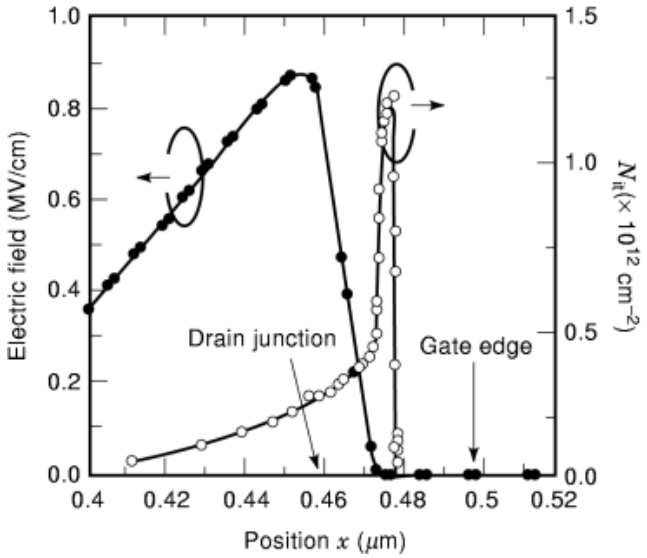

Fig. 20. Interface states generated versus lateral position by a maximum substrate current stressing of an *n*-MOSFET (25). (© 1997 IEEE)

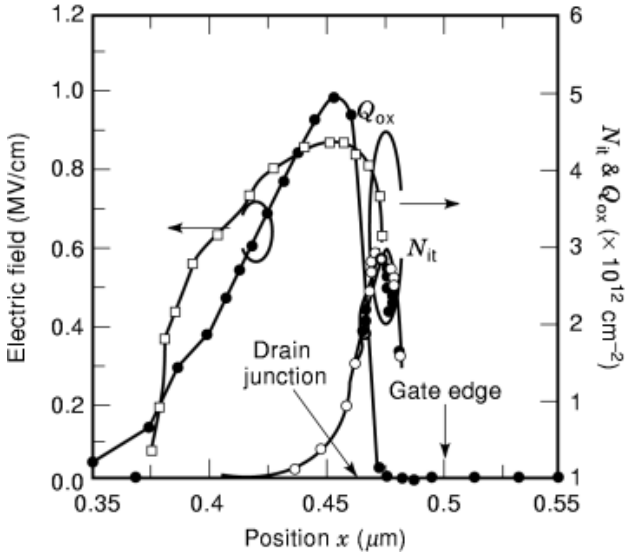

Fig. 21. Positive hole trapping and interface state density versus position resulting from hot hole stressing of an *n*-MOSFET (25). (© 1997 IEEE)

The degradation of *n*-MOSFETs by hot carriers is quantified in three device *I–V* quantities. First, the threshold voltage shows a positive shift in value. The shift is attributed to interface state creation and/or electron trapping. Figure 22 shows an example of the shift of the threshold voltage from before stressing to after stressing (4). Not only did the threshold voltage increase, but the transconductance ($g_m = \Delta I_D/\Delta V_G$) also decreases with degradation. The reduction in the transconductance is the second quantity that is reduced

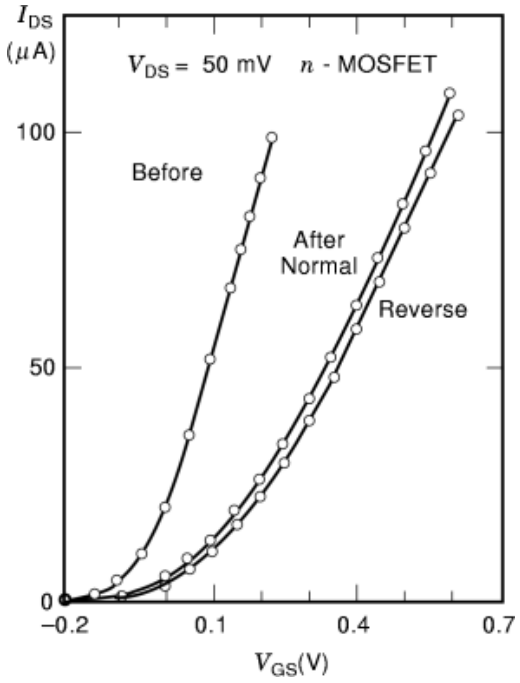

Fig. 22. The threshold voltage shifts to a higher voltage as a result of hot carrier degradation (4). (© 1985 IEEE)

with degradation. The last quantity that is commonly quantified in terms of degradation change is the shift in subthreshold current swing

$$\Delta S = \frac{\partial V_G}{\partial \log I_D}$$

A plot showing the change in the subthreshold characteristics is found in Fig. 23 (4). The degradation can also be seen in the standard current-voltage (I_D versus V_D) curves. The drain current flow at a given bias voltage is reduced as the degradation of the threshold voltage proceeds (3).

The dominant mechanism of n-MOSFET degradation changes as a function of stressing condition as seen in Figs. 19, 20, 21. Overall, the dominant mechanism of n-MOSFET degradation, under normal operating voltages at room temperature, is interface state generation. However, at lower temperatures near 77 K, the dominant degradation can change to be electron trapping in the oxide (26). Additionally, it has been shown that the bias for creating the most degradation is the maximum substrate current condition ($V_G \sim 1/2V_D$) at room temperature. In contrast, the maximum gate current stress condition ($V_G \sim V_D$) produces the most degradation at lower temperatures (26).

Lifetime Models. The degradation of the MOSFET quantities ΔV_{th} (threshold voltage), ΔN_{it} (interface state density), ΔS (subthreshold current swing), and Δg_m (transconductance) can be semiquantitatively predicted with the general model described below (3). The quantity changing due to degradation is denoted Δ. The rate of degradation of Δ is proportional to the number of carriers with enough energy to produce the degradation. As an example, for interface state generation, the threshold energy is ϕ_{it} (3.5 eV for the silicon/silicon

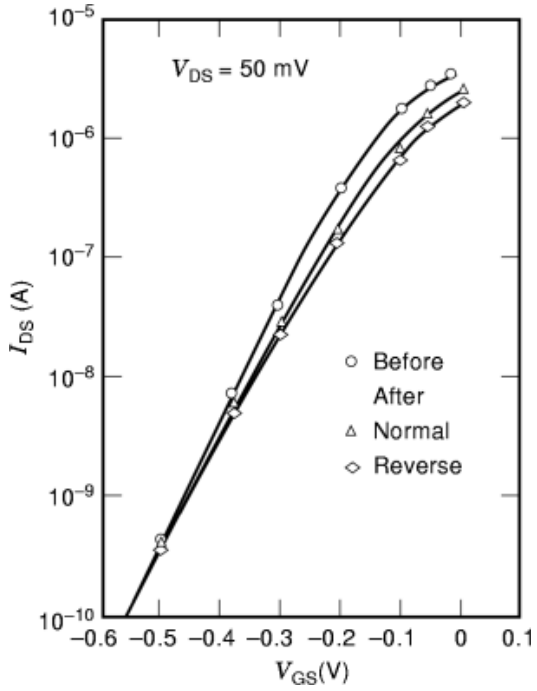

Fig. 23. A change occurs in the subthreshold current swing as a result of hot carrier degradation of an n-MOSFET (4). (© 1985 IEEE)

dioxide interface), and the degration rate is written as

$$\frac{d\Delta}{dt} \propto G(\Delta)\frac{I_D}{W}\exp\left(\frac{-\phi_{it}}{q\lambda E_m}\right) \tag{4}$$

where $G(\Delta)$ represents the dependence of the degradation rate on existing damage. An example $G(\Delta)$ dependency is the decrease in the rate of increase of interface state generation with increasing ΔN_{it}. This is due to the atomic hydrogen, which is released by Si–H bond dissociations, rebonding to a dangling bond eliminating an interface state created earlier. The term I_D/W is a width-independent measure of the concentration of electrons in the channel.

Since E_m is difficult to know, the number of hot electrons is estimated from an easily measured quantity such as the substrate current or the gate current. The most commonly used measure of the hot carriers is the substrate current. Rewriting Eq. (3) for the substrate current gives

$$I_{SUB} = I_D \exp\left(\frac{-\phi_i}{q\lambda E_m}\right) \tag{5}$$

where ϕ_i is the threshold energy for impact ionization (1.3 eV in silicon). By eliminating the exponential term in Eqs. (4) and (5), the degradation rate is expressed as

$$\frac{d\Delta}{dt} \propto G(\Delta)\frac{I_D}{W}\left(\frac{I_{SUB}}{I_D}\right)^{\phi_{it}/\phi_i}$$

Putting all the Δ terms on the left side of the equation and integrating gives

$$\int \frac{d\Delta}{G(\Delta)} \equiv F(\Delta) = \frac{I_D}{W}\left(\frac{I_{SUB}}{I_D}\right)^{\phi_{it}/\phi_i} t \qquad (6)$$

If f is defined as the inverse of F, the degradation can be written as

$$\Delta = f\left[\frac{I_D}{W}\left(\frac{I_{SUB}}{I_D}\right)^{\phi_{it}/\phi_i} t\right]$$

A commonly used formulation for $G(\Delta)$ is $G(\Delta) = \Delta^{-k}$, which gives by defining $n = 1/(1+k)$

$$\Delta \propto \left[\frac{I_D}{W}\left(\frac{I_{SUB}}{I_D}\right)^{\phi_{it}/\phi_i} t\right]^n \qquad (7)$$

where n is an empirical fitting parameter. Typical values for n range from 0.3 to 0.7.

Using this degration model, the lifetime can be estimated. The device lifetime is found as the stress time when a selected degradation is reached, such as $\Delta V_{th} = 10$ mV. This occurs according to Eq. (7), when $\Delta =$ selected constant (e.g., $\Delta^{-n} = C_5$).

$$\frac{I_D}{W}\left(\frac{I_{SUB}}{I_D}\right)^{\phi_{it}/\phi_i} t = C_5$$

Solving for the lifetime τ gives

$$\tau = C_5\frac{W}{I_D}\left(\frac{I_D}{I_{SUB}}\right)^{-\phi_i/\phi_{it}}$$

Experimental degradation data have shown that the degradation rate versus time is $\Delta \sim t^n$, where $n = 0.3$ to 0.7 and the lifetime goes as $t \sim (I_{SUB})^{-m}$, where m is measured from 2.5 to 3.5. An example plot of degradation of threshold voltage versus time for five different MOSFET devices of channel lengths ranging from 1.2 μm to 2 μm and oxide thicknesses ranging from 11 nm to 82 nm are shown versus time in Fig. 24.

p-Mosfet Hot Carrier Effects

Hot carrier effects in p-MOSFET mirror those of n-MOSFET in several ways. The holes in the conducting channel are accelerated at the drain end of the channel to high energies, producing impact ionization. The electrons produced from the ionization can flow to the substrate, producing substrate current. An example plot

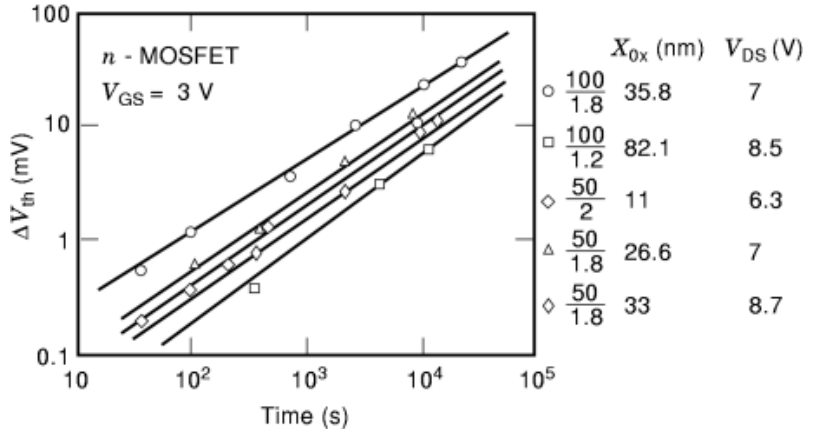

Fig. 24. The degradation of the threshold voltage increases with stressing time following a degradation rate proportional to t^n (4). (© 1985 IEEE)

(3,27) of the substrate current in a *p*-MOSFET is shown in Fig. 25. This *p*-MOSFET has a channel length of 1 μm and an oxide thickness of 25 nm. As expected, larger negative drain voltages produce more substrate current. With respect to the gate current, hot holes injected over the oxide barrier are not significant as a source of gate current (26,27). This occurs because the potential barrier for hot holes (4.7 eV) is larger than the barrier for hot electrons (3.2 eV). However, gate current is measured in *p*-MOSFETs and it can be larger than in *n*-MOSFETs. This gate current is due to electrons created by impact ionization of the holes. As seen in Fig. 25, the larger gate currents occur at the gate voltage values closer to the threshold voltage. This is in contrast to the *n*-MOSFET, where the larger gate current occurs at $V_G \sim V_D$.

The primary degradation mechanism in *p*-MOSFET transistors is the trapping of electrons in the gate oxide near the gate/drain interface (3,26). The trapped electrons cause a shortening of the effective channel length. The shorter channel length produces an increase in the drain current and in the transconductance g_m. It also produces a shift in the threshold voltage and an increase in the subthreshold leakage current. One of the failure mechanisms for the *p*-MOSFET is punchthrough, where current flows from the source to the drain without any gate control. One consequence of the increased subthreshold leakage current is a decreased punchthrough voltage. An example of the degradation of the punchthrough voltage (28) is shown in Fig. 26.

Bipolar Transistor Hot Carrier Effects

The primary hot carrier effect in bipolar transistor is the degradation of the common emitter current gain, h_{FE}, as shown in Fig. 27 (29). The *npn* transistor in Fig. 27 was stressed with a constant reverse bias of 4 V across the base–emitter junction. The current gain decrease occurs because of an increase in the base current with stress time, as shown in Fig. 28. The base current at small V_{BE} values is seen to increase versus stress time. The nonideality factor of the base current increases from an initial value near 1 to a value appoaching 2. The nonideality factor is the variable n in the dependency $I_B \sim \exp(V_{BE}/nkT)$.

The mechanism of degradation is believed to be high electric fields at the emitter–base junction and near the oxide surface, creating hot carriers. These hot carriers generate interface traps that are sites for recombination and/or generation at the silicon/silicon dioxide interface. The nonideality factor of 2 supports the conclusion that the degradation induced current is due to generation-recombination current.

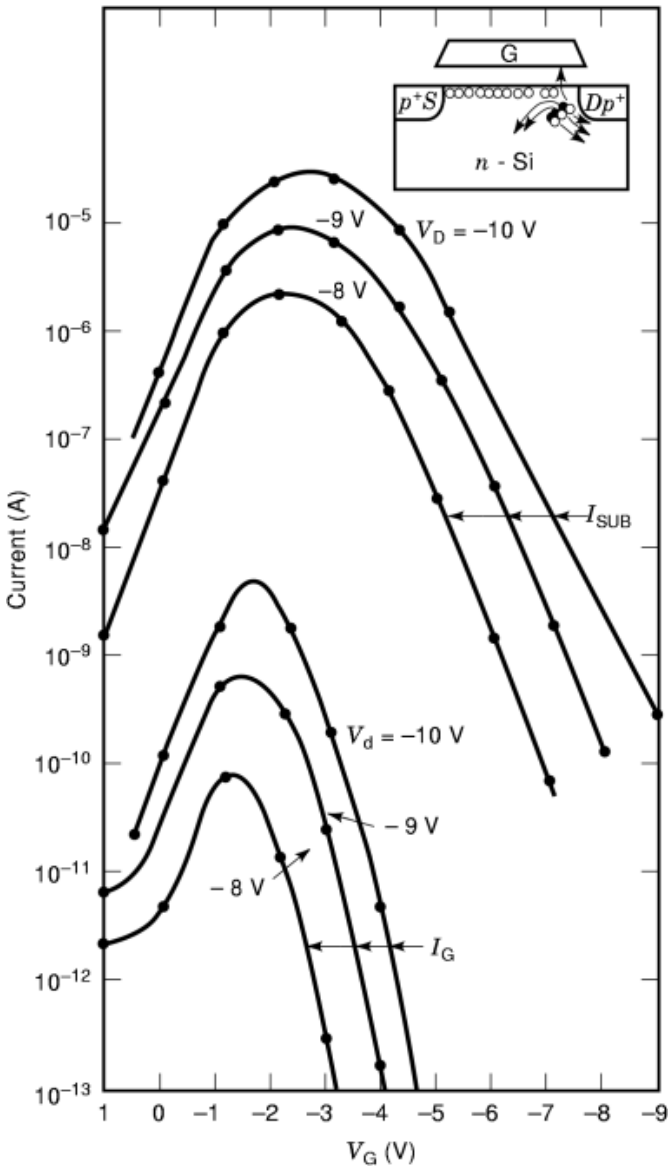

Fig. 25. Substrate current and gate current produced by hot carriers in a p-MOSFET (27). (© 1983 IEEE)

The quantification of the degradation in bipolar transistors has been shown to follow a dependence of $\Delta I_B \sim Q^m$, where Q is the accumulated reverse bias stess charge (30). This stress charge is the time integrated current that flows across the reverse biased emitter–base junction. A example plot of ΔI_B versus Q is shown in Fig. 29. The value of m for the data shown in this figure is approximately 0.5.

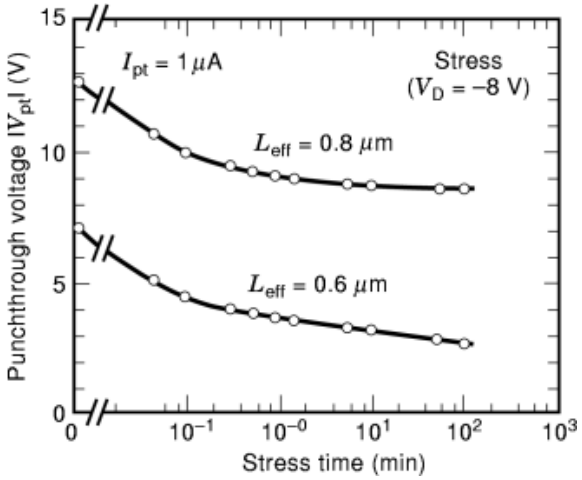

Fig. 26. The punchthrough voltage is reduced in *p*-MOSFETs as a result of hot carrier degradation (28). (© 1986 IEEE)

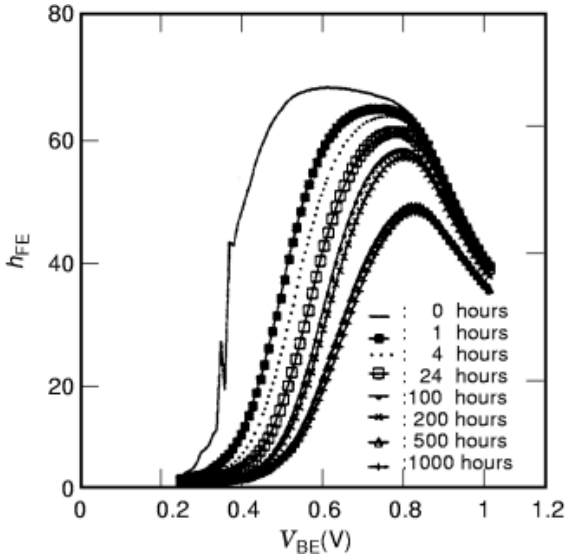

Fig. 27. Common emitter current gain of a *npn* transistor decreases with stressing of the emitter–base junction due to hot carrier degradation (29). (© 1993 IEEE)

Accelerated Testing and Ac-Stressing

Most semiconductor devices are designed with a time-to-failure of 10 years when operated within their design specification. The standard method used to predict the lifetime of devices is accelerated testing. Accelerated testing is the process of stressing semiconductor devices at operating voltages which produce degradation in reasonably short times. Then the accelerated degradation data are used to predict the device lifetime. The lifetime is the time to produce a predetermined degradation such as a threshold voltage shift in a MOSFET of 10 mV. Another facet of lifetime prediction is how realistic operating conditions (pulsed or ac signals) affect the stressing results, which are typically done under dc conditions.

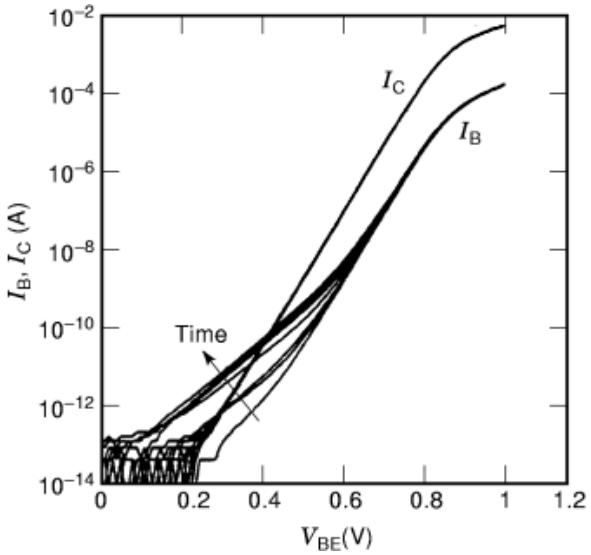

Fig. 28. Base current increases at low base–emitter bias due to degradation by hot carriers generated via a reverse applied to the base–emitter junction of 4 V (29). (© 1993 IEEE)

Accelerated Testing. An example of accelerated testing is shown in Fig. 30. *n*-MOSFETs are stressed at various stress conditions. The hot carrier effects are monitored by the value of the substrate current, I_{SUB}, which is produced by the hot carriers. Plots are then generated of the lifetime versus number of hot electrons as estimated by I_{SUB}/W. As expected, the trend is a shorter lifetime at higher substrate currents (i.e., more hot carriers). A relationship is established for the lifetime versus substrate current of the form

$$\tau = C_5 \left(\frac{I_{SUB}}{W} \right)^{-m}$$

where m has a value of 3 in Fig. 30. Once this relationship is established, τ can be set to the desired lifetime (e.g., 10 years) and the substrate current corresponding to this lifetime is calculated as I_{SUB} (τ = 10 years). This substrate current value then represents the maximum substrate current that can be permitted so that the device operates reliably for 10 years.

The lifetime model generally extracted for *n*-MOSFET transistors is

$$\tau = B \left(\frac{1}{I_{SUB}} \right)^{m}$$

where m has the numerical value between 2.5 to 3.5. This is the model for room temperature operation. At lower temperatures (e.g., 77 K) the degradation has been shown to be more directly related to the gate current, so a lifetime model of the form

$$\tau = B \left(\frac{1}{I_{GATE}} \right)^{m}$$

is more appropriate to the experimental data.

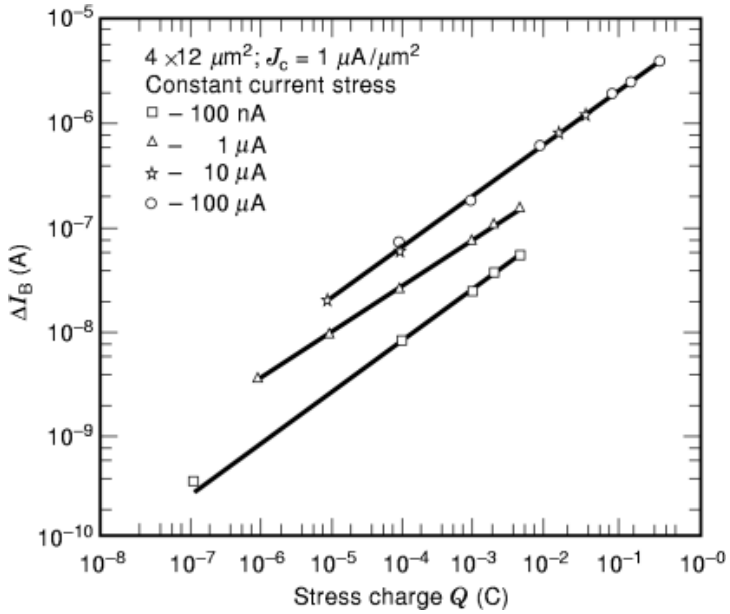

Fig. 29. Base current increases at low base-emitter biases in *npn* transistors as a function of the accumulated stress charge (30). (© 1988 IEEE)

The lifetime model for *p*-MOSFET is of the form

$$\tau = B\left(\frac{1}{I_{\mathrm{GATE}}}\right)^m$$

where m has an empirical value generally between 2 and 3.

Ac-Stressing. The hot carrier degradation effects discussed to this point have been under dc bias conditions. In actual integrated circuits the operation is dynamic, with voltages and current changing versus time. A commonly used ac hot-carrier degradation model is based on the idea of hot carrier "age." The "age" is defined, in a form similar to Eq. (6), as

$$\mathrm{age} = \int_0^T \left(\frac{I_{\mathrm{D}}(t)}{WH}\right)\left(\frac{I_{\mathrm{SUB}}(t)}{I_{\mathrm{D}}(t)}\right)^m dt$$

where H is a technology-dependent constant and T is the device operating time. The degradation is then treated as

$$\Delta N_{\mathrm{it}} = (\mathrm{age})^n$$

where n is the degradation time dependence factor. With this model, the accumulative degradation of various operating modes (pulsed, ac) can be analyzed.

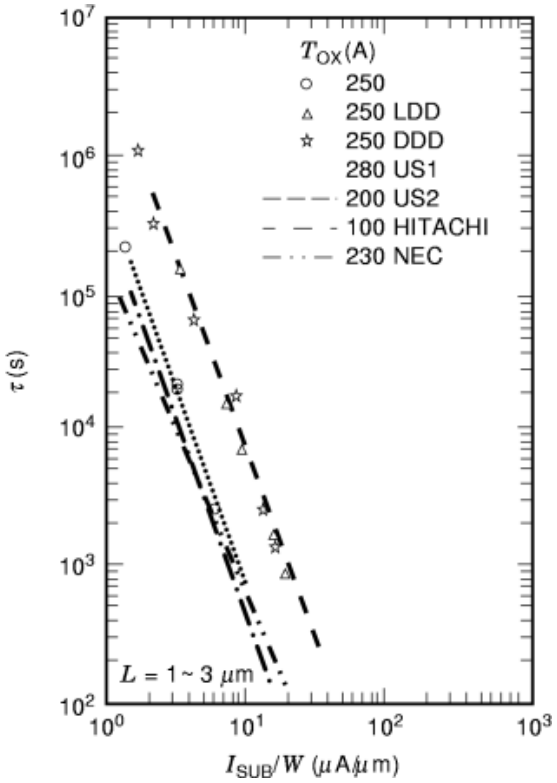

Fig. 30. Accelerated testing is used to predict the lifetime of MOSFETs (3).

Final Remarks

The occurrence of hot carrier effects is a major design consideration, as each generation of integrated circuits has smaller feature sizes. One direction to reduce hot carrier effects is to design carefully controlled doping profiles, to reduce the electric field in vulnerable regions of semiconductor devices. One such example is the development of LDD (*lightly doped drain*) and similar structures for reduction of the peak electric fields in MOSFETs. As semiconductor devices have been shrunk to feature sizes of less than a micrometer, the management of hot carrier effects has included reductions in the operating voltage. A long-time standard voltage for CMOS circuits was 5 V. The first widespread reduction in operating voltage was to 3.3 V. Even smaller dimension devices are now proposed, with operating voltages at or near 1 V. The hot carrier effects are reduced at these lower voltages, but not entirely eliminated. In fact, because of charged carrier energy exchange (e.g., via electron–electron scattering) the carriers can acquire energies larger than energies expected, by just considering movement of the carriers through a given potential. Another direction in hot carrier effect management is the improvement of the oxide quality and semiconductor/oxide interface quality. This includes improvements in the interface, to reduce the number of dangling bonds and hydrogen–silicon passivating bonds, which can form interface states via hot carrier degradation. Also included is the deposition or growth of oxides with fewer traps.

As a last word, hot carrier effects are a continuing semiconductor device design consideration as each new integrated circuit fabrication technology is developed to produce faster, smaller, and more complex circuits.

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TIMOTHY A. GROTJOHN
Michigan State University