GATE DIELECTRICS

The thermal oxidation process associated with semiconductor technology has been used primarily in conjunction with silicon. Attempts to oxidize germanium and compound semiconductors thermally have been generally unsuccessful, except by employing a field-assisted process such as anodizing. Silicon (Si) semiconductor technology has depended heavily on

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the thermal oxidation process since the 1950s. Investigations by Atalla, Tannenbaum, and Scheibner (1), Liginza and Spitzer (2), and other workers at Bell Laboratories led in 1960 to the planar process [Hoerni (3)] and the metal-oxide–semiconductor (MOS) transistor [Kahng and Atalla (4)]—two very significant developments.

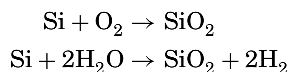
The pervasiveness of silicon-based semiconductors in electronic systems is a result of the unique ability of single-crystal silicon to grow thermally an amorphous stoichiometric oxide with an interface (transition zone) only a few atomic layers wide. Metal-oxide–silicon field-effect transistors (MOSFETs) are used in circuits ranging from memories to microprocessors to custom logic circuits for diverse functions such as echo cancellation, voice recognition, data encryption, and high-definition television. Indeed, the power of silicon circuits is limited only by their size or the level of integration.

A major hurdle to achieving ultralarge/gigascale-integration (ULSI/GSI, more than 50 million transistors on one chip) has been the inability of the process technologist to grow ultrathin oxides with low defect densities and atomically sharp interfaces. Combined with shallow junctions and fine-line geometry, such high-quality ultrathin oxides will make scaled-down devices possible for integration into ULSI/GSI circuits through multilevel interconnects.

In this article, we describe the oxidation process with present-day knowledge of kinetics and mechanisms of growth with special emphasis on the Si/SiO_2 interface properties. The evolution of thin gate oxide process is reviewed as the industry went from 0.9 μm to 0.18 μm technology. The impact of light nitrogen incorporation and stacking for scaled gate oxides are also discussed. A summary and a discussion of future trends are presented in the last section.

SILICON THERMAL OXIDATION MECHANISM AND KINETICS

Silicon dioxide (SiO_2) has the unique ability to passivate the Si surface ($Si \rightarrow SiO_2$, $\Delta F = 200$ kcal/mol) where ΔF is free energy of formation. Thermal oxidation provides the best passivation characteristics for silicon devices (number of surface electronic states) compared with any other deposition techniques. In the thermal oxidation process (5), silicon reacts with either oxygen or water (steam) at temperatures between 600° and 1250°C to form silicon dioxide. The oxidation reaction may be represented by the following two reactions:



$$Si + O_2 \rightarrow SiO_2$$
$$Si + 2H_2O \rightarrow SiO_2 + 2H_2$$

Special marker experiments have demonstrated that oxidation proceeds by the diffusion of either an oxygen or water species through the oxide already formed, which then reacts with the silicon at the Si/SiO_2 interface. As oxidation continues, the interface moves into the silicon and a new, clean silicon surface is produced. As a result, the original silicon surface states (unsatisfied bonds) and contamination are consumed and optimized device passivation is achieved. From the density and molecular weights of silicon and amorphous silicon dioxide, it can be shown that for every thickness x_o of oxide formed, $0.45x_o$ of silicon is consumed. The exact nature and charge of the diffusing oxidation species (O_2, O, O_2^-, O^-, H_2O, H_3O^+, OH^-, etc.) have not yet been identified. It is known, however, that for steam oxidation, considerable exchange occurs between the already formed silicon dioxide and the diffusing water species. On the other hand, very little exchange takes place between oxygen and the oxide network.

The following general oxidation relationship has been derived by Deal and Grove (5,6):

$$x_o^2 + Ax_o = B(t + \tau) \tag{1a}$$

also written in the form

$$(x_o^2 - x_i^2)/B + (x_o - x_i)/A = t \tag{1b}$$

where x_o is the oxide thickness, t is the oxidation time, and A, B, τ, and x_i are the constants as defined below:

$$A = 2D_{\text{eff}}(1/k + 1/h) \tag{2}$$

$$B = 2D_{\text{eff}}C^*/N_1 \tag{3}$$

$$\tau = (x_o^2 + Ax_i)/B \tag{4}$$

where D_{eff} is the effective oxidant diffusion constant in the oxide; k and h are the rate constants at the Si/SiO_2 and gas–oxide interface, C^* is the equilibrium concentration of the oxide species in oxide, N_1 is the number of oxidant molecules in the oxide unit volume, and x_i is the initial oxide thickness at the start of oxidation.

Two limiting forms of Eq. (1) can be noted. At long oxidation times, that is, $t \gg A^2/4B$ and $t \gg \tau$,

$$x_o^2 = Bt \tag{5}$$

This equation represents a parabolic oxidation, and B is the parabolic rate constant. For short oxidation time, $t \ll A^2/4B$, the linear oxidation expression is obtained:

$$x_o = B/A(t + \tau) \tag{6}$$

where B/A is the linear rate constant.

From Eqs. (2) and (3), it can be noted that when the oxidation process is controlled primarily by the parabolic rate constant (at high temperatures or thick oxides), the kinetics are affected by changes in the diffusion process or oxidant solubility in the oxide. The latter is proportional to the ambient pressure. On the other hand, at low temperatures or for thin oxides, where the linear rate constant predominates, the oxidation is also sensitive to oxidant solubility in the oxide (and ambient pressure) but depends on those factors affecting the interface rate constants h and k.

Proposed Models for Thin Dry Oxidation

Space Charge/Electrical Effects (6–8). Electrochemical [Deal and Grove (6)], oxygen vacancy [Hu (7)], and positive oxide charge [Schafer and Lyon (8)] fall into the space charge/electrical effects classification. A number of observed effects initially made this type of mechanism attractive for explaining the initial deviation from the linear-parabolic expression.

Structural Effects (9,10). The oxide structural effects category includes micropores (9) and blocking layer models. While these mechanisms are feasible, the difficulty in observing and

identifying them from other defects and impurities makes it difficult to support this concept.

Stress Effects (10). Many investigators have provided evidence that stress effects in thermally oxidized silicon can play an important role in the kinetics of silicon thermal oxidation—especially in the early stage. This phenomenon is also undoubtedly related to the break observed in the activation energy plot of the parabolic rate constant at about 950°C.

Silicon Surface and Substrate Effects (11,12). Some very interesting observations have been reported regarding effects of preoxidation cleaning treatments on dry O_2 oxidation kinetics. Likewise, other possible contributors to kinetic deviation due to dissolved oxygen or silicon structure have been proposed. While these models are somewhat speculative, there is little question that the nature of the silicon itself is extremely important and can have considerable effect on subsequent oxidation processes.

Parallel Oxidation Processes (13). An oxidation process that initially incorporates two separate but parallel reactions has been proposed to account for the so-called "rapid" oxidation observed for the 0 nm to 30 nm range of silicon oxidation in dry O_2. This model used a modified linear-parabolic growth law and takes the form

$$dx_o/dt = B_1/(2x_o + A_1) + B_2/(2x_o + A_2) \tag{7}$$

where B_1, B_2 and A_1, A_2 are the respective values of the constants in Eq. (1) for processes 1 and 2. Initially, for very thin oxides, one of the two parallel processes controls the oxidation process. It may be based on a parabolic mechanism. Fairly rapidly, the second parallel process "takes over" and the kinetics are in the linear regime of the linear-parabolic expression.

It has been observed that such a parallel growth law satisfies dry O_2 oxidation data over a wide range of thicknesses and temperatures. Han and Helms (13) have proposed that the second parallel reaction contribution to the oxidation kinetics in the thin region may be a diffusion reaction of a species such as atomic oxygen or an oxygen vacancy. It is also possible that the parallel model may be related to several of the other proposed mechanisms.

Review of SiO_2 Structure and Chemistry (14,15)

The basic bonding unit for all allotropic forms of SiO_2 except stishovite is the SiO_4 tetrahedral shown in Fig. 1(a). Each silicon is surrounded by four oxygen atoms in a tetrahedral geometry with the silicon–oxygen distance ranging from 0.152 nm to 0.169 nm; the O–Si–O bond angle is the tetrahedral angle 109.18°. The bonding configuration around the oxygen is illustrated in Fig. 1(b). Each oxygen is bonded to two silicon atoms with the bond angle varying from 120° to 180°.

The basic properties of silicon indicate that the formation of bonds in SiO_2 should be based on the silicon sp^3 hybrid orbital. Even though this is certainly a good starting point, the bonding is definitely more complicated. This was noted early by Pauling in deriving the atomic radii of the elements. Using Pauling's atomic radii, the nearest-neighbor distance is the simple sum of the radii of the constituents. For SiO_2 the sum of the covalent radii is 0.183 nm compared with the 0.162

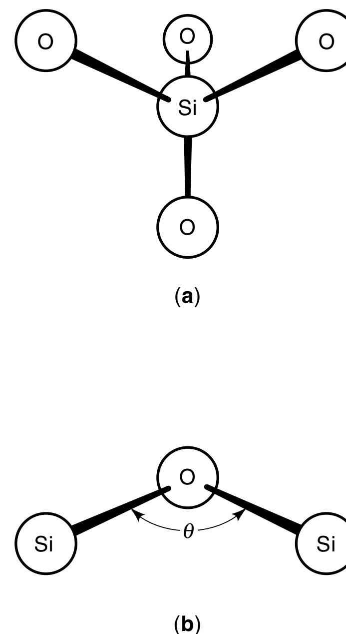


Figure 1. (a) SiO_4 structural unit of most forms of SiO_2 showing tetrahedral coordination. (b) Si_2O bonding configuration with the Si–O–Si bond angle θ varying from 120° to 180°, depending on the form of SiO_2.

nm actually observed in the more common forms. This is probably due to the fact that silicon in the atomic form has low-lying unfilled $3d$ electronic levels. These levels are available for bonding to the otherwise nonbonding p orbital of the oxygen (or fluorine, etc.). The Si–O–Si bond angles observed in the various forms of SiO_2 are also indicative of the complicated nature of the bonding in SiO_2.

In addition to the oxygen s interaction and the silicon $3d$ oxygen $p\pi$ bonding contribution, the additional non-nearest-neighbor repulsive interactions due to the partial ionic character of SiO_2 are probably responsible for these effects. The importance of non-nearest-neighbor interactions becomes obvious if we look at the distances between non-near-neighbor atoms in the various forms of SiO_2. Figure 2 shows an Si_2O_7 building block for SiO_2 for which the Si–O–Si bond angle is shown as a variable.

Intrinsic Defects in These Structures: Broken-Bond Configurations

One important constraint placed on the idealized models of the Si/SiO_2 interface that is never achieved in practice is that

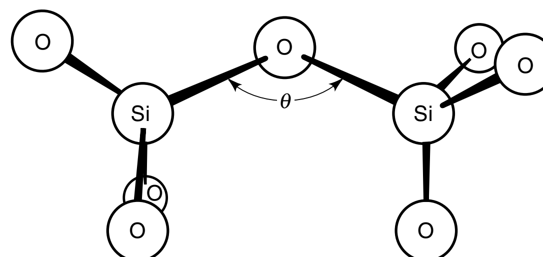


Figure 2. Si_2O_7 structural unit of SiO_2 with the angle between the two corner-sharing tetrahedra shown as a variable.

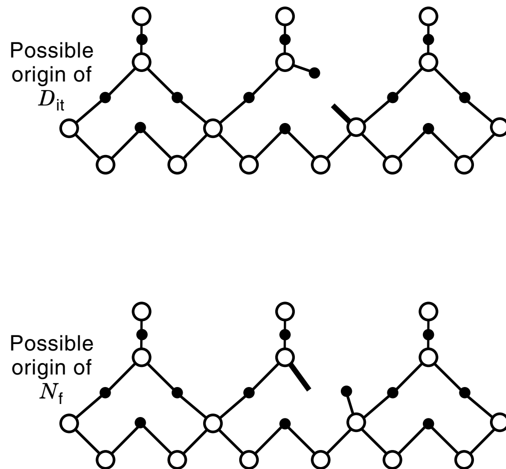
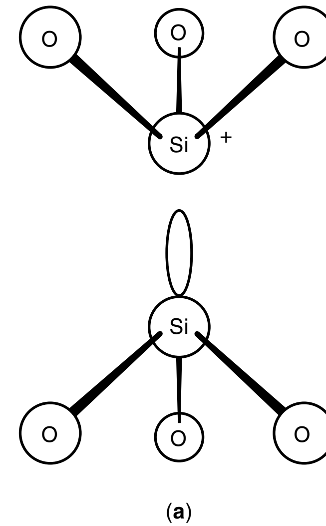


Figure 3. Examples of the possible structure of broken-bond defects at the Si/SiO_2 interface.



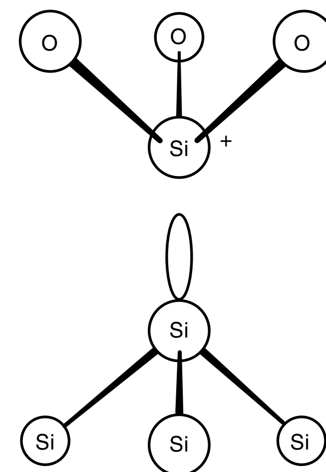


Figure 4. (a) Model of the broken bond-defect believed associated with the E' center in SiO_2. (b) Related defect at the Si/SiO_2 interface that would appear as a P_b center in ESR spectra.

there be no broken bonds or impurities present in the interface region. It is difficult to separate these two effects in actual device structures since broken bonds at the interface almost certainly attract impurities, especially hydrogen.

Of all the defects postulated to occur, only one has been experimentally verified: the silicon center bonded to three other silicon atoms. This center was first observed by Poindexter and co-workers using electron spin resonance (ESR) (16). They found that thermally oxidized silicon exhibited an ESR signal previously designated as the P_b center, which is also observed in damaged silicon and is undoubtedly due to the unpaired spin of a silicon dangling bond but with the atom otherwise bonded to other silicon atoms (see Figs. 3 and 4). By successive etches of the SiO_2, they demonstrated that this center was located near the Si/SiO_2 interface and found concentrations up to $2 \times 10^{12}/cm^2$.

Oxide Charges

Fixed Oxide Charge Q_f. As indicated in Fig. 5, the fixed oxide charge is positive and located in the oxide very close to the Si/SiO_2 interface (17,18). It is due primarily to structural defects (ionized silicon) in the SiO_2 lattice and directly dependent on conditions of oxidation. For instance, its density, which ranges from $10^{10}/cm^2$ to $10^{12}/cm^2$, depends on oxidation ambient and temperature, anneal and cooling conditions, and silicon orientation. Its density normally does not vary with surface potential, which distinguishes it from interface trapped charge—hence the name fixed oxide charge.

An important Q_f process relationship is that the density of Q_f for either steam or dry O_2 oxidation increases with decreasing temperature (18). However, a subsequent anneal in an inert ambient such as argon will decrease the density of Q_f to a minimum equilibrium value. Another important property of fixed oxide charge is that its effective density can be increased by the application of high negative fields to field plates of an MOS structure at moderate temperatures (100° to 400°C). This increase is proportional to the applied field as well as the initial Q_f. The interface trapped charge density also increases as a result of negative field application. Such an effect can lead to instabilities in p-channel MOS devices.

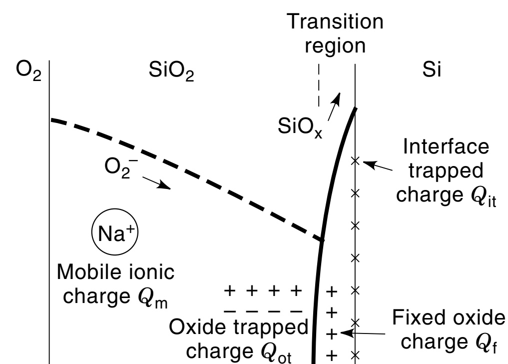


Figure 5. Names and location of charges associated near the silicon–SiO_2 interface.

Mobile Ionic Charge Q_m. The mobile ionic charge is primarily due to the positive alkali-metal ions, Li^+, Na^+, K^+, and also possibly H^+. In addition, it is possible to observe charge effects due to the larger negative ions such as F^-, Cl^-, and also Cs^+, Au^+. These latter ions normally do not migrate at typical device temperatures, however, and will not lead to instabilities. Likewise, their presence is more difficult to detect. The field-induced "drift" of the alkali-metal ions is the leading cause of instabilities in MOS devices and the rate of drift is inversely proportional to ion size ($Li^+ > Na^+ > K^+$).

Interface Trapped Charge Q_{it}, D_{it}. Closely related in physical origin to the fixed oxide charge, both charges arise from the formation of partially ionized silicon species during the thermal oxidation process. The main difference is that Q_{it} may be charged or discharged as a function of surface potential, while Q_f is not in electrical communication with the silicon and remains charged. Interface trapped charge does have many of the same process dependencies as Q_f, such as oxidation temperature, silicon orientation, and annealing conditions. One significant difference between the two charges, however, is that interface traps can be complexed at low temperatures (300° to 500°C) with an active hydrogen species and thus their effective density is reduced significantly. As-oxidized Q_{it} (D_{it}) densities are normally in the $10^{12}/cm^2$ range, while after a 400°C forming gas anneal their values drop to below $10^{10}/cm^2$.

Oxide Trapped Charge Q_{ot}. The fourth type of oxide charge is due to the presence or generation of trapped holes or electrons in the oxide. Generally these are produced by ionizing radiation, avalanched junction high currents through the oxide, or other reactions that either break Si–O bonds in the oxide or otherwise lead to carrier trapping on sites or traps already present in the oxide. Charge trapping, either due to ionizing radiation or the presence of high fields leading to avalanching, has been cause for concern in the past and will be even more of a problem as device geometry shrinks and radiation producing processes are employed.

Condition of the Silicon Surface Before Oxidation

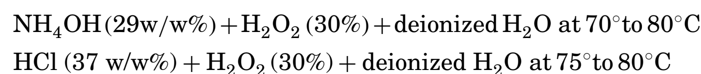
The crystal lattice at the surface is disrupted compared to the bulk silicon substrate. The degree of lattice strain and roughness varies substantially. Due to the very high affinity of silicon for oxygen, the silicon surface in a normal ambient in terms of pressure, temperature, and composition is always oxidized to form an oxide 5 Å to 15 Å thick. The chemical content of the native, spontaneously grown oxide is difficult to determine as it varies significantly depending on the treatments given to the surface, ambient conditions, and methods of wafer handling. In general, it is nonuniform across the depth of the film and in average does not reach the SiO_2 stoichiometry. Besides Si–O bonds and unoxidized silicon, the native oxide also includes Si–H and Si–OH groups (19). To complicate the situation even further, the vulnerability of the silicon surface to either physically or chemically absorbed contaminants accounts for one more destabilizing factor with a potentially profound impact on the subsequently grown oxide. Again, the nature and content of contaminants are to a great extent controlled by the process conditions and wafer handling prior to oxidation. The common contaminants of concern are organic compounds, such as hydrocarbon Si–CH groups, transition metals, and alkali-metal ions. Due to the nature of the treatments preceding thermal oxidation, which often involve an HF dip resulting in a hydrophobic surface, the role of fluorine in the chemistry of silicon surface during oxidation should be also considered.

All the above contaminants are enclosed within the native oxide and near-surface region of silicon. Beside these atomic scale contaminants, the particles of various sizes and composition are encountered even in the cleanest oxide fabrication environment. The submicron-size particle, once allowed to contact the surface, is very difficult to remove since the total force of this adhesion exceeds gravitational force by factors greater than 100. Clearly, even the smallest particle will eventually lead to oxide failure, usually observed by low-field breakdown. Therefore, protection of the silicon surface before oxidation against particles is a necessity. The role of the features of the silicon surface subsequently subjected to thermal oxidation cannot be generalized as it will depend on the response of each of them to the heat treatment and progressing surface penetration by the growing oxide. Typically, each can have a measurable effect on either the oxide growth kinetics or properties of an oxide and Si/SiO_2 interface, or both.

The objective of wafer cleaning is the removal of particulate and chemical impurities from the semiconductor surface without damaging or deleteriously altering the substrate surface. Dry-physical, wet-chemical, and vapor-phase methods can be used to achieve these objectives. An array of equipment is available for implementing the various processes for industrial applications.

The traditional approach of wafer cleaning is based on wet-chemical processes, which use mostly hydrogen peroxide solutions. Successful results have been achieved by this approach for the past 25 years. However, the relatively large consumption of chemicals required by these processes, the disposal of chemical waste, and the incompatibility with advanced concepts in integrated processing (such as cluster tooling) are the main reasons why methods based on gas-phase cleaning are now being developed that are less affected by these limitations.

The original RCA cleaning (20) consisted of two cleaning solutions:



$$NH_4OH\,(29 w/w\%) + H_2O_2\,(30\%) + \text{deionized } H_2O \text{ at } 70^\circ \text{ to } 80^\circ C$$
$$HCl\,(37\ w/w\%) + H_2O_2\,(30\%) + \text{deionized } H_2O \text{ at } 75^\circ \text{ to } 80^\circ C$$

The purpose of the first step, known as Standard Clean 1 or SC-1, is to oxidize surface organic films and remove some metal ions. The second step, known as Standard Clean 2 or SC-2, is to remove alkali-metal cations and other cations like Al^{3+}, Fe^{3+}, and Mg^{2+}. The solutions were mixed typically in the ratio 1 : 1 : 5.

Much attention has been given to the wafer-cleaning process, but the drying of the clean wafers is equally critical. In fact, wafer drying may be the most important step for ensuring that a cleaning process is successful in eliminating contamination. The drying process must remove water from the surface before it can evaporate and leave residue behind. There are three basic drying mechanisms: physical separation as in centrifugal drying, solvent displacement of deionized (DI) water followed by solvent removal as in vapor drying, and evaporation as in hot-water drying techniques.

The most widely used wafer-cleaning methods in very large scale integration (VLSI) and ULSI silicon circuit fabrication are still, after 25 years, the hydrogen peroxide–based wet-chemical processes. High-purity reagents are now available, such as aluminum-free H_2O_2, that have led to improved performance results. However, the concentration of ammonium hydroxide in the original RCA SC-1 solution (5 : 1 : 1 H_2O–H_2O_2–NH_4OH) has been reduced by at least fourfold to avoid microroughening of the silicon surface by nonuniform microetching, resulting in improved gate oxide integrity and increased yields of MOS capacitors. It is also advisable not to exceed 70°C for 10 min of the RCA SC-1 or SC-2 wafer cleaning treatment. Removal of the native or chemical oxide film before and after SC-1 and SC-2 treatments by optimized etching with dilute (1 : 50 to 1 : 100) ultrapure HF solution can be beneficial. Remarkable results have also been achieved by wet-chemical cleaning of silicon wafers with aqueous solutions of chlorine–H_2O_2–surfactant, H_2O–HF–HCl, and H_2O–H_2O_2–HF. New techniques of wafer drying have been devised of which isopropyl alcohol vapor drying after cold DI water megasonic rinsing is one.

While the use of advanced wet-chemical cleaning techniques for producing ultrapure silicon wafers will persist for at least several more years, the trend is toward a shift from liquid to gaseous reactants for several reasons. Removal of oxide layers by HF vapor-phase etching is now well established, and the elimination of organic contaminants by UV or ozone has been amply demonstrated. Processes for removing trace metals by vapor-phase analogs of SC-1 and SC-2 treatments are being pursued vigorously.

OXIDATION TECHNIQUES AND SYSTEMS

Thermal oxidation of silicon is normally carried out in a fused quartz tube in a resistance-heated furnace. The silicon wafers are placed vertically in slots in a flat quartz “boat,” most present-day furnaces accommodating up to 200 wafers. For dry O_2 oxidation, high-purity oxygen from a liquid source is transported into the furnace tube through suitable regulators, valves, traps, filters, and flow meters. For a number of years, water or steam oxidation was carried out by bubbling O_2 or N_2 through a flask of deionized water maintained at a particular temperature. Thus, a specified vapor pressure of water could be provided in the oxidizing ambient. More recently, however, pyrogenic systems have been employed that permit H_2 to react with O_2 at the inlet end of the oxidation tube, thus providing water vapor of much higher purity and control.

Atmospheric oxide growth, the most commonly used technique, is typically carried out in a horizontal diffusion tube, although vertical diffusion furnaces are being used more frequently. In the case of the horizontal furnace, the wafers are held vertically in a slotted paddle (boat), which is normally loaded using cassette-to-cassette equipment. Typical oxidation temperatures range from 700° to 1150°C and should be held to within ±1°C to ensure uniformity. In a standard procedure the wafers are chemically cleaned, dried, loaded onto the paddle, and automatically inserted into the 700° to 900°C furnace, which is then ramped up to oxidation temperature. Ramping is used to prevent wafer warpage. Following oxidation, the furnace is ramped down and the wafers are removed.

The major new development in oxidation equipment is vertical diffusion furnaces, which have the processing tube in the vertical position. The wafers can be loaded from either the top or bottom, depending on the system, and are horizontal during oxidation, facing either up or down. In certain systems the wafers can be rotated to provide better uniformity. The claim of these systems is that they provide excellent thickness uniformity and low particle density. The quoted temperature uniformity range from ±0.25° to ±1.0°C along the flat zone with oxide uniformity in the ±1% range. In some systems the heating element can be moved relative to the wafers, allowing rapid cool down. Wafers in the vertical systems are usually supported at three or four points or fully supported around most of the periphery.

Oxidation Process Description

After the conventional preoxidation cleaning described in the preceding section oxidation is usually done in a four-zone resistance heated furnace (vertical or horizontal) that utilizes a quartz or SiC tube. Temperature and gas-flow ratio controls and sequencing for predetermined time intervals are done automatically by the furnace microprocessor. The temperature within the flat zone are maintained within ±0.2°C over a length of 150 cm during oxidation (800° to 950°C). Figure 6 shows schematically a generalized thermal schedule and gas flow sequence for SiO_2 growth. This schedule essentially have six stages (21):

1. Boat travel-in (horizontal) or tower pushing (vertical) into the furnace and temperature stabilization at 600° to 750°C in 1% to 10% O_2 diluted N_2 ambient
2. Ramp-up to oxidation temperature T_{ox} (typically 5° to 10°C/min for a conventional furnace and 50° to 100°C/min for a fast-ramp furnace) in 1% to 10% O_2 diluted N_2 ambient
3. Temperature stabilization (15 min to 30 min) and preoxidation anneal in 1% to 10% O_2-diluted N_2 ambient at T_{ox} (800° to 950°C)
4. Oxidation at T_{ox} in oxidizing Cl-containing ambient (O_2, 25% to 100%; Cl, 0% to 5%; balanced N_2)
5. Postoxidation anneal in N_2 for 15 min to 45 min at T_{ox}
6. Ramp-down in N_2 (2° to 3.5°C/min for a conventional furnace and 50°C/min for a fast-ramp furnace) to 600° to 750°C

The ambients during stages (1) and (2) are mildly oxidizing as a 100% inert ambient often results in silicon etching and contamination during ramp-up. 100% O_2 during ramp-up results in a higher amount of (>40 Å) inferior-quality SiO_2 growth that is undesirable for thinner gate oxides (<100 Å) (22,23). During ramp-up to T_{ox} there used to be a overshoot of 3° to 4°C; however, using a model-based temperature controller this overshoot can be reduced to less than 0.5°C. This preoxidation anneal at T_{ox} (15 min to 30 min) minimizes local variation in the strain field near the silicon surface during the initial stages of SiO_2 growth. The addition of Cl^--bearing species in the reactant gas phase during oxidation reduces the following:

1. The concentration of mobile ions
2. Oxidation-induced stacking faults in the underlying Si
3. Oxide defects

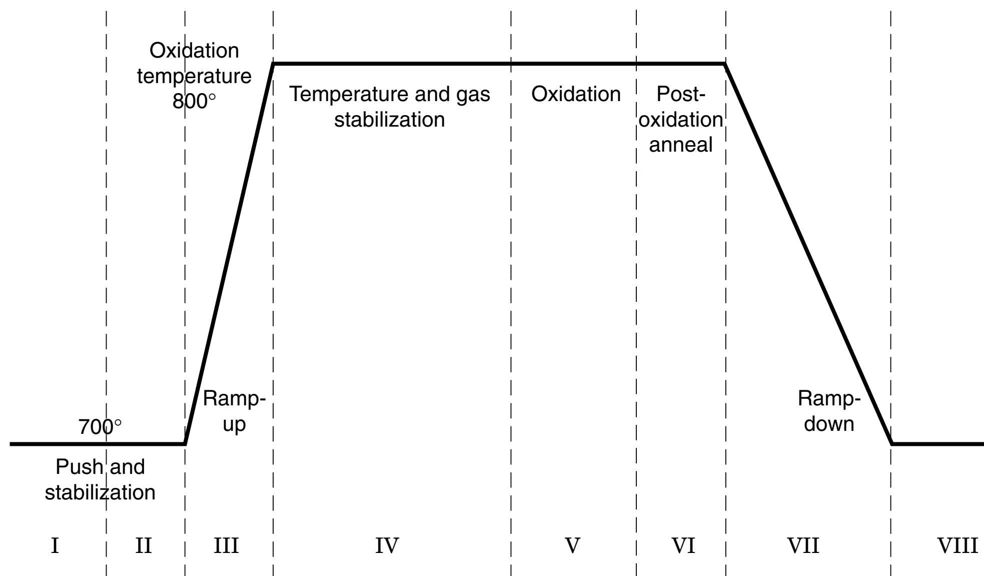


Figure 6. A typical gate oxide process in an atmospheric furnace. The solid line indicates the temperature cycle.

Modern clean rooms have minimum mobile ion contamination problems. Therefore, we are reducing Cl^- concentration in the ambient as excess Cl^- often causes silicon surface pitting and increases oxide trapped charge.

Recently, lightly nitrided SiO_2 has drawn much attention as a candidate for submicron devices (22–25) due to its improved reliability, robustness to ULSI processing, and resistance to boron diffusion from poly-Si in *p*-gate metal oxide–semiconductor (PMOS) devices. In particular, much attention has been paid to oxynitridation process using N_2O due to process simplicity. Several groups have reported nitrogen incorporation in thin SiO_2 films through rapid thermal processing (RTP) (23,25). For smaller amounts of nitrogen incorporation (<3%) near the interface, conventional low-thermal-budget (800° to 900°C) furnace oxidation is attractive for its process simplicity and in generating gate oxide with superior breakdown, wear-out, endurance, and hot-carrier resistance characteristics without compromising on charge-trapping behavior (22,24). This N_2O/O_2 oxidation is appealing since nitrogen incorporation in SiO_2 is simply a perturbation to conventional gate oxide (GOX) process. Furthermore, N_2O/O_2 oxidation is relatively self-limiting compared to a conventional O_2 oxidation. This results in a better GOX thickness uniformity and easy implementation for manufacturing.

The postoxidation anneal at T_{ox} in N_2 ambient is to control fixed charge (Q_f) and breakdown field distribution within SiO_2. For many new low-thermal-budget oxidation process this step can be omitted since during poly-Si/amorphous-Si deposition and doping the gate oxide is subjected to sufficient thermal treatment to reduce Q_f. This postoxidation annealing step can be done in N_2O or NO to grow the last 0.5 nm to 1.0 nm oxide at a much smaller growth rate for ultrathin GOX (<6.5 nm). This light nitridation (<2% N) near the interface not only generates better-quality oxide (leakage and wear-out) but also improved oxide thickness uniformity (<1%) than conventional oxidation.

Grow–Deposit–Grow Stacked Oxide (26)

The stacked gate oxide synthesis process involves a three-step process sequence of growing, depositing, and growing SiO_2 layers by thermal oxidation, chemical vapor deposition, and densification/oxidation, respectively.

The First Layer—Thermally Grown SiO_2. Thermally grown SiO_2 passivates the semiconductor silicon surface more than any other kind of deposited oxide film. *Passivation* is the reduction of the number of surface states (10^{15} cm^{-2}) arising from unsatisfied chemical bonds at the free surface of Si. Thermal oxidation of Si lowers the number of dangling bonds to about 10^{10} states/cm^2 with the formation of a very stable SiO_2, and the first layer of the stacked oxide therefore is grown thermally [Fig. 7(a)].

The Second Deposited SiO_2 Layer. The passivation of a silicon surface is no longer critical after the growth of the SiO_2 layer, and surface-state generation is minimized when the deposited second SiO_2 layer is stacked on the first grown layer [see Fig. 7(b)]. More importantly, the second layer must be deposited rather than grown if it is to form a virtual interface that reduces effective defect density (D_o) and acts as a stress-accommodating layer (26). Thin SiO_2 films are usually deposited by low-pressure chemical vapor deposition (LPCVD) methods from oxidation of silane (SiH_4) with oxygen or nitrous oxide (N_2O) or from pyrolysis of tetraethyl orthosilicate [TEOS, $Si(OC_2H_5)_4$].

The Third Grown Layer—Oxidation/Densification. The final step of the synthesis is to grow a third SiO_2 layer underneath the first grown layer by an oxidizing reaction at the interface. This occurs during densification oxidizing anneal. The newly grown SiO_2 is structurally superior because the growth occurs in near-equilibrium condition in the presence of a stress-accommodating virtual interface layer (26) between the depos-

ited and thermally grown SiO_2 layers. The newly formed Si/SiO_2 interface [Fig. 7(c)] is structurally smoother with very little local stress variation and interfacial asperities. Furthermore, the interface states do get annealed during densification, and the stacked oxide structures therefore have superior charge-trapping characteristics (26).

There are three major advantages for the stacked oxide approach: (1) mismatch of the micropores present in the thermal oxide and the CVD layer reduced the defect density dramatically; (2) silicon substrate consumption is less than conventional thermal gate oxide and thus fewer substrate defects are incorporated into the bottom thermal oxide; and (3) stress compensation between the bottom thermal oxide layer and the CVD layer reduces the stress at the thermal oxide–silicon substrate interface.

These advantages make the stacked gate oxide very attractive for submicron technology. The benefits are clearly shown in Fig. 8, the breakdown voltage histograms of submicron static random access memory (SRAM) array capacitors comparing the thermal oxide and stacked gate oxide. (27). The 4 times lower incidence of low-voltage failures for the stacked dielectric is similar to the improvement observed for area capacitors.

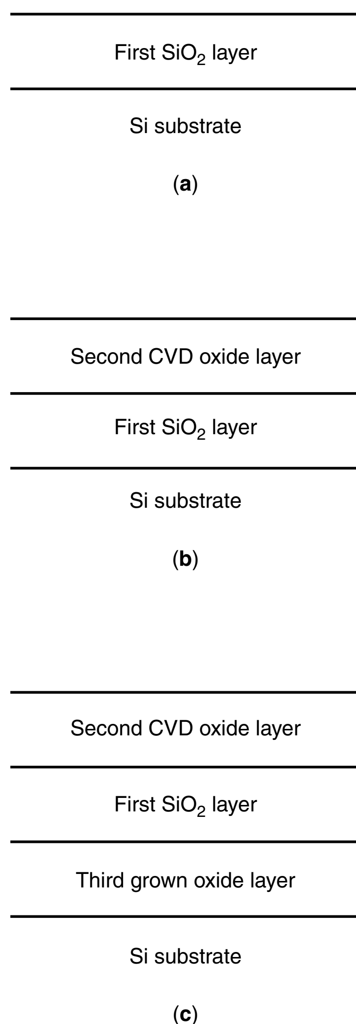


Figure 7. Three-step grow–deposit–grow gate stack formation steps. (a) First step, oxide layer formed by thermal oxidation. (b) Second step, oxide layer formed with CVD process. (c) Third step, oxide layer formed at the SiO_2/Si interface, while densifying the second-layer CVD oxide.

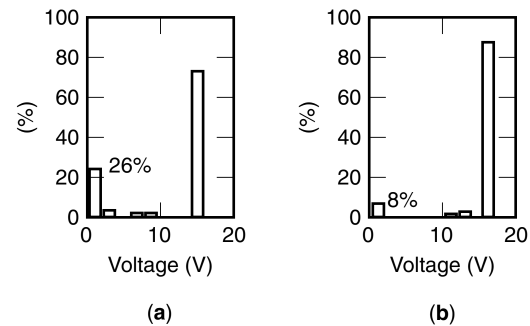


Figure 8. Breakdown histograms for 512K SRAM defect array. (a) Thermal gate oxide. (b) CVD stacked gate oxide densified at 950°C.

Process-induced damage of gate oxide or of the Si/SiO_2 interface may result in device degradation problems such as threshold voltage scatter. The problem is especially pronounced for submicron technology. In addition to offering a low-area defect density, a stacked gate oxide decreases process-induced device degradation dramatically. Figures 9 and

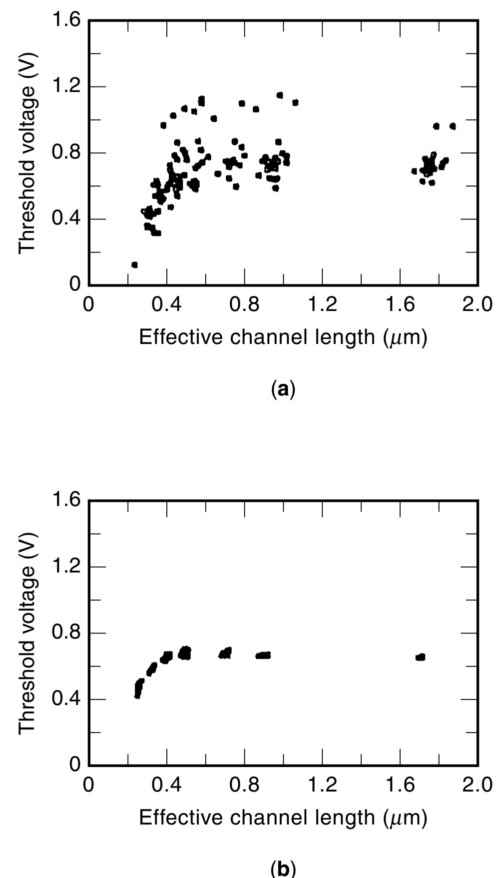


Figure 9. Effects of via-etch-induced damage on NMOS threshold-voltage roll-off. (a) Thermal gate oxide. (b) CVD stacked gate oxide densified at 950°C.

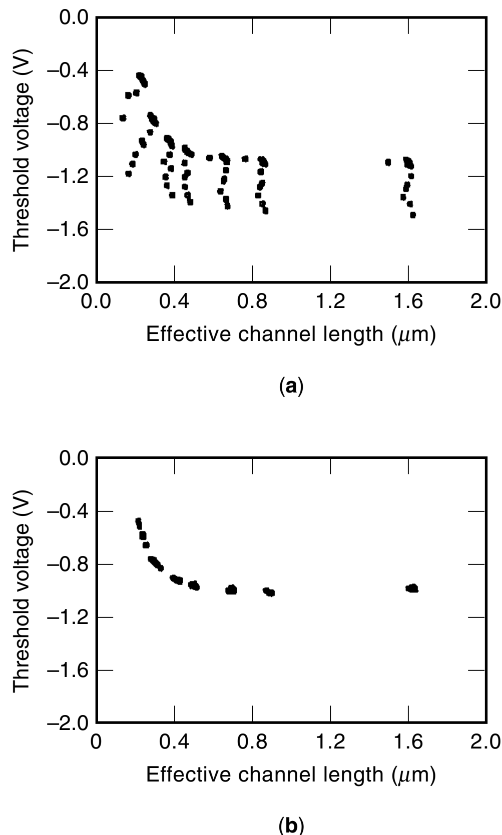


Figure 10. Effects of via-etch-induced damage on PMOS threshold-voltage roll-off. (a) Thermal gate oxide. (b) CVD stacked gate oxide densified at 950°C.

10 show the threshold-voltage roll-off for NMOS and PMOS devices, respectively, under conditions of severe via-etch-induced degradation. In contrast to the gross threshold-voltage scatter observed for the thermal gate oxide, the stacked gate oxide shows a very tight distribution. The data presented here were obtained during abnormal via etch conditions and therefore serve to demonstrate the increased margin provided by the stacked gate oxide.

Because the stress in silicon near the Si/SiO_2 interface for the stacked oxide is much smaller than that of the thermal oxide (26), the midgap interface state density (D_{it}) for the stacked oxide is 4 times smaller and has a 10 times smaller standard deviation as shown in Fig. 11. It is speculated that the low-stress interface of the stacked gate oxide is less prone to damage induced by an abnormal via etch, therefore resulting in less threshold-voltage scatter and lower D_{it}. This interpretation is supported by the C–V results as shown in Fig. 11. The quasistatic C–V curves are measured for p-well area capacitors (6.25×10^{-4} cm^2) before and after Fowler-Nordheim (FN) stressing at -0.01 A/cm^2 current density for 10 sec. In addition to the higher degree of distortion after FN stressing, the thermal oxide results in a higher negative shift for the high-frequency C–V curve than that of the stacked gate oxide. The larger negative shift of high-frequency C–V curves for the thermal gate oxide suggests that more positive charge is accumulated in the thermal oxide than in the stacked gate oxide after stressing. Because of the stress compensation between the CVD layer and the thermal oxide layer, the stress in the silicon substrate and the oxide near the Si/SiO_2 interface for the stacked gate oxide is much smaller than that of the thermal oxide (27).

The improved resistance of stacked gate oxide devices to process-induced damage is also demonstrated (27) with hot-carrier stressing of discrete transistors. n-channel transistors with a 25/0.7 drawn width/length ratio were stressed for a period of 500 min. under various gate and drain bias conditions. In Fig. 12, shifts in the linear extrapolated threshold voltage with time at 6.0/2.3, V_{drain}/V_{gate} ratio, are shown for both gate oxide processes. The transistors with the thermal oxide are clearly much more susceptible to hot-carrier-induced threshold-voltage degradation, shifting over 100 mV during stressing. The devices with the stacked gate oxide are much more robust, exhibiting negligible shifts in threshold voltage. Because the stacked oxide is not damaged by the via etch, the devices are less susceptible to hot-carrier injection damage, and this results in a negligible threshold-voltage shift under the same stressing condition. In addition to an enhanced electron-trapping efficiency, the transistors with thermal oxide are also more susceptible to the hot-carrier-induced interface state creation. This is demonstrated by comparing the degradation in the inverse subthreshold slope, a measure of change in interface-state density, under hot-carrier stressing. As can be seen in Fig. 13, the transistors with the thermal oxide were much more susceptible to degradation in the inverse subthreshold slope at a V_{drain}/V_{gate} ratio of 6.0/

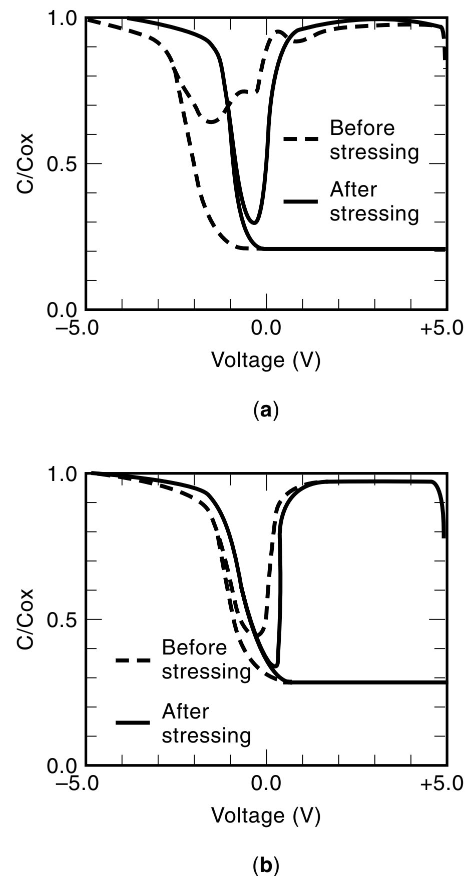


Figure 11. Fowler-Nordheim stressed midgap interface-state density. $Q_{inj} = 0.1$ C/cm^2. (a) Thermal gate oxide. (b) CVD stacked gate oxide densified at 950°C.

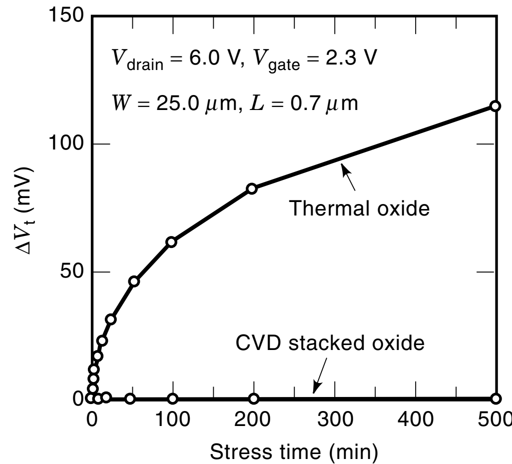


Figure 12. Subthreshold characteristics of stacked and conventional gate oxide transistors.

2.3 (27). This is consistent with the more robust interface provided by the stacked gate oxide.

Conventional stacked oxidation involves a three-step synthesis of growing, depositing, and growing oxides in three separate furnace operations. This process generates high-quality oxides but suffers from some important manufacturing issues, such as throughput, cycle time, and cost. Furthermore, the first grown oxide (2.0 nm to 7.5 nm) for the conventional stacked oxide is done in an atmospheric furnace typically at 800° to 1000°C. Under such conditions, control of growth rate and thermal and stress budgets become serious issues in the ultrathin (1.0 nm to 2.5 nm) regime. A single-cluster step stacked oxide process (28) has been achieved recently through a low-pressure (<2 Torr) Si oxidation at lower temperatures (600° to 750°C) to attain ultrathin (<6.5 nm), high-quality oxides that are robust and manufacturable for sub-0.5-μm complementary metal-oxide semiconductor (CMOS) and bipolar CMOS (BiCMOS) technologies and their enhancement modules. Figures 14 and 15 show some of the device characteristics of the stacked oxide processed through the single-furnace-cluster stacking sequence.

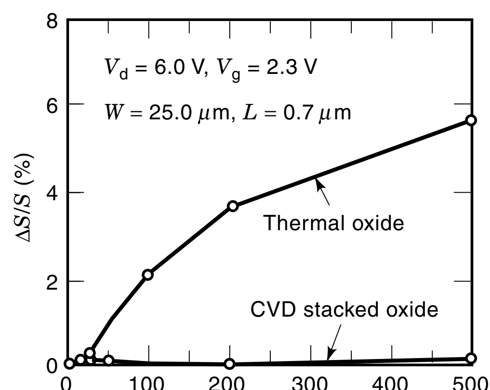


Figure 13. Inverse subthreshold slope shift ($\Delta S/S$) after hot-carrier–injection stressing.

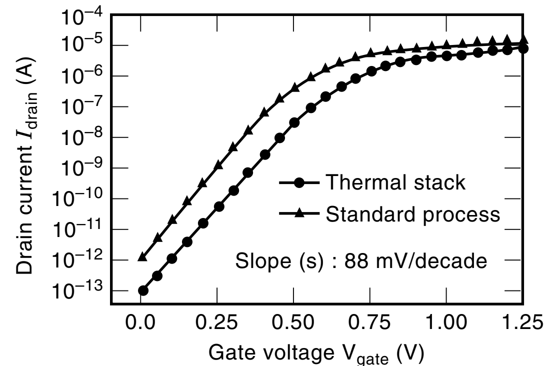


Figure 14. Comparative Drain Current characteristics for stacked and conventional gate oxide.

ELECTRICAL CHARACTERIZATION OF THE GATE OXIDE

There has been a strong demand for advances in electrical characterization of gate oxides. Capacitance–voltage (*C–V*), current–voltage (*I–V*), and full-flow device characterization require significant processing before the information becomes available. Noncontact characterization has the ability to speed process development in research and development facilities and to reduce the amount of product at risk in a manufacturing environment. The cost benefits of wafer reuse are also clear: metal contamination concerns usually prevent reuse of electrical test wafers, but noncontact techniques allow immediate reuse of wafers.

Quantox® Corona Oxide Semiconductor Technology (29,30)

The technique presented in this section uses a combination of charge deposition, noncontact voltage measurement, and surface photovoltage response to build a quasistatic sweep similar to that from a low-frequency *C–V* plotter. The technology is called corona oxide–semiconductor (COS) to emphasize the similarity to metal-oxide–semiconductor (MOS) charge analysis. Charge-pulsed measurements are also possible with COS, allowing the measurement of near-surface doping and minority-carrier generation lifetime in a fashion similar to pulsed MOS analysis.

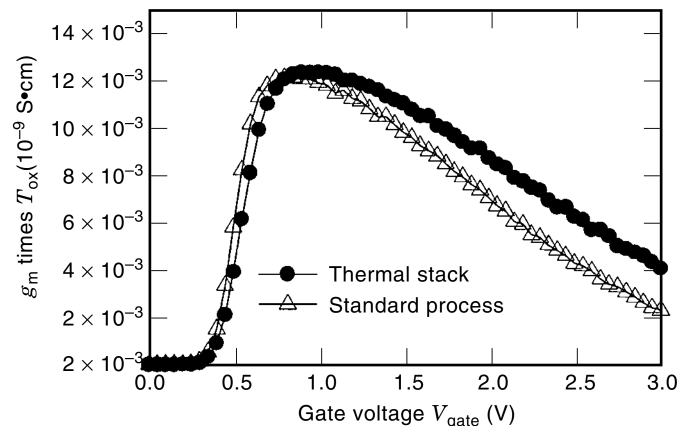


Figure 15. Variation of transconductance (g_m) with gate voltage for stacked and conventional gate oxides.

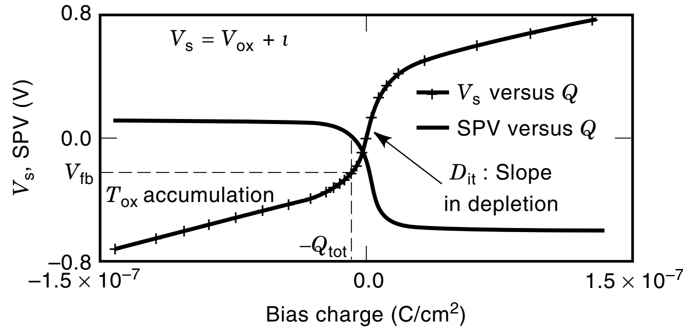


Figure 16. Raw data from a 67 Å SiO_2 gate oxide: T_{ox} = 66.8 Å, V_{fb} = −0.257 V, D_{it} = 5.29 × 10^{10}/eV · cm², Q_{tot} = −1.87 × 10^{-8} C/cm².

Conventional C–V parameters are extracted from COS data as shown in Fig. 16. The bias charge (shown on the x axis) is generated by a high-impedance room air ionizer (the corona source). Air molecules are ionized and directed toward the sample surface, and each charge deposition, ΔQ, is measured by a coulombmeter connected in series with the wafer chuck. Typical bias sweeps extend from -1.5×10^{-7} C/cm² to $+1.5 \times 10^{-7}$ C/cm² (−0.5 MV/cm to +0.5 MV/cm), and the sweep range is dynamically adjusted to accommodate samples that exhibit high D_{it}.

The response of the sample is monitored using surface voltage (V_s) and surface photovoltage (SPV) measurements. After each small charge deposition, V_s is measured by a noncontact electrostatic voltmeter or *vibrating Kelvin probe.* Subsequent to the measurement of V_s, a pulsed light source is directed at the wafer. The resultant surface SPV is capacitively coupled to the probe, and the signal is analyzed to determine the silicon band bending. The surface voltage at SPV = 0 is reported as the flatband voltage: $V_{fb} = V_s|_{\psi=0}$. The magnitude of charge that is deposited to achieve the flatband condition is defined as total oxide charge, $-Q_{tot}$.

T_{ox} is extracted from the slope of the Q–V_s curve in accumulation. The procedure includes a second-order correction for the equilibrium band bending to improve accuracy on thin oxides (27). Dielectrics as thin as 20 Å have been measured using this technique with 3σ repeatability at less than 0.7 Å. The technique is significantly simpler than conventional polycapacitor measurements, because there is no polysilicon depletion effect or probe punch-through, and the COS technique is not as sensitive to leakage through oxide pinholes. The oxide resistivity in strong accumulation, ρ_{ox}, is also determined during the sweep shown in Fig. 16, and a quasistatic analysis of the Q–V_s curve yields the density of interface traps (D_{it}) using the Berglund method:

$$D_{\text{it}} = \frac{1}{q}\left(\frac{dQ}{d\Psi}(\text{measured}) - \frac{dQ}{d\Psi}(\text{theoretical})\right) \tag{8}$$

The Quantox tool may also be used to measure high-field oxide leakage. In this application, bias charge densities as high as 9×10^{-7} C/cm² (E_{max} = 30 MV/cm) are applied in order to induce tunneling, Fig. 17. The maximum surface voltage is clamped by the tunneling of carriers through the oxide, and the tunneling field (E_{tun}) may be calculated:

$$E_{\text{tun}} = \frac{V_{s_{\max}} - \Psi_{\text{Si}} - \text{WF}}{T_{\text{ox}}} \tag{9}$$

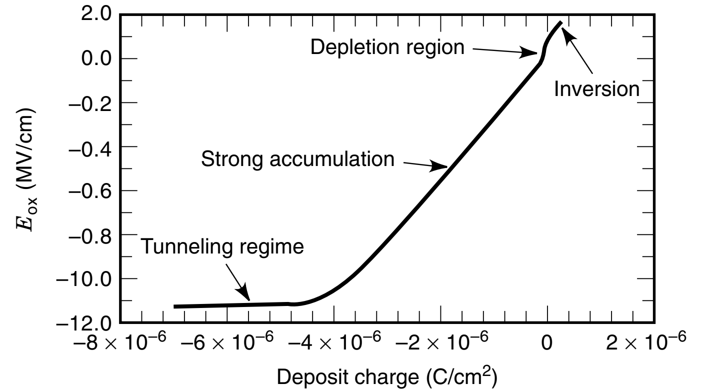


Figure 17. Cross-wafer uniformity (nine sites) of tunneling field (E_{tun}) on a 120 Å SiO_2 gate oxide. E_{tun} ranged from −11.3 MV/cm to 11.5 MV/cm (less than a 2% variation across the wafer).

In Eq. (9), WF is the probe to the silicon work-function difference and Ψ_{Si} is the band bending.

Near-surface doping (N_{surf}) is measured using a pulsed Q-V_s technique that is very similar to pulsed C–V techniques. The carrier generation lifetime (τ_{gen}) is also derived from the pulse into deep depletion, as outlined in Fig. 18. Photon-injected carriers are used to bring the junction out of deep depletion rapidly. The final recovery from forward bias back to the equilibrium condition is used to measure the surface recombination lifetime (τ_{sr}).

In-Process Oxide Zone Tester (24,26)

These testers are short-loop gate oxide module testers to determine the leakage, breakdown, tunneling, and wear-out characteristics of the gate oxide. Figure 19(a) describes the physical and electrical schematics for measuring oxide leakage by a voltage ramp on large-area (0.1 cm²) capacitors. Tests were performed by applying a negative ramp, −1 V/s (negative polarity forces the capacitor into an accumulative regime), and measuring the leakage current as a function of applied bias until 100 μA was reached. The negative polarity with respect to p substrates forces the capacitor into accumulation. The setup recorded both self-healing and destructive events. To ensure high levels of confidence, typically 300 ca-

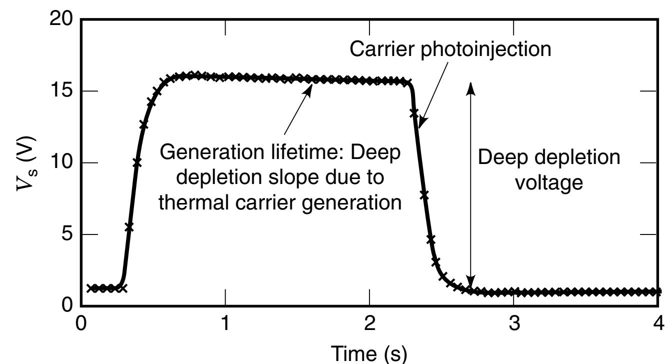


Figure 18. Analysis of near-surface doping and generation lifetime (p-type substrate, 40 Å thermal SiO_2 grown at 850°C with 1% dichloroethylene (DCE), τ_{gen} = 1194 μs, N_{surf} = 9.4 × 10^{14}/cm³). This technique works equally well on epitaxial samples.

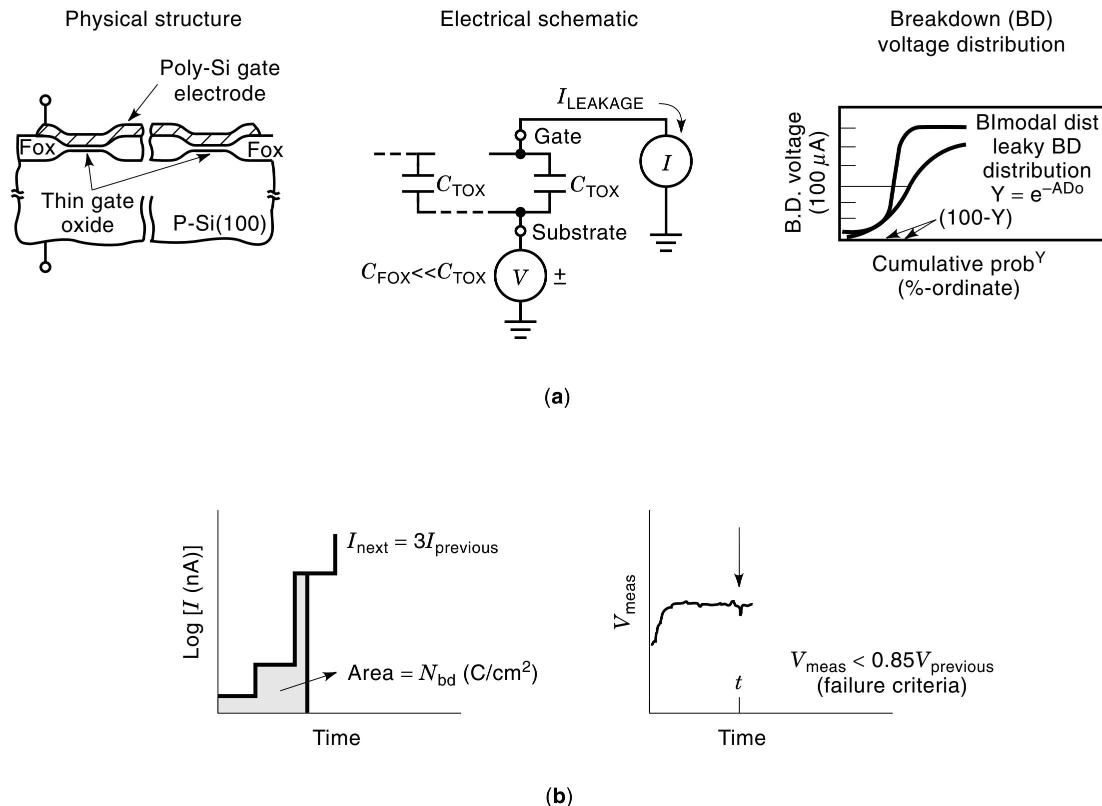


Figure 19. (a) Voltage ramp on a large-area test structure for measuring oxide leakage. (b) Current ramp on small-area capacitor structures for the accelerating aging test. The arrow on the right indicates the onset of dielectric breakdown.

pacitors (half the sites per wafer) are tested in each run. Results are described as probability distribution plots of the measured breakdown voltage for a 100 μA leakage criterion. D_o was calculated from the yield (Y) data [percentage of sites passed under ~8 MV/cm for an area (A) of 0.1 cm^2] from the equation $Y = e^{-AD_o}$.

These testers also have small-area thin oxide (TOX) capacitors (2.5×10^{-4} cm^2). These small-area capacitors can be subjected to a current ramp [see Fig. 19(b)] and the voltage across the capacitors is measured as a function of time, until failures in the oxide occur. A failure is arbitrarily defined when the measured voltage V_m across the capacitors is less than 85% of the previous value at time t. The area under the current ramp curve (log I versus t) at t_m is the charge to breakdown (log N_{bd}, C/cm^2) or the total charge fluence characteristics of the thin oxide. The tunneling voltage, V_{FN}, is evaluated as the reciprocal of the slope of the Fowler–Nordham (FN) tunneling curve. The breakdown voltage V_{bd} is estimated from the median of the voltage generated on all small-area GOX capacitors by forcing final current before destructive

Table 1. Electrical Characteristics of Conventional and Lightly Nitrided Gate Oxides

Oxide Thickness (Å)	Defect Density D_0 (no./cm^2)	Charge Fluence, log N_{bd} (C/cm^2)	Breakdown Voltage V_{bd} (V)	Tunneling Voltage V_{FN} (V)
Conventional Thermally Grown Oxides				
35	0.55	−0.57	6.51	4.58
50	0.35	−0.09	8.85	6.15
65	0.23	0.28	12.1	7.68
90	0.15	0.29	18.0	8.70
Lightly Nitrided Oxides (N_2O Postoxidation Anneal)				
35	0.47	−0.37	6.73	4.78
50	0.18	0.14	9.35	6.52
65	0.12	0.3	12.3	7.76
90	0.08	0.4	18.5	8.90

Table 2. Characteristics of Ultrathin Gate Oxides

	Defect Density D_0 (no./cm^2)	Charge Fluence, log N_{bd} (C/cm^2)	Breakdown Voltage, V_{bd} (V)	Tunneling Voltage, V_{tun} (V)
		35 Å		
O_2 grown	0.55	−0.57	6.51	4.58
N_2O annealed	0.47	−0.37	6.73	4.78
N_2O stack	0.25	−0.28	7.73	5.52
		50 Å		
O_2 grown	0.35	−0.09	8.85	6.15
N_2O annealed	0.18	0.14	9.35	6.52
N_2O stack	0.10	0.10	9.85	6.55
		65 Å		
O_2 grown	0.23	0.28	12.1	7.68
N_2O annealed	0.12	0.3	12.3	7.76
N_2O stack	0.05	0.31	12.53	7.70

rupture. Tables 1 and 2 show results of these in process testers for ultrathin conventional, lightly nitrided, and stacked oxides for various sub-0.5-μm CMOS technologies.

SUMMARY AND FUTURE DIRECTIONS

Process technologists thus far have successfully met the challenges of technology evolution in silicon ICs from 1.0 μm to 0.13 μm, especially in scaling thin gate oxide areas for the last few decades. This has been achieved through a leapfrog advance in both equipment and process technologies. Our understanding of oxidation kinetics, mechanisms, and Si/SiO_2 interface has led to significant improvements in oxide quality and generation of a myriad of interface engineered ultrathin gate oxides that are of very high quality and robust to aggressive IC processing.

There has been a strong demand for advances in electrical characterization. Conventional capacitance–voltage, current–voltage, and full-flow device characterizations require significant processing before the information becomes available. Noncontact characterization has the ability to speed process development and reduce the amount of product at risk in a manufacturing environment. The use of noncontact surface photovoltage characterization (COS) techniques provides cost-effective rapid feedback on dielectric quality, reducing costs through the reutilization of control wafers and the elimination of processing time. This technology has been applied to characterize most of the relevant C–V parameters, including the flatband voltage (V_{fb}), interface trap density (D_{it}), mobile charge density (Q_m), oxide thickness (T_{ox}), oxide resistivity (ρ_{ox}), total charge (Q_{tot}), and tunneling voltage (V_{tun}) for gate oxides.

Impacts of stacking and nitridation on leakage (D_o), breakdown (F_{bd}), wear-out (N_{bd}), and charge trapping behavior (D_{it} and Q_f) are more dramatic for thinner oxides in which Si/SiO_2 interface substructure plays a critical role. Stacked oxide synthesis generates a planar and stress-free interface and is more resistant to process-induced damage that causes variability in MOSFET parameters and degradation during hot-carrier and Fowler-Nordheim stressing. Light nitrogen incorporation (<5%) improves thickness uniformity, charge to breakdown, and endurance. Nitrogen near Si/SiO_2 interface also reduces Si–H bonds by replacing them with Si–N bonds. This reduces electron traps in oxides and increases interface resistance to current stress. For transistors with feature sizes below 0.1 μm with gate oxides below the tunneling limit of 25 Å for SiO_2, the tunneling current exceeds 1 A/cm^2. Furthermore, SiO_2 is not a good diffusion barrier for gate electrode dopants such as boron. Even with nitrogen incorporation such ultrathin nitrided oxides cannot be utilized for sub-0.18-μm technologies due to high tunneling current and a rough Si/SiO_2 interface. Therefore, a high dielectric constant (k) material of equivalent electrical dielectric thickness is a viable alternative to thermally grown SiO_2. However, these high-k materials usually are associated with unacceptable levels of interface traps (D_{it}), bulk fixed charges (Q_f), low interface carrier mobilities, and phase stability issues. Hence, a significant silicon–dielectric interface engineering is needed before high-k dielectrics can be used as a gate material in CMOS technologies. Recently (31) a novel synthesis of a stacked SiO_2–Ta_2O_5–SiO_2 gate dielectric has alleviated these interface substructure problems; thus it has opened up new frontiers in gate dielectric scaling beyond the current 0.18 μm design rules.

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PRADIP K. ROY
YI MA
Bell Laboratories

GATE OXIDES, CMOS. See GATE DIELECTRICS.

GATE TURN-OFF THYRISTORS, GTOS. See THYRISTORS FOR POWER ELECTRONICS.