C–V PROFILES

It is well acknowledged that capacitance is an intrinsic property of microelectronic devices and its evaulation as a function of applied voltage is necessary for the characterization of semiconductor substrates, insulators, metals, and interfaces. The capacitance–voltage (C–V) profiling of semiconductor devices is therefore presented in this article. A review of the basic techniques for C–V profiling and the accomplishment in the determination of device properties including the dielectric constants, substrate doping concentrations, oxide purity, interface and surface states are presented below.

Solid-state materials exist in three basic forms: metals, semiconductors, or insulators. These are the basic materials used in the fabrication of microelectronics devices. The most fundamental property that differentiates these materials from one another is the electrical conductivity. Insulators, such as SiO_2, Al_2O_3, and Si_3N_4, are characterized by low electrical conductivity compared to metals, such as aluminum, or semiconductors, such as silicon. The conductivity of a typical insulator may be as low as $10^{-15}\ (\Omega \cdot \mathrm{m})^{-1}$, while that of a typical metal may be as high as $10^{7}\ (\Omega \cdot \mathrm{m})^{-1}$, with that of a semiconductor in between the two values. The low value of conductivity in insulators is due to the lack of transportation of

charge carriers. While the free transportation of electrons in metals and of holes and electrons in semiconductors is responsible for their conductivity, the positive and negative charges in insulators are immobile.

Unlike conductors, insulators can be viewed as a collection of positive charges surrounded by clouds of electrons, which become distorted by the electric field whenever a voltage is applied. The applied voltage separates the positive from the negative charges in a process called polarization. The dielectric behavior of insulators and hence the capacitance C of systems containing them are the direct consequence of the field-induced electronic polarization.

CAPACITANCE AND SEMICONDUCTOR DEVICES

Capacitance is one of the fundamental properties of semiconductor devices. The capacitance of semiconductor devices, including (1) the parallel-plate capacitor, (2) the p–n junction, (3) Schottky diodes, and (4) the metal–oxide–semiconductor (MOS) capacitor, is presented and illustrated in this section.

Parallel-Plate Capacitors

A device in which an insulator is positioned between two parallel metal plates, called *electrodes,* is called a *parallel-plate capacitor.* Figure 1 is an illustration of a parallel-plate capacitor with a voltage, V, applied to the metal plates. The applied voltage separates the charges in the insulators, which also induce opposite charges on the metal plates. The quantity of charge per unit area, Q (C/cm^2), induced on either plate is proportional to the applied voltage.

The *p–n* Junction

Electrons and holes are the fundamental particles that transport negative and positive charges, respectively, in a semiconductor. Semiconductors with equal numbers of electrons and holes are called *intrinsic* semiconductors. When impurity elements that contribute an electron per atom are incorporated into the semiconductor, excess electrons are made available to transport negative charges. Such a semiconductor is called *n-type,* and the impurity a *donor,* since electrons have been *donated* into the semiconductor. Examples are group V elements such as P or As in Si. Similarly when group III elements such as B or Al are incorporated into Si, they capture an electron, leaving an equal number of holes behind. The Si is called *p-type,* and the impurity introduced an *acceptor,* since each atom of the impurity has accepted an electron per atom from the silicon structure to complete its bond.

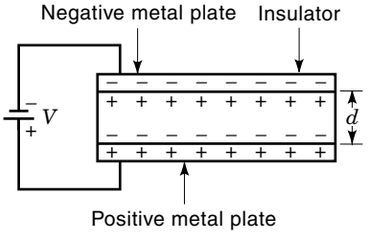

Figure 1. Two metal plates separated by an insulator (a dielectric layer) with field-induced charges on the plates.

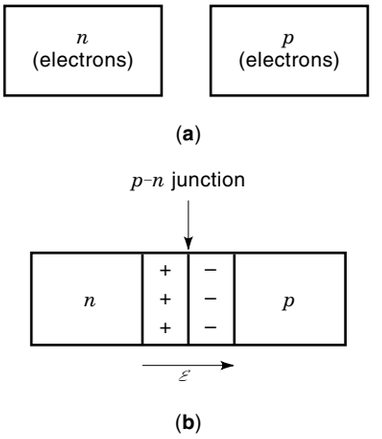

Figure 2. (a) Separate n-type and p-type pieces of semiconductor, and (b) n-type and p-type semiconductor pieces brought together to form a p–n junction; an electric field is created because of the depletion of mobile charges, leaving positive and negative ions separated by the junction.

A semiconductor device with n-type and p-type regions existing side by side, with a junction separating them, is called a *p–n junction.* Various techniques, including the growth of n-type on p-type material (or vice versa), diffusion of dopant atoms, alloying, and ion implantation, are used for the formation of a p–n junction (1–3).

The performance of most semiconductor devices strongly depends on the electrical properties of the p–n junction. The fundamental theory of the electrical characteristics of p–n junctions can be found in Refs. 4–8.

A p–n junction is a two-terminal device whose main characteristic is to allow electrical current to flow in one direction only. It is easy to visualize the p–n junction as two separate p-type and n-type semiconductor pieces brought in contact with each other, and this is illustrated in Fig. 2. Prior to joining, the n- and p-type pieces are filled with electrons and holes, respectively. When the two pieces are joined, a large carrier concentration gradient, corresponding to a nonequilibrium situation, sets in. Electrons from the n-side diffuse into the p-side and holes from the p-side diffuse into the n-side within a distance W from the junction, called the depletion width. Positively charged immobile ions are left on the n-side while negatively charged immobile ions are left on the p-side following the interdiffusion of the charge carriers. An electric field is therefore set up because of the charge polarization at the p–n junction. This is identical to the electric field in the parallel-plate capacitor shown in Fig. 1.

Schottky Diodes

Metal–semiconductor contacts are crucial to the performance and reliability of semiconductor devices. Contacts are either ohmic, when the relation between applied voltage and current is linear as in a resistor, or Schottky, when the contact is rectifying as in a p–n junction. While the ohmic contact is crucial in connecting a device to the "outside world," the rectifying or Schottky contact has the basic characteristics of a semiconductor diode. Details of the electrostatic properties,

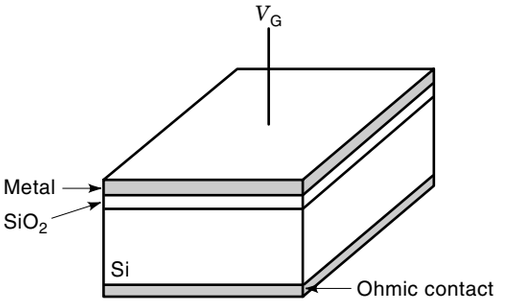

Figure 3. A schematic illustration of an ideal MOS capacitor.

I–V characteristics and ac responses of the Schottky diode can be found elsewhere (1,4,8).

In a Schottky diode charges of opposite signs are built up on both sides of the metal–semiconductor interface. That is, the charges are polarized as in the parallel-plate capacitor or a *p–n* junction. The capacitance–voltage characteristics can be evaluated similar to that of the *p–n* junction shown in the next section.

The MOS Capacitor

Figure 3 shows a schematic of an ideal MOS capacitor. The structure consists of a thin SiO_2 layer, about 10 nm to 30 nm thick, sandwiched between a metal layer and a silicon substrate. For the purpose of electrical evaluation an ohmic contact is made to the back of the silicon substrate. The MOS configuration mimics the gate structure of an MOS field-effect transistor.

Figure 4 shows the band diagram of the ideal zero-bias MOS structure, using a *p*-type semiconductor. With the metal, oxide, and semiconductor in intimate contact, the Fermi levels, E_F, in the metal and semiconductor are aligned so that the metal work function ϕ_m equals the semiconductor work function ϕ_s. The work functions are the energies required to remove an electron from the Fermi level into vacuum.

When a bias is applied to the capacitor through the metal gate, and the semiconductor is grounded, the Fermi level in the metal shifts relative to that in the semiconductor. Whether the shift is up or down depends on the polarity of the applied voltage. One other feature of the capacitor affected by the applied voltage is the shape of the conduction energy level E_c or the valence energy level E_v near the oxide–semiconductor interface. When the applied voltage V_G (G meaning gate) is negative ($V_G < 0$) both energy bands, E_c and E_v, bend upward, whereas they bend downward when V_G is positive ($V_G > 0$), as illustrated in Fig. 5(a) and (b). The upward band bending in the semiconductor for $V_G < 0$ enhances the accumulation of charge carriers (holes in this case) at the oxide–semiconductor interface. An increase in $E_i - E_F$ at the interface gives rise to the enhanced concentration of holes, a phenomenon called *accumulation.* The downward band bending at the interface when a positive voltage is applied results in the depletion of the majority charge carriers, a process called *depletion.* In this case, $E_i - E_F$ is very small, close to zero. For the depletion case the concentration in the semiconductor is due to ionized acceptor atoms, and this is obtained as $Q = -qN_AW_d$, where N_A is the acceptor atom concentration (atoms/cm^3) and W_d is the width of the depletion region.

The downward band bending at the interface increases with increase in the applied positive voltage, and for some value of V_G the intrinsic energy level E_i crosses the Fermi level E_F at the oxide–semiconductor interface. That is, $E_i - E_F$ becomes negative, as illustrated in Fig. 5(c). For this case the electron concentration at the oxide–semiconductor interface is greater than the concentration of holes. The surface is said to be inverted, and the process is called an *inversion* process. The total charge per unit area, Q, under inversion is the sum of electronic charge per unit area and the ionized impurity charge per unit area, Q_s. That is, $Q = Q_e + Q_s$ and $Q_s = -qN_AW_m$, where W_m equals the maximum width of the depletion layer. The charge distribution for each bias case is illustrated in Fig. 5(a), (b), and (c).

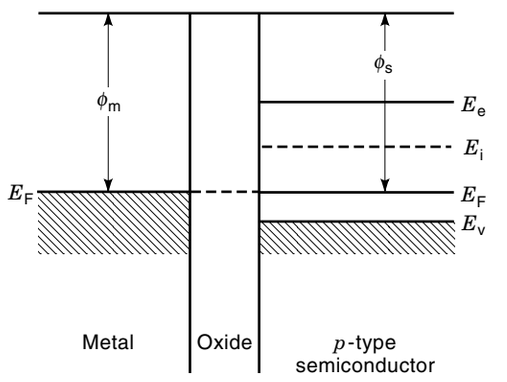

Figure 4. Energy band diagram of a nonbiased MOS capacitor, showing that the Fermi level E_F is constant throughout the structure.

CAPACITANCE OF SEMICONDUCTOR DEVICES

It has been demonstrated in the preceding section that the positive and negative charges in semiconductor devices are well separated in parallel-plate capacitors (when an applied voltage is applied), Schottky diodes, *p–n* junctions, and MOS capacitors with or without applied voltages. The most important property common to these devices is the capacitance, C, which is directly related to the applied voltage or to the change in the applied voltage in the devices.

Capacitance–voltage profiling techniques are the direct capacitance–voltage measurement and the photoelectrochemical profiling method. While the first technique is direct and more common, the latter technique profiles depth through photo-etching thus covering a great depth not accessible to either the *p–n* junction or the Schottky barrier profiling. Details of this technique are not covered in this article.

Capacitance of a Parallel-Plate Capacitor

When a voltage is applied to a parallel-plate capacitor, equal but opposite charges are induced on the metal plates. The quantity Q (C/cm^2) of charge on either of the two plates is proportional to the applied voltage V (V). That is,

$$Q = \mathscr{C}V \tag{1}$$

where the constant of proportionality, $\mathscr{C}$, is the capacitance of the insulator in coulombs per volt, or *farads* (F). The value of

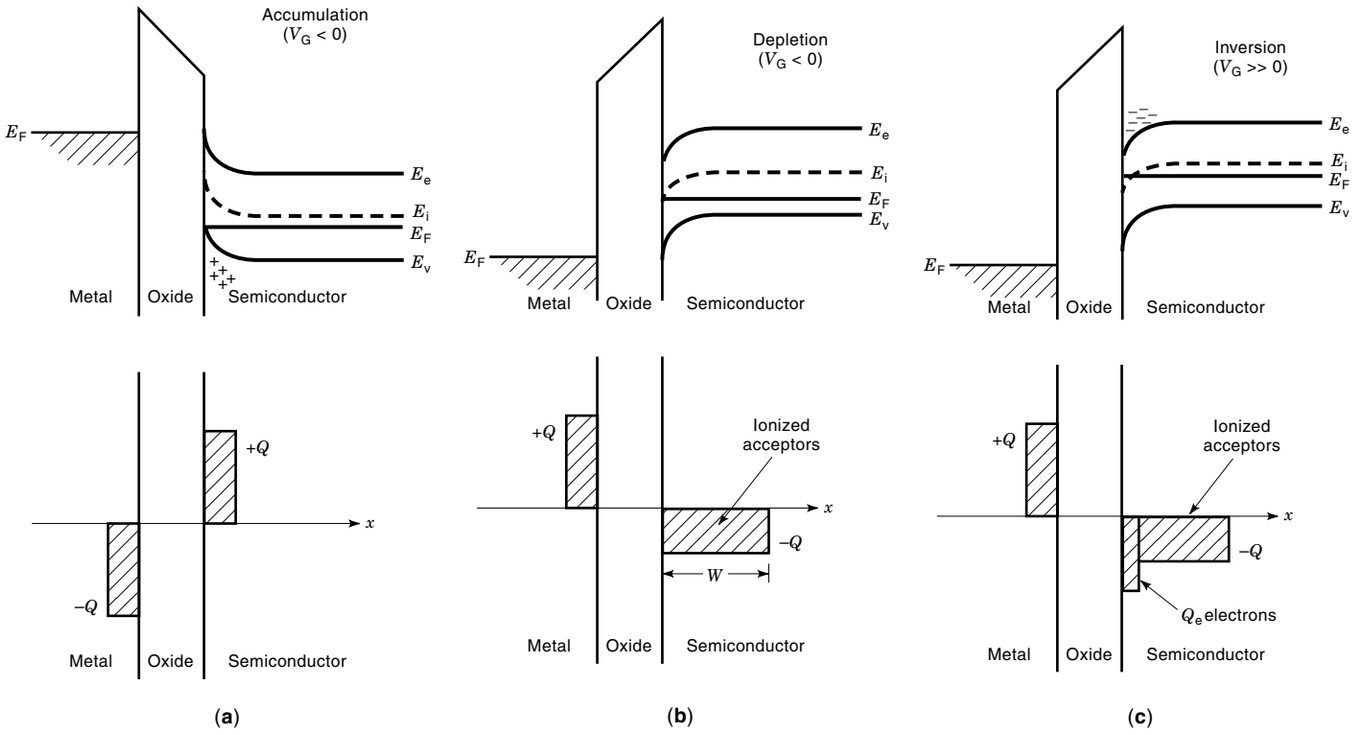

Figure 5. Energy band diagram and corresponding charge distributions of a MOS capacitor describing (a) accumulation ($V_G < 0$), (b) depletion ($V_G > 0$), and (c) inversion ($V_G \gg 0$).

$\mathscr{C}$ depends on the area A of each plate and the separation d between them through the relation

$$\mathscr{C} = \epsilon \frac{A}{d} \tag{2}$$

so that the capacitance per unit area, C, is

$$C = \frac{\mathscr{C}}{A} = \frac{\epsilon}{d} \tag{3}$$

where ϵ is called the permittivity of the insulator.

If the insulator between the two parallel plates is replaced with vacuum, then the capacitance becomes

$$\mathscr{C} = \epsilon_0 \frac{A}{d} \tag{4}$$

where ϵ_0 is the permittivity of vacuum, a constant with a value of 8.85×10^{-12} F/m. The permittivity ϵ of the insulator or any dielectric medium is related to ϵ_0 as

$$\epsilon = \epsilon_r \epsilon_0 \tag{5}$$

where ϵ_r is the relative permittivity, or dielectric constant, of the insulator, and its value depends on the material. For SiO_2, $\epsilon_r = 3.9$.

Capacitance–Voltage Characteristics of *p–n* Junctions

Two types of capacitance associated with a p–n junction are the junction capacitance (also called the depletion capacitance) and the charge storage or diffusion capacitance. The depletion layer capacitance dominates when the junction is reverse biased, and the diffusion capacitance dominates when the junction is forward biased. Capacitance is very significant in the application of p–n junctions and in providing information on the charge distribution at the junction.

When the voltage applied to a p–n junction is changed by an incremental amount dV, the depletion width increases, with a corresponding incremental change in the charge at the p–n junction. The capacitance C per unit area due to the change dV in the applied voltage and charge is defined as

$$C = \frac{dQ}{dV} \tag{6}$$

where dQ is the increase in charge per unit area when the applied voltage increases by dV. The depletion widths of both the n and p regions increase, corresponding to an increase dQ in the charge density (C/cm^2).

Figure 6 shows (a) the depletion layer, (b) the charge density distribution, and (c) the electric field as a function of position x, in a p–n junction with an applied voltage V (solid lines) and when the voltage increases by dV (dashed lines). If x_n and x_p are the lengths of the space-charge regions on the n- and p-type regions, respectively, when a voltage V is applied, then dx_n and dx_p are the changes in the space charge regions corresponding to a change dV in the applied voltage. The charge density on either side of the p–n junction will also increase by dQ. At equilibrium, the depletion width is the sum of x_n and x_p, while the change dW in the depletion width equals the sum of dx_n and dx_p.

At equilibrium, the total charge per unit area on one side of the junction is equal and opposite to that on the other side.

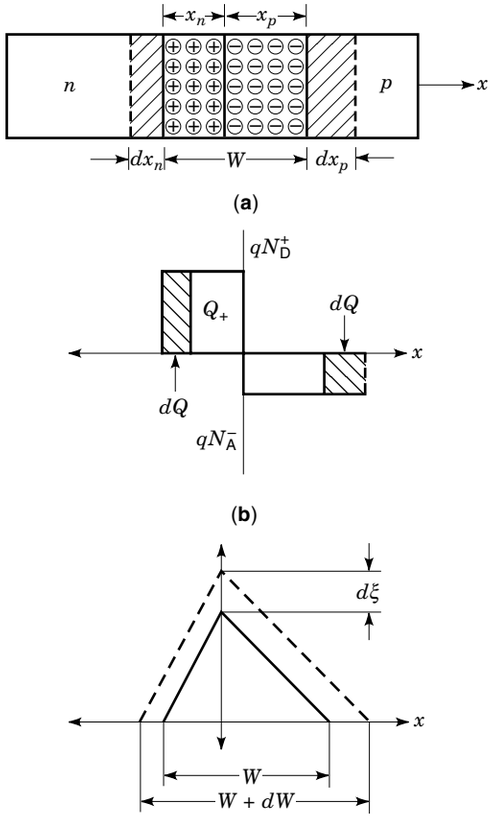

Figure 6. The distribution of (a) ionized space charge, (b) charge density, and (c) electric field in a p–n junction under equilibrium (solid lines) and with applied bias (dashed lines); the applied bias increases the depletion width from W to $W + dW$.

The magnitude of the total charge can be expressed as

$$|Q| \equiv qx_nN_D = qx_pN_A \tag{7}$$

The maximum value of the electric field at the p–n junction is

$$\mathscr{E} = \frac{qx_nN_p}{\epsilon} = \frac{qx_pN_A}{\epsilon} \tag{8}$$

where $\epsilon = \epsilon_r\epsilon_0$. The potential across the depletion width is the area of the triangle (solid lines) in Fig. 6(c), and this is

$$\Phi = \tfrac{1}{2}\mathscr{E}_m W = \frac{1}{2}\frac{qx_nN_D}{\epsilon} = \frac{1}{2}\frac{qx_pN_A}{\epsilon} \tag{9}$$

Using Eq. (7) in Eq. (9) and $W = x_n + x_p$, the depletion width of a step junction in equilibrium is a function of potential and is obtained as

$$W = \left[\frac{2\epsilon}{q}\left(\frac{N_A + N_D}{N_AN_D}\right)\Phi\right]^{1/2} \tag{10}$$

With an applied reverse bias, V_r, the expression for W becomes

$$W = \left[\frac{2\epsilon}{q}\left(\frac{N_A + N_D}{N_AN_D}\right)(\Phi + V_r)\right]^{1/2} \tag{11}$$

The capacitance per unit area, C, is

$$C = \frac{\epsilon}{\text{width}} = \frac{\epsilon}{W} \tag{12}$$

Substituting Eq. (11) in Eq. (12), the capacitance per unit area becomes

$$C = \left(\frac{q\epsilon}{2(\Phi + V_r)}\frac{N_DN_A}{N_D + N_A}\right)^{1/2} \tag{13}$$

Thus, the capacitance of a reverse-biased p–n junction decreases with increasing applied voltage. The plot of $1/C^2$ versus V_r is a straight line with intercept ϕ on the horizontal axis. The slope of the line provides the charge density in the depletion layer.

For a one-sided step junction with the n-side more heavily doped than the p-side, $N_D \gg N_A$ and $x_n = W$, the expression for the depletion width W [Eq. (11)], therefore, becomes

$$W = \left(\frac{2\epsilon}{qN_A}(\Phi + V_r)\right)^{1/2} \tag{14}$$

and the expression for the capacitance [Eq. (19)] is

$$C = \left(\frac{2\epsilon}{q(\Phi + V_r)}N_A\right)^{1/2} \tag{15}$$

Thus, Fig. 7(a) shows that the capacitance of a p–n junction decreases with increasing applied voltage in the reverse direction. Figure 7(b) is the plot of $1/C^2$ versus V_r. The slope of the curve yields the charge concentration N_A on the p-side if that is the lightly doped side of the p–n junction (or N_D if the n-

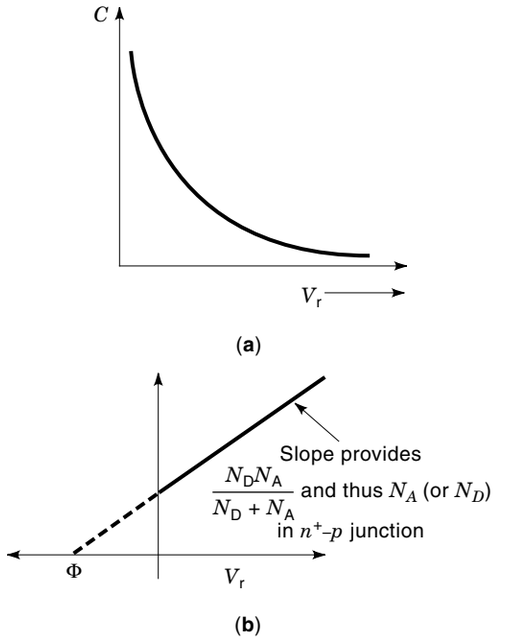

Figure 7. (a) Capacitance–voltage profile of a reverse-biased p–n junction, showing that the capacitance decreases with increasing applied reverse bias V_r, and (b) linear relation for $1/C^2$ versus reverse voltage V_r for a uniformly doped p–n junction.

side is lightly doped). The built-in potential at the junction is the intercept on the V_r axis.

A p–n junction that utilizes the C–V variation described in Eq. (15) is called a *varactor,* derived from the combination of *variable* and *reactor.* The applications of varactors are found in voltage-variable tuning circuits, signal mixing, harmonic generation, and detection (9,10).

The expression for the capacitance C per unit area in Eq. (13) is a valid approximation for a uniformly doped p–n junction. For a linearly graded junction where the net charge concentration varies linearly with distance, the capacitance per unit area varies as $V_r^{-1/3}$. Thus, a plot of $1/C^3$ versus V_r is linear.

For a forward-biased p–n junction, the charge storage capacitance dominates, and the capacitance is proportional to the current at the junction. The capacitance can be expressed as

$$C_f = \frac{dQ}{dV} = \frac{qI}{kT}\,\tau \tag{16}$$

where τ is the carrier lifetime of the charge, k is the Boltzmann constant, and T the absolute temperature in kelvin.

Any arbitrary distribution of impurity $N(W)$ in a p–n junction can be obtained fairly accurately from the capacitance–voltage profiles (11,12).

Capacitance–Voltage Characteristics of MOS Capacitors

The capacitance profile of MOS capacitors varies with the applied voltage, and it provides a powerful technique for the evaluation of insulators and semiconductors. A careful C–V profiling reveals the deviation from the ideal in both the semiconductor and the oxide layer. A MOS capacitor is considered ideal if (1) the difference in work function between the metal and semiconductor is zero with no applied bias, (2) the oxide is nonconducting, (3) both the metal and the semiconductor are sufficiently thick, and (4) all the charges in the capacitor reside inside the semiconductor.

The charge distribution inside the accumulated MOS capacitor, shown in Fig. 5(a), is basically equivalent to that of a parallel-plate capacitor with equal concentrations of positive and negative charges separated by the oxide layer. One can therefore conclude that the capacitance per unit area of an accumulated MOS capacitor is that of the oxide, C_o, and is related to the oxide thickness d as

$$C_o = \frac{\epsilon_o}{d} \tag{17}$$

where ϵ_o is the permittivity and d is the thickness of the oxide layer.

A depleted MOS capacitor, shown in Fig. 5(b), is characterized by charges per unit area of $+Q$ on the gate electrode and $-Q$ due to ionized impurities in the p-type semiconductor. The charge $-Q$ is uniformly distributed in a region inside the semiconductor of width W at the oxide–semiconductor interface. Under dc bias and for all measurement frequencies, the total capacitance of the MOS structure is the series combination of the oxide capacitance C_o and the semiconductor capacitance C_{si}. That is, the total capacitance C_d is given by

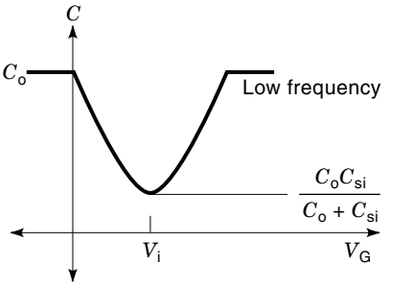

Figure 8. Low-frequency C–V profile of a MOS capacitor showing accumulation, depletion, and inversion: the capacitance remains constant at C_o in accumulation, decreases to a minimum value $C_oC_{si}/(C_o + C_{si})$ in depletion, and increases to C_o at inversion.

$$\frac{1}{C_d} = \frac{1}{C_o} + \frac{1}{C_{si}} \tag{18}$$

or

$$C_d = \frac{C_oC_{si}}{C_o + C_{si}} \tag{19}$$

where

$$C_{si} = \frac{\epsilon_{si}}{W} \tag{20}$$

and $\epsilon_{si} = \epsilon_r\epsilon_0$.

In terms of d and W,

$$C_d = \frac{C_0}{1 + \dfrac{\epsilon_0 W}{\epsilon_{si} d}} \tag{21}$$

Since W increases with increasing applied gate voltage V_G, the capacitance decreases as the bias increases as shown in Fig. 8.

Once a large enough bias is applied to achieve inversion, E_i lies below E_F and the extent of band bending at the interface is defined by the quantity $q\Phi_{sc}$ for strong inversion with the oxide–semiconductor interface strongly populated with electrons for a p-type substrate. E_i is positioned far below E_F, and the potential is obtained as

$$\Phi_{sc}(\text{inv}) = 2\,\frac{kT}{q}\ln\frac{N_A}{n_i} \tag{22}$$

where n_i is the intrinsic carrier concentration. The maximum value W_{max} of the depletion width in Eq. (21) above is obtained as

$$W_{max} = \sqrt{\frac{2\epsilon_{si}\Phi_{sc}(\text{inv})}{qN_A}} = 2\sqrt{\frac{\epsilon_{si}kT\ln(N_A/n_i)}{q^2N_A}} \tag{23}$$

At inversion, therefore, when the applied dc bias V_G has increased to V_i, the capacitance C_i of the inverted MOS struc-

ture is given as

$$C_d = \frac{C_o C_{si}}{C_o + C_{si}} = \frac{C_0}{1 + \dfrac{\epsilon_0 W_{max}}{\epsilon_{si} d}} \tag{24}$$

The Si component of the capacitor, C_{si}, remains constant at inversion, because there is no further increase in the width of the depletion layer.

Overall, a systematic theoretical analysis can be made by considering the capacitor of an MOS structure evaluated in accumulation, depletion and inversion. The capacitance has been shown to be constant in accumulation, decreases with increasing dc bias in depletion and remains constant at inversion with a value close to that of C_o at low frequency and to the minimum value C_d at high frequencies. For the *p*-type semiconductor substrate, the dc bias V_G is negative for accumulation, positive in depletion and inversion.

DOPING PROFILES

Doping Profiles in *p–n* Junctions

The expression in Eq. (15), for a one-sided step junction, provides the doping profile on the lightly doped side of a *p–n* junction. Doping profiles are routinely evaluated in semiconductor laboratories using automated capacitance–voltage equipment. The Keithley System 82 and System 83 are the latest equipment systems for measuring high-frequency *C–V* curves sequentially. Figure 9 shows the schematic illustration of such a system. The system consists of (1) a *C–V* meter employing a small signal at a given frequency (e.g. 1 MHz or 2 MHz), (2) a dc power supply, (3) a computer and monitor for data acquisition and analyses, and (4) a probe box on which the wafer or device under investigation is placed. The back contact is provided by a chuck, while the front of the device is contacted by a probe. The device is automatically measured once the program has been set up.

If both sides of Eq. (15) are squared and inverted, the relation between capacitance and reverse bias V_r becomes

$$\frac{1}{C^2} = \frac{2}{qN_A \epsilon_r \epsilon_0}(\Phi + V_r) \tag{25}$$

A plot of $1/C^2$ versus V_r is a straight line from which both the doping concentration N_A and the built-in voltage are obtained: the slope of the curve provides N_A, and the intercept on the horizontal axis provides the built-in voltage Φ, as shown in Fig. 7(b).

Doping Profiling of MOS Capacitors

The electronic properties of silicon can be investigated using the electrical properties of MOS capacitors. Information such as the doping type (*n*- or *p*-type), the deep depletion condition, and the doping profile can be obtained from the characteristics of the MOS structure. For example, the doping type can be determined using either high- or low-frequency *C–V* characteristics. However, the high-frequency *C–V* characteristics are much more commonly used because of their higher symmetry. Figure 10 shows high-frequency *C–V* profiles measured on (a) *p*-type and (b) *n*-type substrates. The *C–V* curve goes from accumulation to inversion with increasing gate bias for *p*-type, while it goes from accumulation to inversion with decreasing gate bias for *n*-type, independent of the doping concentration and the oxide–Si interface properties.

The *deep-depletion C–V* profile is the third main type (in addition to low-frequency and high-frequency) of *C–V* characteristics measured in MOS structures. Details of the deep-depletion profiles can be found in a number of sources (13–15).

The performance of MOS-based devices are usually influenced by the distribution of dopant impurities in the Si substrate. The impurity concentration in the bulk of the semiconductor is generally not the same as on the surface. There are various reasons for this nonuniformity. Regardless of the cause or causes, device properties are better understood if the doping profile is known.

C–V characterization of MOS structures, *p–n* junctions, and Schottky diodes provides an excellent technique for doping profiling in silicon substrates. The *C–V* profiling of MOS structures has a number of advantages. These include the following: (1) the processing of MOS structures alters the doping profile in the substrate much less than the processing of *p–n* junctions or Schottky diodes; (2) the doping profile can be evaluated much closer to the Si surface; (3) the doping profile can be measured even if the doping concentration is high. However, care must be taken to minimize errors introduced by defects and interface traps, as these can significantly affect the profile. There are methods for minimizing such errors. Nicollian and Brews (13) applied the second harmonic method to MOS capacitor characterization to minimize errors introduced by the interface condition. By applying the depletion approximation, Deal et al. profiled the redistribution of impu-

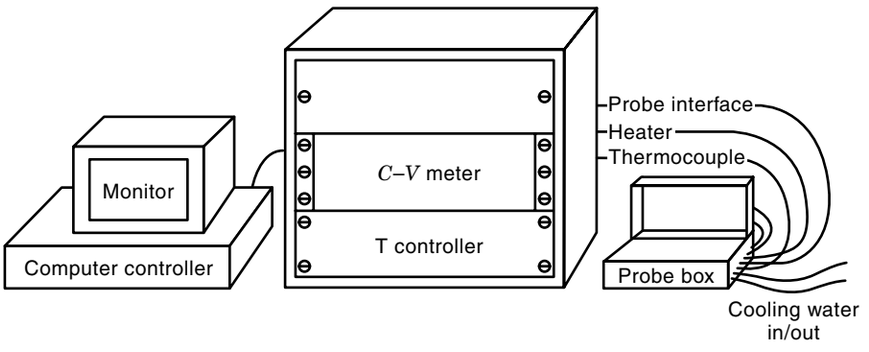

Figure 9. Block diagram of a *C–V* measurement system showing the *C–V* meter, the temperature controller, the data accumulation unit (computer and monitor), and the probe box.

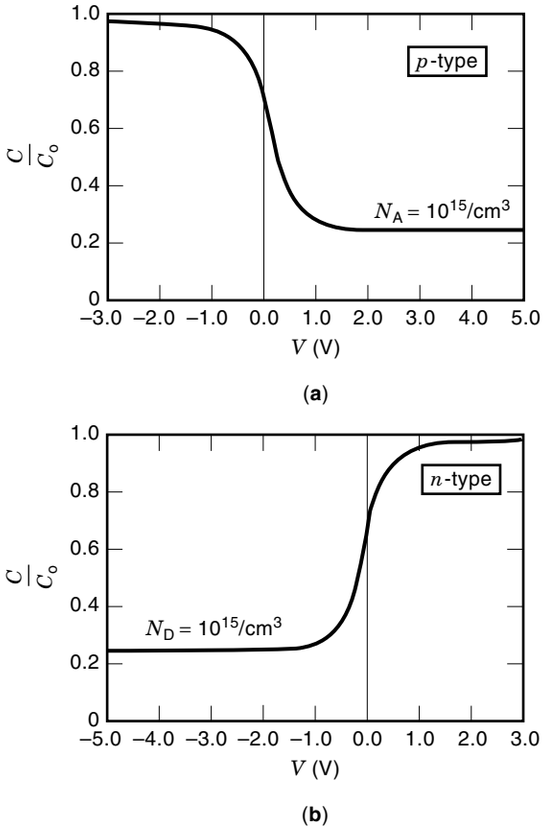

Figure 10. High-frequency C–V profiles of MOS capacitors, showing the effect of substrate type (p or n). The curves also depend on the doping concentration (not shown); higher doping increases the capacitance in depletion and inversion.

rities using the MOS capacitor (13). Also, Van Gelder and Nicollian superposed a small frequency ac signal on a voltage pulse to the gate electrode of an MOS capacitor and then obtained the doping profile by C–V characterization. Details of the C–V methods used for the profiling of Schottky diodes and p–n junctions can be found elsewhere (1,11,12).

Analysis of Doping Profiling of the MOS Structure. Doping profiling in the MOS capacitor depends on how accurately the carrier charge densities in accumulation, depletion, and inversion can be determined. In accumulation and inversion, the carrier charge densities are exponentially dependent on band bending, with the densities showing as preexponential factors, making it difficult to obtain accurate values of the charge density. Therefore, accurate values can be obtained only in depletion.

The doping profile using the MOS structure is obtained from the slope of a $1/C_d^2$ versus V_G curve, where C_d is the depletion capacitance and V_G is the gate bias. With a change dV_G in the bias, an incremental charge dQ_G is added to the gate of the capacitor, and it is given by

$$dQ_G = C_d\, dV_G \tag{26}$$

If the density of ionized donor impurity at the depletion layer edge, a distance W from the oxide–silicon interface, is $N(W)$ and the depletion layer edge moves a distance dW due to the change in bias, then the charge added to the gate per unit area is

$$dQ_G = -qN(W)\, dW \tag{27}$$

The depletion layer capacitance, using the depletion approximation, is

$$C_{si} = \frac{\epsilon_{si}}{W} \tag{28}$$

as shown in Eq. (20), where C_{si} is the depletion layer capacitance per unit area and ϵ_{si} is the dielectric permittivity of Si. The total capacitance measured in depletion, C_d, satisfies the same relationship. That is,

$$C_d = \frac{\epsilon_{si}}{W} \tag{29}$$

Therefore, the change in $1/C_d$ when the gate bias is changed by dV_G is

$$dW = \epsilon_{si} d\left(\frac{1}{C_d}\right) \tag{30}$$

But the total capacitance per unit area is the series combination of the silicon capacitance per unit area and the oxide capacitance per unit area. That is,

$$\frac{1}{C_d} = \frac{1}{C_o} + \frac{1}{C_{si}} \tag{31}$$

as shown in Eq. (18), where C_o is the oxide capacitor per unit area and is independent of the applied voltage.

To obtain an expression for $N(W)$ in terms of C_d, we equate Eq. (26) to Eq. (27) to obtain

$$-qN(W)\, dW = C_d\, dV_G \tag{32}$$

Substituting $dW = \epsilon_{si}\, d(1/C_d)$, we obtain

$$-qN(W)\epsilon_{si}\, d\left(\frac{1}{C_d}\right) = C_d\, dV_G \tag{33}$$

$N(W)$ is therefore obtained as

$$N(W) = -\left(q\epsilon_{si}\frac{1}{C_d}\frac{d(1/C_d)}{dV_G}\right)^{-1} \tag{34}$$

Using the expression $(d/dx)(1/x^2) = -(2/x)(d/dx)(1/x)$, $N(W)$ becomes

$$N(W) = 2\left[q\epsilon_{si}\frac{d}{dV_G}\left(\frac{1}{C_d^2}\right)\right] \tag{35}$$

This expression was first derived by Van Gelder and Nicollian (13). The equation shows that $N(W)$ can be extracted from the slope of the $(1/C_d)^2$ versus V_G curve. A positive slope gives a negative value of $N(W)$ for acceptors, while a negative slope gives a positive $N(W)$ for donors. The doping profile versus depth from the oxide–silicon interface is obtained by calculat-

ing $N(W)$ at each value of V_G using Eq. (35). The corresponding value of W is obtained by solving Eq. (28), combining with Eq. (31) to obtain

$$W = \epsilon_{si}\left(\frac{1}{C_d} - \frac{1}{C_o}\right) \tag{36}$$

SURFACE STATES

The performance of gate-insulated electronic devices depends on the properties of the MOS interfaces. Problems associated with either the metal–oxide or the oxide–semiconductor interface include defects, charges, ions, and impurities. Charges and defects inside the oxide also present problems of reliability and performance in MOS-based devices. Capacitance–voltage profiling provides a reliable method of evaluating the defects, charges, and impurity distribution in the MOS capacitor.

At present the most commercially viable MOS-based devices are Si-based, with Si as the semiconductor, SiO_2 the oxide, and Al or its alloys, the metal. Thus, the MOS capacitors that will be discussed in this section are based on Si technology. However, the C–V properties of an MOS structure using oxidized AlN as the oxide have been found similar to those of SiO_2-based MOS capacitors (16,17).

Discussions have focused so far on the C–V characteristics of ideal MOS structures. The C–V capacitance of the metal–Si–SiO_2 structure generally deviates from the ideal because of the nature of Si and SiO_2 and their interfaces. Departure of the C–V curves from the ideal is caused by factors including (1) interface traps, (2) fixed oxide charges, and (3) the work-function difference. These factors can be evaluated by comparing the C–V curves of the Si-based MOS capacitors with the ideal curves.

Effect of Interface Traps

Interface traps are defects located at the interface between SiO_2 and the Si substrate. The defects can capture or emit electrons or holes. Interface traps are therefore either positively or negatively charged. The energy levels of the traps are distributed throughout the Si band gap, and their occupancy changes with gate bias. The trap density at the oxide–silicon interface is often high, affecting the results of doping profiles through a change in the slope of the C–V curve. It is therefore necessary to modify Eq. (36) to reflect the effect of these traps.

The ac response of interface traps can be avoided by performing characterization at such a high frequency that interface traps cannot respond over the applied voltage range that corresponds to depletion. Assuming C_{hf} is the high-frequency capacitance, Eq. (36) is modified as

$$W = \epsilon_{si}\left(\frac{1}{C_{hf}} - \frac{1}{C_o}\right) \tag{37}$$

This modification reflected in the C–V slope in depletion leads to a condition called *voltage stretch-out.*

The density of interface traps can be extracted by one of the following methods: (1) comparing the measured low-frequency capacitance with an ideal low-frequency capacitance, and (2) comparing high-frequency capacitance with an ideal theoretical capacitance. A more sensitive and accurate method for extracting interface density is the measurement of equivalent parallel conductance described by Nicollian and Brews (13).

The capacitance–voltage curve of a MOS capacitor with Si–SiO_2 interface traps indicates stretchout in the direction of the applied gate voltage axes. The stretchout in the C–V curve provides a method for revealing interface traps in MOS structures, and the interface traps contribute to the total capacitance of the capacitor.

The interface traps are either the donor type or the acceptor type. A donor trap is neutral when filled and positive when empty; an acceptor trap is negative when filled and neutral when empty. The interface traps of thermally grown device-quality oxides are predominantly the donor type and reside close to the conduction band of Si. The origin of stretchout is better understood when one considers two capacitors, one with interface traps and the other without.

Let δQ_G be the change in charge of the gate corresponding to a change of δV_G in bias. Charge neutrality requires that the change δQ_G in the gate charge be balanced by an equal but opposite charge $-\delta Q_{si}$ in Si, which makes the total charge zero. That is,

$$\delta Q_G + \delta Q_{si} = 0 \tag{38}$$

When interface traps are present, a change in gate charge density also induces an interface trap charge density δQ_{it} along with the charge δQ_{si} in Si. The condition of charge neutrality therefore requires

$$\delta Q_G + \delta Q_{si} + \delta Q_{it} = 0 \tag{39}$$

Comparing Eq. (38) with Eq. (39), δQ_{si} for a MOS structure without interface traps is seen to be larger than with interface traps. Thus, the band bending in the MOS capacitor with interface traps is less than that without. A larger change in gate charge and, hence, gate voltage is required to drive a capacitor with interface traps from accumulation to inversion, corresponding to a stretchout of the C–V profile along the voltage axis.

An extremely small change in the interface trap charge, dQ_{si}, is directly proportional to the band bending in Si. That is,

$$dQ_{it} = -C_{it}\, d\Phi_{si}$$

or

$$C_{it} = \frac{-dQ_{it}}{d\Phi_{si}} \tag{40}$$

where $d\Phi_{si}$ is the infinitesimal change in Si band bending and is the capacitance per unit area due to interface traps. Similarly,

$$C_{si} = \frac{-dQ_{si}}{d\Phi_{si}} \tag{41}$$

The low-frequency capacitances per unit area for silicon and for the interface traps are in parallel, and are in series with C_o, the oxide capacitance per unit area. That is,

$$\frac{1}{C_{\rm lf}} = \frac{1}{C_{\rm o}} + \frac{1}{C_{\rm si} + C_{\rm it}} \tag{42}$$

or

$$C_{\rm lf} = \frac{(C_{\rm si} + C_{\rm it})C_{\rm o}}{C_{\rm o} + C_{\rm si} + C_{\rm it}} \tag{43}$$

Thus, the measured low-frequency capacitance per unit area, $C_{\rm lf}$, has increased due to $C_{\rm it}$. From Eq. (42), $C_{\rm it}$ can be obtained as

$$C_{\rm it} = \left(\frac{1}{C_{\rm lf}} - \frac{1}{C_{\rm o}}\right)^{-1} - C_{\rm si} \tag{44}$$

The oxide capacitance is measured in accumulation.

At high frequency, interface traps do not respond to applied ac voltage and therefore do not contribute to capacitance; they only cause the *C–V* curves to stretch out along the voltage axis. The phenomenon is illustrated in Fig. 11, which compares a hypothetical high-frequency *C–V* curve with interface traps with that of a similar ideal capacitor.

At high frequency $C_{\rm it} = 0$, since interface traps contribute nothing to the capacitance. The oxide and Si capacitance are therefore in series. That is,

$$\frac{1}{C_{\rm hf}} = \frac{1}{C_{\rm o}} + \frac{1}{C_{\rm si}} \tag{45}$$

or

$$C_{\rm hf} = \frac{C_{\rm si}C_{\rm o}}{C_{\rm o} + C_{\rm si}} \tag{46}$$

The value of $C_{\rm hf}$ corresponds to that of an ideal MOS capacitor.

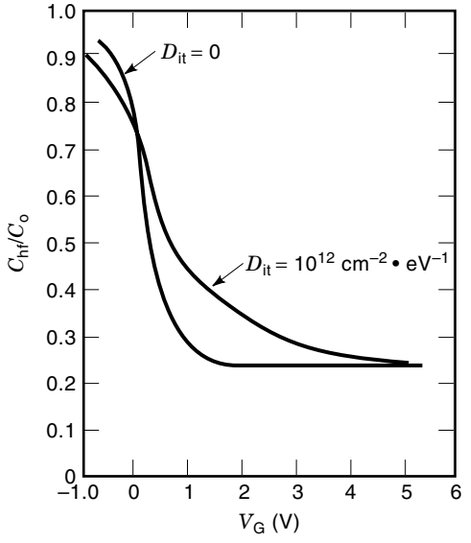

Figure 11. A theoretical high-frequency *C–V* curve with interface trap stretchout compared with a theoretical *C–V* curve with no interface traps. The parameters $N_{\rm D} = 10^{15}$ cm^{-3}, $x_{\rm o} = 1000$ Å, and $D_{\rm it} = 10^{12}$ cm$^{-2} \cdot$ eV^{-1} are taken from E. H. Nicollian and J. R. Brews (13).

Maximum–Minimum-Capacitance Technique. The high-frequency capacitance technique involves measuring the maximum high-frequency capacitance at accumulation and the minimum high-frequency capacitance at inversion. The technique is not influenced by interface traps, since the maximum capacitance at accumulation is the oxide capacitance $C_{\rm o}$, and the minimum capacitance is measured at inversion, where there is no capacitance due to interface traps, $C_{\rm it}$. The method is simple and accurate and is commonly used for profiling uniformly doped substrates.

At strong inversion, when the high-frequency capacitance is minimum, the width of the depletion layer is maximum and is obtained from Eq. (37) as

$$W_{\rm max} = \epsilon_{\rm si}\left(\frac{1}{C_{\rm hf}^{(\rm min)}} - \frac{1}{C_{\rm o}}\right) \tag{47}$$

Maximum band bending is also obtained in inversion, and $\Phi_{\rm si} \approx \Phi_{\rm m}$ is the maximum band bending in Si. Using the depletion approximation, the expression for the maximum depletion width becomes

$$W_{\rm max}^2 = \frac{2\epsilon_{\rm si}\Phi_{\rm m}}{qN_{\rm A}} \tag{48}$$

for a *p*-type Si substrate. $N_{\rm A}$ is the acceptor concentration (atoms/cm^3). The maximum band bending can be approximated as

$$\Phi_{\rm m} = 2\Phi_{\rm B} + \frac{kT}{q}\ln\left(\frac{2q\Phi_{\rm B}}{kT - 1}\right) \tag{49}$$

where the built-in potential $\Phi_{\rm B}$ is defined as

$$\Phi_{\rm B} = \frac{kT}{q}\ln\frac{N_{\rm A}}{n_i} \tag{50}$$

Combining Eq. (47) with Eq. (48) and using Eq. (49) and Eq. (50), an expression for the doping concentration is obtained as

$$\frac{N_{\rm A}}{\ln\dfrac{N_{\rm A}}{n_i} + \dfrac{1}{2}\ln\left(2\ln\dfrac{N_{\rm A}}{n_i} - 1\right)} = \frac{43kT\epsilon_{\rm o}^2}{q\epsilon_{\rm si}x_{\rm o}^2}\left(\frac{C_{\rm o}}{C_{\rm hf}^{(\rm min)}} - 1\right) \tag{51}$$

where $\epsilon_{\rm o}$ is the dielectric permittivity of SiO_2, $x_{\rm o}$ is the oxide thickness, and n_i is the intrinsic carrier concentration. Equation (51) can be solved by iteration, and Fig. 12 shows the plot of $N_{\rm A}$ versus $C_{\rm hf}(\rm min)/C_{\rm o}$, with oxide thickness as a parameter. $N_{\rm A}$ and the doping profile can be obtained from the graph if the doping is uniform.

Simultaneous High- and Low-Frequency *C–V* Technique. A high- and a low-frequency *C–V* profile of a MOS structure can be measured simultaneously to evaluate interface traps (13,18). The theoretical computation of $C_{\rm si}$ and the evaluation of the doping profile are not required in this technique. From Eq. (45) the expression for the capacitance of the silicon substrate becomes

$$C_{\rm si} = \left(\frac{1}{C_{\rm hf}} - \frac{1}{C_{\rm o}}\right)^{-1} \tag{52}$$

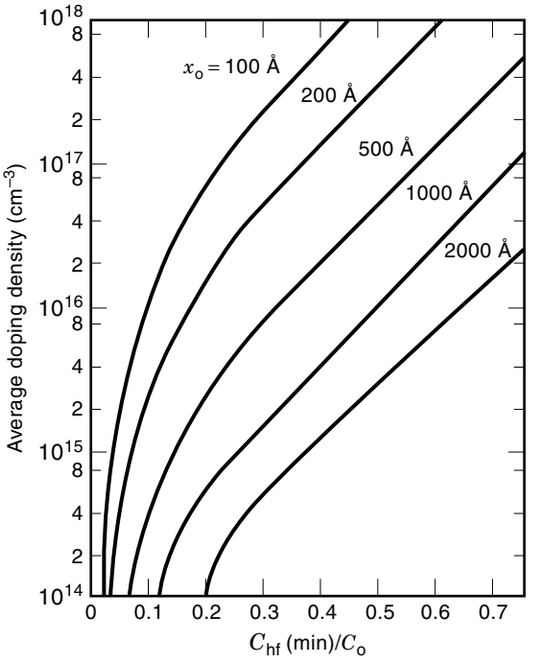

Figure 12. Acceptor doping concentration N_A versus $C_{hf}(\text{min})/C_o$ with oxide thickness as parameter, from E. H. Nicollian and J. R. Brews (13).

Substituting C_{si} in Eq. (44), the expression for the value of C_{it} measured at low frequency is obtained as

$$C_{it} = \left(\frac{1}{C_{lf}} - \frac{1}{C_o}\right)^{-1} - \left(\frac{1}{C_{hf}} - \frac{1}{C_o}\right)^{-1} \tag{53}$$

Thus, C_{it} can be evaluated directly from the C–V curve.

The interface trap density, D_{it}, can also be obtained from the value of capacitance at low and high frequencies through the expression

$$D_{it} = \left(1 - \frac{C_{hf} + \Delta C}{C_o}\right)^{-1} \left(1 - \frac{C_{hf}}{C_o}\right)^{-1} \tag{54}$$

where $\Delta C = C_{lf} - C_{hf}$.

Bulk Charge in SiO_2

Evaluation of the oxide charge is critical for the quality and reliability of electronic devices and integrated circuits. Charged impurities in SiO_2 can be profiled using the C–V technique in which the flatband voltage is evaluated after the oxide layer is etched off in successive increments.

In order to obtain the charge profile in the oxide layer the charge density and oxide thickness must be obtained each time a layer of oxide is removed, usually by etching. The oxide thickness x_o is calculated from the slope of the curve of $(C_o/C_{hf})^2$ versus V_G, the gate voltage, and this can be expressed as

$$x_o = \left(\frac{2\epsilon_o^2}{q\epsilon_{si}}\right)^{1/2} (nN)^{-1/2} = 1.17 \times 10^3\,(mN)^{-1/2} \tag{55}$$

where m is the slope of the linear portion of the curve and N is the doping concentration in silicon.

The volume charge density in oxide layer is then obtained by measuring the flatband voltage as a function of depth. The incremental etchoff procedure is good only for uniformly distributed or slowly varying oxide charges. With this technique, it was discovered that oxide fixed charge and interface traps are within about 20 nm of the silicon surface (19,20).

Figure 13 is a schematic representation of the types of charge inside SiO_2 and at the SiO_2–Si interface. The interface trap charge, Q_{it}, is located at the interface between Si and the nonstoichiometric region of SiO_2, hereafter called SiO_x. Aside from the interface traps, there are three other main bulk oxide charges inside the SiO_2 layer. The first is the oxide fixed charge Q_f, which is the charge that is left after the interface trap charge has been removed, usually by annealing. This charge is within about 20 nm (200 Å) of the Si–SiO_2 interface. The second is the oxide trapped charge, Q_t, usually found at the metal–SiO_2 or Si–SiO_2 interface or uniformly distributed inside the SiO_2. The oxide trapped charge is caused by a variety of factors, including ionizing irradiation, injection of hot electrons and holes by plasma, and injection of charges by photoemission. The third type of oxide charge is the mobile ionic charge Q_m, caused by contamination with ionized alkali metals such as sodium or potassium. This charge is located either at the metal–SiO_2 interface or inside the SiO_2 layer. The charge is mobile and drifts around inside the oxide layer.

The Flatband Voltage. The flatband voltage is determined by comparing the high-frequency C–V profile of an MOS capacitor with the theoretical C–V profile of an ideal structure. The ideal theoretical profile is for a MOS capacitor with neither oxide charges nor work function difference. The oxide thickness and doping profile are assumed to be the same for the experimental and for the ideal capacitor. The two curves are plotted using the same axes, and the shift between the two curves provides the flatband voltage V_{FB}. Nicollian and Brews provided a detailed analysis of how V_{FB} is obtained when the experimental profile contains stretchout (13,20,21).

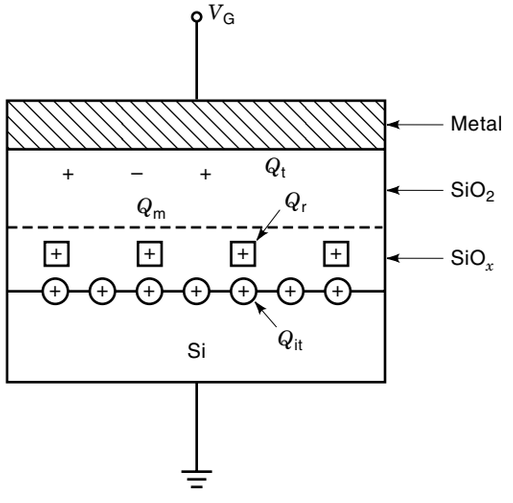

Figure 13. Schematics of charge distribution in a metal–SiO_2–Si structure. Q_{it} = interface trap charge, Q_f = oxide fixed charge, Q_t = oxide trapped charge, and Q_m = mobile ionic charge.

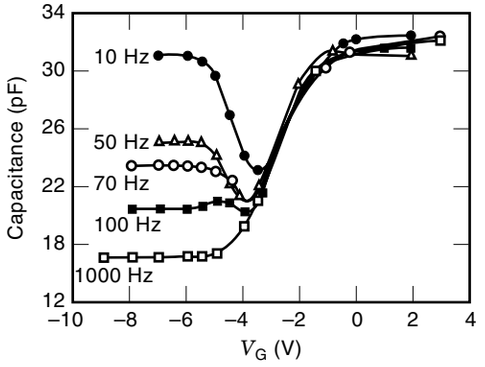

Figure 14. Capacitance as a function of bias measured at 300 K with frequency as parameter. Sample is *n*-type, oriented in the [100] direction. Gate diameter is 370 μm, donor density is 1.2×10^{16} cm^{-3}, and oxide layer capacitance is 2.84×10^{-8} F/cm^2. After E. H. Nicollian and J. R. Brews (13).

For thermally grown oxides, the oxide charge Q_o, which is the sum of Q_f, Q_t, and Q_m, can be calculated from the measured flatband voltage V_{FB} and the difference in work function between the metal and silicon, Φ_{ms}. These quantities are related by this expression:

$$V_{FB} = \Phi_{ms} - \frac{x_o Q_o}{\epsilon_o} \tag{56}$$

That is,

$$V_{FB} = \Phi_{ms} - \frac{Q_o}{C_o} \tag{57}$$

where $C_o = \epsilon_o / x_o$ is the capacitance per unit area of the oxide layer.

Equation (57) shows that the capacitance–voltage curve of a MOS capacitor, measured at high frequency, is shifted by $V_{FB} - \Phi_{ms}$ along the voltage axis in the presence of Q_o from an ideal *C–V* curve. The shift is illustrated with in Fig. 14 with a positive charge Q_o inside SiO_2 on (a) a *p*-type Si substrate and (b) an *n*-type Si substrate. In both cases the shift is toward negative gate bias. Similar curves can be obtained for negative oxide charges on either an *n*-type or a *p*-type substrate, and the voltage shift is in the direction of the applied voltage. Thus, both the quantity and polarity of Q_o can be evaluated from *C–V* profiling. The effect of the mobile ionic charge on the *C–V* curve can be separated from that of the fixed oxide charge. The details are presented by Nicollian and Brews (13).

RESPONSE TIME

Majority Carrier Response Time

At both low and high frequencies majority carriers respond instantaneously to applied ac voltages. In MOS structures, *C–V* characteristics in accumulation and depletion results from the flow of majority carriers in and out of the depletion layer in response to the applied ac voltage. The response will only arise if the period of the applied voltage is longer than the dielectric relaxation time of silicon, τ_D. That is, $1/w \gg \tau_D$, where w is the angular frequency of the applied ac voltage. When there is complete ionization of the dopant atoms ($N_D = n$ or $N_A = p$), the majority carrier response time τ_{mj} becomes equal to τ_D. For Si τ_{mj} is obtained as

$$\tau_{mj} = \frac{\epsilon_{si}}{q\mu p} \tag{58}$$

or

$$\tau_{mj} = \frac{\epsilon_{si}}{a} \tag{59}$$

for a *p*-type silicon substrate, where μ is the carrier mobility (cm^2/V · s) and σ is the conductivity. If the dopant density at the depletion layer edge is $p \approx 10^{16}$ cm^{-3}, then $\mu \approx 450$ cm^2/V · s, $\epsilon_{si} = 1 \times 10^{-12}$ F/cm, and $\tau_{mj} \approx 1.3 \times 10^{-12}$ s. This last quantity is the same as the dielectric relaxation time in Si.

Minority Carrier Response Time

In contrast with accumulation and depletion, where the role of majority carriers is very significant, minority carriers play the dominant role in the steady-state characteristics of MOS capacitors in inversion. Important processes that determine the minority carrier response time are therefore presented in this subsection.

The minority carrier response time in silicon at room temperature (300 K) is long, typically 0.01 s to 1 s in strong inversion. For this reason, minority carriers lag behind small changes in the applied ac voltage, and the capacitance in inversion is therefore frequency-dependent. The observation is illustrated in Fig. 15, which shows the dependence of capacitance on frequency as the applied voltage varies. It can be deduced that at low frequencies, the period of the ac signal is greater than the minority carrier response time. That is, $1/w \gg \tau_r$. At extremely low frequencies ($\leq$10 Hz), the capacitance at inversion reverts back to C_o, the capacitance of the oxide layer. This is in contrast with high frequencies ($\geq$1 kHz), at which the capacitance in inversion saturates at its minimum value.

The mechanism for determining the minority carrier response time depends on the method of gettering minority carriers to and from the inversion layer (13). At low temperatures ($\leq$300 K) the generation–recombination mechanism determines the minority carrier response time, whereas at high temperatures diffusion becomes the dominant mechanism. The transition temperature from the generation–recombination mechanism to the diffusion mechanism depends on the doping concentration in Si and the density of bulk traps in the oxide layer.

C–V PROFILING ON WIDE BAND-GAP SEMICONDUCTOR SUBSTRATES

Wide band-gap semiconductor materials including aluminum nitride (AlN, $E_g = 6.2$ eV), gallium nitride (GaN, $E_g = 3.2$ eV), and silicon carbide (SiC, $E_g = 3.0$ eV) are generally recognized for high-temperature and high-power devices capable of blue-light emission. Emphasis on these semiconductor materials has been on discrete devices, and efforts to obtain integration of common devices on a common substrate, as it is generally

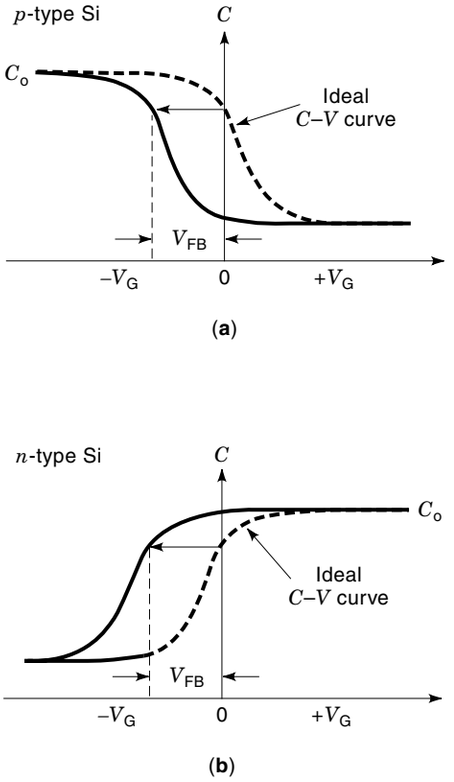

Figure 15. Determination of flatband voltage from high-frequency C–V curves. The curves are on (a) p-type Si and (b) n-type Si. The MOS structures used in both cases have the same positive oxide charge, and the curves marked "ideal" are theoretical curves with no oxide charge.

done in microelectronic chips, would require the fabrication of p–n junctions, Schottky diodes, and MOS (MIS) structures.

So far, problems associated with the growth and processing of these materials have made it difficult to fabricate the basic devices. Other device-related difficulties in wide band-gap materials include (a) obtaining a Schottky diode on n-type material because it is required that the work function of the metal be less than that of the semiconductor, (b) obtaining ohmic contact on p-type material, since the work function of the metal has to be greater than that of the semiconductor, (c) obtaining defect-free epitaxial layers, and (d) growing pure and defect-free oxides of the materials (22). Some of these difficulties are currently being solved by improved doping and growing techniques.

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CYBERCASTING. See BROADCASTING VIA INTERNET.