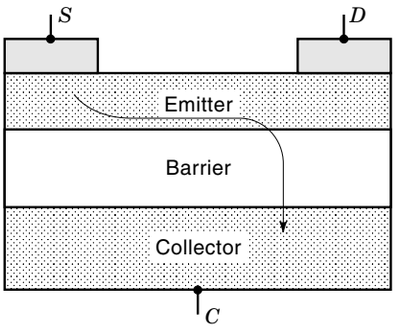


Figure 1. Schematic diagram of a charge injection transistor. Carriers in the emitter layer are heated by the source to drain electric field and undergo real-space transfer, as indicated by the arrow.

CHARGE INJECTION DEVICES

The term *charge injection* describes the operation of a generic class of electronic and optoelectronic multiterminal semiconductor devices, based on the real-space transfer of hot carriers over a potential barrier into adjacent and separately contacted layers. Charge injection devices allow the implementation of compact optoelectronic gates endowed with a powerful logic functionality.

OPERATION OF A CHARGE INJECTION DEVICE

The concept of real-space transfer (RST) (1–3) describes the process in which electrons in a narrow semiconductor layer, accelerated by an electric field parallel to the layer, acquire high average energy (become "hot") and then spill over an energy barrier into the adjacent layers. Redistribution of carriers between parallel layers of different mobility, leading to a negative differential resistance (NDR) and an unstable current-voltage characteristic in a two-terminal device, was the original intended application of RST (4).

Transistor applications of the RST began with the proposal by Kastalsky and Luryi (5) of a three-terminal structure where hot-electron injection occurs between *separately contacted* conducting layers. This structure, called the charge injection transistor, or CHINT, is illustrated in Fig. 1. One of the two layers (emitter) has source and drain contacts and plays the role of a hot-electron cathode. The other layer (collector) is separated by a potential barrier. When carriers in the emitter layer are heated by the source-drain field, most of them do not reach the drain but are injected over the barrier into the collector layer; a strong NDR develops in the drain circuit. The transistor action results from an efficient control of the electron temperature T_e and hence the injection current I_C by the input voltage V_{DS}.

Experimentally, CHINT was demonstrated for the first time at Bell Laboratories in 1984 (6) in a GaAs/AlGaAs heterostructure. Since then many other heterojunctions have been used to implement different versions of charge injection devices (7–9). We briefly review the main variations. The second section of this article describes the operation of CHINT in more detail, while the third section discusses a different operation of the same device that is based on the NDR effect in the channel. Logic properties of charge injection devices are described in the fourth section, and the last section describes light-emitting charge injection devices.

CHARGE INJECTION TRANSISTOR

The operation of CHINT is based on the control of the collector current by the heating voltage V_{DS}. The majority of CHINT devices have been implemented in III–V heterostructure materials and have employed the RST of hot electrons. Having higher mobility than holes, electrons are more easily heated by a lateral electric field to high effective temperatures. Nevertheless, the RST of holes has also been used in CHINT structures.

Recently, encouraging results were obtained in a $Si/Si_{0.7}Ge_{0.3}$ heterostructure. The $Si_{1-x}Ge_x$ material is of practical interest because of the possibility of integration of charge injection devices with standard silicon BICMOS logic. Since almost all of the band gap discontinuity between the strained $Si_{0.7}Ge_{0.3}$ channel layer and the Si barrier falls in the valence band and since the presence of a heterostructure barrier is essential for the device operation, a $Si_{1-x}Ge_x$ CHINT must necessarily employ the RST of hot holes.

The cross section of the device structure is illustrated in Fig. 2. The $Si/Si_{1-x}Ge_x$ layers were grown by rapid thermal epitaxy (RTE) on a 125 mm p-type Si substrate. The Ge fraction (x) in the emitter channel and in the collector layer is 30%, and the strained layer thickness is about 15 nm, which is below the mechanical equilibrium critical thickness for this composition. Shallow source and drain ohmic contacts are the most critical processing step for any CHINT device, because the contact must reach the thin channel layer without penetrating into the underlying barrier layer. The RTE of a boron-doped Ge layer followed by rapid thermal annealing was used to form the junction contacts with an estimated final depth $\leq$90 nm and an active surface concentration greater than $10^{20}\,cm^{-3}$. Finally, 10 nm Ti, 100 nm TiN, and 500 nm aluminum layers were deposited on the front side of the wafer and patterned to form the source, drain, and collector contacts.

Figure 3 shows the room temperature current-voltage characteristics of the Si/SiGe CHINT. The drain current, Fig. 3(a), shows a strong NDR for V_D above 1 V, with a peak to valley ratio (PVR) that increases with the collector bias. Simultaneously, the collector current increases, as illustrated in Fig. 3(b). Prior to the onset of RST ($V_D < 1$ V), a small I_C is present due to the thermionic emission of "cold" holes from the channel into the collector (this behavior is common to all CHINT devices and is not peculiar to the $Si_{1-x}Ge_x$ structure described here). For $V_C = -5.5$ V, PVR of the drain current greater than 2 is demonstrated. Further increase of the collector bias does not enhance the real PVR in the drain characteristic. In fact, as V_C increases, the leakage of "cold" holes also goes up, primarily because of their accumulation at the heterointerface (increasing the Fermi level) but also due to hole tunneling. As a result, the I_D curves shift down, almost rigidly, bringing about only an apparent increase of the PVR.

Variability of the RST current is obviously limited by the energy relaxation time associated with the equilibration of carriers in the channel. However, since this time is very short ($\leq$ 1 ps), the frequency performance of the device is believed to be limited in practice by the time of flight of hot electrons over high-field regions of the device (i.e., over distances of order the barrier-layer thickness). Experimental study (10), subsequently supported by Monte Carlo simulations (11), showed that the intrinsic short circuit current gain cutoff frequency, f_t, of CHINT is higher than that of an FET fabricated from the same material with an equivalent channel length. Belenky et al. (12) demonstrated a high-frequency operation of CHINT fabricated in an InP/InGaAs heterostructure and

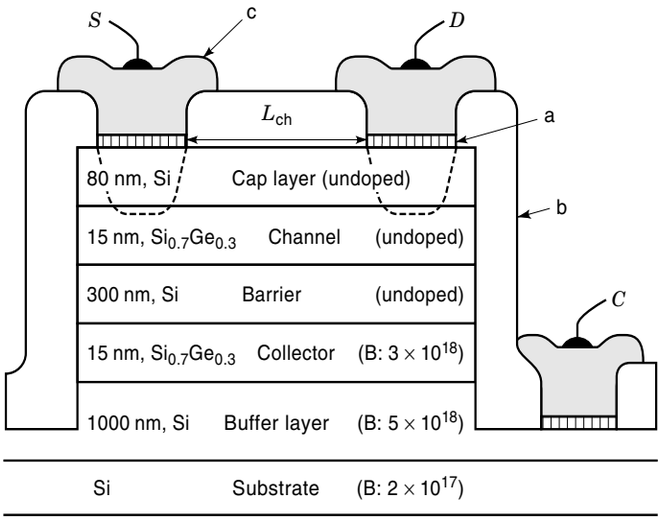


Figure 2. Schematic cross section of the $Si/Si_{0.7}Ge_{0.3}$ charge injection transistor structure. (After Ref. 9.)

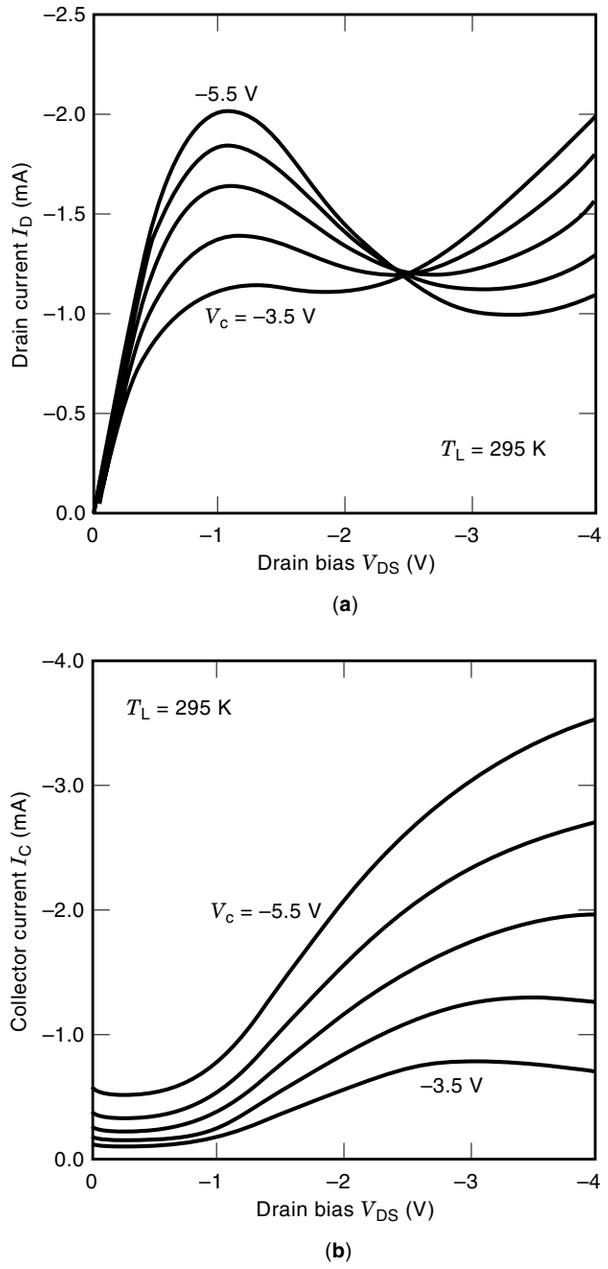


Figure 3. Room temperature characteristics in the drain (a) and collector (b) circuits at different collector biases for a 0.5 μm $\times$ 40 μm Si/SiGe CHINT.

based on electronic RST. Using a top-collector structure, in which parasitic capacitances are suppressed, they extrapolated a cutoff frequency of over 100 GHz for the short-circuit current gain $|h_{21}|$ measured at room temperature in a device with $L_{ch} = 1.0$ μm.

NEGATIVE DIFFERENTIAL RESISTANCE DEVICES

The name *negative resistance field-effect transistor* (NERFET) refers to the second mode of operation of the same structure, which is based on the NDR effect in the drain current. At the onset of RST, electrons (or holes in a p-channel device) deviate from the channel into the collector, causing a reduction of drain current. It is important to note that the NDR effect in the drain current is not a necessary consequence of the RST of channel carriers. The RST without NDR is a typical situation for high sheet carrier concentrations in the channel.

An extreme example of this situation would be to use a thin bismuth layer for the emitter channel separated from a semiconductor collector by a Schottky barrier, as proposed by Luryi and Kastalsky (13). On the other hand, in specially designed structures, the decrease of I_D can be very pronounced. Figure 4 shows the room temperature current-voltage characteristics of a 25 μm wide NERFET device fabricated (7) by molecular beam epitaxy (MBE) in InGaAs/InAlAs heterostructure lattice matched to InP substrate. Evidently, the NERFET characteristics are extremely nonlinear, with the $I_D(V_D)$ dependence exhibiting a strong and abrupt NDR with sharp steps. The observed peak to valley ratio is more than 1000.

Monte Carlo (MC) simulations (14,15) of the NERFET indicate that the NDR instability is accompanied by internal switching and formation of high-field domains. These large-scale instabilities arise due to a positive feedback between the RST and the heating electric field in the emitter channel. Both the experimental measurements and the MC calculations have been limited in analyzing the RST instabilities by the necessity of tracing IV characteristics exclusively in voltage increments. Significant progress in clarifying the nature of these instabilities was achieved (16,17) with the help of continuation modeling and transient device simulation. These studies revealed for the first time that the device has *multiply connected* two-terminal IV characteristics.

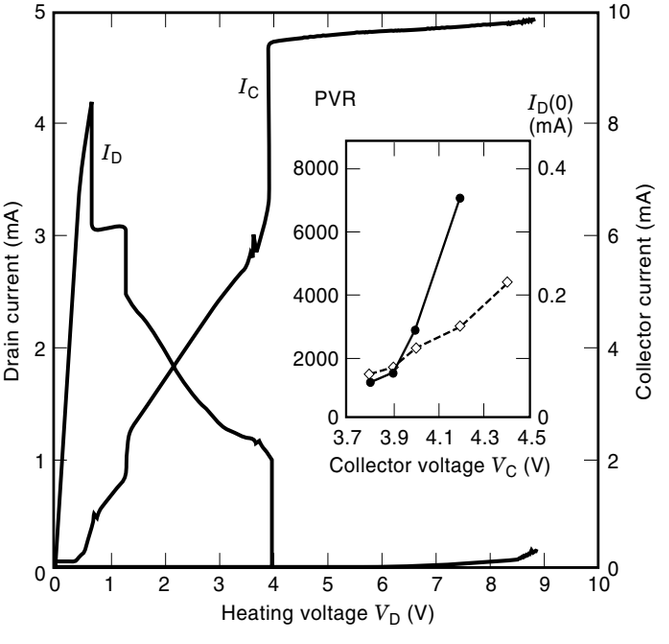


Figure 4. Room temperature current-voltage [$I_D(V_D)$ and I_C (V_D)] characteristics at a fixed collector bias $V_C = 3.9$ V for a device with $L_{ch} = 1.0$ μm. Inset: Collector-bias dependence of the peak-to-valley ratio and the leakage current, defined as the magnitude of I_D at $V_D = 0$ V. (After Ref. 7.)

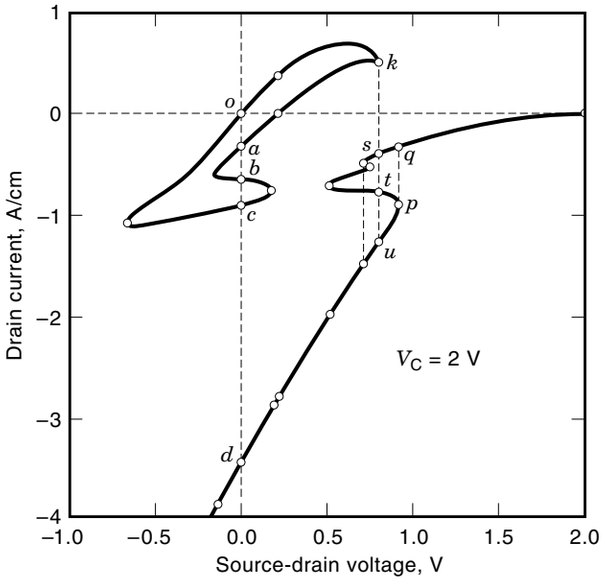


Figure 5. Simulation of the current-voltage characteristics of a InGaAs/InAlAs NERFET structure obtained by the continuation method. (After Ref. 16.)

The curves in Fig. 5 correspond to the locus of points in the (V_D, I_D) plane for which the device has a steady state at a given V_C. Any transition between disconnected components of the graph requires a global redistribution of the state fields corresponding to the formation or repositioning of high-field, high-temperature domains in the structure. Such a redistribution, reminiscent of a phase transition, is forced as V_D increases beyond the rightmost point (k) of the bounded graph component. The device makes a transition to point (s) where the drain current is negative. The "absolute negative resistance" occurs because of a thermoelectric effect that raises the channel potential above the drain value. The negative I_D has never been conclusively demonstrated, but it has become clear that there can be no limit to the value of PVR available in NERFET. Recently, Wu et al. (18) reported a PVR of 4×10^5.

The NDR instability in NERFET can be efficiently controlled by the third terminal (V_C). This property may be attractive for the design of circuits (19) with the improved performance in terms of reduced area and enhanced speed compared with standard (ECL) circuits. However, much additional work in circuit design is required to ascertain the advantage of employing NERFET devices.

CHARGE INJECTION LOGIC DEVICES

A fundamental property of CHINT is the symmetry equivalence (17) between the internal states $S[V_D, V_C]$ of the device at different applied biases:

$$S[V_D, V_C] \rightleftarrows S[-V_D, (V_C - V_D)] \tag{1}$$

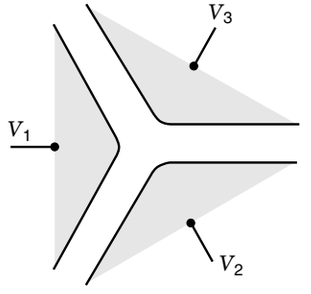
This correspondence follows from the reflection symmetry of the device. Although a similar relation exists between internal states $S[V_D, V_G]$ in a field-effect transistor, the difference is that unlike the gate of a FET, the CHINT collector is the output terminal, and the symmetry expressed by Eq. (1) implies that I_C is invariant under an interchange of the input voltages V_S and V_D. Thus the device exhibits an exclusive-OR (xor) dependence of the output current on the input voltage regarded as binary logic signals.

Even more powerful logic functionality is obtained in a device with three input terminals (20). This device, which we shall refer to as the ORNAND gate, has a cyclic three-fold symmetry (Fig. 6). Its truth table corresponds to ornand($\{V_j\}$) $\equiv$ norand, where

$$\text{norand}(V_j) = (V_1 \cap V_2 \cap V_3) \cup (\overline{V_1} \cap \overline{V_2} \cap \overline{V_3}) \tag{2}$$

and the symbols $\cap$, $\cup$, and $\bar{A}$ stand for logic functions and, or, and notA, respectively. The ornand equals or(V_1, V_2) when V_3 is low, and nand(V_1, V_2) when V_3 is high.

The first monolithic ORNAND device was demonstrated by Mastrapasqua et al. (21) in InGasAs/InAlAs heterostructure material. The device operates at room temperature with an on/off ratio of 7 in the output current (the device also emits a light signal with the same logic table as the collector current and even better on/off ratio). Perhaps promising for potential applications has been the demonstration of a SiGe/Si ORNAND device based on an epitaxial layer structure with strained $Si_{0.7}Ge_{0.3}$ (9). Although the SiGe/Si ORNAND devices have been demonstrated only at cryogenic temperatures, simulations show that room-temperature operation is quite feasible.



Logic input	V_3	0				1			
	V_2	1	0	0	1	1	0	0	1
	V_1	0	0	1	1	0	0	1	1
Output	I_C	1	0	1	1	1	1	1	0
Function		or				nand			

Figure 6. Principle of the multiterminal logic device ORNAND. Three input terminals arranged with a three-fold cyclic symmetry (top figures) defined three channels, 1–2, 2–3, and 3–1. The RST current I_C, as a function of the voltage V_1, V_2 and V_3 regarded as logic signals, obeys the truth table shown. The value of I_C is low (logic-0) in two states when $V_1 = V_2 = V_3$, and is high (logic-1) in the other six states.

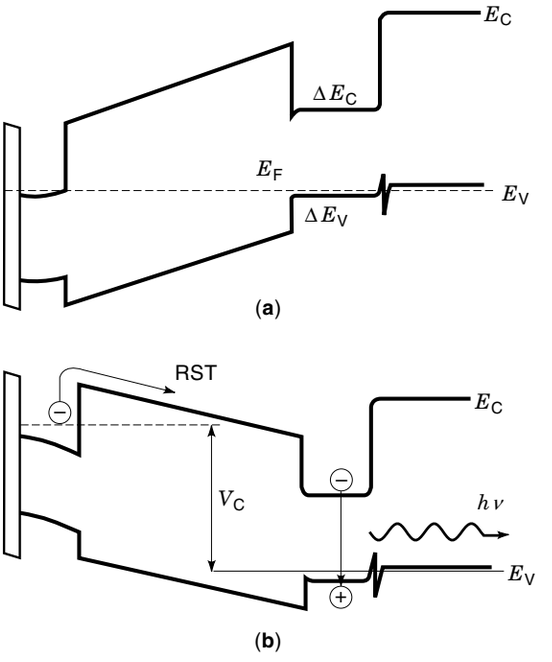


Figure 7. Schematic energy band diagram of a light-emitting charge injection device in equilibrium (a) and under a positive collector bias (b).

LIGHT-EMITTING CHARGE INJECTION DEVICES

In 1991 Luryi discussed (22) the possibility of using the RST of *minority carriers* in a collector layer of complementary conductivity type. This allows the implementation of light-emitting devices endowed with a logic functionality similar to that of the purely electronic charge injection devices described in the preceding section.

Figure 7(a) shows the energy band diagram of a light-emitting charge injection device. In the operating regime corresponding to a positive collector bias, Fig. 7(b), the collector-emitter *p-n* junction is forward biased and the only obstacle to current is due to the band discontinuities ΔE_C and ΔE_V. The heterostructure barriers are sufficiently high that the collector leakage current is relatively small even at room temperature. When the emitter electrons are heated by the lateral channel field, the electron temperature T_e substantially exceeds the lattice temperature T and a large RST injection current results. In a complementary structure, the injection current I_C is accompanied by a luminescence signal arising from the recombination of the injected electrons with holes in the collector active region. The purpose of the *p*-type wide energy-gap layer in the collector is spatially to confine the minority carriers. The confinement is necessary for a good radiative efficiency; otherwise most of the injected electrons would reach the collector contact prior to recombination.

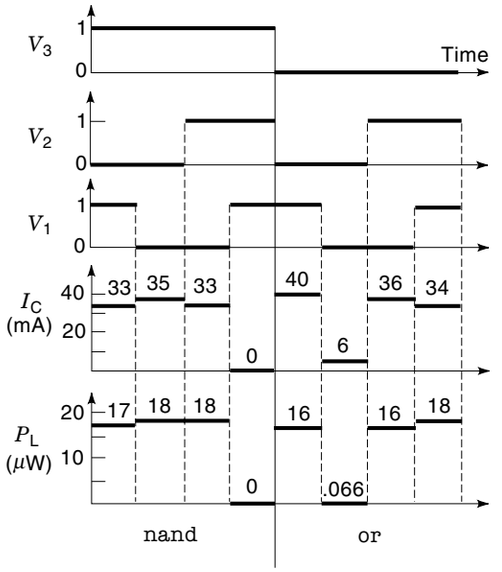


Figure 8. Optical and electrical logic operation of the light-emitting ORNAND gate, obtained in quasi-stationary measurements at room temperature for $V_C = 2.4$ V. The binary values `logic-0` and `logic-1` of the input signals V_1, V_2, and V_3 correspond to 0 and 3 V, respectively. The particular grouping of the states into OR and NAND reflects the choice of V_3 as the "control" electrode. (After Ref. 21.)

The first complementary CHINT was demonstrated in 1992 by Mastrapasqua et al. (23) using a InGaAs/InAlAs heterostructure. The `xor` operation of a light signal at 1.6 μm was studied in detail (24). Subsequently, a multiterminal light emitting ORNAND gate was also implemented (21), demonstrating the `or` and `nand` functions—both in the output light and the collector current—as well as the electrical switching between these functions (Fig. 8). The evidently superior logic characteristics for the light emission compared with those for the I_C current (Fig. 8) are explained by the fact that the leakage current, which in the InGaAs/InAlAs heterostructure is due to thermionic emission of holes from the active region, is not accompanied by any appreciable radiation. Holes injected in the channel recombine nonradiatively.

Recently Lai et al. (25) reported the fabrication of a light-emitting charge injection device with strained GaAs/$In_{0.2}Ga_{0.8}As$/AlAs heterostructures. The successful use of a strained active region is promising for the implementation of charge injection semiconductor lasers.

CONCLUSIONS

In principle, charge injection devices can be used in a variety of applications. As a high-speed device, CHINT has the advantage in that its ultimate speed is limited by the time of flight of hot electrons over distances on the order the barrier thickness rather than the source-to-drain time of flight characteristic of an FET. However, this time-of-flight advantage proves illusory when the device is scaled into deep submicron regime. The NDR property of the NERFET can have a variety of circuit applications, such as voltage-controlled local oscillators, where the control of NDR by the third electrode may be an important advantage. The powerful functionality of the ORNAND gate is very attractive, but its general-purpose logic application prospects suffer in view of the relatively large power dissipation. We believe the most attractive potential applications of charge injection devices will be found in the area of optoelectronics.

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