CAMAC

Computer automated measurement and control (CAMAC) is a standardized modular instrumentation and digital interface system. The CAMAC standard consists of mechanical, electrical, and logical specifications that define a method of electrically connecting a physical system to a computer for measurement and control. CAMAC was designed to be a data acquisition and control system for nuclear and elementary particle physics experiments. It was originally designed by physicists and engineers in 1968 and in many ways reflects the state of electronics and computers in that period. It is a tribute to the foresight of the designers that CAMAC is still in active use in universities and laboratories and remains a usable standard. It is found in research applications in many

Figure 1. A typical single-width CAMAC module. The 86-contact dataway connector is on the left. Above the dataway connector there is another edge connector in the free access area at the rear of the CAMAC crate. This area is available for any user-defined purpose. (Courtesy of LeCroy Corporation and Highland Technology.)

other disciplines—for example, chemistry, biology, and medicine. Although CAMAC is not often found on the factory floor, it is used in many industrial research and engineering test and data acquisition systems (for example, jet engine testing, automotive dynamometer test stands and military aircraft diagnostic test sets). CAMAC is a relatively simple, easy to use, yet powerful, modular system that is completely independent of the host computer. CAMAC satisfies the need for a simple, easy-to-use data acquisition system in laboratories all over the world.

The basic CAMAC unit is the module, which consists of a printed circuit board, a mechanical frame, and a front panel. The connection to the CAMAC dataway is via an 86-contact printed circuit edge connector. The module contains all of the circuitry associated with the measurement or control function and a simple interface to the CAMAC dataway. A typical module is shown in Fig. 1. Hundreds of different modules have been designed for a wide range of functions, from high-performance charge-integrating analog-to-digital converters for physics experiments to stepping motor controllers for industrial applications. A large part of the appeal of CAMAC is the ease with which a CAMAC module can be designed and constructed for a special application.

The CAMAC dataway is a parallel bus with up to 25 module stations. The first 24 are normal stations and the bus contains 8 power lines, 24 write data lines, 24 read data lines, and 19 control lines. The control lines include 9 encoded lines [5 for the function and 4 for the subaddress (within the module)] and 2 timing signals (S1 and S2). The pin assignments for a normal station are shown in Table 1. The rightmost (25th) station on the dataway is the control station. Instead of the 48 data lines, there are two sets of 24 radial lines [24 N (station number) lines and 24 L (look-at-me, or LAM) lines] that are not bused. The pin assignments are shown in Table 2, and the standard uses of these lines are shown in Table 3. Each pair of N and L lines connect to only one of the 24 normal stations. The module stations are addressed with the 24 N lines. Multiple N lines may be asserted simultaneously for broadcast operations. The 24 L lines are used by the module as an interrupt to request service from the controller. The CAMAC dataway was designed as a dedicated data acquisition and control bus, not as a general-purpose computer bus. There is no wide address bus for accessing memory, and there is no continuously running clock.

The module plugs into a chassis, called a crate, that provides mechanical support, electrical power, forced air cooling, and the CAMAC dataway. A full-size CAMAC crate fits in a standard 19 in. rack and holds 23 modules plus the double-width controller. A typical CAMAC crate is shown in Fig. 2. The crate dimensions allow NIM modules (Standard Nuclear Instrument Modules, United States Atomic Energy Commission report TID-20893, July 1964, and United States Department of Energy report DOE/ER-0457T, May 1990) to be installed with a power adapter that plugs into the CAMAC dataway. A single width NIM module occupies two CAMAC stations. Smaller crates are available for portable and bench-top applications. The crate supplies ± 24 V ($\pm 1\%$) and ± 6 V ($\pm 2.5\%$) dc power to the dataway. The crate may optionally supply ± 12 V ($\pm 1\%$) and supplementary ± 6 V ($\pm 2.5\%$).

The CAMAC crate controller is a special module that occupies stations 24 and 25 (the two right-most stations) in the crate and connects the CAMAC dataway to the host computer system, either directly or as part of a network of CAMAC crates. A wide variety of crate controllers have been designed and built at laboratories and by commercial suppliers. Crate controllers have been designed for many computers and buses over the years, including the Digital Equipment Corporation PDP-11 (Unibus and Q-bus), Small Computer System Interface (SCSI), General Purpose Interface Bus (GPIB), and Ethernet. A SCSI bus controller is shown in Fig. 3. Intelligent crate controllers (incorporating microprocessors) can convert a CAMAC crate into a complete stand-alone data acquisition and control system.

The basic CAMAC command cycle is synchronous and 1 μs long. During the CAMAC cycle, up to 24 bits of data can be transferred, a control function can be executed, or the status of a selected feature in the module can be tested. An oscilloscope record of a CAMAC dataway cycle is shown in Fig. 4.

At the start of a CAMAC command the crate controller asserts the (individual) N line for the module (or modules) to be addressed, and it asserts the busy signal, function code, and subaddress on the dataway. The function code determines the behavior of the rest of the command. The subaddress selects a location in the module. If data is to be transferred to the module (a write command, function codes 16 to 23), the data are placed on the 24 write lines. The module decodes the function and subaddress and asserts the response on the appropriate dataway lines. The X bus line indicates that the command is valid and has been accepted by the module. During read commands (function codes 0 to 7), the module places the data on the 24 read lines. During read commands, the Q bus line (a general-purpose 1-bit response line) is usually used to indicate that the data are available and valid.

When the S1 timing pulse is asserted (by the controller), all signals on the dataway must be in the correct state. The

Table 1. Pin Assignments at a Normal Station (1–24), Viewed from Front of Crate[a]

			#		#			
Bus line	Free bus line	P1	1	*	2	B	Busy	Bus line
Bus line	Free bus line	P2	3	*	4	F16	Function code	Bus line
Individual patch contact	P3	F8	5	*	6	F8	Function code	Bus line
Individual patch contact	P4	F4	7	*	8	F4	Function code	Bus line
Individual patch contact	P5	F2	9	*	10	F2	Function code	Bus line
Bus line	Command accepted	X	11	*	12	F1	Function code	Bus line
Bus line	Inhibit	I	13	*	14	A8	Subaddress	Bus line
Bus line	Clear	C	15	*	16	A4	Subaddress	Bus line
Individual line	Station number	N	17	*	18	A2	Subaddress	Bus line
Individual line	Look-at-me	L	19	*	20	A1	Subaddress	Bus line
Bus line	Strobe 1	S1	21	*	22	Z	Initialize	Bus line
Bus line	Strobe 2	S2	23	*	24	Q	Response	Bus line
Bus line	W24 = MSB	W24	25	*	26	W23		Bus line
Bus line		W22	27	*	28	W21		Bus line
Bus line		W20	29	*	30	W19		Bus line
Bus line		W18	31	*	32	W17		Bus line
Bus line		W16	33	*	34	W15		Bus line
Bus line		W14	35	*	36	W13		Bus line
Bus line	24 Write bus lines	W12	37	*	38	W11		Bus line
Bus line		W10	39	*	40	W9		Bus line
Bus line		W8	41	*	42	W7		Bus line
Bus line		W6	43	*	44	W5		Bus line
Bus line		W4	45	*	46	W3		Bus line
Bus line		W2	47	*	48	W1	W1 = LSB	Bus line
Bus line	R24 = MSB	R24	49	*	50	R23		Bus line
Bus line		R22	51	*	52	R21		Bus line
Bus line		R20	53	*	54	R19		Bus line
Bus line		R18	55	*	56	R17		Bus line
Bus line		R16	57	*	58	R15		Bus line
Bus line		R14	59	*	60	R13		Bus line
Bus line	24 Read bus lines	R12	61	*	62	R11		Bus line
Bus line		R10	63	*	64	R9		Bus line
Bus line		R8	65	*	66	R7		Bus line
Bus line		R6	67	*	68	R5		Bus line
Bus line		R4	69	*	70	R3		Bus line
Bus line		R2	71	*	72	R1	R1 = LSB	Bus line
Power bus line	−12 V dc	−12	73	*	74	−24	−24 V dc	Power bus line
Power bus line	Reserved [c]		75	*	76	−6	−6 V dc	Power bus line
Power bus line	Reserved [a]		77	*	78		Reserved [b]	Power bus line
Power bus line	Auxiliary −6 V supply	Y1	79	*	80	E	Clean earth	Power bus line
Power bus line	+ 12 V dc	+12	81	*	82	+24	+24 V dc	Power bus line
Power bus line	Auxiliary +6 V supply	Y2	83	*	84	+6	+6 V dc	Power bus line
Power bus line	0 V (Power return)	0	85	*	86	0	0 V (Power return)	Power bus line

[a] The ±12 V power supplies and the auxiliary ±6 V supplies are optional, and may not be found in all crates.

module has decoded the command and placed any required response on the appropriate dataway lines. At S1 time, the controller accepts the data on the X and Q lines (and R lines for a read operation). The module accepts data on the W lines (for write commands) and performs any action (possibly irreversible) required by the function code and subaddress. The S2 timing pulse occurs shortly after the S1 pulse and is used to initiate actions that may change the signals (R or Q lines) on the dataway. After the S2 pulse, all dataway lines are released and the CAMAC cycle is complete.

The maximum rate of CAMAC command operations is 1 MHz. This corresponds to a maximum data transfer rate between the controller and a module of 3 Mbytes/s.

HISTORY OF CAMAC

CAMAC was actually designed by a committee. During the 1960s, computers began to be used in elementary particle and nuclear physics experiments. At that time, computers were usually built with discrete components (transistors, diodes, etc.) on small cards that plugged into wire-wrapped backplanes. Logic signal voltage levels were not standardized, and neither were word lengths. The computers used for experiments came with 12-, 18-, 24-, or 36-bit words. Interfacing a computer to an experiment was a difficult task, and there were no standard components that would easily plug together. Nearly everything was a custom design, and not all

Table 2. Pin Assignments at the Control Station (25), Viewed from Front of Crate[a]

			#		#			
Individual patch contact	P1	P1	1	*	2	B	Busy	Bus line
Individual patch contact	P2	P2	3	*	4	F16	Function code	Bus line
Individual patch contact	P3	F8	5	*	6	F8	Function code	Bus line
Individual patch contact	P4	F4	7	*	8	F4	Function code	Bus line
Individual patch contact	P5	F2	9	*	10	F2	Function code	Bus line
Bus line	Command accepted	X	11	*	12	F1	Function code	Bus line
Bus line	Inhibit	I	13	*	14	A8	Subaddress	Bus line
Bus line	Clear	C	15	*	16	A4	Subaddress	Bus line
Individual patch contact	P6	P6	17	*	18	A2	Subaddress	Bus line
Individual patch contact	P7	P7	19	*	20	A1	Subaddress	Bus line
Bus line	Strobe 1	S1	21	*	22	Z	Initialize	Bus line
Bus line	Strobe 2	S2	23	*	24	Q	Response	Bus line
Individual line	24 Individual	L24	25	*	26	N24	24 Individual	Bus line
Individual line	Look-at-me	L23	27	*	28	N23	Station number	Individual line
Individual line	Lines	L22	29	*	30	N22	Lines	Individual line
Individual line		L21	31	*	32	N21		Individual line
Individual line		L20	33	*	34	N20		Individual line
Individual line	L1 connects to	L19	35	*	36	N19	N1 connects to	Individual line
Individual line	Station 1, etc.	L18	37	*	38	N18	Station 1, etc.	Individual line
Individual line		L17	39	*	40	N17		Individual line
Individual line		L16	41	*	42	N16		Individual line
Individual line		L15	43	*	44	N15		Individual line
Individual line		L14	45	*	46	N14		Individual line
Individual line		L13	47	*	48	N13		Individual line
Individual line		L12	49	*	50	N12		Individual line
Individual line		L11	51	*	52	N11		Individual line
Individual line		L10	53	*	54	N10		Individual line
Individual line		L9	55	*	56	N9		Individual line
Individual line		L8	57	*	58	N8		Individual line
Individual line		L7	59	*	60	N7		Individual line
Individual line		L6	61	*	62	N6		Individual line
Individual line		L5	63	*	64	N5		Individual line
Individual line		L4	65	*	66	N4		Individual line
Individual line		L3	67	*	68	N3		Individual line
Individual line		L2	69	*	70	N2		Individual line
Individual line		L1	71	*	72	N1		Individual line
Power bus line	−12 V dc	−12	73	*	74	−24	−24 V dc	Power bus line
Power bus line	Reserved [c]		75	*	76	−6	−6 V dc	Power bus line
Power bus line	Reserved [a]		77	*	78		Reserved [b]	Power bus line
Power bus line	Auxiliary −6 V supply	Y1	79	*	80	E	Clean earth	Power bus line
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Power bus line	0 V (Power return)	0	85	*	86	0	0 V (Power return)	Power bus line

[a] The ±12 V power supplies and the auxiliary ±6 V supplies are optional, and may not be found in all crates.

researchers followed good engineering practices. A typical experiment was a tangle of cables between the computer and the detectors. Reliability was not always achieved.

Recognizing these problems, the scientists and engineers at many of the European laboratories and research institutes collaborated on a solution in which most of the system is independent from the choice of computer. In 1969 the European Standards on Nuclear Electronics (ESONE) committee issued a report (EUR 4100e) describing a modular system of instrumentation that incorporated a digital data and control highway. To quote from the introduction to that report (1):

> The increasing demand for data processing has generated a need for a modular system which communicates efficiently and in a standardized manner with a digital controller or computer. At the same time the use of integrated circuit elements has reduced the volume required for individual units, while increased reliability makes it possible to envisage more complex assemblies. . . . The new system, known as CAMAC, is not restricted to nuclear instrumentation but is applicable to all forms of data processing which make use of a digital computer.

This first report specified the logical, mechanical, and electrical details of the module, the dataway, and the crate. In 1970 the parallel branch highway system and type A crate controller were specified by EUR 4600e.

The ESONE reports were endorsed by the US Atomic Energy Commission (AEC) Nuclear Instrumentation Modules (NIM) Committee in March 1970, and the development of CAMAC became a collaboration between Europe and the United

Table 3. Standard CAMAC Dataway Usage

Command		
Station number	N	Selects module (individual line from control station)
Function	F1, 2, 4, 8, 16	Defines function to be performed in module
Subaddress	A1, 2, 4, 8	Selects section of module
Data		
Write	W1–W24	Write to module (F16–23)
Read	R1–R24	Read from module (F0–7)
Timing		
Strobe 1	S1	Controls first phase of command (all dataway lines are stable except S1) Controller accepts read data and module accepts write data at S1 Module should not take any irreversible action before S1
Strobe 2	S2	Controls second phase of command Data (R1–R24 and W1–W24) signals may change at S2
Status		
Look-at-me	L	Indicates request for service (individual line to control station)
Busy	B	Indicates that dataway operation is in progress
Response	Q	Indicates status of feature selected by command
Command accepted	X	Indicates that module is able to perform action required by command
Common controls		
Initialize	Z	Sets module to defined initial state (accompanied by S2 and B)
Inhibit	I	Optional; disables features for duration of signal
Clear	C	Optional; clears module (accompanied by S2 and B)
User specified dataway signals		
Free bus-lines	P1, P2	Bus line (station 1–24)
Patch contacts	P3–P5	Not bussed

States. The description of CAMAC, with minor changes and corrections, was issued as AEC reports TID-25875, TID-25876, and TID-25877.

The CAMAC Serial Highway was specified in 1973. The serial highway allowed CAMAC to be used for large distributed data acquisition and control systems. Specifications for analog signals and a CAMAC computer language, IML, were added in 1974 and 1975. CAMAC joined the IEEE in 1975 as IEEE Std 583-1975. The IEEE CAMAC standards are still active, having been reaffirmed several times, most recently in 1994.

The CAMAC module and dataway specifications have changed very little since 1969. In 1971 the originally reserved X bus line was defined as the command-accepted signal. In 1979 three rarely used optional power lines—the alternating-current (ac) power line connection, ACL and ACN, and the +200 V line (intended for neon indicator lamps)—were removed from the dataway for safety reasons (these lines are now called reserved a, b, and c). By 1982 the two reserved power lines, Y1 and Y2, were defined as optional supplementary ±6 V power lines. Since 1982 there have been no changes to the CAMAC module and dataway specifications. As a result, most CAMAC modules are still usable today (even those designed and built to the original specifications in 1969). A CAMAC crate from 1969 would also be usable, if the optional power lines had not been implemented (or were removed).

Figure 2. An empty full-size rack mount CAMAC crate with 25 module stations. The dataway connectors and the free space above the dataway are clearly visible. (Courtesy of Kinetic Systems Corporation.)

Signal Standards on the CAMAC Dataway

The signals on the CAMAC dataway are compatible with ordinary TTL (or HCT) receivers. All signals are driven with open collector drivers, rather than TTL totem pole drivers. The logic is negative; that is, logic 1 corresponds to the driver sinking current to ground (the voltage on the dataway is less than 0.5 V). Logic 0 corresponds to the driver off. Each signal line has a pull-up current source (typically a resistor to +5 V located in the controller) which causes logic 0 on the dataway to be between 3.5 V and 5.5 V. A voltage less than 0.8 V is detected by the receiving module as a logic 1, and a signal between 2 V and 5.5 V is detected as a logic 0.

A full CAMAC crate contains 24 module stations and a control station. The loading allowed also corresponds to ordinary TTL. Each module that receives a signal may supply up to 1.6 mA (one ordinary TTL load) when the bus is at logic 1, and it may supply up to 100 μA when the bus is at logic 0. The controller must supply the logic 1 current to 24 modules (38.4 mA) for the lines that are received by all modules (the

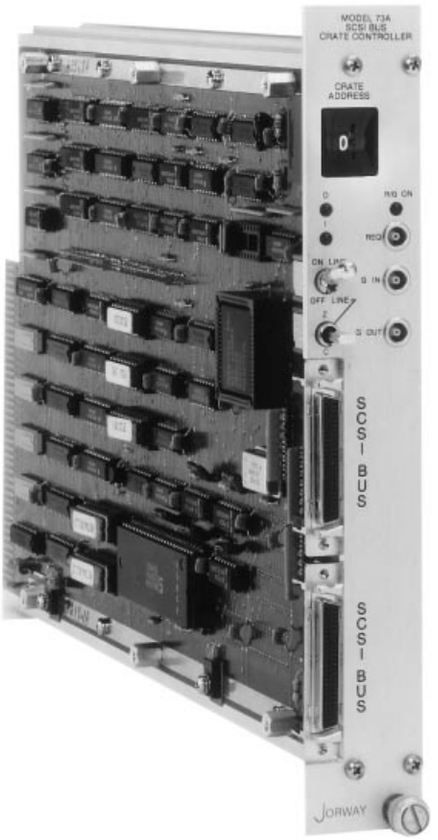

Figure 3. A CAMAC crate controller. This particular model connects to the host computer via the SCSI bus. (Courtesy of Jorway Corporation.)

control lines and the write lines). A module need supply only 16 mA on those lines that it drives, since the only loads are the controller and any auxiliary controllers. Although modern HCT circuits are compatible and have much lower input current requirements, the designer should assume that all other modules in the crate use ordinary TTL receivers.

All dataway lines are driven with intrinsic OR (open collector) drivers. This allows signals to be wire-OR'ed on the dataway and avoids potentially damaging bus conflicts. When CAMAC was designed, there were no tristate driver integrated circuits, and open collector drivers are a simple method of driving a shared bus. The rise time and the fall time of the signals are not the same. The signal rise time (logic 1 to logic 0) on the dataway is proportional to the pull-up resistance and the capacitive load (of the dataway and the modules) and can be as long as 250 ns (*RC* time constant). The fall time is much less but is required to be at least 10 ns to minimize noise and crosstalk on the dataway.

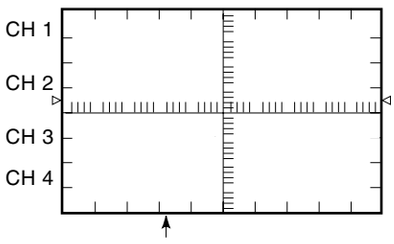

Figure 4. An oscilloscope recording of a CAMAC operation on the dataway. Ch1 is the busy line, indicating an operation in progress. The other control lines (N line, Function Code and Subaddress) are similar to the busy line. Ch2 and Ch3 are the two strobe signals, S1 and S2. Ch4 is a data line, which is valid during S1 and allowed to return to logic 0 at S2. The horizontal scale is 200 ns per division. The CAMAC dataway uses negative logic, a high signal is logic 0 and a low signal is logic 1.

Open collector bus drivers are becoming obsolete and may not be easy to obtain in the future. Some CAMAC designers are using TTL totem pole or CMOS tristate drivers to achieve higher density and lower power. This is not a recommended practice, since transient bus conflicts will inevitably occur and the system behavior may not be predictable. The preferred alternative is to use a complex programmable logic device (CPLD). These are available from several manufacturers and can readily emulate open collector drivers (the output drivers must have individual output enables).

CRATE CONTROLLERS

The crate controller is the link between the CAMAC dataway and the host system. It occupies two module positions, usually station 24 and 25. Station 24 provides access to the data lines, and station 25 provides access to the N and L lines. The crate controller can connect directly to the host computer or computer network (such as GPIB or Ethernet); or it can connect indirectly, through a network of CAMAC crates. The CAMAC standard defines two such networks of CAMAC crates, the parallel branch highway (IEEE Std 596) and the serial highway (IEEE Std 595). These CAMAC highways are designed to be independent from the choice of host computer system. A computer-specific driver module provides the interface between the CAMAC highway and the host system. This interface module can connect directly to the host computer by its internal bus (such as Unibus, PCI, or ISA bus) or be a part of another network or bus system, such as SCSI or VME.

The parallel branch highway system uses a 132-contact pin and socket connector and 66 twisted pair transmission lines (each signal has its own ground return line, but the signal itself is single-ended). As many as seven CAMAC crates can share a parallel branch highway. The cable is daisy-chained from crate to crate and is terminated at both ends. The total cable length is limited to about 30 m by signal loss considerations.

During a branch highway operation the BTA timing signal from the branch driver and the seven crate response lines (BTB1-7) are interlocked and determine the time of the S1 and S2 dataway pulses in the addressed CAMAC crate(s). This is an asynchronous protocol, and the length of the CAMAC cycle depends on the branch driver, the crate controller, and the length of the branch highway cable. The BTA and BTB signals are integrated to suppress noise, and delays are introduced to compensate for signal skew. A branch highway dataway cycle is usually less than 2 μs long.

Two crate controllers, type A-1 and type A-2, have been specified for the branch highway. The type A-2 controller adds an arbitration protocol that allows multiple controllers to share a CAMAC dataway.

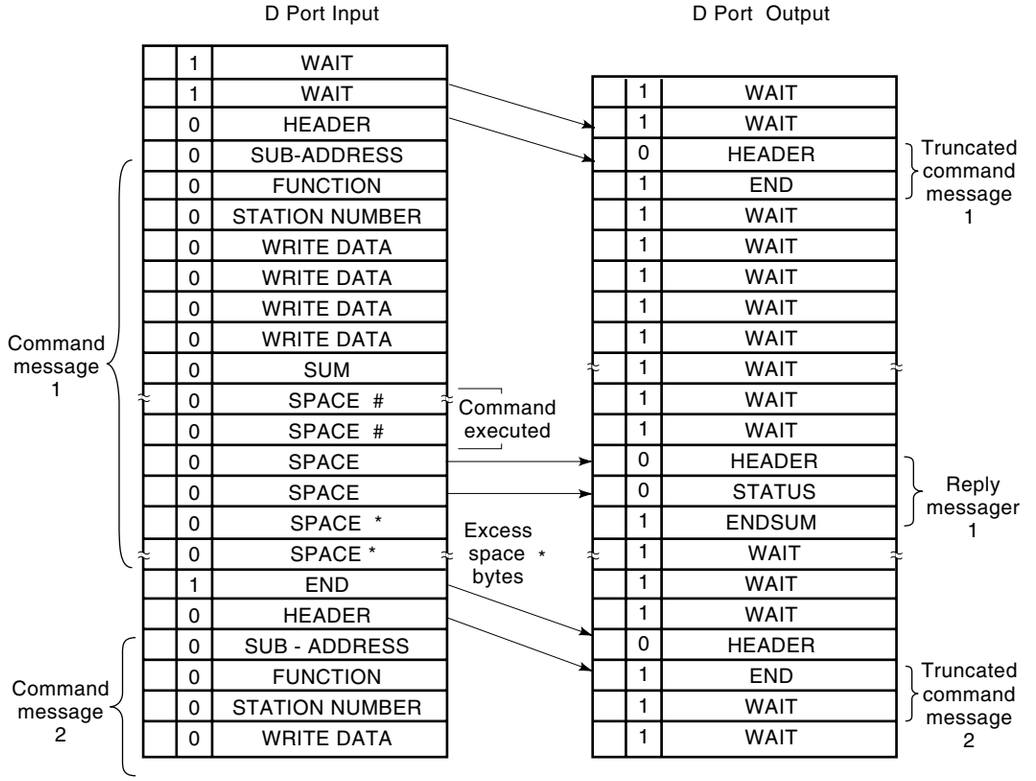

Figure 5. The CAMAC Serial Highway command and reply byte sequence for a Write operation.

The crate controller itself is addressed by normal CAMAC commands and otherwise unused station numbers. There is a station number register (SNR) at station 30, subaddress 8, which allows addressing several selected stations simultaneously, by addressing the command to station 24. Several other standard features are accessed at stations 28 and 30.

The serial highway interface system uses a 25-pin connector to implement either a byte serial or bit serial synchronous system. The byte serial system uses RS-422 differential signals on a nine-pair cable, an 8-bit byte, and a clock. The bit serial system uses only two wire pairs, data and clock, and employs start and stop bits to separate the bytes in the stream. The clock can be any speed required, up to 5 MHz. As many as 62 CAMAC crates are organized in a unidirectional loop topology, which passes through each connected CAMAC crate. Command messages are sent around the loop by the serial driver as multibyte frames that contain a sufficient number of space bytes to allow time for the addressed crate to execute the CAMAC cycle and space to insert the reply message in the byte stream. When the command message completes the trip around the loop and returns to the driver, it has been truncated and is followed by the reply message that contains the X and Q responses and the data (for read commands). This byte sequence is shown in Fig. 5 for a write command. In the absence of a command, wait bytes are continuously sent around the loop by the driver to maintain message synchronism and allow LAM messages to be inserted in the byte stream by CAMAC crates requiring service. The serial highway protocol contains error detection and recovery procedures and is quite robust. The asynchronous loop topology (with synchronous messages) places no limit on the length of cables or the time delay for a message to traverse the loop. The serial highway system is not limited to RS-422 data transmission. Adapters can be used to employ any available transmission medium. If fiber-optic adapters and cables are used, the practical limit extends to several kilometers between crates. Telephone lines (with modems) or the Internet can be used to extend a serial highway loop as far as required.

AUXILIARY CRATE CONTROLLERS

More than one controller may be installed in a CAMAC crate (IEEE Std 675, Multiple Controllers in a CAMAC Crate). Sharing control of the dataway is achieved with a 40-conductor auxiliary control bus (ACB) located at the rear of each controller. The primary controller (located in stations 24 and 25) is the only controller with access to the N lines and the L lines on the dataway. The primary controller retransmits the 24 dataway L lines on the ACB (making them available to all auxiliary controllers) and receives an encoded N signal from the auxiliary controller. The primary controller must drive the N lines with the encoded N signal whenever it does not have control of the dataway. An auxiliary crate controller can be a single-width module since it does not require direct access to the control station.

Arbitration among the multiple controllers in a crate is provided by two different access mechanisms, request/grant (R/G) and auxiliary controller lockout (ACL). In the R/G method, the controller requesting control asserts the request

bus line in the ACB. This signal becomes the grant-in to the controller with the highest priority and then passes through a grant-out grant-in priority chain to all other controllers. If two controllers request access simultaneously, the highest-priority (earliest in the chain) controller receives access first. The controller that gains access asserts the request inhibit signal on the ACB and proceeds with CAMAC operations. When the operations are complete, the request inhibit is removed and all controllers requesting control arbitrate again. There is no time limit for releasing control of the dataway. A controller may elect to maintain control for several dataway cycles or to relinquish control after each cycle. This mechanism works well for any number of controllers, as long as they can tolerate a variable delay between the request and the grant of access.

The ACL arbitration method is used when a controller cannot tolerate variable access delays or otherwise requires immediate access to the dataway. Note that only one controller in a crate can use the ACL method. All other controllers must use the R/G method. If another controller (that gained control through the R/G mechanism) has control of the dataway when the ACL line is asserted, it must either abort the CAMAC operation (if S1 has not yet been generated) or relinquish control as soon as the current command is complete.

The two standard CAMAC controllers—type A-2 (parallel branch) and SCC type L2 (serial highway) crate controllers—allow multiple crate controllers. The type A-2 may operate in either R/G or ACL mode. The SCC type L2 operates only with ACL, since it cannot tolerate delays in access. The SCC type L2 must execute the CAMAC command and transmit the reply within the byte frame allotted by the serial driver. The SCC type L-2 does not have an ACB connector; however, the serial graded LAM connector (SGL) contains the necessary signals (except request).

Commercial serial highway drivers and crate controllers have been designed which remove some of the limitations of the SCC type L2 (without requiring changes to the standard). These controllers are a superset of the type L2, and they allow the use of either the ACL or R/G arbitration method. The serial highway driver simply extends the command byte frame by inserting extra space bytes (as many as needed) until the reply is received (or the command times out). This R/G serial controller can be mixed in a serial system with standard SCC type L2 controllers.

BLOCK TRANSFERS

The CAMAC dataway protocol provides only a single CAMAC operation. Block transfers are implemented in the controller, or in the host software, as a sequence of single CAMAC operations. Several block transfer modes are described in IEEE Std 683. Many combinations of address sequencing, data synchronizing, and termination mode are possible. For example, the Q-stop mode allows reading variable (and unknown) length data blocks from a single address (station number and subaddress). The Q = 1 response indicates that valid data were transferred, and Q = 0 indicates that the transfer has completed. Another useful mode is the address scan. The subaddress is incremented after each transfer. When Q = 0 is detected (or when the subaddress rolls over), the station number is incremented and the subaddress is set to zero. This can be used to read a long sequence of registers (such as scalers or digital input registers) from an entire CAMAC crate.

For the serial highway system a special enhanced serial block transfer method (originally developed by KineticSystems Corp.) is available from several manufacturers. This method expands the data portion of the command/reply serial message so that multiple CAMAC cycles can be executed during the command/reply byte stream. The data portion of the byte stream is expanded by 5 bytes for each extra dataway cycle. This enhanced method allows reads and writes over the serial highway at a data rate up to 3 Mbytes/s.

THE FUTURE OF CAMAC

When the CAMAC standard was designed, it was considered to be a high-speed system. By today's standards, CAMAC is quite slow, but the maximum transfer rate of 3 Mbytes/s is still adequate for many applications, and CAMAC is still widely used. For many applications, however, CAMAC is just not fast enough and higher-speed alternatives, such as FASTBUS or VME are usually employed. Although much faster, these bus systems come with a much more complex protocol. Recently a compatible extension to CAMAC (FASTCAMAC) has been designed that allows data transfers at rates up to 60 Mbytes/s. FASTCAMAC is backward compatible with older CAMAC modules. All FASTCAMAC modules will also operate as normal CAMAC modules. FASTCAMAC controllers will operate both standard and FASTCAMAC modules. This extension is expected to become part of the CAMAC standard. It will be the first substantial change to the CAMAC dataway protocol since its original publication in 1969.

The CAMAC dataway speed is addressed in FASTCAMAC by adding a block transfer to the existing CAMAC protocol. CAMAC employs a simple 1 μs cycle which combines addressing, operation selection and data transfer. By separating the addressing and mode selection from the data transfer, it is possible to achieve speeds competitive with FASTBUS and VME, without sacrificing the simplicity and ease of use of CAMAC.

The normal CAMAC cycle consists of an addressing phase, a single data transfer (S1), and a closing phase (S2). FASTCAMAC modifies the CAMAC cycle by adding multiple S1 data strobes within a single extended CAMAC cycle. The addressing and closing phases are not changed, and they are compatible with normal CAMAC. The net effect is to replace the single data transfer with a high-speed block transfer. A FASTCAMAC timing example is shown in Fig. 6.

Although FASTCAMAC is more complicated and will be initially more difficult to design and use, the reward is appropriate for the effort involved. The FASTCAMAC standard is organized in two levels, with several options. This allows a wide range of performance to be realized, with a corresponding range of implementation effort required.

The most basic level of FASTCAMAC simply adds multiple S1 pulses, transferring data on each pulse, without increasing dataway speed or replacing dataway drivers. This simple change increases the maximum data transfer rate to 7.5 Mbytes/s, an increase of 2.5 times over normal CAMAC. The effort to achieve this is minimal, and many existing CAMAC modules have been modified to operate with this basic FAST-

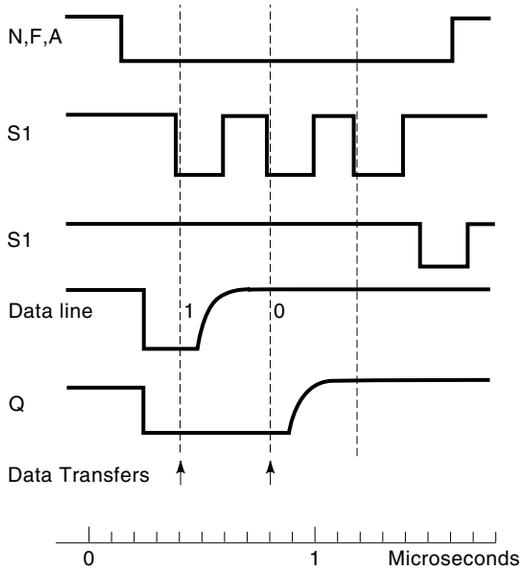

Figure 6. A FASTCAMAC basic Level 1 READ operation. Two data words are transferred, and the extended CAMAC command terminates on no Q.

CAMAC protocol with only a few wire changes or reprogramming a programmable logic device.

At the upper extreme, 60 Mbytes/s (20 times faster than normal CAMAC), the dataway is operated as a 48-bit bidirectional bus, transferring data on both edges of a sequence of 100 ns wide S1 pulses. This requires improved dataway drivers and substantial logical changes from normal CAMAC. This is not a simple modification, but it is easily implemented with modern programmable logic. FASTCAMAC is compatible with normal CAMAC, and FASTCAMAC modules will operate in a normal CAMAC crate.

The latest FASTCAMAC information and a complete specification of the extension can be found on the Internet at http://www.yale.edu/fastcamac/.

SUMMARY

The simplicity of the protocol is a major advantage that CAMAC enjoys over newer modular bus standards. It is relatively easy to design and build a CAMAC module for a special application. In the 1970s, a complete CAMAC dataway interface could be implemented with less than a dozen small-scale integrated (SSI) circuits. Today, the same interface can be implemented in one complex programmable logic device (CPLD). CAMAC modules do not rapidly become obsolete, but often have a long useful life. A data acquisition system tailored to an application is easily assembled from standard CAMAC modules, crates, and controllers and perhaps one or two special CAMAC modules. These are the features of CAMAC that have kept CAMAC in constant use in universities, laboratories, and industry for the past 30 years.

The two CAMAC network standards, the parallel branch highway and the serial highway, were designed before the wide use of computer networks. Until very recently, they have been much faster (and simpler) than most computer network systems. With the advent of low-cost, high-speed local area networks (LANs) such as Gigabit Ethernet and FireWire, the situation is changing and these standards are becoming obsolete. The concept of a dedicated interface between CAMAC and a specific computer is also obsolete, and we expect the future to bring more CAMAC connectivity to standard LAN architectures. Coupling the basic simplicity of CAMAC with standard high-speed LANs will make CAMAC easier to use with modern computing systems. The addition of FASTCAMAC to the protocol will ensure that CAMAC will be able to meet the demands of future experiments for many years to come.

There are several commercial manufacturers of CAMAC, some of which have been making CAMAC equipment since 1969. A search of the World Wide Web with the keyword CAMAC will find the current suppliers and many of the users of CAMAC. The CERN (www.cern.ch) and FERMILAB (www.fnal.gov) on-line library catalogues contain many CAMAC documents and articles. There have been many published articles on CAMAC, primarily in *Nuclear Instruments and Methods,* the *IEEE Transactions on Nuclear Science,* and the *Proceedings of the Annual IEEE Nuclear Science Symposia.* The IEEE standards are the best resource for designers of CAMAC equipment.

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