THERMAL ANALYSIS AND DESIGN OF ELECTRONIC SYSTEMS

TRENDS AND NEEDS IN THERMAL MANAGEMENT

Thermal Packaging Roadmaps

The challenges posed by high chip heat fluxes and ever more stringent performance and reliability constraints make thermal management a key enabling technology in the development of microelectronic systems for the 21st century. Thus, thermal packaging efforts must be performed in the context of the salient trends and parameters that characterize the IC technology and the electronic products industry.

Recent road-mapping efforts, including the Semiconductor Industry Association's (SIAs) National Technology Roadmap for Semiconductors (1) and NEMI's National Electronics Manufacturing Technology Roadmap (2), have affirmed the expectation that improvements in CMOS semiconductor technology will continue unabated into the early part of the 21st century. Exploiting the potential of this IC technology, with the attendant increase in chip size, switching speed, and transistor density will necessitate significant improvements in packaging technology. Furthermore, under the influence of growing product complexity, packaging is evolving from an IC technology enabler, to a primary electronic product/system differentiator. Consequently, future packaging technology may well be driven primarily by market application requirements, with reduced cost per function providing the major technology development and execution challenges.

The SIA and NEMI roadmaps recognize the six categories of market applications listed in Table 1. Together these categories encompass the majority of the product stream of the semiconductor industry. It is anticipated that system costs will remain fixed in each of these categories, despite ever increasing functionality. It is also assumed that power, voltage, operating and chip junction temperatures, as well as package thickness, will be determined by market requirements, whereas all other needs are derived from scaling laws or physics-based extrapolations.

Table 2 summarizes the range expected to prevail in the salient IC device characteristics, across the six categories. As may be seen in Table 2, by the year 2006, at the leading edge, chip frequency is expected to reach 1250 MHz with a chip size of 900 mm^2 and a chip power 140 W. In assessing the technology needed for each of these categories, emphasis was placed on the revenue "center-of-gravity."

Based on these considerations, the NEMI Packaging Working Group determined that the following research and development issues needed to be addressed:

- Ariving innovation with aggressive cost-reduction targets, for all but the Cost-Performance segment
- Achieving the breakthroughs needed for 0.2 mm chip thinning and handling
- EMI and noise margin management, for high-speed, low-voltage applications
- Integration of design, chip fabrication, assembly and packaging and test technologies beyond 2001
- Anticipation of an accelerating shift from peripheral to area array chip interconnects

The NEMI Working Groups also concluded that significant improvements in thermal management are required to support power–cost targets and that automotive needs $T_j >$ 185°C) will require new quality and reliability techniques and packaging.

It may thus be seen that the challenges posed by high chip heat fluxes and ever more stringent performance and reliability constraints make thermal management one of the key enabling technologies for microelectronic systems in the 21st century. Focusing more specifically on cooling needs, the NEMI Working Groups proposed the following topology for thermal packaging technology:

- Commodity products—natural convection
- Hand-held products—natural convection with heat spreaders
- Cost and performance products—forced convection with heat sinks
- High performance products—forced convection, aggressive heat sinking, heat pipes, impingement cooling, and liquid cooling

Thermal Packaging Options

When the heat flux dissipated by an electronic component, device, or assembly and the local ambient temperature are known and the allowable temperature is specified, the equations of the following sections can be used to determine which heat transfer process or combination of processes (if any) can be employed to meet the desired performance goals. Figure 1 shows the variation of attainable temperature differences with surface heat flux for a variety of heat transfer modes and coolant fluids.

Examination of Fig. 1 reveals that for a typical allowable temperature difference of 60°C between the component surface and the ambient, natural cooling in air, relying on both free convection and radiation, is effective only for heat fluxes below approximately 0.05 W/cm^2. Although forced convection cooling in air offers approximately an order-of-magnitude improvement in the heat transfer coefficient, this thermal configuration is unlikely to provide heat removal capability in excess of 1 W/cm^2 even at an allowable temperature difference of 100°C.

To facilitate the transfer of moderate and high heat fluxes from component surfaces, the thermal designer must choose between the use of finned air-cooled heat sinks and direct or indirect liquid cooling. Finned arrays and sophisticated techniques for improving convective heat transfer coefficients can extend the effectiveness of air cooling to progressively higher component heat fluxes but often at ever-increasing weight, cost, and volume penalties. Alternatively, reliance on heat transfer to liquids flowing at high velocity through so-called cold plates can offer a dramatic improvement in the trans-

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Table 1. SIA/NEMI Roadmap Product Categories

Product	Description
Low cost − <$300	Commodity consumer products, disk drives, displays, and microcontrollers
Hand held − <$1000	Battery-powered products, PDAs, and cellular telephones
Cost/performance − <$3000	Notebooks, desktop computers, and telecommunications
High performance − >$3000	High-end workstations, servers, and supercomputers
Harsh environments	Under-the-hood automotive, mining, and resource exploration
Memory	DRAMs and SRAMs

ferrable heat flux even at temperature differences as low as 10°C, when the conduction resistance in the cold plate wall is negligible.

A similarly high heat flux capability is offered by boiling heat transfer to fluorochemical liquids. The high dielectric properties of these liquids make it possible to immerse most components. This direct liquid contact allows the removal of component heat fluxes in excess of 10 W/cm^2 with saturated pool boiling at temperature differences typically less than 20°C. Immersion cooling can also offer significant advantages and, as seen in Fig. 1 (3), serves to bridge the gap between direct air cooling and cold plate technology.

Unfortunately, when addressed within stringent cost targets, the cooling requirements of 21st century microelectronic

Table 2. SIA National Technology Roadmap—Parameter Range for 2006

Parameter	Value
Chip frequency	300 to 1250 MHz
Chip size	75 to 900 mm^2
Package inputs/outputs	400 to 2200
Chip power	1 to 28 to 140 W
Junction temperature	100 to 195°C
Ambient temperature	45 to 170°C
Voltage	0.90 to 3.30 V

Source: Semiconductor Industry Association (1).

components cannot be met by today's thermal packaging technology. Rather, ways must be sought to improve on currently available technology, to leverage and combine the best features of existing thermal packaging hardware, and to introduce unconventional, perhaps even radical, thermal solutions into the electronic product family. In so doing, attention must be devoted to three primary issues:

1. *Highly Effective Air Cooling.* Removing dissipated power from one or several advanced chips within minimal volumes and with low air-side pressure drops.
2. *Heat Spreading.* Transporting heat from a relatively small area contiguous with the chip to a relatively large heat sink or cold plate base
3. *Interfacial Heat Transfer.* Thermal resistances between the chip and the next level of thermal packaging

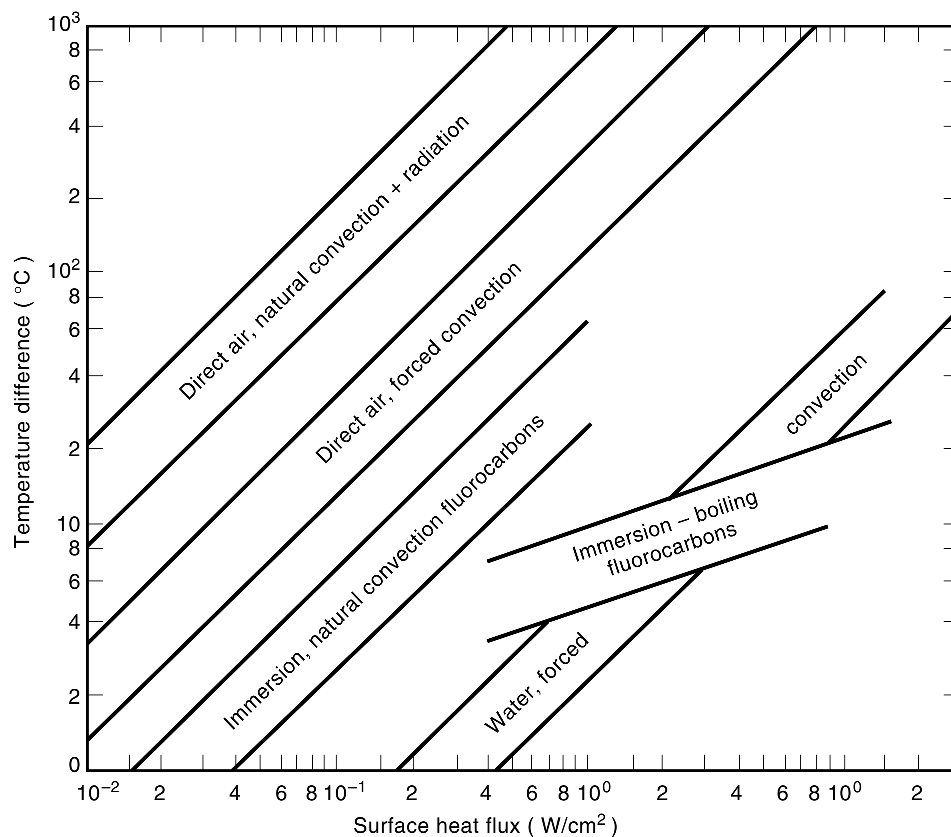

Figure 1. Temperature differences attainable as a function of heat flux for various heat transfer modes and various coolant fluids (3).

Attention now turns to a detailed discussion of basic heat transfer and the determination of the various types of thermal resistances often encountered in electronic equipment.

THERMAL MODELING

To determine the temperature differences encountered in the flow of heat within electronic systems, it is necessary to recognize the relevant heat-transfer mechanisms and their governing relations. In a typical system, heat removal from the active regions of the microcircuit(s) or chip(s) may require the use of several mechanisms, some operating in series and others in parallel, to transport the generated heat to the coolant or ultimate heat sink. Practitioners of the thermal arts and sciences generally deal with four basic thermal transport modes: conduction, convection, phase change, and radiation.

Conduction Heat Transfer

One-Dimensional Conduction. Steady thermal transport through solids is governed by the Fourier equation, which in one-dimensional form, is expressible as

$$q = -kA\frac{dT}{dx} \tag{1}$$

where q is the heat flow, k is the thermal conductivity of the medium, A is the cross-sectional area for the heat flow, and dT/dx is the temperature gradient. As depicted in Fig. 2 (4), heat flow produced by a negative temperature gradient is considered positive. This convention requires the insertion of the minus sign in Eq. (1) to assure a positive heat flow, q. The temperature difference resulting from the steady-state diffusion of heat is thus related to the thermal conductivity of the material, the cross-sectional area, and the path length, L, according to

$$(T_1 - T_2)_{\mathrm{cd}} = q\frac{L}{kA} \tag{2}$$

The form of Eq. (2) suggests that, by analogy to Ohm's Law governing electric current flow through a resistance, it is possible to define a thermal resistance for conduction, R_{cd}, as

$$R_{\mathrm{cd}} \equiv \frac{(T_1 - T_2)}{q} = \frac{L}{kA}$$

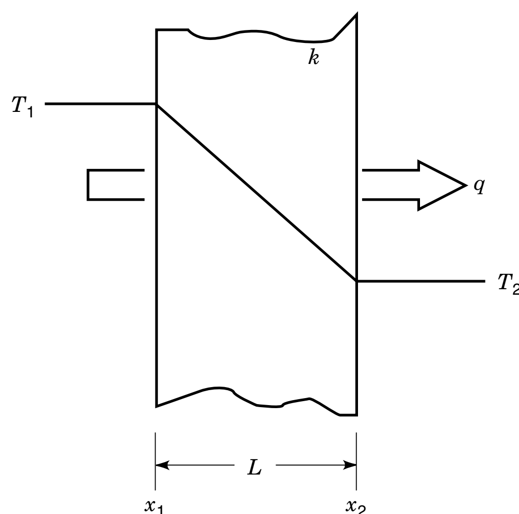

Figure 2. One-dimensional conduction through a slab (4).

One-Dimensional Conduction with Internal Heat Generation. Situations in which a solid experiences internal heat generation, such as that produced by the flow of an electric current, give rise to more complex governing equations and require greater care in obtaining the appropriate temperature differences. The axial temperature variation in a slim, internally heated, conductor subjected to a constant and uniform internal heat generation and whose edges (ends) are held at a temperature T_0, is found to equal

$$T = T_0 + q_{\mathrm{g}}\frac{L^2}{2k}\left[\left(\frac{x}{L}\right) - \left(\frac{x}{L}\right)^2\right]$$

When the volumetic heat generation rate, q_{g}, in watts per cubic meter, is uniform throughout, the peak temperature is developed at the center of the solid and is given by

$$T_{\max} = T_0 + q_{\mathrm{g}}\frac{L^2}{8k}$$

Alternatively, since q_{g} is the volumetric heat generation, $q_{\mathrm{g}} = q/LW\delta$, the center-edge temperature difference can be expressed as

$$T_{\max} - T_0 = q\frac{L^2}{8kLW\delta} = q\frac{L}{8kA} \tag{3}$$

where the cross-sectional area, A, is the product of the width, W, and the thickness, δ. An examination of Eq. (3) reveals that the thermal resistance of a conductor with a distributed heat input is only one quarter that of a structure in which all of the heat is generated at the center.

In the design of airborne electronic systems and equipment to be operated in a corrosive or damaging environment, it is often necessary to conduct the heat dissipated by the components down into the substrate or printed circuit board (PCB) and, as shown in Fig. 3, across the substrate–PCB to a cold plate or sealed heat exchanger. For a symmetrically cooled substrate–PCB with approximately uniform heat dissipation on the surface, a first-estimate of the peak temperature at the center of the board can be obtained by use of Eq. (3).

This relation can be used effectively in the determination of the temperatures experienced by conductively cooled substrates and conventional PCBs, as well as PCB's with copper lattices on the surface, metal cores, or heat-sink plates in the center. In each case, it is necessary to evaluate or obtain the effective thermal conductivity of the conducting layer. As an example, consider an alumina substrate, 0.20 m long, 0.15 m wide, and 0.005 m thick with a thermal conductivity of 20 W/mK, whose edges are cooled to 35°C by a cold-plate. Assuming that the substrate is populated by 30 components, each dissipating 1 W, the substrate center temperature will equal 85°C when calculated using Eq. (3).

Spreading Resistance. In chip packages that provide for lateral spreading of the heat generated in the chip, the increasing cross-sectional area for heat flow at successive layers be-

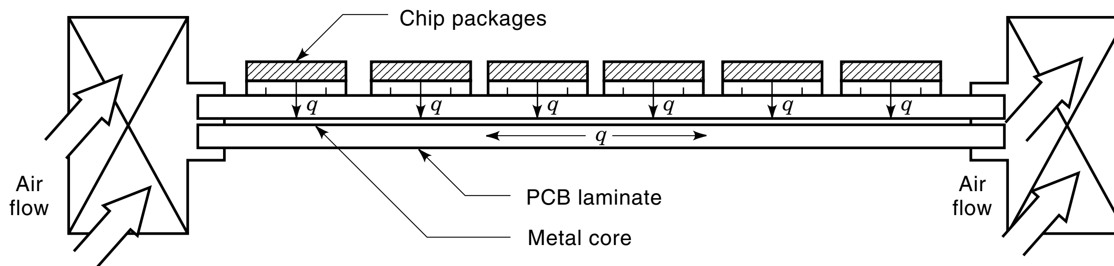

Figure 3. Edge-cooled printed circuit board populated with components (4).

low the chip reduces the internal thermal resistance. Unfortunately, however, there is an additional resistance associated with this lateral flow of heat. This, of course, must be taken into account in the determination of the overall chip package temperature difference.

For the circular and square geometries common in microelectronic applications, Negus et al. (5) provided an engineering approximation for the spreading resistance for a small heat source on a thick substrate or heat spreader (required to be three to five times thicker than the square root of the heat source area) can be expressed as

$$R_{\mathrm{sp}} = \frac{0.475 - 0.62\epsilon + 0.13\epsilon^2}{k\sqrt{A_{\mathrm{c}}}} \tag{4}$$

where ϵ is the ratio of the heat source area to the substrate area, k is the thermal conductivity of the substrate, and A_c is the area of the heat source.

For relatively thin layers on thicker substrates, such as encountered in the use of thin lead frames, or heat spreaders interposed between the chip and substrate, Eq. (4) cannot provide an acceptable prediction of R_{sp}. Instead, use can be made of the numerical results plotted in Fig. 4 to obtain the requisite value of the spreading resistance.

Interface and Contact Resistance. Heat transfer across the interface between two solids is generally accompanied by a measurable temperature difference, which can be ascribed to a contact or interface thermal resistance. For perfectly adhering solids, geometrical differences in the crystal structure (lattice mismatch) can impede the flow of phonons and electrons across the interface, but this resistance is generally negligible in engineering design. When dealing with real interfaces, the asperities present on each of the surfaces, as shown in an artist's conception in Fig. 5, limit actual contact between the two solids to a very small fraction of the apparent interface area. The flow of heat across the gap between two solids in nominal contact is, thus, seen to involve solid conduction in the areas of actual contact and fluid conduction across the open spaces. Radiation across the gap is of increasing importance for elevated surface temperatures and in a vacuum environment when convective and conductive mechanisms are suppressed.

The total contact conductance, h_{co}, is taken as the sum of the solid-to-solid conductance, h_c, and the gap conductance, h_g

$$h_{\mathrm{co}} = h_{\mathrm{c}} + h_{\mathrm{g}} \tag{5}$$

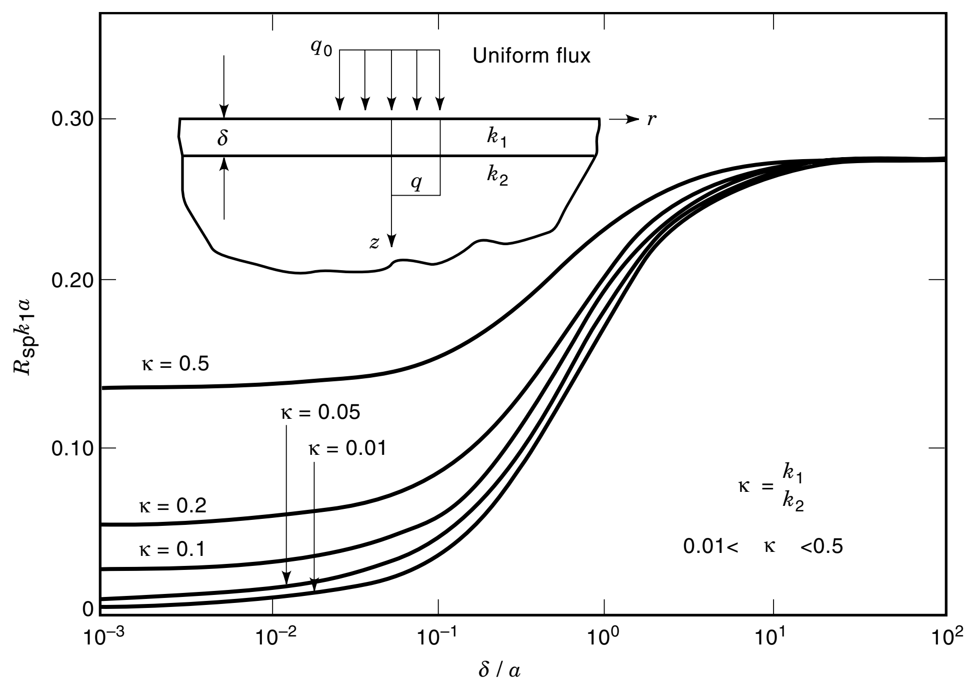

Figure 4. The thermal resistance for a circular heat source on a two-layer substrate (6).

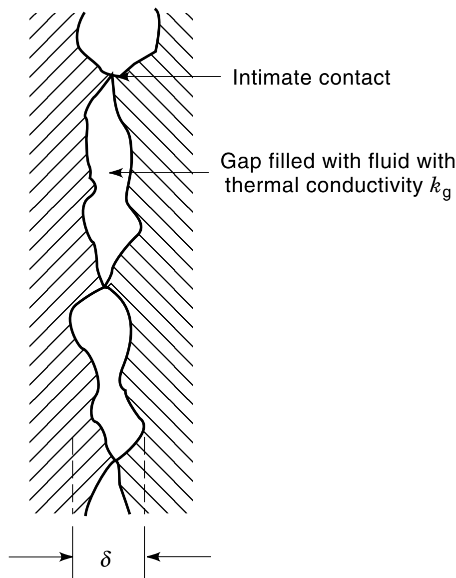

Figure 5. Physical contact between two nonideal surfaces (4).

and the contact resistance based on the apparent contact area, A_a may be defined as

$$R_{co} \equiv \frac{1}{h_{co}A_a} \tag{6}$$

In Eq. (5), h_c is given by Yovanovich and Antonetti (6) as

$$h_c = 1.25k_s \left(\frac{m}{\sigma}\right)\left(\frac{P}{H}\right)^{0.95} \tag{7}$$

where P is the contact pressure and H is the microhardness of the softer material (both in Pa), k_s is the harmonic mean thermal conductivity for the two solids with thermal conductivities, k_1 and k_2,

$$k_s = \frac{2k_1k_2}{k_1 + k_2}$$

σ is the effective rms surface roughness developed from the surface roughnesses of the two materials, σ_1 and σ_2,

$$\sigma = \sqrt{\sigma_1^2 + \sigma_2^2}$$

and m is the effective absolute surface slope composed of the individual slopes of the two materials, m_1 and m_2,

$$m = \sqrt{m_1^2 + m_2^2}$$

In the absence of detailed information, the σ/m ratio can be taken equal to 5 to 9 μm for relatively smooth surfaces (7).

For normal interstitial gases near atmospheric pressure, h_g in Eq. (5) is given by

$$h_g = \frac{k_g}{Y} \tag{8}$$

where k_g is the thermal conductivity of the gap fluid and Y is the distance between the mean planes given by

$$Y = 1.185\left[-\ln\left(3.132\frac{P}{H}\right)\right]^{0.547}\sigma$$

Equations (7) and (8) can be added and, in accordance with Eq. (6), the total contact resistance becomes

$$R_{co} \equiv \left\{\left[1.25k_s\left(\frac{m}{\sigma}\right)\left(\frac{P}{H}\right)^{0.95} + \frac{k_g}{Y}\right]A_a\right\}^{-1} \tag{9}$$

Transient Heating or Cooling. An internally heated solid, of relatively high thermal conductivity, which is experiencing no external cooling, will undergo a constant rise in temperature according to

$$\frac{dT}{dx} = \frac{q}{mc} \tag{10}$$

where q is the rate of internal heat generation, m is the mass of the solid, and c is the specific heat of the solid. Equation (10) assumes that all of the mass can be represented by a single temperature and this relation is frequently termed the *lumped capacity* solution for transient heating.

Expanding on the analogy between thermal and electric resistances, the product of mass and specific heat can be viewed as analagous to electric capacitance and thus to consitute the thermal capacitance.

When the same solid is externally cooled, the temperature rises asymptotically toward the steady-state temperature, which is itself determined by the external resistance to the heat flow, R_{ex}. Consequently, the time variation of the temperature of the solid is expressible as

$$T(t) = T(t-0) + qR_{ex}[1 - e^{-t/mcR_{ex}}]$$

The lumped capacitance model is accurate when the ratio of the internal conduction resistance of a solid to the external thermal resistance is small. This ratio is represented by the Biot number (Bi), and the criterion for applicability of the lumped capacitance model is typically given as

$$\text{Bi} = \frac{hL_c}{k} < 0.1$$

where the characteristic length, L_c, is typically defined as the ratio of the solid's volume to its surface area. More generally, L_c should be taken as the distance over which the solid experiences its maximum temperature difference (8).

Convective Heat Transfer

The Heat-Transfer Coefficient. Convective thermal transport from a surface to a fluid in motion can be related to the heat transfer coefficient, h, the surface-to-fluid temperature difference, and the wetted surface area, S, in the form

$$q = hS(T_s - T_{fl}) \tag{11}$$

The differences among convection to a rapidly moving fluid, a slowly flowing or stagnant fluid, and variations in the convec-

tive heat transfer rate for various fluids are reflected in the values of h. For a particular geometry and flow regime, h may be found from available empirical correlations and/or theoretical relations. Use of Eq. (11) makes it possible to define the convective thermal resistance, as

$$R_{cv} \equiv \frac{1}{hS}$$

Dimensionless Parameters. Common dimensionless quantities that are used in the correlation of heat transfer data are the *Nusselt number,* Nu, which relates the convective heat transfer coefficient to the conduction in the fluid where the subscript, fl, pertains to a fluid property,

$$\mathrm{Nu} \equiv \frac{h}{k_{fl}/L} = \frac{hL}{k_{fl}}$$

the *Prandtl number,* Pr, which is a fluid property parameter relating the diffusion of momentum to the conduction of heat,

$$\mathrm{Pr} \equiv \frac{c_p \mu}{k_{fl}}$$

the *Grashof number,* Gr, which accounts for the bouyancy effect produced by the volumetric expansion of the fluid,

$$\mathrm{Gr} \equiv \frac{\rho^2 \beta g L^3 \Delta T}{\mu^2}$$

and the *Reynolds number,* Re, which relates the momentum in the flow to the viscous dissipation,

$$\mathrm{Re} \equiv \frac{\rho V L}{\mu}$$

Natural Convection. Despite increasing performance demands and advances in thermal management technology, direct air-cooling of electronic equipments continues to command substantial attention. Natural convection is the quietest, least expensive, and most reliable implementation of direct fluid cooling. In more demanding systems, natural convection cooling with air is often investigated as a baseline design to justify the application of more sophisticated techniques.

In natural convection, fluid motion is induced by density differences resulting from temperature gradients in the fluid. The heat transfer coefficient for this regime can be related to the buoyancy and the thermal properties of the fluid through the *Rayleigh number,* Ra, which is the product of the Grashof and Prandtl numbers,

$$\mathrm{Ra} = \frac{\rho^2 \beta g c_p}{\mu k_{fl}} L^3 \Delta T$$

where the fluid properties, ρ, β, c_p, μ, and k, are evaluated at the fluid bulk temperature, and ΔT is the temperature difference between the surface and the fluid.

Empirical correlations for the natural convection heat transfer coefficient generally take the form

$$\mathrm{Nu} \equiv C(\mathrm{Ra})^n$$

where n is found to be approximately 0.25 for $10^3 < \mathrm{Ra} < 10^9$, representing laminar flow, 0.33 for $10^9 < \mathrm{Ra} < 10^{12}$, the region associated with the transition to turbulent flow, and 0.4 for $\mathrm{Ra} > 10^{12}$, when strong turbulent flow prevails. The precise value of the correlating coefficient, C, depends on fluid, the geometry of the surface, and the Rayleigh number range. Nevertheless, for common plate, cylinder, and sphere configurations, it has been found to vary in the relatively narrow range of 0.45 to 0.65 for laminar flow and 0.11 to 0.15 for turbulent flow past the heated surface (3).

Vertical Channels. Vertical channels formed by parallel PCBs or longitudinal fins are a frequently encountered configuration in natural convection cooling of electronic equipment. The historical work of Elenbaas (9), a milestone of experimental results and empirical correlations, was the first to document a detailed study of natural convection in smooth, isothermal parallel plate channels. In subsequent years, this work was confirmed and expanded both experimentally and numerically by a number of researchers, including Bodoia (10), Sobel et al. (11), Aung (12), Aung et al. (13), Miyatake and Fujii (14), and Miyatake et al. (15).

These studies have revealed that the value of the Nusselt number lies between two extremes associated with the separation between the plates or the channel width. For wide spacing, the plates appear to have little influence upon one another and the Nusselt number in this case achieves its *isolated plate limit*. On the other hand, for closely spaced plates or for relatively long channels, the fluid attains its *fully developed* value and the Nusselt number reaches its *fully developed limit*. Intermediate values of the Nusselt number can be obtained from a composite expression for smoothly varying processes and have been verified by the detailed experimental and numerical studies of Bar-Cohen and Rohsenow (16).

For an isothermal channel, at the fully-developed limit, the Nusselt number takes the form

$$\mathrm{Nu} = \frac{\mathrm{El}}{C_1 \mathscr{A}} \tag{12}$$

where El is the Elenbaas number, defined as

$$\mathrm{El} \equiv \frac{c_p \rho^2 g \beta (T_w - T_{amb}) H^4}{\mu k l}$$

where H is the channel spacing, l is the channel length, and $(T_w - T_{amb})$ is the temperature difference between the channel wall and the ambient, or channel, inlet. For an asymmetric channel, or one in which one wall is heated and the other is insulated, the appropriate value of C_1 is 12, whereas for a symmetrically heated channel, $C_1 = 24$.

For an isoflux channel, at the fully developed limit, the Nusselt number has been shown to take the form

$$\mathrm{Nu} = \sqrt{\frac{\mathrm{El}'}{C_1}} \tag{13}$$

where the modified Elenbaas number, El′, is defined as

$$\mathrm{El}' \equiv \frac{c_p \rho^2 g \beta q'' H^5}{\mu k^2 l}$$

where q'' is the heat flux leaving the channel wall(s). When this Nusselt number is based on the maximum wall temperature ($x = l$), the appropriate values of C_1 are 24 and 48 for the asymmetric and symmetric cases, respectively. When based on the midheight ($x = l/2$) wall temperature, the asymmetric and symmetric C_1 values are 6 and 12, respectively.

In the limit where the channel spacing is very large, the opposing channel walls influence each other neither hydrodynamically nor thermally. This situation may be accurately modeled as heat transfer from an isolated vertical surface in an infinite medium. Natural convection from an isothermal plate can be expressed as

$$\mathrm{Nu} = C_2 \mathrm{El}^{1/4} \tag{14}$$

where McAdams (17) suggests a C_2 value of 0.59. Natural convection from an isoflux plate is typically expressed as

$$\mathrm{Nu} = C_2 \mathrm{El}^{1/5} \tag{15}$$

with a leading coefficient of 0.631 when the Nusselt number is based on the maximum ($x = l$) wall temperature and 0.73 when the Nusselt number is based on the midheight ($x = l/2$) wall temperature.

Composite Equations. When a function is expected to vary smoothly between two limiting expressions, which are themselves well defined, and when intermediate values are difficult to obtain, an approximate composite relation can be obtained by appropriately summing the two limiting expressions. Using the Churchill and Usagi (18) method, Bar-Cohen and Rohsenow (19) developed composite Nusselt number relations for natural convection in parallel plate channels of the form

$$\mathrm{Nu} = [(\mathrm{Nu}_{\mathrm{fd}})^{-n} + (\mathrm{Nu}_{\mathrm{ip}})^{-n}]^{-1/n} \tag{16}$$

where $\mathrm{Nu}_{\mathrm{fd}}$ and $\mathrm{Nu}_{\mathrm{ip}}$ are Nusselt numbers for the fully developed and isolated plate limits, respectively. The correlating exponent n was given a value of 2 to offer good agreement with Elenbaas's (9) experimental results.

For an isothermal channel, combining Eqs. (12) and (14) yields a composite relation of the form

$$\mathrm{Nu}_{\mathrm{comp}} = \left[\frac{C_3}{\mathrm{El}^2} + \frac{C_4}{\sqrt{\mathrm{El}}}\right]^{-1/2} \tag{17}$$

while for an isoflux channel, Eqs. (13) and (15) yield a result of the form

$$\mathrm{Nu}_{\mathrm{comp}} = \left[\frac{C_3}{\mathrm{El}'} + \frac{C_4}{\mathrm{El}'^{2/5}}\right]^{-1/2} \tag{18}$$

Values of the coefficients C_3 and C_4 appropriate to various cases of interest appear in Table 3.

In electronic cooling applications where volumetric concerns are not an issue, it is desirable to space the PCBs far enough apart that the isolated plate Nusselt number prevails along the surface. In lieu of choosing an infinite plate spacing, the composite Nusselt number may be set equal to 99%, or some other high fraction, of its associated isolated plate value. The composite Nusselt number relation may then be solved for the appropriate channel spacing.

For an isothermal channel, the channel spacing which maximizes the rate of heat transfer from individual PCBs takes the form

$$H_{\max} = \frac{C_5}{P^{1/4}} \tag{19}$$

where

$$P = \frac{c_p \rho^2 g \beta (T_w - T_{amb})}{\mu k l} = \frac{\mathrm{El}}{H^4}$$

while for an isoflux channel, the channel spacing which minimizes the PCB temperature for a given heat flux takes the form

$$H_{\max} = \frac{C_5}{R^{1/5}} \tag{20}$$

where

$$R = \frac{c_p \rho^2 g \beta q''}{\mu k^2 l} = \frac{\mathrm{El}'}{H^5}$$

Values of the coefficient C_5 appropriate to various cases of interest appear in Table 3.

Optimum Spacing. In addition to being used to predict heat-transfer coefficients, the composite relations presented may be used in optimizing the spacing between PCBs. For isothermal arrays, the optimum spacing maximizes the total heat transfer from a given base area or the volume assigned to an array of PCBs. In the case of isoflux parallel plate arrays, the total array heat transfer for a given base area may be maximized by increasing the number of plates indefinitely. Thus, it is more practical to define the optimum channel spacing for an array of isoflux plates as that spacing which will yield the maximum volumetric heat dissipation rate per unit temperature difference. Despite this distinction, the optimum spacing is found in the same manner.

The total heat transfer rate from an array of vertical, single-sided plates can be written as

$$\frac{Q_{\mathrm{T}}}{lsWk\Delta T} = \left(\frac{\mathrm{Nu}}{H(H+d)}\right) \tag{21}$$

where the number of plates, $m = W/(H + d)$, d is the plate thickness, W is the width of the entire array, and s is the depth of the channel. The optimum spacing may be found by substituting the appropriate composite Nusselt number equa-

Table 3. Appropriate Values of the C_i Coefficients Appearing in Eqs. (12 through 25)

Case	C_1	C_2	C_3	C_4	C_5	C_6	C_7
Isothermal							
In general	X	Y	X^2	Y^{-2}	$\left(\frac{X^2Y^2(0.99)^2}{1-(0.99)^2}\right)^{1/6}$	$\frac{1}{(XY)^2}$	$(\sqrt{2}XY)^{1/3}$
Symmetric heating	24	0.59	576	2.87	4.63	0.0050	2.72
Asymmetric heating	12	0.59	144	2.87	3.68	0.0199	2.16
Isoflux							
In general	X	Y	X	Y^{-2}	$\left(\frac{XY^2(0.99)^2}{1-(0.99)^2}\right)^{1/3}$	$\frac{2}{(XY)^2}$	$\left(\frac{XY^2}{2}\right)^{1/3}$
Symmetric heating							
maximum temp.	48	0.63	48	2.52	9.79	0.105	2.12
midheight temp.	12	0.73	12	1.88	6.80	0.313	1.47
Asymmetric heating							
maximum temp.	24	0.63	24	2.52	7.77	0.210	1.68
midheight temp.	6	0.73	6	1.88	5.40	0.626	1.17

tion into Eq. (21), taking the derivative of the resulting expression with respect to H, and setting the result equal to zero. Use of the isothermal composite Nusselt number of Eq. (21) yields a relation of the form

$$(2b + 3d - C_6 P^{3/2} b^7)_{\text{opt}} = 0 \tag{22}$$

or

$$b_{\text{opt}} = \frac{C_7}{P^{1/4}} \tag{23}$$

when d, the PCB thickness, is negligible. Use of an isoflux composite Nusselt number yields

$$(b + 3d - C_6 R^{3/5} b^4)_{\text{opt}} = 0 \tag{24}$$

or

$$b_{\text{opt}} = \frac{C_7}{R^{1/5}} \quad (d = 0) \tag{25}$$

Values of the coefficients C_6 and C_7 appropriate to various cases of interest appear in Table 3.

Limitations. These smooth-plate relations have proven useful in a wide variety of applications and have been shown to yield very good agreement with measured empirical results for heat transfer from arrays of PCBs. However, when applied to closely spaced PCBs, these equations tend to underpredict heat transfer in the channel due to the presence of between-package wall flow and the nonsmooth nature of the channel surfaces (20).

Forced Convection. For forced laminar flow in long, or very narrow, parallel-plate channels, the heat transfer coefficient attains an asymptotic value (a fully developed limit), which for symmetrically heated channel surfaces is equal approximately to

$$h = \frac{4k_{\text{fl}}}{d_{\text{e}}}$$

where d_e is the *hydraulic diameter* defined in terms of the flow area, A, and the wetted perimeter of the channel, P_w

$$d_{\text{e}} \equiv \frac{4A}{P_{\text{w}}}$$

In the inlet zones of such parallel-plate channels and along isolated plates, the heat- transfer coefficient varies with the distance from the leading edge. The low-velocity or laminar flow, average convective heat transfer coefficient for Re $< 2 \times 10^5$ is given by (3)

$$h = 0.664 \left(\frac{k}{L}\right) \text{Re}^{1/2} \text{Pr}^{1/3} \tag{26}$$

where k is the fluid thermal conductivity and L is the characteristic dimension of the surface.

A similar relation applies to flow in tubes, pipes, ducts, channels, and/or annuli with the equivalent diameter, d_e, serving as the characteristic dimension in both the Nusselt and Reynolds numbers. For laminar flow, Re ≤ 2100

$$\frac{hd_{\text{e}}}{k} = 1.86 \left[\text{RePr}\left(\frac{d_e}{L}\right)\right]^{1/3} \left(\frac{\mu}{\mu_{\text{w}}}\right)$$

which is attributed to Sieder and Tate (21) and where μ_w is the viscosity of the convective medium at the wall temperature. Observe that this relationship shows that the heat transfer coefficient attains its maximum value for short channels and decreases as L increases.

In higher velocity turbulent flow, the dependence of the convective heat-transfer coefficient on the Reynolds number increases and, in the range Re $\geq 3 \times 10^5$, is typically given by (3)

$$h = 0.036 \left(\frac{k}{L}\right) (\text{Re})^{0.80} (\text{Pr})^{1/3} \tag{27}$$

In pipes, tubes, channels, ducts, and/or annuli, turbulent flow occurs at an equivalent diameter based Reynolds number of 10,000 with the flow regime bracketed by

$$2100 \leq \mathrm{Re} \leq 10,000$$

usually referred to as the transition region. Hausen (22) has provided the correlation

$$\frac{hd_e}{k} = 0.116[\mathrm{Re} - 125](\mathrm{Pr})^{1/3}\left(1 + \frac{d_e}{L}\right)^{2/3}\left(\frac{\mu}{\mu_w}\right)$$

and Sieder and Tate (21) give for turbulent flow

$$\frac{hd_e}{k} = 0.23(\mathrm{Re})^{0.80}(\mathrm{Pr})^{1/3}\left(\frac{\mu}{\mu_w}\right)$$

Additional correlations for the coefficient of heat transfer in forced convection for various configurations may be found in the heat transfer textbooks (8,23–25).

Phase-Change Heat Transfer. When heat exchange is accompanied by evaporation of a liquid or condensation of a vapor, the resulting flow of vapor toward or away from the heat-transfer surface and the high rates of thermal transport associated with the latent heat of the fluid can provide significantly high heat transfer rates than single phase heat transfer alone.

Boiling. Boiling heat transfer displays a complex dependence on the temperature difference between the heated surface and the saturation temperature (boiling point) of the liquid. In nucleate boiling, the primary region of interest, the ebullient heat transfer rate is typically expressed in the form of the Rohsenow (26) equation

$$q = \mu_f h_{fg}\sqrt{\frac{g(\rho_f - \rho_g)}{\sigma}}\left[\frac{c_{pf}}{C_{sf}Pr_f^{1.7}h_{fg}}\right]^{1/r}(T_s - T_{sat})^{1/r} \quad (28)$$

where $1/r$ is typically correlated with a value of three, and C_{sf} is a function of characteristics of the surface–fluid combination. Rohsenow recommended that the fluid properties in Eq. (28) be evaluated at the liquid saturation temperature.

For pool boiling of the dielectric liquid FC-72 (T_{sat} = 56°C at 101.3 kPa) on a plastic-pin-grid-array (PPGA) chip package, Watwe (27) obtained values of 7.47 for $1/r$ and 0.0075 for C_{sf}. At a surface heat flux of 10 W/cm^2, the wall superheat at 101.3 kPa is nearly 30°C, corresponding to a average surface temperature of approximately 86°C.

The departure from nucleate boiling, or critical heat flux (CHF), places an upper limit on the use of the highly efficient boiling heat transfer mechanism. CHF can be significantly influenced by system parameters such as pressure, subcooling, heater thickness and properties, and dissolved gas content. Watwe et al. (28) presented the following equation to predict the pool boiling critical heat flux of dielectric coolants, on a horizontal surface and under a variety of parametric conditions.

$$\mathrm{CHF} = \left\{\frac{\pi}{24}h_{fg}\sqrt{\rho_g}[\sigma_f g(\rho_f - \rho_g)]^{1/4}\right\}\left(\frac{\delta\sqrt{\rho_h c_{ph} k_h}}{\delta\sqrt{\rho_h c_{ph} k_h} + 0.1}\right)$$
$$\{1 + [0.3014 - 0.01507L'(P)]\}$$
$$\left\{1 + 0.03\left[\left(\frac{\rho|f}{\rho|g}\right)^{0.75}\frac{c_{pf}}{h_{fg}}\right]\Delta T_{sub}\right\} \quad (29)$$

The first term on the right-hand side of Eq. (29) is the classical Kutateladze-Zuber prediction, which is in the upper limit on the saturation value of CHF on very large heaters. The second term represents the effects of heater thickness and thermal properties on the critical heat flux. The third term in Eq. (29) accounts for the influence of the length scale. The last term is an equation representing the best-fit line through the experimental data of Watwe et al. (28) and represents the influence of subcooling on CHF. The pressure effect on CHF is embodied in the Kutateladze-Zuber and the subcooling model predictions, which make up Eq. (29), via the thermophysical properties. Thus, it can be used to estimate the combined influences of various system and heater parameters on CHF. The critical heat flux, under saturation conditions at atmospheric pressure, for a typical dielectric coolant like FC-72 is approximately 17 W/cm^2.

Condensation. Closed systems involving an evaporative process must also include some capability for vapor condensation. Gerstmann and Griffith (29) correlated film condensation on a downward-facing flat plate as

$$\mathrm{Nu} = 0.81\mathrm{Ra}^{0.193} \quad 10^{10} > \mathrm{Ra} > 10^8$$
$$\mathrm{Nu} = 0.69\mathrm{Ra}^{0.20} \quad 10^8 > \mathrm{Ra} > 10^6$$

where

$$\mathrm{Nu} \equiv \frac{h}{k}\left(\frac{\sigma}{g(\rho_f - \rho_g)}\right)^{1/2}$$
$$\mathrm{Ra} \equiv \frac{g\rho_f(\rho_f - \rho_g)h_{fg}}{k\mu\Delta T}\left(\frac{\sigma}{g(\rho_f - \rho_g)}\right)^{3/2}$$

The Nusselt number for laminar film condensation on vertical surfaces was correlated by Nusselt (30) and later modified by Sadasivan and Lienhard (31) as

$$\mathrm{Nu} = \frac{hL}{k_f} = 0.943\left[\frac{g\Delta\rho_{fg}L^3h'_{fg}}{k_f v_f(T_{sat} - T_c)}\right]^{1/4}$$

where

$$h'_{fg} = h_{fg}(1 + C_c Ja)$$
$$C_c = 0.683 - \frac{0.228}{\mathrm{Pr}_l}$$
$$Ja = \frac{c_{pf}(T_{sat} - T_c)}{h_{fg}}$$

Flow Resistance. The transfer of heat to a flowing gas or liquid that is not undergoing a phase change, results in an increase in the coolant temperature from an inlet tempera-

ture of T_{in} to an outlet temperature of T_{out}, according to

$$T_{out} - T_{in} = \frac{q}{\dot{m}c_p}$$

To facilitate the use of a resistance network representation for the analysis of convectively cooled packaging configurations, it is possible to use the above equation to define an effective flow resistance, R_{fl}, as

$$R_{fl} \equiv \frac{1}{\dot{m}c_p} \tag{30}$$

where $\dot{m}$, the mass flow rate, is given in kilograms per second.

In multicomponent systems, determination of individual component temperatures requires knowledge of the fluid temperature adjacent to the component. The rise in fluid temperature relative to the inlet value can be expressed in a flow thermal resistance, as done in Eq. (30). When the coolant flow path traverses many individual components, care must be taken to use R_{fl} with the total heat absorbed by the coolant along its path, rather than the heat dissipated by an individual component. For system-level calculations aimed at determining the average component temperature, it is common to base the flow resistance on the average rise in fluid temperature, that is, one-half the value indicated by Eq. (30).

Radiative Heat Transfer

Unlike conduction and convection, radiative heat transfer between two surfaces or between a surface and its surroundings is not linearly dependent on the temperature difference and is expressed instead as

$$q = \sigma S \mathscr{F}(T_1^4 - T_2^4)$$

where $\mathscr{F}$ includes the effects of surface properties and geometry and σ is the Stefan–Boltzmann constant, $\sigma = 5.67 \times 10^{-8}$ W/m$^2 \cdot$K^4. For modest temperature differences, this equation can be linearized to the form

$$q = h_r S(T_1 - T_2) \tag{31}$$

where h_r is the effective radiation heat transfer coefficient

$$h_r = \sigma \mathscr{F}(T_1^2 + T_2^2)(T_1 + T_2)$$

and, for small $\Delta T = T_1 - T_2$, h_r is approximately equal to

$$h_r = 4\sigma \mathscr{F}(T_1 T_2)^{3/2}$$

It is of interest to note that for temperature differences of the order of 10 K with absolute temperatures around room temperature, the radiative heat transfer coefficient, h_r, for an ideal (or black) surface in an absorbing environment, is approximately equal to the heat transfer coefficient in natural convection of air.

Noting the form of Eq. (31), the radiation thermal resistance, analogous to the convective resistance, is seen to equal

$$R_r \equiv \frac{1}{h_r S}$$

THERMAL RESISTANCE NETWORKS

The expression of the governing heat transfer relations in the form of thermal resistances greatly simplifies the first-order thermal analysis of electronic systems. Following the established rules for resistance networks, thermal resistances that occur sequentially along a thermal path can be simply summed to establish the overall thermal resistance for that path. In similar fashion, the reciprocal of the effective overall resistance of several parallel heat transfer paths can be found by summing the reciprocals of the individual resistances. In refining the thermal design of an electronic system, prime attention should be devoted to reducing the largest resistances along a specified thermal path and/or providing parallel paths for heat removal from a critical area.

While the thermal resistances associated with various paths and thermal transport mechanisms constitute the building blocks in performing a detailed thermal analysis, they have also found widespread application as figures-of-merit in evaluating and comparing the thermal efficacy of various packaging techniques and thermal management strategies.

Chip Module Thermal Resistances

Definition. The thermal performance of alternative chip and packaging techniques is commonly compared on the basis of the overall (junction-to-coolant) thermal resistance, R_T. This packaging figure-of-merit is generally defined in a purely empirical fashion,

$$R_T \equiv \frac{T_j - T_{fl}}{q_c}$$

where T_j and T_{fl} are the junction and coolant (fluid) temperatures, respectively, and q_c is the chip heat dissipation.

Unfortunately, however, most measurement techniques are incapable of detecting the actual junction temperature, that is, the temperature of the small volume at the interface of p-type and n-type semiconductors. Hence, this term generally refers to the average temperature or a representative temperature on the chip.

Examination of various packaging techniques reveals that the junction-to-coolant thermal resistance is, in fact, composed of an internal, largely conductive, resistance and an external, primarily convective, resistance. As shown in Fig. 6, the internal resistance, R_{jc}, is encountered in the flow of dissipated heat from the active chip surface through the materials used to support and bond the chip and onto the case of the integrated circuit package. The flow of heat from the case directly to the coolant, or indirectly through a fin structure and then to the coolant, must overcome the external resistance, R_{ex}.

Internal Thermal Resistance. As previously discussed, conductive thermal transport is governed by the Fourier equation, which can be used to define a conduction thermal resistance, as in Eq. (3). In flowing from the chip to the package surface or case, the heat encounters a series of resistances associated with individual layers of materials such as silicon, solder, copper, alumina, and epoxy, as well as the contact resistances that occur at the interfaces between pairs of materials. Although the actual heat flow paths within a chip package are rather complex and may shift to accommodate varying external cooling situations, it is possible to obtain a first-order estimate of the internal resistance by assuming

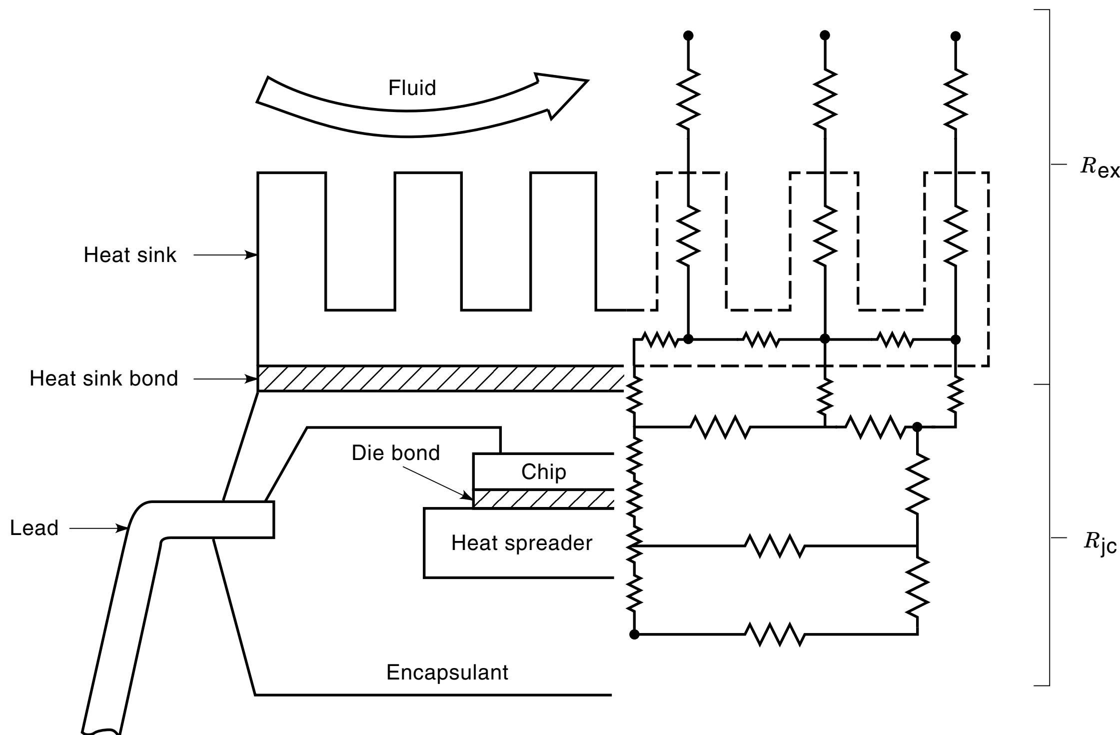

Figure 6. Primary thermal resistances in a single-chip package (4).

that power is dissipated uniformly across the chip surface and that heat flow is largely one-dimensional. To the accuracy of these assumptions, Eq. (32)

$$R_{jc} = \frac{T_j - T_c}{q_c} = \sum \frac{x}{kA} \tag{32}$$

can be used to determine the internal chip module resistance, where the summed terms represent the conduction thermal resistances posed by the individual layers, each with thickness x. As the thickness of each layer decreases and/or the thermal conductivity and cross-sectional area increase, the resistance of the individual layers decreases. Values of R_{cd} for packaging materials with typical dimensions can be found using Eq. (32) or Fig. 7, to range from 2 K/W for a 1000 mm^2 by 1 mm thick layer of epoxy encapsulant to 0.0006 K/W for a 100 mm^2 by 25 μm (1 mil) thick layer of copper. Similarly, the values of conduction resistance for typical soft bonding materials are found to lie in the range of approximately 0.1 K/W for solders and 1 K/W–3 K/W for epoxies and thermal pastes for typical x/A ratios of 0.25 to 1.0.

Comparison of theoretical and experimental values of R_{jc} reveals that the resistances associated with compliant, low thermal conductivity bonding materials, and the spreading resistances, as well as the contact resistances at the lightly loaded interfaces within the package, often dominate the internal thermal resistance of the chip package. Thus, it is not only necessary to correctly determine the bond resistance but to also add the values of R_{sp}, obtained from Eq. (4) and/or Fig. 4, and R_{co} from Eqs. (6) or (9) to the junction-to-case resistance calculated from Eq. (32). Unfortunately, the absence of detailed information on the voidage in the die-bonding and heat-sink attach layers and the present inability to determine, with precision, the contact pressure at the relevant interfaces, conspire to limit the accuracy of this calculation.

External Resistance. An application of Eq. (26) or Eq. (27) to the transfer of heat from the case of a chip module to the coolant, shows that the external resistance, $R_{ex} = 1/hS$, is inversely proportional to the wetted surface area and to the coolant velocity to the 0.5 to 0.8 power and directly proportional to the length scale in the flow direction to the 0.5 to 0.2 power. It may, thus, be observed that the external resistance can be strongly influenced by the fluid velocity and package dimensions and that these factors must be addressed in any meaningful evaluation of the external thermal resistances offered by various packaging technologies.

Values of the external resistance, for a variety of coolants and heat transfer mechanisms, are shown in Fig. 8 for a typical component wetted area of 10 cm^2 and a velocity range of 2 m/s to 8 m/s. They are seen to vary from a nominal 100 K/W for natural convection in air, to 33 K/W for forced convection in air, to 1 K/W in fluorocarbon liquid forced convection, and to less than 0.5 K/W for boiling in fluorocarbon liquids. Clearly, larger chip packages will experience proportionately lower external resistances than the displayed values. Moreover, conduction of heat through the leads and package base into the PCB or substrate will serve to further reduce the effective thermal resistance.

In the event that the direct cooling of the package surface is inadequate to maintain the desired chip temperature, it is common to attach finned heat sinks, or compact heat exchangers, to the chip package. These heat sinks can considerably increase the wetted surface area but may act to reduce the convective heat transfer coefficient by obstructing the flow channel. Similarly, the attachment of a heat sink to the pack-

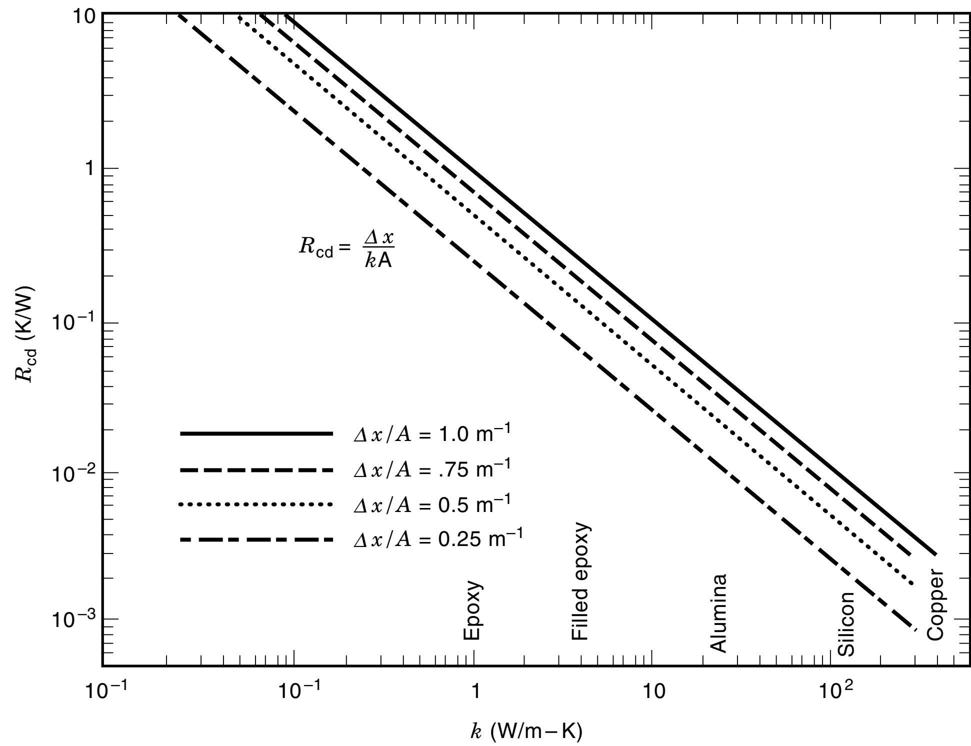

Figure 7. Conductive thermal resistances for packaging materials (4).

age can be expected to introduce additional conductive resistances in the adhesive used to bond the heat sink and in the body of the heat sink. Typical air-cooled heat sinks can reduce the external resistance to approximately 10 K/W to 15 K/W in natural convection and to as low as 3 K/W to 5 K/W for moderate forced convection velocities.

When a heat sink or compact heat exchanger is attached to the package, the external resistance accounting for the bond-layer conduction and the total resistance of the heat sink, R_{sk}, can be expressed as

$$R_{ex} = \frac{T_c - T_{fl}}{q_c} = \sum \left(\frac{x}{kA}\right)_b + R_{sk} \tag{33}$$

where R_{sk}

$$R_{sk} = \left[\frac{1}{nhS_f\eta} + \frac{1}{h_b S_b}\right]^{-1}$$

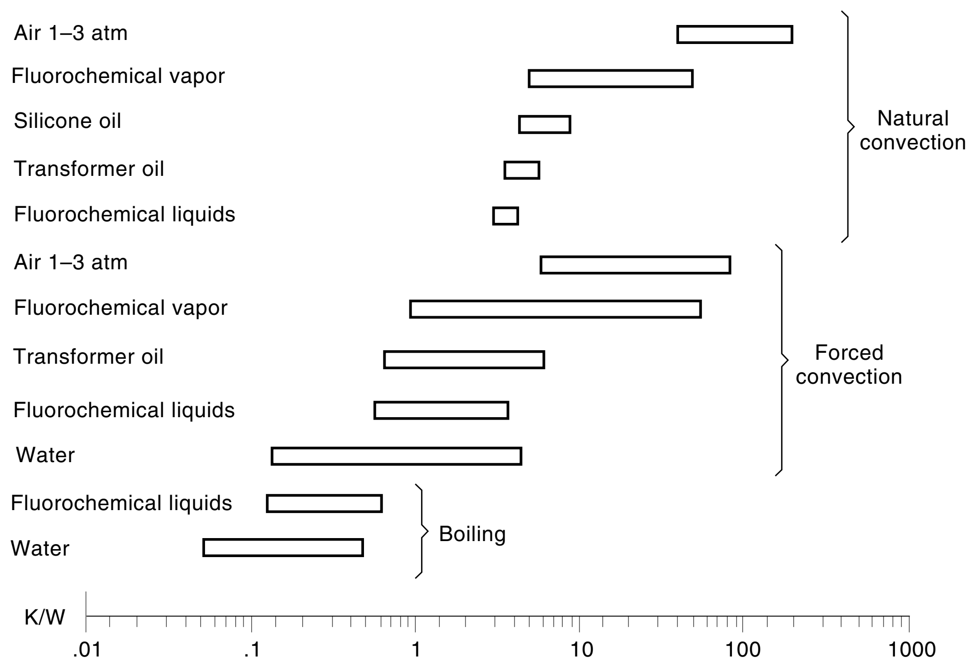

Figure 8. Typical external (convective) thermal resistances for various coolants and cooling modes (4).

is the parallel combination of the resistance of the n fins

$$R_f = \frac{1}{nhS_f\eta}$$

and the *bare* or base surface not occupied by the fins

$$R_b = \frac{1}{h_b S_b}$$

Here, the base surface is $S_b = S - S_f$ and the heat-transfer coefficient, h_b, is used because the heat-transfer coefficient that is applied to the base surfaces is not necessarily equal to that applied to the fins.

An alternative expression for R_{sk} involves an *overall surface efficiency,* η_0, defined by

$$\eta_0 = 1 - \frac{nS_f}{S}(1-\eta)$$

where S is the total surface composed of the base surface and the finned surfaces of n fins

$$S = S_b + nS_f$$

In this case, it is presumed that $h_b = h$ so that

$$R_{sk} = \frac{1}{h\eta_0 S}$$

In an optimally designed fin structure, η can be expected to fall in the range of 0.50 to 0.70 (4). Relatively thick fins in a low velocity flow of gas are likely to yield fin efficiencies approaching unity. This same unity value would be appropriate, as well, for an unfinned surface and, thus, serve to generalize the use of Eq. (33) to all package configurations.

Total Resistance of Single Chip Packages. To the accuracy of the assumptions employed in the preceding development, the overall single chip package resistance, relating the chip temperature to the inlet temperature of the coolant, can be found by summing the internal, external and flow resistances to yield

$$\begin{aligned} R_T &= R_{jc} + R_{ex} + R_{fl} \\ &= \sum \frac{x}{kA} + R_{int} + R_{sp}\frac{1}{\eta h A} + \left(\frac{Q}{q}\right)\left(\frac{1}{2\rho Q c_p}\right) \end{aligned} \quad (34)$$

In evaluating the thermal resistance by this relationship, care must be taken to determine the effective cross-sectional area for heat flow at each layer in the module and to consider possible voidage in any solder and adhesive layers.

As previously noted in the development of the relationships for the external and internal resistances, Eq. (34) shows R_T to be a strong function of the convective heat transfer coefficient, the flowing heat capacity of the coolant, and their geometric parameters (thickness and cross-sectional area of each layer). Thus, the introduction of a superior coolant, use of thermal enhancement techniques that increase the local heat-transfer coefficient, or selection of a heat-transfer mode with inherently high heat-transfer coefficients (boiling, for example) will all be reflected in appropriately lower external and total thermal resistances. Similarly, improvements in the thermal conductivity and reduction in the thickness of the relatively low conductivity bonding materials (such as soft solder, epoxy, or silicone) would act to reduce the internal and total thermal resistances.

Applications of R_{jc}. The commonly used junction-to-case thermal resistance, relying on just a single case temperature, can be used with confidence only in the relatively unlikely circumstance that the package case is isothermal. In a more typical packaging configuration, when substantial temperature variations are encountered among and along the external surfaces of the package, Andrews (32), Furkay (33), and Wilson (34), among others, showed that the use of the reported R_{jc} can lead to grossly erroneous chip temperature predictions. This is especially of concern in the analysis and design of plastic chip packages, due to the inherently high thermal resistance of the plastic encapsulant and the package anisotropies introduced by the large differences in the conductivity and the resulting conductance between the lead frame and/or heat spreader and the plastic encapsulant. Although the use of R_{ja} is best suited to the determination of the actual chip temperature, not only does it contain the drawbacks of R_{jc}, but the variability of the convective (external) component in R_{ja} makes this an inappropriate parameter for the thermal characterization of the chip package itself.

Despite these limitations, the persistent demand for chip temperature prediction and control has sustained the use of the R_{ja} and R_{jc} metrics in the thermal characterization of chip packages. As an alternative, it is possible to model a chip package with a resistor network, in which each of the primary thermal paths is represented by a single thermal resistor, typically connecting the chip to one of the external package surfaces. This compact model approach was discussed and illustrated by Krueger and Bar-Cohen (35) and Bar-Cohen and Krueger (36) and was implemented by the French Telecom Research Centre (CNET) in creating a databank for thermal characteristics of electronic components used in the telecommunication industry (37). When calibrated with empirical data, such a resistor network model could provide a universal thermal representation of a chip package, which is nearly independent of the package attachment and cooling configuration. Using this model, the design engineer could then determine the chip temperature as a function of known temperatures and/or heat-transfer relations at each of the exposed surfaces.

Recognition of the popularity and longevity of the single-valued, junction-to-case thermal resistance leads to a recasting of the chip package thermal-network model in the form of surface-weighting factors, which could be used to obtain the appropriate average case temperature for various thermal-packaging configurations. This approach makes it possible to extend the use of the conventional R_{jc} to situations in which the exterior case is highly nonisothermal, including thermal insulation of one or more surfaces.

R_{jc} with Weighted Average Case Temperature

Since R_{jc} is strictly valid only for an isothermal package surface, a method must be found to address the individual contributions of the various surface segments according to their influence on the junction temperature. In the next subsection,

the theory and assumptions underpinning this approach and the derivation of the relevant "thermal influence coefficients" as well as evaluation of the accuracy attained will be presented. It will be shown that the use of the junction-to-case thermal resistance can be extended to nonisothermal packages by defining an appropriately weighted, average surface temperature based on numerically derived thermal influence coefficients for each package surface (or segment) of interest.

Expanded R_{jc} Methodology. It is convenient to introduce the expanded R_{jc} methodology with a thermal model of a chip package that can be approximated by a network of three thermal resistances connected in parallel from the chip to the top, sides and bottom of the package, respectively. This type of compact model is commonly referred to as a star network and, in this model, the heat flow from the chip is

$$q = q_1 + q_2 + q_3$$

or

$$q = \frac{T_j - T_1}{R_1} + \frac{T_j - T_2}{R_2} + \frac{T_j - T_3}{R_3} \tag{35}$$

This compact model of an electronic device is shown schematically in Fig. 9.

Equation (35) can be rearranged to yield the dependence of the chip (or junction) temperature on the temperature of the three surface segments as

$$T_j = \left(\frac{R_2R_3}{R_s}\right)T_1 + \left(\frac{R_3R_1}{R_s}\right)T_2 + \left(\frac{R_1R_2}{R_s}\right)T_3 + \left(\frac{R_1R_2R_3}{R_s}\right)q \tag{36}$$

where $R_s = R_1R_2 + R_1R_3 + R_2R_3$

Equation (36) may be generalized to admit n distinct elements along the package surface, or

$$T_j = \sum_{k=1}^{n} A_kT_k + A_{n+1}q \tag{37}$$

A comparison of Eqs. (36) and (37) shows that the coefficients of the specified surface temperatures, the A_k's are totally determined by the internal resistances of the chip package

$$A_1 = \frac{R_2R_3}{R_s} \quad A_2 = \frac{R_3R_1}{R_s}$$
$$A_3 = \frac{R_1R_2}{R_s} \quad A_4 = \frac{R_1R_2R_3}{R_s}$$

The temperature coefficients needed to generate a junction temperature relation of the form shown in Eq. (37) can thus be determined from previously calculated internal resistances or, in the absence of such values, by extraction from empirical data or numerical results for the junction temperature. Furthermore, inspection of Eq. (36) reveals that the sum of the coefficients of the various surface temperatures, whether expressed in terms of the directional, internal resistances, as in Eq. (36), or in terms of influence coefficients, as in Eq. (37), is identically equal to unity for all boundary conditions. Alternatively, as shown by Furkay (33), the power dissipation coefficient, $A_{n+1}q$, is, in fact, the familiar R_{jc}, the isothermal, junction-to-case thermal resistance. Consequently, Eq. (37) may be rewritten as

$$T_j = \sum_{k=1}^{n} A_kT_k + R_{jc}q \tag{38}$$

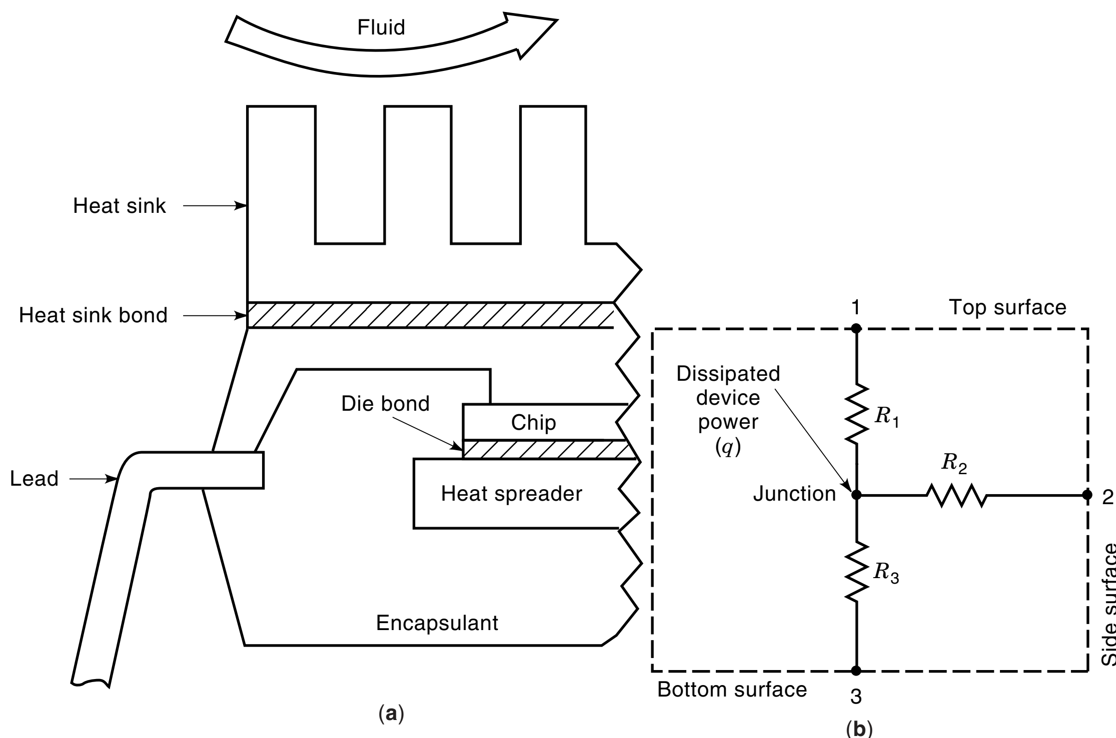

Figure 9. Geometry of a 28-lead PLCC device. (a) The compact model schematic and (b) the actual device cross section (37).

or, returning to R_{jc}

$$R_{\mathrm{jc}} = T_{\mathrm{j}} - \frac{\sum_{k=1}^{n} A_k T_k}{q} = \frac{T_{\mathrm{j}} - \overline{T}_{\mathrm{c}}}{q} \tag{39}$$

where $\overline{T}_{\mathrm{c}}$ is the average case temperature

$$\overline{T}_{\mathrm{c}} = \frac{\sum_{k=1}^{n} S_k}{S_{\mathrm{T}}} T_k \tag{40}$$

where S_k is the surface area of the kth surface and S_{T} is the surface area of the entire package.

Equation (39) can be viewed as a generalized and expanded junction-to-case thermal resistance, based on an appropriately weighted, average case temperature. As previously noted, several different approaches may be taken in determining the average temperature of a nonisothermal chip package or case. The most basic approach involves calculating a simple average of, for example, the top, bottom, and four-side surface temperature. A somewhat better value can be found by surface area averaging of these temperatures in accordance with Eq. (40).

In a package with anisotropic conduction, the simple average and area-average approaches yield an erroneous case temperature by neglecting the variation in resistance to heat flow from the chip to the surface element. This shortcoming is addressed by this approach, which provides an improved weighted-average temperature based on the importance to heat transfer of the various package surfaces. The average case temperature should be found in the prescribed manner, that is, by

$$\overline{T}_{\mathrm{c}} = \sum_{k=1}^{n} A_k T_{k,1} \tag{41}$$

With this particular value of $\overline{T}_{\mathrm{c}}$, the conventional R_{jc} obtained empirically or numerically from isothermal case results, can be used to find T_{j} for all operating conditions, subject to the assumption that each surface segment is itself isothermal. When necessary, a single surface may be divided into several zones, each of which is more nearly isothermal than the entire surface and is recognized with its own index in Eq. (41). It should be noted that the weighting imposed by this equation on the average case temperature addresses variations in the size of the surface segments, as well as variations in the internal thermal paths between the chip and each of the surface elements.

The Insulated Surface. In many applications, chip packages are cooled selectively along particular exposed surfaces. One such example is a package cooled from the top and side surfaces while the bottom surface is insulated. The thermally active surfaces may vary from application to application, and the thermal analyst needs to quantify the effect of thermally insulating one or more areas on a package of known thermal resistance. For the assumptions used in the development of the expanded R_{jc} model, insulation of surface m results in zero heat flow through resistance, R_m. This causes the temperature of surface m to equal the chip temperature. With this in mind, the junction temperature for a package with a single insulated surface given by Eq. (38) is found to equal

$$T_{\mathrm{j}} = \sum_{k \neq m} \left(\frac{A_k}{1 - A_m} \right) T_k + (R_{\mathrm{jc}}^{*}) q \tag{42}$$

The weighted average case temperature for this thermal configuration is found to equal

$$\overline{T}_{\mathrm{c}} = \sum_{k \neq m} \left(\frac{A_k}{1 - A_m} \right) T_k \tag{43}$$

and the modified junction to case resistance, R_{jc}^{*} is

$$R_{\mathrm{jc}}^{*} = \frac{R_{\mathrm{jc}}}{1 - A_m} \tag{44}$$

Implementation. To thermally characterize any electronic package by relations of the form of Eqs. (40) and (42), it is necessary to compute or measure the relevant influence coefficients or the equivalent set of internal resistances. Several difficult issues will arise in undertaking such an effort. Fundamentally, a strictly experimental approach to thermal characterization of electronic devices would suffer from measurement errors and nonlinearities. Even more esoteric, is a precise experimental definition of what temperatures must be measured on the electronic component. Precise measurement of the *p-n* junction operating temperature is usually not practical. Approximations using signal characteristics, or implanted temperature sensors are generally used for experimental purposes.

Numerical simulation of the thermal behavior of a finite element (or finite difference) model of a chip package can provide the necessary temperatures and heat flows for a variety of operating conditions. Such a model can properly represent the conduction temperature field in each of the solid elements constituting the package but unfortunately cannot yet faithfully reproduce the thermal resistances at the interfaces (the so-called contact thermal resistances) between these elements. Regrettably, these contact resistances, and especially the values along the chip surfaces where the heat fluxes are highest, can account for a significant fraction of the package resistance (38). Thus, in the near term, empirical contact resistance data must be used in generating an accurate finite element or finite difference thermal model of an integrated circuit package. For typical contact resistance values, the reader is referred to Refs. 6 and 30.

ADVANCED TOPICS

Convection Between Populated Printed Circuit Boards

The relations presented previously for natural convection in vertical channels have proved useful in a wide variety of applications and have been shown to yield very good agreement with measured empirical results for heat transfer from arrays of PCBs. However, these traditional models, employing smooth-walled channel relations and based on the free channel spacing, underestimate heat transfer for narrowly spaced PCB configurations and overestimate optimum PCB spacings. Furthermore, when an attempt is made to maximize volumetric heat dissipation in an array of PCBs, the optimum PCB

spacing is overestimated and, as a result, the maximum array dissipation is underestimated.

Teertstra et al. (39) proposed an analytical friction factor correlation for fully developed flow through an idealized array of uniformly sized and spaced cuboid blocks on one side of a parallel plate channel.

$$f_{2H} = \left[\left(\frac{96\mathscr{A}}{Re_{2H}} \right)^3 + \left(\frac{0.347\mathscr{B}}{Re_{2H}^{1/4}} \right)^3 \right]^{1/3} \tag{45}$$

This coposite equation connects the laminar and turbulent limiting cases and is applicable for a full range of Reynolds numbers, $1 \leq Re_{2H} = 2HV/\nu \leq 100000$.

The $\mathscr{A}$ and $\mathscr{B}$ factors appearing in Eq. 45 are expressed solely in terms of the component array geometry

$$\mathscr{A} = \frac{\gamma^2}{\zeta^3 \chi} \tag{46}$$

$$\mathscr{B} = \frac{\gamma^{5/4}}{\zeta^3 \xi} \tag{47}$$

where

$$\gamma = \left[1 + \frac{B}{H} \frac{H}{L} \frac{1}{1 + S/L} \right] \tag{48}$$

$$\zeta = \left[1 - \frac{B}{H} \frac{1}{1 + S/L} \right] \tag{49}$$

$$\chi = \left[\frac{B}{H} + \left(1 - \frac{B}{H} \right) \left(1 + \frac{2B}{H} \frac{H}{L} \frac{1}{1 + S/L} \right) \right] \tag{50}$$

and

$$\xi = \left[\frac{B}{H} + \left(1 - \frac{B}{H} \right) \frac{1}{1 + S/L} \right] \tag{51}$$

Figure 10 illustrates the definitions of the geometrical parameters B, H, S, and L appearing in Eqs. (48–51). The groupings B/H and S/L represent the nondimensional package array height and spacing, respectively, where H/L provides the needed link between them.

Despite the complexity of the dependence, it is clear that as the package size shrinks (i.e., $B/H \to 0$) and/or as the spacing increases (i.e., $S/L \to \infty$) $\mathscr{A}$ and $\mathscr{B}$ approach unity, and the associated laminar and turbulent friction factors reduce to appropriate smooth plate values. With finite package size, however, $\mathscr{A}$ and $\mathscr{B}$ increase steeply with increasing package size. As $\mathscr{A}$ and $\mathscr{B}$ increase, the friction factor associated with the channel also increases, leading to deteriorated channel flow with increased protuberance size. Thus, by representing the actual populated PCB by an equivalent array of cuboid blocks mounted on a flat plate, the package-corrected friction factor for the PCB channel may be predicted using Eq. (45).

Knowledge of the friction factor may be used to calculate the pressure loss and flow rate in the channel.

$$\left. \frac{\partial P}{\partial x} \right|_{\text{loss}} = \frac{-f_{2H} \rho Re_{2H}^2 \nu^2}{16 H^3} \tag{52}$$

This flow rate may then be used in standard forced convection correlations to obtain a heat transfer coefficient.

In an approach to a real situation, the deviation of the friction factor characteristics of an actual PCB channel from that of an idealized smooth channel could be obtained and used to more accurately predict the flow rate and thus the convective heat transfer in the channel.

Air-Cooled Heat Sinks

The simplicity and cost-effectiveness of air-cooled heat sinks, continue to expand the design space for this most ubiquitous

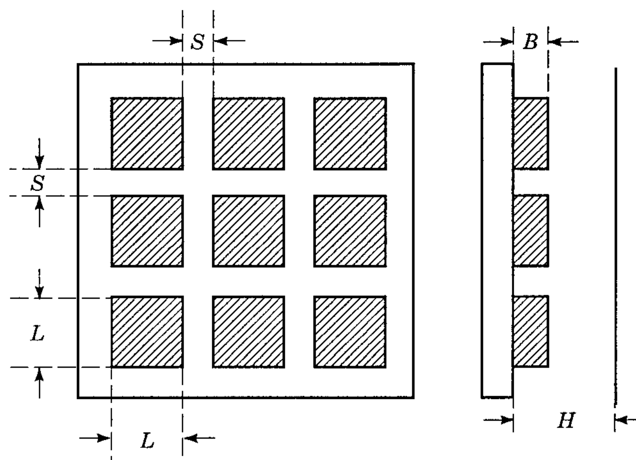

Figure 10. Definition of the various geometrical parameters used in Eqs. (48 through 51).

of all thermal management hardware in the electronic industry. When attached to modules, chip packages, or directly to chips, heat sinks can enhance both the reliability and functional performance of electronic, telecommunication, and power conversion systems. However, rapidly increasing chip power dissipation and concerns over weight, cost, acoustic noise, and time-to-market are constraining the successful application of these thermal devices. Greater attention to the underlying thermal, fluid, and structural interactions, as well as an appreciation for the cost and limits of available materials and fabrication processes, will be needed to maintain the viability of this cooling technique.

Extended surface heat-transfer relations, which describe the thermal performance of individual fins and fin arrays, can be manipulated to provide criteria for the selection of fin geometries that will minimize the volume and mass required to meet a target dissipation. Attention must also be devoted to the impact of the fluid dynamic design on the pressure drop, dissipated pumping power, and acoustic noise generated by the heat sink. All three of these penalty quantities vary nonlinearly with velocity and that a desire for quiet operation may lead to the selection of higher air flow rates at lower pressures.

Use of a large, high-performance heat sink to cool a single chip requires that the base of the heat sink serve as a heat spreader. The trade-offs involved in optimizing the base in terms of volume, mass, and performance suggest that one consider the use of new, engineered materials, such as ceramics, composite materials, and embedded heat pipes.

Although the use of a heat sink is intended to improve the reliability of an individual electronic component, potential failure modes of the material layer or coating used to attach the heat sink may compromise this goal. Thermally induced stresses may lead to cracking, delamination, and rupture of the heat-sink bond. Unfortunately, although thermal stress considerations favor a relatively thick interfacial layer, thermal performance demands that this low thermal conductivity layer be as thin as possible.

In the design and selection of high-performance, compact heat sinks, attention must be paid to the immediate physical surroundings. Neglecting the potential for air flow by-passing the heat sink and leaking out can lead to serious overpredictions in heat sink performance. Moreover, care must often be taken to minimize the volume occupied by the thermal solution and its impact on the form and shape of the packaged product. Although analysis and testing can provide guidelines for dealing with these issues, today's commercial computational fluid dynamics (CFD) software is most effective in identifying solutions and optimization opportunities early in the design cycle and can be used successfully to tailor the thermal solution to the specified physical and performance envelope.

Air-cooled, least-material optimum fin arrays are typically characterized by large aspect ratio fins and interfin spacings that are beyond the range of conventional casting, extrusion, and machining operations. The design of cost-effective heat sinks requires that attention be devoted to manufacturing considerations. The performance and manufacturing costs of various suboptimal (thermal) configurations must be sufficiently well understood to perform a more generalized optimization.

Using the present as prologue, it appears clear that future heat-sink design will need to address the myriad of concerns and constraints, that define the electronic product envelope. In the coming era, the limits on heat sink performance will be established not by thermal performance alone but by the cost-effectiveness of the thermal design, including material and manufacturing/fabrication costs, as well as the less visible costs of reliability, acoustic noise, space utilization, and time-to-market. To assist in this multidimensional design process, it can be expected that, in the future, automated design will play a far greater role in heat sink development. Such second-generation CAD tools can be expected to provide sophisticated inverse-design capability, which will help define the optimal configurations to offer virtual reality displays—this will aid the designer in tailoring the heat sink to the size and shape of the available space and to afford easy access to rapid prototyping tools that generate heat sinks samples for rapid evaluation of proposed solutions.

For a thorough treatment of heat-sink design and analysis, the reader is referred to Ref. 4.

Passive Immersion Modules

The challenges posed by high chip heat fluxes make direct liquid cooling a leading candidate for future thermal packaging systems. Passive immersion modules (PIMs) consist of active microelectronic components encapsulated in a liquid-filled enclosure. The dielectric liquid wets the surface of the component, and heat is removed by convection and/or boiling. As liquid circulates within the enclosure, heat is spread to the module walls. The external surfaces of the module are then cooled by the ambient air. The module walls may be internally finned, externally finned, or both (40).

The circulation of the liquid within a PIM, including the formation, collapse, and additional buoyancy of vapor bubbles generated through boiling, may be used overcome the barriers posed by thermal conduction through solids and across solid-to-solid interfaces (a dominant concern in the application of conventional heat sink technology). Although high-velocity-flow boiling, liquid jet impingement, and liquid sprays could all be used to cool the anticipated high flux chips of 2006, the SIA/NEMI cost constraints appear to favor development of modules that passively reject the generated heat to air.

A PIM consists of heat-dissipating microelectronics enclosed in a liquid-filled module. In such PIMs, high heat fluxes may lead to boiling on the component surfaces. Vapor bubbles generated in the module rise, coalesce, and condense in the liquid, inducing considerable circulation and bubble-pumped convection along the module walls that serve as submerged condensers. The thermal performance of such a PIM is constrained by the departure from nucleate boiling or critical heat flux (CHF), on the surface of the components and the maximum attainable heat transfer rate at the submerged condenser surfaces.

Markowitz and Bergles (41) proposed that the complex phenomena occurring within a PIM could be effectively represented in a performance map, similar to that depicted in Fig. 11, relating the heat dissipation, Q, to the temperature difference, ΔT_{hc}, between the chips (heaters) and the con-

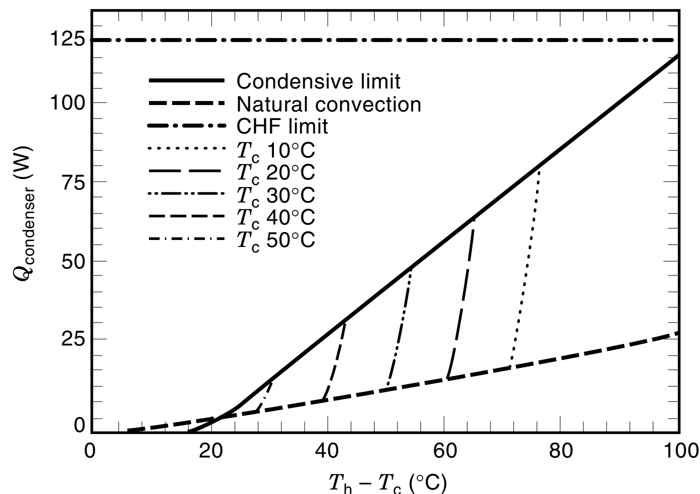

Figure 11. Theoretical performance map for a PIM.

denser. In creating a theoretical performance map for a PIM the lower bound of the performance envelope is defined by natural convection on both the chip and condenser surfaces. In modules where the condenser surface is at the top of the module where vapor can collect, the upper bound for the performance envelope is vapor-space condensation. However, for tall, narrow modules where the majority of the heat is removed from side-wall submerged condenser, vapor-space condensation does not represent a realistic upper limit for the performance of the condenser. A more realistic upper bound may be that of bubble pumped convection with noncondensing bubbles. A semiempirical correlation by Bar-Cohen et al. (42), for this maximal bubble pumped convection on a vertical plate, is given by

$$\mathrm{Nu} = (1 + \lambda Z)^{1/3}\mathrm{Nu}_{\mathrm{nc}} \tag{53}$$

where

$$Z = \frac{(\rho_{\mathrm{f}} - \rho_{\mathrm{g}})QW}{\sqrt{gD_0}\,\rho_{\mathrm{f}}\rho_{\mathrm{g}}h_{\mathrm{fg}}\beta(T_{\mathrm{sat}} - T_{\mathrm{s}})V} \tag{54}$$

and $\mathrm{Nu}_{\mathrm{nc}}$ is the appropriate single-phase natural convection Nusselt number. In Eq. (53), λ is an empirically determined factor which depends on the heater and condenser configuration of the module, typically ranging in value from 2 to 9.

Between the lower bound of natural convection and the upper bound of vapor-space condensation, the temperature difference between the chips and the submerged condenser surface is governed primarily by nucleate boiling on the chips and bubble-pumped convection on the condenser. With sufficient condenser capacity, the performance of the PIM may be limited by the critical heat flux at the chip surfaces, which is accompanied by vapor blanketing of the surface and a large increase in surface temperature.

Kitching et al. (40) studied the thermal characteristics of a prototype, air-cooled, PIM and addressed the upper-bound and bubble-pumped augmentation on the finned submerged condenser surface. The experimental observations and supporting modeling studies revealed that thermal performance maps could be used to represent the behavior of finned, submerged condenser PIMs. Moreover, in this study, a two- to threefold improvement in the convective heat-transfer coefficient was attained along a horizontal, submerged condenser surface, consisting of square pin fins. This augmentation was achieved with a relatively modest bubble (void) fraction of 2% to 3% in the enclosed liquid. Condensation on the exposed fin surfaces represents the upper bound for operation of a horizontal PIM.

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