PACKAGING RF DEVICES AND MODULES

Initially implemented in military radar, microwaves have been used in communication, space, scientific, and commercial applications. The term *microwave* usually refers to the frequency spectrum ranging from 300 MHz to 300 GHz. Strictly speaking, millimeter-wave (mm-wave) begins at about 30 GHz; therefore, the term *radio frequency* (RF) is used, instead of *microwave,* to represent both microwave (300 MHz to 30 GHz) and mm-wave (30 GHz to 300 GHz) frequency spectrum.

Radio frequency (RF) packaging is becoming more and more important due to the significant growth of military and commercial applications in wireless communication and sensing. Packaging strongly affects performance, cost, and reliability; it is a determining factor in application growth. Many RF packaging issues are the same as those for microelectronic packaging, which are covered in other articles. However, RF packaging has three distinguishing features:

1. *Frequency range.* Table 1 lists application examples at frequencies ranging from 1 GHz to 100 GHz (1). There is another long list for frequencies less than 1 GHz. For such a wide spectrum of applications, it is not practical to develop a few "standard" packaging solutions to meet requirements that are usually frequency-dependent.
2. For frequency higher than 1 GHz, the package strongly affects RF performance. It is a part of the circuit, not just a housing. The package parasitic becomes more critical as frequency increases (2,3).
3. The number of inputs/outputs (I/O) in RF packages is small, for instance 6 I/Os or 12 I/Os; however, electromagnetic waves must be transmitted in and out with minimum losses.

Table 1. Examples of RF Applications at Frequencies from 1 GHz to 100 GHz

Frequency (GHz)	Applications
1.9 to 2.1	Personal communication services (PCS)
4 to 8	Cooperative engagement military communication
5.1 to 5.3	Supernet band for PCS
12.4 to 12.7	Direct broadcast satellite (DBS)
20 and 44	Military MILSTAR
27.5 to 30	Local multipoint distribution service (LMDS)
26 to 40	Military precision guided missiles
60	Wireless communication links
77	Vehicular collision avoidance radar
75 to 110	Concealed-weapon detection

RF packaging technologies have been driven by military applications; as a result, most packages are semicustom or custom designed for performance, reliability, and small volume manufacturing. With the growth of commercial applications, cost is becoming the predominant factor. As a result, plastic and low-cost ceramics are used for mass production of RF packages for PCS applications at frequencies around 2 GHz. They are being developed for higher frequencies around 5 GHz.

High-volume applications in mm-wave frequencies, for example, 23 GHz, 26 GHz, 30 GHz, 38 GHz, 60 GHz, and 77 GHz, are to be implemented in the near future. Packaging these RF devices and modules is critical to a successful implementation. Package complexity is increasing substantially in order to support these new commercial systems using microwave and millimeter-wave integrated circuits (MMICs), active antennas, antenna arrays, microelectromechanical systems (MEMSs), substrates with ferroelectric or superconductor or other novel components.

RF packaging technologies are advancing rapidly. This article provides basic knowledge to understand the technology advances. Most packaging issues common to those for microelectronics packaging will not be covered here, and they can be found in other articles. The following sections will focus on unique issues for RF packaging. Representative packages and assembly technologies will be reviewed. Critical considerations of RF performance and reliability will be introduced. The reliability section will cover both thermal management and mechanical integrity. A case study will be presented to illustrate a typical design procedure considering various factors. In addition, computer-aided-design (CAD) issues and advanced packaging concepts will be introduced, to understand future challenges.

RF PACKAGES

A typical microwave and mm-wave system is shown in Fig. 1. Signals are generated by an oscillator and transmitted from an antenna driven by an amplifier. The signals are received by another antenna and propagated to a receiver. There are many transmission line components to interconnect these basic devices. In many cases, the transmission line is a part of the circuits. The trend is to integrate all the devices and components more and more using MMIC and advanced packaging technologies. High integration could eliminate layers of interconnects for cost reduction and performance enhancement.

Figure 2 shows an example of two levels of RF packaging. For a single-chip package, an RF device is connected to a package substrate through wire bonding or flip-chip soldering/bonding. Usually there are transmission lines on

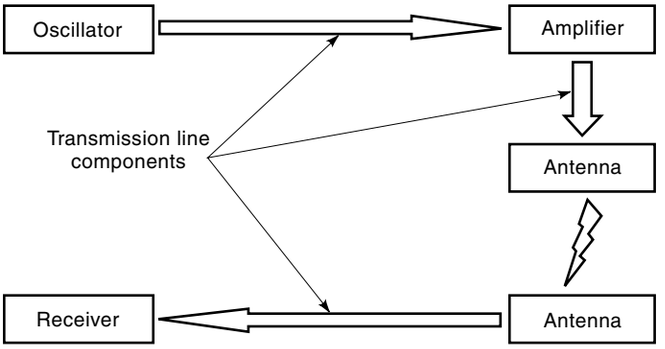


Figure 1. A typical microwave or millimeter-wave system consisting of major functional modules and circuits for signal transmitting and receiving. The integration of the oscillator, amplifier and antenna is for signal transmitting. The integration of the antenna and receiver is for signal receiving. For high-frequency applications, the transmission line components should be reduced as much as possible for high efficiency.

the substrate; the lines are connected to the external ports through feedthroughs or vias. The external ports are connected to the next level board assembly. For a multichip RF module, bare-die devices and RF components are connected to a multilayer substrate with transmission lines as interconnects. These single-chip and multichip modules will be briefly reviewed in what follows (see Fig. 2).

Single-Chip Packages

Figure 3 shows a photo of a typical RF package with various components of a package shown in Fig. 4. The wall of housing is usually made of metal or ceramic. The feedthroughs are gold-coated leads passing through a metal or ceramic wall. With a metal wall, feedthroughs are isolated from the wall by glass. A gold plated Kovar (iron-nickel-cobalt alloy) or CuW (copper-tungsten) base is soldered to the bottom of the package, and a gold plated Kovar lid is typically attached to the wall with AuSn (gold-tin) solder.

There are many different packaging approaches other than the above example. Several factors should be addressed before an individual packaging method is chosen (4):

- Low-loss electrical interconnect with impedance matching
- Dimensional stability and achievable tolerances
- Three-dimensional package characterization with antiresonance housing
- Electromagnetic shielding

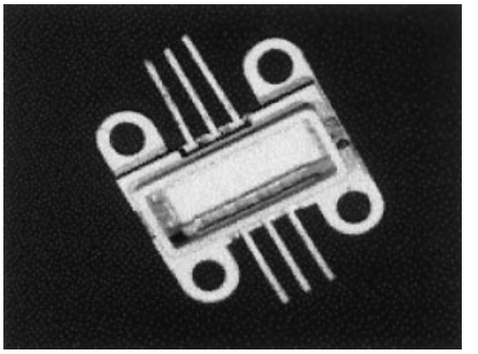


Figure 3. Photo of a typical single-chip RF package. Details of the package are described in Fig. 4.

- Efficient thermal management
- Matching of material properties for reliable connections
- System constraints such as size, weight, shape, hermeticity, or the special positioning of the packages or modules in the array
- Test and validation
- Overall cost including assembly and rework as well as package manufacturability

With these considerations, a designer can chose a proper packaging solution. A summary of different packages are described below.

Package Materials. RF single-chip packages can be categorized by package material such as metal wall, ceramic wall, glass ceramic, and plastic packages. Their major characteristics are listed in Table 2 qualitatively, and a brief description is given in this section.

Metal Wall Package. The metal wall is usually Kovar coated with nickel and gold. Its feedthroughs for output leads are striplines isolated from the wall. Striplines are described later. A good package can be used up to 90 GHz with low insertion loss and excellent isolation. However, thermal performance is poor using Kovar and the cost can be high. Thermal performance can be enhanced substantially with a CuW base plate. To reduce cost, metal injection molding can be used for fabricating the metal housing (5).

Ceramic Wall Package. The ceramic wall is usually made by high-temperature cofired ceramic (HTCC) coated with nickel and gold. The process for HTCC is described in Ref. 6. The feedthrough conductor can be tungsten striplines without additional electrical isolation. A good package can be used up to 60 GHz with low insertion loss and good isolation. The

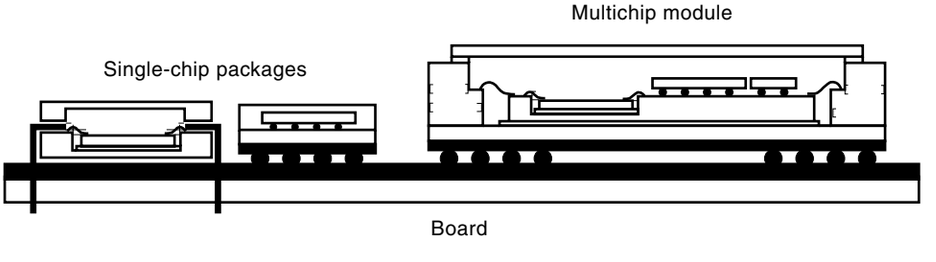


Figure 2. Single-chip and multichip RF packages mounted on a board. The single-chip package can be through-hole or surface mount types. The multichip module can be assembled using wire bonding or flip-chip connections; the module can be mounted onto the board using through-hole or surface mount technologies. All the critical elements for the first- and the second-level packaging are shown in the figure.

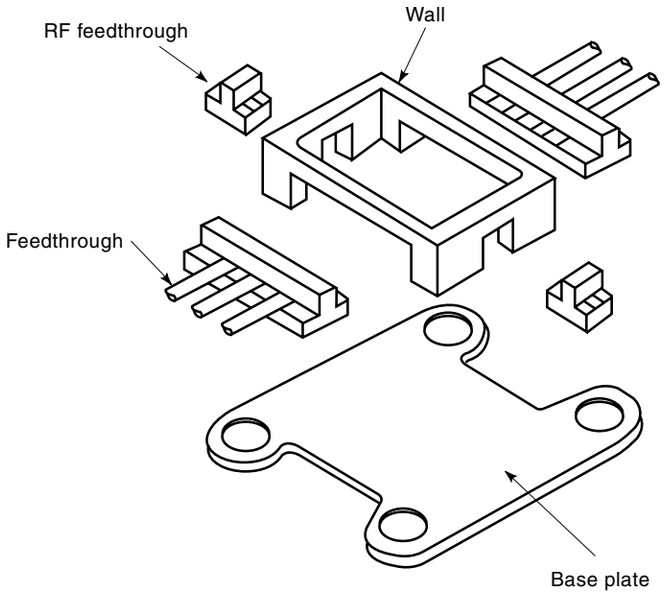


Figure 4. Structure of an RF package consisting of a wall, feedthroughs, and a baseplate. The baseplate carries the RF device that is connected to RF ports through wire bonding pads and feedthroughs. The metal wall is to provide electrical, thermal, and mechanical protection of the device.

package cost can be lower than that of the metal wall package's, but it may still be high.

Glass Ceramic Package. The package material is a compound mixing glass and alumina. It is also called low-temperature cofired ceramic (LTCC) with copper as the conductor. The substrate is ideal for surface mount package and multichip modules. A good package can be used up to 40 GHz with low insertion loss. Its cost is low because the use of copper as the conductor; however, without enhancement, its thermal performance can be poor.

Figure 5 shows a surface-mounted ceramic package with RF vias. The external ports can be designed for leadless chip carrier or ball-grid-array (BGA) surface-mount technologies. The insertion loss can be high, and the operation frequency is limited to a band between 18 GHz to 26 GHz. With higher frequencies, the typical $\lambda/4$ length scale is close to length scales of package discontinuities caused by bonding wires or joints, vias, walls, and other elements. To reduce the loss at a selected high-frequency band, the electromagnetic coupling at critical interfaces should be designed to smooth such discontinuities. Figure 6 is a package with coupling designed for 77 GHz.

Plastic Package. The plastic package is fabricated by injection molding of a device on a pedestal/leadframe for die attachment and I/O leads. The package is excellent in manufacturability and ideal for surface-mount technology. However, it is usually used for frequencies less than 10 GHz due to high insertion loss. The manufacturing processes are the same as those for plastic packages used in microelectronics; however, the inductance of bonding wire and leadframe should be evaluated for high-frequency packages. A new premolded plastic package can enhance the performance, which is described later. The cost of a plastic package is low; however, it may not be lower than that of the glass ceramic package if both are designed for reach the same electrical performance.

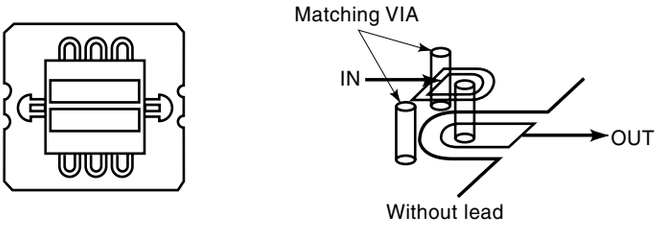


Figure 5. A surface mount package with RF vias. At the end of each port, the RF signal passes through the via to a solder pad for surface mounting. No lead is needed for better RF performance because of short connections. Surface mount is important to automatic assembly of the package onto a board.

Boards. The single-chip RF packages are generally mounted on a board. The board technologies are very similar to those for RF modules; these technologies are to be described in the next section.

Multichip Modules

Multichip module (MCM) technologies are being applied to design and manufacture RF modules. It is defined as a substrate of dielectric and conduction layers, on which integrated circuits ("chips") and passive components (if any) are mounted directly on (or inside) the substrate, without separate packaging for most of the active components. The entire MCM may be placed in a hermetic package much like a large single-chip carrier, or may be directly covered with a sealant material to protect the components from physical damage (7). A good MCM example is shown in Fig. 7, which is a drawing of a photo taken from Ref. 8. The module consists of components on both sides. The front side has RF multicavities with all the MMICs and a large cavity with low-frequency components, for example, ASICs and discrete components for power supply and distribution. The backside is a nonhermetic area where all the surface mount components are assembled.

The advantages and concerns of MCM and single-chip packaging are listed in Table 3. MCM technologies are emerg-

Table 2. Different Materials for Single-Chip RF Packages

	Metal Wall	Ceramic Wall	Glass Ceramic	Plastic
Features	Broadband	Broadband	Low loss	Low cost
	Low loss	Lower cost than metal wall	Suitable for single-chip and MCM	Suitable for high volume applications
	Antiresonation	Low loss	Surface mount	Surface mount
	Structure	Anticavity resonation	Suitable for high-volume applications	
	Excellent shielding	Good shielding		
	Excellent isolation	Good isolation	Excellent design flexibility	

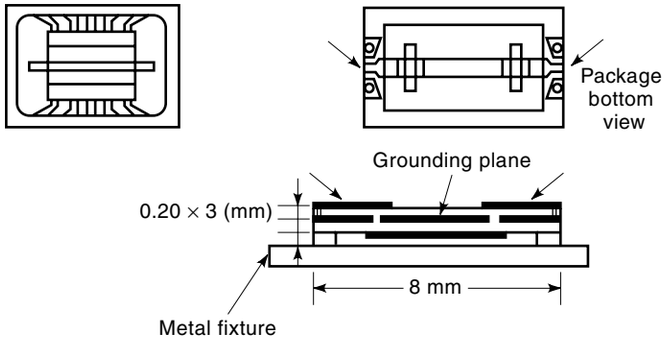
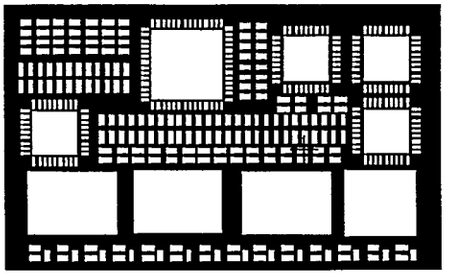
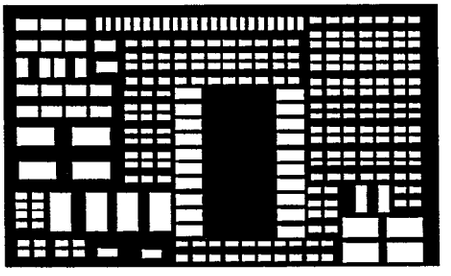


Figure 6. Structure of an electromagnetic coupling package. The top-layer microstrip line is coupled to the bottom one through the slot on the ground plane. The structure achieves the low insertion loss in a selected high frequency band. Such a specific RF design is important to reduce losses in millimeter-wave applications.

ing as a cost-effective technology for next-generation devices because of their advantages in small size, performance enhancement, better reliability, low power consumption, package cost reduction, and potential overall cost reduction for high-volume applications (9). It is the predominant approach for mm-wave modules with frequencies higher than 30 GHz. However, its cost can be very high if manufacturing yield is low. With the establishment of MCM manufacturing infrastructure for microelectronics, the manufacturing barrier is being reduced substantially. In addition, sizes of single-chip packages are reduced significantly with chip-scale-package (CSP) technology. These packages for some RF and microelectronic devices can be integrated with other devices to form an MCM. It is anticipated that more MCM-based RF modules will be developed for size, weight, performance, power, or cost advantages in future.



Front side



Backside

Figure 7. Substrate for a mixed multichip module. The front side consists of low frequency microelectronics and RF areas. Critical devices are sealed separately to avoid crosstalk. The back side is a nonhermetic area for all low frequency surface mount components. A multichip module is much more complicated than single-chip packages; it is custom-designed and fabricated to interconnect many devices to reach specific targets on cost, performance, size, weight, or reliability.

Table 3. Advantages and Concerns for Single-Chip and Multichip Packaging

	Single Chip	MCM
Advantages	Each device testing Good yield as module Device to device isolation Hermeticity for individual device Volume manufactuability	Size reduction Lightweight Assembly cost reduction/ cycle time reduction Performance enhancement Reliability enhancement Power reduction
Concerns	Electrical performance as module level	Bare die testing and yield Rework Use of via for RF line dc/RF shielding

MCMs can be fabricated using thin-film, thick-film, or thick/thin film technologies. Typical substrate materials important to RF packaging are listed in Table 4 (10,11) for hard and Table 5 (12) for soft substrates.

Alumina/Glass Alumina. Alumina and glass alumina are popular substrates for MCMs. The fabrication of alumina substrate usually employs cofired technology, which includes low-temperature cofired ceramic (LTCC) and high-temperature cofired ceramic (HTCC). LTCC and HTCC are alumina/glass systems that differ in glass content (50% vs. 4%) and firing temperature (850°C vs. 1500°C). The LTCC firing tempera-

Table 4. Properties of Hard Substrate Materials

	CTE $\times 10^{-6}$/°C	Thermal Conductivity W/m · K	Dielectric Constant ϵ_r (10 GHz)	Tan δ $\times 10^{-4}$ (10 GHz)
Alumina (HTCC)[a]	6.9	20	9.1	12
Alumina thin film[b]	7.2	33	9.5	0.9
Glass ceramic[c]	5.9	2.5	5.7	12
ALN	4.7	150	8.6	53
BeO	9	260	6.7	40
Fused quartz	0.5	1.4	3.75	15
Sapphire	6	46.1	10.3	20
Si (high resistivity)	2.6	148	12	10–100
Gallium arsenide	5.7	58	12.9	16

[a] Alumina A443 by Kyocera Corporation.
[b] Alumina A493 by Kyocera Corporation.
[c] Glass ceramic G-55 (GL550) by Kyocera Corporation.
Note: For properties of BeO the reader is refered to *Integrated Active Antennas and Spatial Power Combining* [J. A. Navarro, K. Chang, 1996]. Properties of fused quartz, sapphire, and Si are covered in *Materials Handbook for Hybrid Microelectronics* [Edited by Joseph Alison King. Artech House 1988]. Properties of gallium arsenide are listed in this table for reference.

Table 5. Properties of Soft Substrate Materials

	CTE $\times 10^{-6}$/°C	Thermal Conductivity W/m · K	Dielectric Constant ϵ_r (10 GHz)	Tan δ $\times 10^{-4}$ (10 GHz)
PTFE[a]	17	0.257	2.33	13
Filled PTFE[b]	35	0.31	3.5	26
FR4[c]	15.8	0.2	4.7	300
Polyimide[d]	16	0.043	4.2	150

[a] Diclad 870 by Arlon Materials for electronics division.
[b] AR 350™ by Arlon Materials for electronics division.
[c] For properties of FR4 refer to *Microelectronics Packaging Handbook* [Edited by R. R. Tummala and E. J. Rymaszewski. New York: Van Nostrand Reinhold, 1989].
[d] 85N by Arlon Materials for electronics division.

ture permits the use of silver, gold, and copper as conductors, while HTCC is limited to the use of a higher melting point refractory alloy, such as tungsten and molybdenum. LTCC substrates thus have lower sheet resistance but higher dielectric loss tangent. Their mechanial strengths and thermal conductivities are also lower than those of HTCC substrates. To achieve better cost/performance ratio, thin-film MCMs can use a harder alumina substrate, for example, A493, listed in Table 4, which has good RF, mechanical, and thermal properties. With thin-film technologies, low-temperature metals can be used for circuits. If planar passive components are needed, either HTCC or LTCC multilayer ceramic can be used as the substrate for thin film. Details on thin-film, thick-film and thin/thick film MCM technologies are given in other articles in this encyclopedia.

With single-layer or multilayer structures, different types of interconnect, for example, stripline, microstrip, and coplanar waveguide, can be used. Thermal conductivities of alumina and glass alumina substrate are usually poor. If needed, thermal performance can be enhanced by the use of metal plates, for example, CuW and Cu-Mo-Cu composites. Alternatively, AIN or BeO can be used.

BeO. Beryllium oxide or beryllia (BeO) is an alternative substrate material with an excellent thermal conductivity of 260 W/mK. However, it is not widely used because of toxicity of outgasing during substrate fabrication. Also, its CTE is 9 ppm/°C, which is quite different from GaAs's CTE. In addition, BeO cannot be used to fabricate multilayer structures.

AIN. AIN, with a thermal conductivity of 150 W/mK, is becoming an appealing alternative to alumina. Its coefficient of thermal expansion (CTE) of 4.7 ppm/°C, which is closer to silicon's and GaAs's CTE. It can be used for single-layer and multilayer thin- or thick-film technologies. AIN substrate also utilizes refractory metallizations, firing at 1800°C. AIN powders are currently more expensive than alumina and result in higher substrate cost. In addition, the electrical loss could be high and the thermal conductivity can be degraded substantially, with processing variations.

Polymers. Laminated substrates are being used widely for personal communication systems (PCS) applications. Their well-established manufacturing infrastructure can be accessed by module designers. The typical substrates can be PTFE, FR-4, and polyimide. Their properties are listed in Table 5. Their CTEs are very large and thermal conductivities are poor, so reliability issues should be considered during module design. For low-loss modules, PTFE with different fillers can be used.

In addition to the properties discussed above, another major concern regarding the materials is dimensional stability. RF performance is affected by the variations of dimensions such as the length and the width of a line, the shape of a line's cross-section, the spacing among lines, the diameter of a via, surface roughness, and many other geometric parameters. In particular, performance in millimeter wave modules is strongly dependent on dimensional stability. For these applications, HTCC, LTCC, and plastic packages might not be good choices; their structural shrinkage or expansion could cause performance degradation. Rigorous process control is needed to limit the dimensional change during manufacturing. Or, thin-film packages could be used. Even for the thin-film interconnects, tight process control or new processing techniques may be needed. For example, reactive ion etching (RIE) instead of a wet etching process may be used to fabricate a precise structure for superior performance (7).

Assembly Technologies

The first-level (device-to-package) assembly technologies are wire bonding, tape automated bonding (TAB), and flip-chip soldering or bonding. The second-level (package-to-board) assembly technologies can be through-hole or surface-mount. The surface-mounted packages can be leaded or leadless peripheral, ball-grid-array (BGA), chip-scale-package (CSP), or direct chip assembly (DCA). The major challenge to the assembly technology is to control its effect on the package performance. Since the unique RF requirements of the second-level packaging are very similar to those of the first-level packaging, only the requirements for the wire bonding, TAB, and flip-chip assembly will be discussed.

Wire Bonding. Wire bonding technology is the earliest and by far the most prevalent technology (>90%) in use today. A typical microwave chip and wire interconnect utilizes 18 μm to 25 μm diameter gold wire which is ball or wedge bonded to gold-plated die and substrate bond pads. The very narrow wires are highly inductive at higher frequencies, and variations in wire length and loop shapes cause performance variations from module to module (13). Length and impedance control are critical issues.

TAB. Tape automatic bonding (TAB) technology is commonly utilized in commercial products requiring lightweight, thin packaging. TAB is typically a reel-to-reel process using solid copper tape or copper prepatterned on a polymide film. The inner leads of the tape are bumped and bonded to the die pads. Finally, the bonded assembly is encapsulated and the outer leads are bonded to a printed wiring board (13). The coplanar film carrier can be made for TAB RF packaging, which has an insertion loss of less than 0.2 dB/mm without resonance over the frequency range from dc to 30 GHz. The electrical performance of a GaAs MMIC module with coplanar film carrier is almost equal to that of an MMIC measured directly on wafer (14).

Flip Chip Assemblies. Flip-chip technology provides a direct metallurgical interconnect between die bond pads and the substrate. Solder-bumped die are soldered or bonded directly to the substrate, providing an excellent electrical connection.

The thermal path is through the solder connection to the substrate. In the case of high-power GaAs MMICs, without the use of thermal bumps, this thermal path is usually inadequate for reliable operation (13). However, flip-chip assembly is becoming more and more important with the following advantages (15–17):

- Automated assembly
- Compact modules
- Minimum interconnect length
- Low inductance and discontinuity
- Compatibility with coplanar interconnects without the use of thin devices
- Efficient thermal management with the use of thermal bumps

RF packaging is very challenging because of the wide spectrum of operation frequencies and strong packaging effects on RF performance. For example, the number of I/Os is substantially less than those for microelectronics; however, it is still very difficult to switch from wire bonding to flip-chip assembly. Such a switch is a paradigm shift, demanding reconsideration of not only package but also device designs. The microstrip lines on an MMIC should be replaced by coplanar waveguides. More important, placement of high-power dissipation MESFETs or other devices should be close to the flip-chip joints. Trade-off considerations on RF performance and reliability must be taken into account before any package design. These two issues are to be discussed in the following sections.

PERFORMANCE OF RF PACKAGES

At microwave and higher frequencies, packaging can affect the RF performance of circuit significantly. RF parameters of the package are frequency-dependent. Insertion loss, return loss, package resonance frequency, and crosstalk caused by electromagnetic coupling are measures of RF performance. As frequency increases, packaging can become the limiting factor of electrical performance by degrading signal propagation, or by contributing to structural configuration that fosters cavity resonances or that propagates waveguide modes.

Single-Chip RF Package

Even though RF performance of multichip modules (discussed later) is superior (3) to that of single-chip package to some extent, the single-chip package is still useful due to several reasons (3):

1. Electrical response of a packaged device is more reproducible and defined. Bond wire and mounting techniques affecting RF characteristics can be defined.
2. Die performance can be tested and validated.
3. Each package can be designed for machine handling.
4. Packages assembled are usually reworkable.

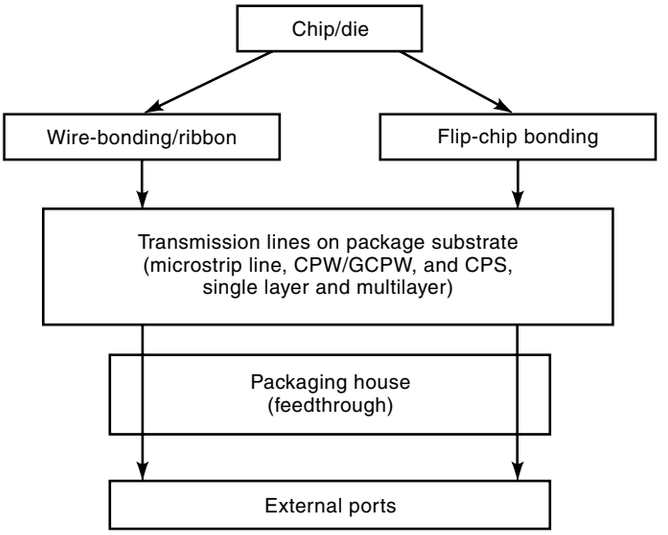


Figure 8. Block diagram of RF components for a general single-chip RF package. Each block represents a critical package element that affects the RF performance of a packaged RF device.

RF Structure of the Package. Figure 8 illustrates typical RF components for a single-chip package. An RF/MMIC chip (die) may be a single device or an integrated circuit consisting of several devices. The chip is bonded to pads on the substrate by using wire/ribbon bonding or flip-chip bonding technology. Transmission lines on the package substrate carry the signal in or out of the chip. Mircostrip lines or coplanar waveguides (CPWs) can be used. Bias and control signal lines are also fabricated on the package substrate. The package substrate can be either single layer or multilayer. For a multilayer substrate, vertical vias are needed to carry the signal or dc power through different layers. The substrate is enclosed in the metal or ceramic housing with external ports. Feedthroughs are needed to carry the RF and other signals in and out through the package housing. A stripline structure is a common choice for these feedthroughs. External ports can be miniature coaxial connectors, through-hole leads, or solder joints for the next-level packaging (see Fig. 2).

Bond Wire and Flip-Chip Interconnect. Bond wires/ribbons and flip-chip interconnects provide electrical connections between a chip and a substrate. Figure 9 shows the comparison of effect of wire bond length and flip-chip interconnects on insertion and return losses. The insertion loss (S_{21}) in two-port RF circuits is found by driving port 1 with a incident wave of unit amplitude, and measuring the transmitted wave voltage amplitude, coming out of port 2, when port 2 is terminated in matched load to avoid reflection. The return loss (S_{11}) is, similar to the insertion loss, the ratio of the amplitude of the wave reflected from port 1 to the incident wave voltage amplitude to port 1 when port 2 is terminated in matched load. The return loss (S_{11}) and insertion loss (S_{21}) are widely used in RF engineering as measures of RF performance. As observed in Fig. 9, the flip-chip interconnect typically results in better performance, particularly for frequencies higher than 4 GHz (7). Most of the discussions in the literature concentrate on S_{21} effects. However, to ensure a minimum amount of standing waves in the assembly and, hence, the

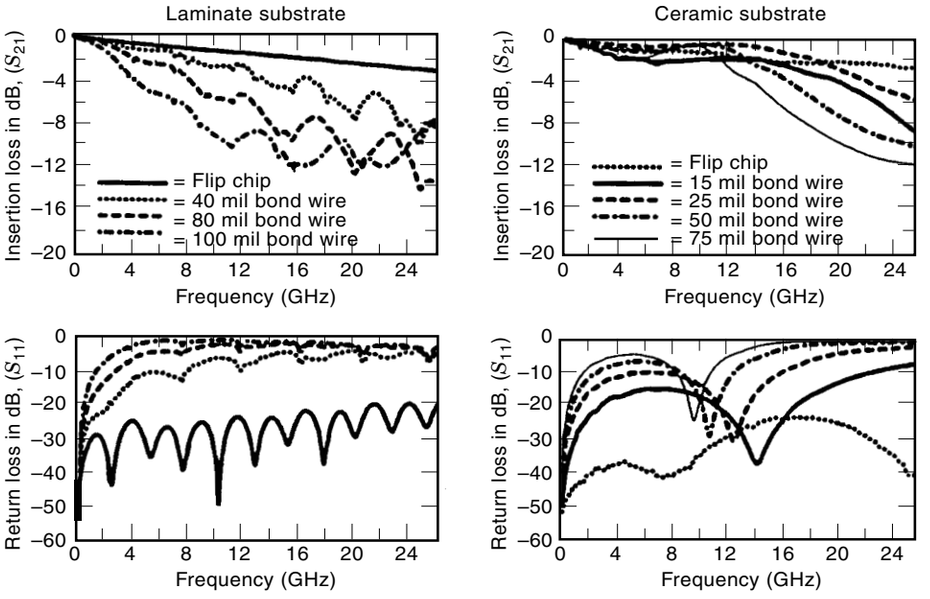


Figure 9. Insertion loss and return loss for flip-chip and bond-wire interconnects with RF chips mounted on a laminate or a ceramic substrate. The losses are strongly dependent on the assembly technologies, substrate materials, and operating frequencies. This figure can be used to estimate losses in a typical RF package. (From Ref. 7, © IEEE 1997, reprinted with permission.)

most uniform behavior across a wide range of frequencies, S_{11} should be less than −20 dB across the entire passband of interest. Here again, wire bonds of all lengths perform poorly in comparison with flip-chip interconnects for frequency above a few hundred megahertz.

Bond Wire or Ribbons. Wire bonding is the most widely used method of connecting a chip to a package. A typical bond wire is around 300 μm long and 200 μm high. This length includes a margin of error due to (1) the height difference between the chip and the substrate, (2) chip contact pads' locations, and (3) an extra length needed to avoid a mechanical failure during thermal cycling. The inductance of the wire length may degrade the electrical performance of the RF chip. Wire bond inductance can be calculated using the following formula (18):

$$L_s = 5l\left[\ln\left(\frac{2l}{p}\right) - \frac{3}{4}\right]$$

where L_s is the self-inductance with the unit of nH, l is the length of the wire in inches, and p is the diameter of the wire in inches. Figure 10 shows calculated return loss and insertion loss of bond wire and bond ribbon interconnect versus normalized wire length L/λ_0 (19). An interconnect with a return loss better than −10 dB requires bond wires not longer than $0.033\lambda_0$, which is only 100 μm at 94 GHz. Bond ribbon has better performance; the limit on the length in this case is $0.063\lambda_0$ for −10 dB return loss (19).

Flip-Chip Interconnects. The use of CPW line on the chip and the substrate is the key step that allows applying flip-chip as an alternative interconnect technique for RF systems. In CPW, the ground conductors are on the same plane as the signal strip. Microstrip line is more commonly used in RF packages. Therefore, flip-chip interconnects are also used with microstrip. Because the ground conductor and signal strip line are not on the same plane in the microstrip line configuration, vias are needed to connect the ground planes on the chip and package substrate. Therefore, most of the comments in this section are limited to CPW flip-chips. Figure 11 shows the structures of flip-chip interconnect on CPW and microstrip lines. The bump height (50 μm to 75 μm) is small compared with the length of bond wire, and the bump diameter (40 μm to 150 μm) is larger than that of the bond wire. Therefore, a considerable improvement in the electrical interconnect properties is achieved. The return loss is less than −10 dB at 100 GHz for bump height 70 μm and bump diameter 40 μm (19). However, chips are flipped so the substrate is very close to the chip. When the fields of the transmission lines on the chip interact with the mounting substrate, the RF performance of the chip can be affected for several reasons: (1) transmission lines on the chip, (2) the gap between the chip and the substrate, (3) the transition into the chip's transmission lines, (4) chip thickness, (5) transmission lines or other structures on the substrate under chip, and (6) di-

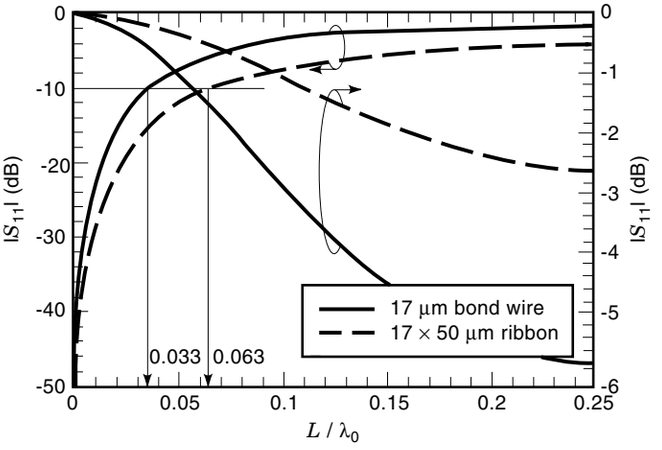


Figure 10. Calculated return and insertion losses of bond wire and bond ribbon interconnect versus normalized wire length L/λ_0. This figure can be used to estimate the right wire length for desirable losses. (From Ref. 19, © IEEE 1996, reprinted with permission.)

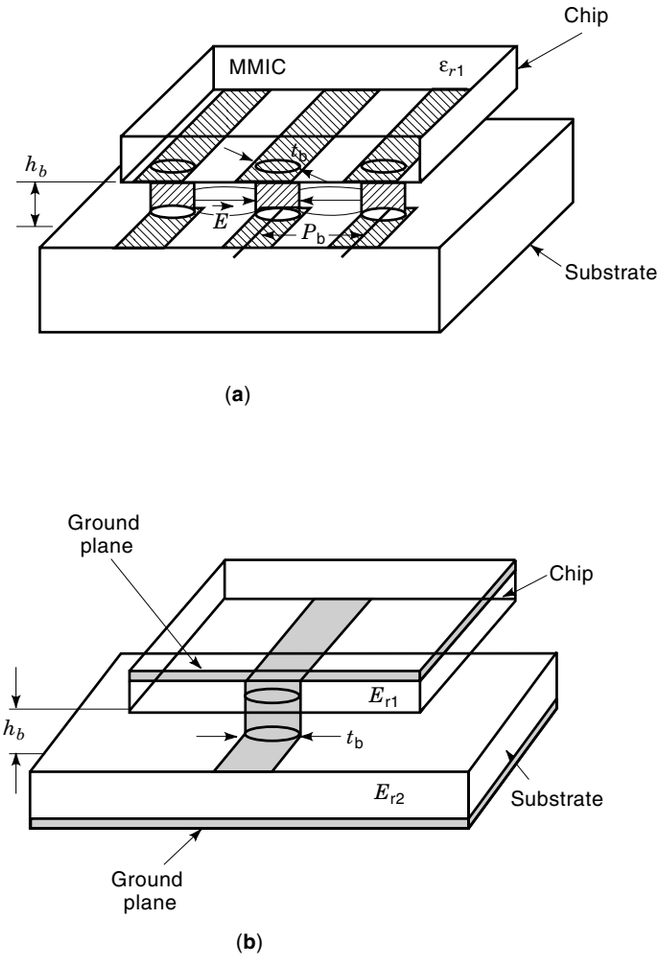


Figure 11. (a) Structure of flip-chip interconnect on a coplanar waveguide (CPW) with h_b as the bump height, P_b as the bump pitch, t_b as the bump diameter. Three solder bumps are needed for one RF and two ground connections. (b) Structure of flip-chip interconnect on a microstrip line. A single solder bump is needed for the RF connection. (From Ref. 19, © IEEE 1996, reprinted with permission.)

electric constants of the chip and the substrate. The change in line impedance for the flipped verse the unflipped case is larger than 5% for microstrip line on GaAs with width 254 μm and air gap 100 μm (20). When a CPW is used as the transmission line for MMICs, the fields in the CPW are well confined within the gaps on the CPW and narrower line widths and gaps are possible for a desired line impedance at the expense of higher transmission line loss. The change in the impedance for CPW on GaAs is less than 0.53% up to 50 GHz with the width 14.2 μm, gap 15.42 μm, and airgap 100 μm (20). As the air gap between the substrate and the chip is reduced, more field fringes into the substrate, which reduces the line impedance; the optimum air gap is about 100 μm for CPW with width 76.2 μm and gap 50.8 μm (20). For protecting the chip from the environment and for increasing the connection reliability, an underfill epoxy can be used for flip-chip interconnects. The effect of underfill for RF performance of chips has been reported (16,17,21). A lumped-element model of flip-chip joint is available (22).

Transmission Lines on Package Substrates. Microstrip line is widely used for MMICs and MCMs, but recently the CPW and coplanar strip (CPS) have been shown to be appealing alternatives. A brief discussion about microstrip line, CPW, and CPS is given below. Detail descriptions of these transmission lines are available in other articles in this encyclopedia.

Microstrip Line. The microstrip line is the most commonly used transmission line for MMICs; it is formed by a strip conductor of a width of W and thickness t, situated on the top side of a planar dielectric substrate and a ground conductor (see Fig. 12).

Given the dimensions of the microstrip line, the characteristic impedance can be calculated as (23):

$$Z_0 = \frac{60}{\sqrt{\epsilon_e}} \ln\left(\frac{8d}{W} + \frac{W}{4d}\right) \qquad \text{for } 1 \geq W/d$$

$$Z_o = \frac{120\pi}{\sqrt{\epsilon_e}[W/d + 1.393 + 0.667\ln(W/d + 1.444)]} \qquad \text{for } W/d \geq 1$$

where W is the width of the strip in microstrip line, d is the thickness of substrate, and ϵ_e is the effective dielectric constant of a microstrip line, which is given approximately by

$$\epsilon_e = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} \frac{1}{\sqrt{1 + 12d/W}}$$

where ϵ_r is the dielectric constant of the substrate.

Given characteristic impedance Z_o and dielectric constant ϵ_r, the W/d ratio can be found as

$$\frac{W}{d} = \frac{8e^A}{e^{2A} - 2} \qquad \text{for } W/d < 2$$

$$\frac{W}{d} = \frac{2}{\pi}\left[B - 1 - \ln(2B-1) + \frac{\epsilon_r - 1}{2\epsilon_r}\left(\ln(B-1) + 0.39 - \frac{0.61}{\epsilon_r}\right)\right] \qquad \text{for } W/d > 2$$

where

$$A = \frac{Z_0}{60}\sqrt{\frac{\epsilon_r + 1}{2}} + \frac{\epsilon_r - 1}{\epsilon_r + 1}\left(0.23 + \frac{0.11}{\epsilon_r}\right) \text{ and } B = \frac{377\pi}{2Z_0\sqrt{\epsilon_r}}$$

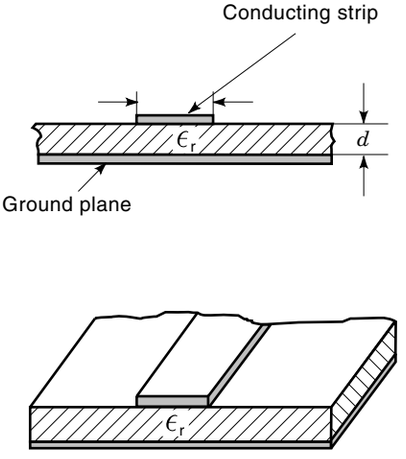


Figure 12. Geometry of a microstrip line with d as the substrate height, W as the width of the conducting strip, and ϵ_r as the relative dielectric constant of the substrate. The impedance of the line is determined by these three parameters.

Microstrip line is used for frequencies below 60 GHz with impedance ranging from 15 Ω to 120 Ω (24). Because the ground plane is usually fabricated on the backside of the chip or the component, it is necessary to fabricate via holes to connect ground bonding pads and the backside. Such via processing is expensive and susceptible to thermal mismatch-induced stresses.

CPW. The structure of a coplanar waveguide (CPW) is shown in Fig. 13. It consists of a signal conductor placed between two ground planes. All the three conductors are deposited on one side of a dielectric substrate. The dominant mode on a CPW is quasi-TEM at low frequencies (25). For an ideal case, when the ground planes are very wide relative to the slot spacing S and the dielectric substrate is much thicker than S, the characteristics of the CPW can be determined by conformal mapping techniques (25). The capacitance of the CPW is given by (25)

$$C = 4\epsilon_o \frac{(\epsilon_r + 1)}{2} \frac{K(\kappa)}{K'(\kappa)}$$

where $K(\kappa)$ and $K'(\kappa) = K(\kappa')$ are the complete elliptical integrals of the first kind. The modulus $\kappa = S/(S + 2W)$ with gap S and width of signal conductor strip W. Consequently, the characteristic impedance is given by

$$Z_0 = \frac{120\pi K'(\kappa)}{\sqrt{\epsilon_e} K(\kappa)}$$

Where ϵ_e is the effective dielectric constant for the CPW ($= (\epsilon_r + 1)/2$). Design equations for CPW with general dimensions are complex and available in Ref. 25, Section 2.1.4. Since the CPW is used in circuits with a higher integration density, attention has been paid to the effect of the distance between the top metal and CPW substrate and of the finite width of conductors on the line parameters (26).

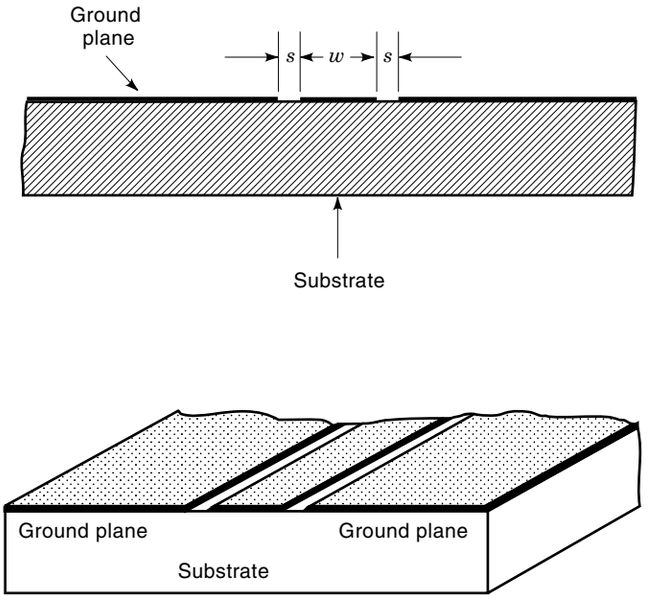


Figure 13. Structure of a CPW transmission line with W as the width of the center conducting strip and S as the spacing between the grounding plane and the center strip. The impedance of the line is determined by these two parameters and the effective dielectric constant of the substrate.

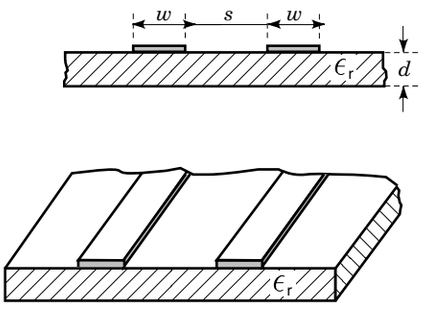


Figure 14. Structure of coplanar strip (CPS) transmission line with W as the width of each strip, S as the spacing between the strips, and d as the thickness of the dielectric substrate.

The principal advantages of CPW are (27): (a) easier construction using thicker substrates without via holes; (b) good grounding for integrated active devices; (c) compatibility with flip-chip assembly technology; (d) less radiation at discontinuities, low conductor loss in some cases, and less dispersion as compared with the microstrip line; and (e) reduced coupling between different lines in the same metallization layer (28). One of major problems with CPW is that a balanced coupled-slotline mode can be excited at nonsymmetric discontinuities. This mode can be avoided by incorporating grounding straps between the ground planes, using either air-bridges or underpasses (27). Number and optimum placing of ground straps are issues of design.

Coplanar Strips. A coplanar strip (CPS) transmission line consists of a pair of strip conductors of width W and separated by a narrow slot of width S on a dielectric substrate, as shown in Fig. 14 (29). As a balanced transmission line, it is ideally suited to balanced mixers and push–pull amplifiers. CPS has several advantages over conventional microstrip line and CPW (29). It facilitates shunting as well as series mounting of active and passive devices and eliminates the need for wraparound/via holes, which introduce additional parasitic elements. In short, CPS has all the advantages of CPW. In addition, CPS makes efficient use of the wafer area, so the die size per circuit function is small. This results in lower cost and larger number of circuit functions for a given die size. Also, CPS propagation parameters are independent of the substrate thickness beyond a certain critical thickness which simplifies heat sinking and circuit packaging. CPS does not require grounding, which is an appealing feature for high-density interconnects. However, the lack of design information has severely restricted its use. More important, transitions from CPS to microstrip/CPW in real applications are very difficult because CPS is a balanced line without a ground plane.

Multilayer Substrate. A multilayer substrate consists of thin dielectric layers and metal conductors formed on a wafer surface. These metal transmission lines and ground planes are connected through vertical via holes. Using multiple dielectric and metal layers, it is possible to get an increased flexibility in circuit layouts, reduce the package size, get more flexible means of interconnect, and maintain low cost. Since the ground plane is used between the signal layers, the crosstalk among the signal lines is reduced. A typical multilayer sub-

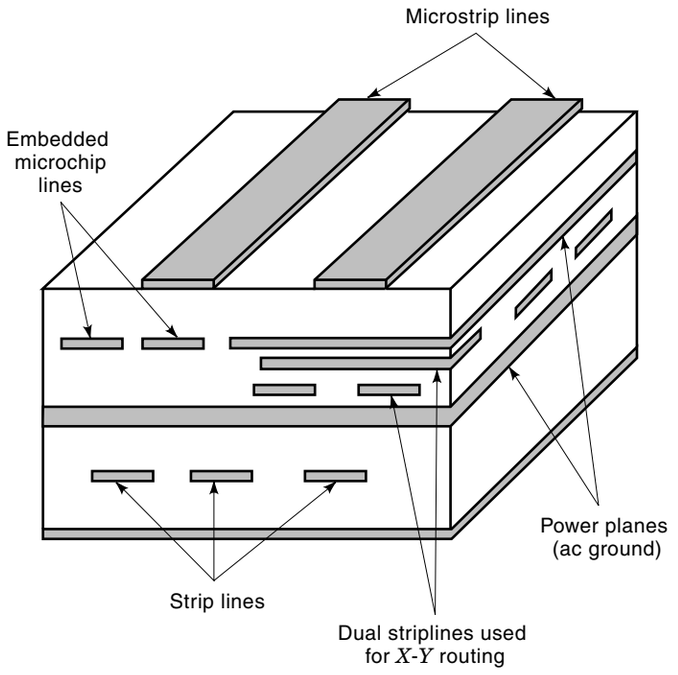


Figure 15. A typical multilayer substrate using microstrip lines and striplines as transmission lines. The substrate is used to interconnect RF packages or bare devices. (From Ref. 30, © ASME 1997, reprinted with permission.)

strate with microstrip lines and striplines (discussed later) is shown in Fig. 15 (30). Analysis methods for multilayer substrates can be found in Ref. 31. Additional discussions about the multilayer substrate will be presented later.

Crosstalk. When frequency increases, the signal energy is not confined to the transmission lines, but gets coupled from one line to others, including the dc power lines. Coupling generally occurs in an unintended manner. The energy can be coupled to undesired propagating modes in the complicated waveguide structure formed by the package. This can result in spurious resonances in the package housing. A signal that is unintentionally coupled to the neighboring lines is called *crosstalk,* a term derived from telephone networks, where faint conversations might be heard from other lines.

Crosstalk actually arises from both the distributed capacitive and the inductive couplings of approximately equal magnitudes (32). Although it may be easier to visualize the electric field of mutual capacitance between adjacent lines, it should be recognized that there is also a corresponding magnetic field coupling between the adjacent lines. When signal energy travels in one direction on the primary line, the portion of the signal coupled into the adjacent line travels in both directions. The magnetic coupling is important to understand the difference between the capacitive and inductive crosstalk at the two ends of a coupled line. The mutual capacitance coupling is in phase with the signal on the primary line at both ends. However, the inductively coupled lines are essentially the primary and secondary of a transformer due to mutual inductance coupling, although both sides of this transformer have only a single "turn." Therefore, the two ends of the inductively coupled secondary have opposite signal polarities (6). Practical circuits often consist of numerous lines, which may be in proximity. Hence the space between lines should be considered for design of microstrip, CPW, or other interconnects in a package. A typical method for reducing spurious coupling is to restrict the routing of conductor lines on adjacent layers to orthogonal directions, so that signals cross only at 90° angles and the coupling is minimized. Also, in the multilayer structure the dielectric layers should be optimized in order to minimize coupling between the lines (33). Grounded isolation lines, which convert the microstrip line into coplanar waveguide with finite size strips, can be used to reduced the coupling between lines in the same layer (26,34).

Housings for RF Packages. RF chips are generally enclosed in a package housing which is metallized on walls to shield the chips from outside EM fields. Because the package housing is almost completely metallized, it can be considered to be a rectangular metal waveguide cavity. Signal energy can be coupled to propagating modes in the complicated waveguide structure. Such a coupling may result in a resonance in the package with undesirable consequences such as power loss, poor isolation, and circuit instabilities. Therefore, package electrical performance is not only associated with the transmission line design and functions of chips, but also affected by package housing geometry and intrinsic material properties (4).

The resonance frequencies of the TE_{mnl} or TM_{mnl} modes in a rectangular enclosure without a dielectric substrate is given by (23)

$$f_{\text{mnl}} = \frac{c}{2\pi}\sqrt{\left(\frac{m\pi}{a}\right)^2 + \left(\frac{n\pi}{b}\right)^2 + \left(\frac{l\pi}{d}\right)^2}$$

where c is the velocity of light, a, b, and d are the dimensions of the cavity in x, y, and z directions, respectively. If $b < a < d$, TE_{101} model will be the dominant resonant mode with the lowest resonance frequency f_{101}. In RF packages, to improve end-to-end isolation and raise cavity resonance frequencies, a large cavity is divided into some subcavities, with partition walls surface mounted to the substrate and grounded with a row of vias (35). For example, an empty package housing of 27.94 mm × 53.85 mm has a resonance frequency of about 6.0 GHz. But the resonance frequency of the 27.94 mm × 14.22 mm empty housing is approximately 11.8 GHz. When a dielectric substrate is inserted in the package cavity, the resonance frequency of the cavity is modified. If the substrate is placed in contact with the bottom wall of the package and has a thickness much smaller than the height of the package, the modified resonance frequency f_r is given by (36)

$$f_r = f_{101}\left[1 - \frac{d}{b}\left(\frac{\epsilon_r - 1}{\epsilon_r}\right)\right]^{1/2}$$

where f_{101} is the resonance frequency for TE_{101} mode, d is the thickness of the substrate, b is the cavity height, and ϵ_r is the dielectric constant of the substrate. In the above formulas, the effect of chips, imperfect cavity end wall (for feedthroughs), and interconnections and passive circuits on the substrate on the resonance frequencies have not been considered. A full-wave simulation is needed to accurately predict the resonance frequencies of a package (35).

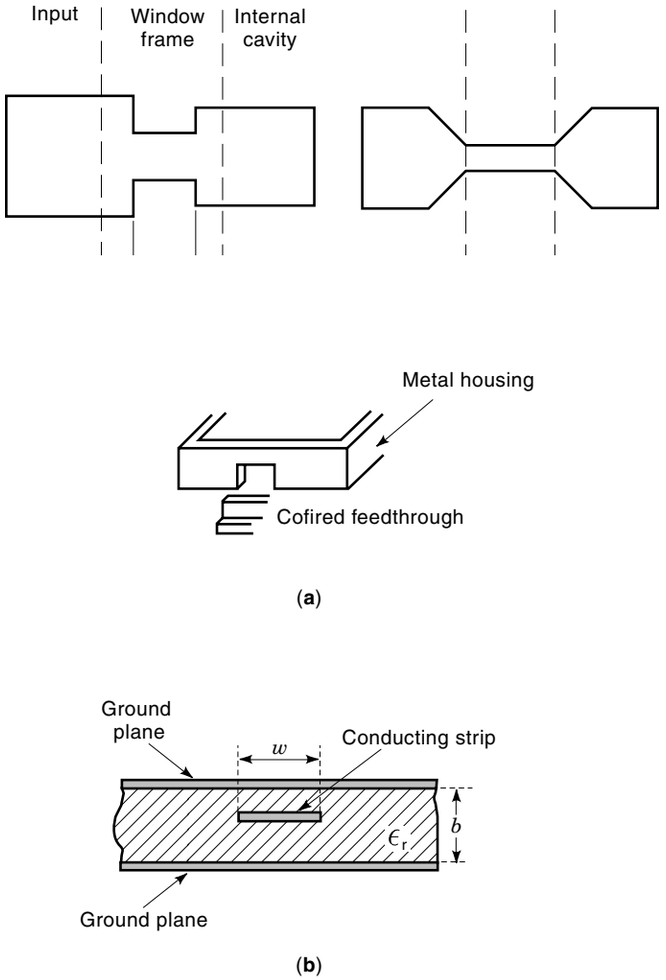


Figure 16. (a) Typical microstrip-stripline-microstrip feedthroughs. There are two different transitions to connect different line widths. The tapered transition has lower losses than those with the sharp transition. A typical configuration for the transition consists of the metal housing and the cofired feedthrough. (b) Cross-section of a stripline commonly used for a feedthrough. (From Ref. 2, © Artech House 1989, reprinted with permission.)

Feedthroughs/Ports in Housing. A design requirement of feedthroughs, which bring the signals through a package sidewall to external ports, is to provide controlled RF impedance and minimize the dc/RF losses. A stripline is used where a planar strip penetrates the dielectric filled hole in the metal wall. Given the desired characteristic impedance of the stripline, spacing between the ground planes b, and dielectric constant ϵ_r, the ratio of the strip width W to the spacing b [see Fig. 16(b)] is given as (23):

$$\frac{W}{b} = \frac{30\pi}{\sqrt{\epsilon_r} Z_0} - 0.441 \qquad \text{for } \sqrt{\epsilon_r} Z_0 < 120$$

$$\frac{W}{b} = 0.85 - \sqrt{1.041 - \frac{30\pi}{\sqrt{\epsilon_r} Z_0}} \quad \text{for } \sqrt{\epsilon_r} Z_0 > 120$$

Different microstrip-stripline-microstrip feedthroughs are shown in Fig. 16(a). Loss properties of the ceramic substrate and physical dimensions of the feedthrough structure could attenuate the high-frequency signal as it travels along the feedthrough. Microstrip-stripline-microstrip feedthroughs behave like low-pass filters. The cutoff frequency is determined by the physical, geometrical, and material properties of the structure (2,4). Coaxial feedthroughs can also be used for RF packages (2).

RF Multichip Module (MCM) Packages

Types of MCMs for RF Circuits. Multichip modules are substrates of dielectric and conducting layers, on which integrated circuits ("chips") and passive components (if any) are mounted directly on (or inside) the substrates, without separate packaging of each of the active components. That is, the chips are mounted "bare" onto the MCMs, which then provide the required power and ground, as well as all the signal interconnects and the electrical interface to the external environment. There are three kinds of MCMs: (1) laminate MCMs (MCM-Ls) are manufactured through the lamination of sheet layers of organic dielectrics. These MCMs exhibit very low line losses up to relatively high frequencies because the lines are thick and wide; however, the vias are typical quite tall and also much wider than the lines, thus causing substantial impedance discontinuities and signal reflections for frequency components above 500 MHz; (2) ceramic MCMs (MCM-Cs) are manufactured by stacking unfired layers of ceramic dielectric, onto which liquid metal lines are silk-screened using a metal ink process. The individual inked layers are then aligned, pressed together, and "cofired" at 800°C to 900°C, or 1500°C to 1600°C into a solid planar structure. Vias in these MCMs are also tall and wide, resulting in substantial impedance discontinuities and signal reflection for frequencies above 500 MHz; (3) deposited MCMs (MCM-D) are manufactured through the deposition of organic or inorganic dielectrics onto a silicon or alumina support substrate. After each dielectric layer is deposited, one of several techniques is used to pattern metal lines as well as metal "vias," which penetrate the dielectric layer to connect adjacent metal layers (7). The chips are then mounted on the upper surface using wire bonding/TAB or flip-chip bonding technology. In MCM-D, line cross-sections are smaller than those in MCM-C or MCM-L. The small cross-section results in higher resistive line losses. However, the via heights are quite small, and the via cross-sections are comparable to the linewidths, resulting in low levels of impedance discontinuity and signal reflections compared with the MCM-Ls and MCM-Cs.

Design Consideration

Multilayer Structure/Via for MCM. A multilayer structure is generally needed for an MCM. It is similar to the multilayer substrate for a single-chip package. Because there are more chips on a substrate, the multilayer substrate for an MCM is more complex than that for a single-chip package. Table 6 lists suggested number of layers for different design restrictions (7). A large number of layers is not desirable due to manufacturing difficulty; four layers are typically used. Vias, interconnects between layers, are lossy (particularly at high frequency) and difficult to model accurately.

Power/Ground Noise. Power/ground noise becomes important when circuits are more complex and there are more circuit signal planes sharing one ground plane. A comprehensive understanding of this noise is being developed (37–39). The

Table 6. Number of Layers Versus Design Restrictions (7)

Number of Metal Layers	Design Restrictions	Suggested Layer Assignments
1		
2	Digital systems up to 25–50 MHz; analog microwave designs using microstrip interconnects with no crossovers	1 Routing/attach; 1 shared power/ground plane
3	Digital system up to 50 MHz with split-plane power delivery; analog microwave designs using microstrip interconnects	2 Routing; 1 shared power/ground plane
4	Digital system up to 1 GHz; analog microwave system requiring microstrip and stripline interconnect.	2 Routing; 1 shared power; 1 ground plane
5	Digital system up to 2.5 GHz; most analog microwave systems	2 Routing; 1 shared power; 2 ground plane
6	Digital system up to 10–12 GHz; analog microwave systems up to 12–16 GHz.	2 Routing; 2 shared power; 2 ground plane
7	All digital and all analog or mixed signal designs are feasible	2 Routing; 1 routing/attach; 1 power plane; 2 ground planes; 1 integrated small capacitor and/or embedded resistor layer
8	All digital and all analog or mixed signal designs are feasible	2 Routing; 1 routing/attach; 2 power plane; 2 ground planes; 1 integrated small capacitor and/or embedded resistor layer

(From Ref. 7, © IEEE 1997, reprinted with permission.)

noise is not a set of random fluctuations caused directly by the state switching of the digital chips; but a complex resonance behavior of an essentially high Q circuit with a very large number of resonant modes, which are pumped by harmonic components in the state switching currents (37).

Many proposed next-generation analog or mixed-signal systems have been demonstrated to be exceptionally sensitive to noise in their power and ground planes (38). These resonances must be characterized for a complete understanding of this phenomenon. Further, suppression of the resonant modes, at least within the signal passband of interest, is required (38,39).

EMC/EMI Considerations for RF Packages

Electromagnetic compatibility (EMC) and electromagnetic interference (EMI) issues have been studied for some time. However, only very simple models to characterize EMC/EMI have been proposed (40,41). The conduction and radiation emission and susceptibility models are still at the component level, and need to be improved to reach the complexity level of real-world problems. The amount of EMI generated by a digital processor is directly related to the edge rates of the signals, the system clock rate, the total amount of switching current, and the size and shielding effectiveness of the device or system. Due to the complexity of an actual processor system, a combined deterministic and statistical approach is necessary to address these problems (7).

RELIABILITY

There are two issues related to RF package reliability. One is thermal management to control the temperatures of RF devices. The other is mechanical integrity to ensure reliable connections among different interfaces and low stresses in RF devices. Most thermal and mechanical considerations are the same as those for microelectronic packaging. However, there are unique requirements for RF packaging. These requirements are described in the following sections.

Thermal Management

Major thermal management challenges for RF packaging are associated with power MESFETs for transmitters. The unique requirements arise because of a very high heat flux.

- At high-frequency operations, power dissipation is high. A single GaAs FET (field effect transistor) is capable of delivering a CW (continuous wave) power output of 15 W at 10 GHz. When a few of these FETs are used along with other parts, this problem is compounded. For higher frequencies in the mm-wave spectrum, the combination of high-frequency and poor efficiency make thermal management a top packaging problem to solve. Heat flux higher than 300 W/cm^2 is not unusual (42), which is an order of magnitude higher than a high-power microprocessor's heat flux level.
- Thermal solutions have to meet constraints demanded by the selection of materials and structures for low-loss RF performance, reliable mechanical integrity, and cost. As shown in Tables 4 and 5, AIN has a high thermal conductivity but also high loss tangent and cost. In most cases, designers are not allowed to choose a high thermal conductivity material just for efficient heat removal.
- An RF device's electrical linearity and efficiency can strongly depend on its junction temperature. In some cases it is necessary to control the temperatures within a range rather than below an upper limit (43,44).
- GaAs, the major RF device material, is a poor thermal conductor. Its thermal conductivity of 50 W/mK (at room temperature) is low and can be even lower at high temperatures. For example, at 150°C, GaAs's thermal conductivity can be as low as 31 W/mK (43). With low-conductivity GaAs, the power dissipated from the FET cannot be spread effectively. As a result, the heat flux to be removed is close to FET level rather than "chip" level, as usually assumed for silicon-based microelectronic chips with the thermal conductivity around 150 W/mK at room temperature. In fact, wire bonded GaAs chips

should be thinned, in order to use conductive material to spread the heat from FET directly to the package.

Heat conduction, convection, and radiation are three typical heat transfer mechanisms. For RF packages, heat conduction and convection are usually considered. To analyze the detail temperature distributions in a package, numerical computation is necessary. However, simple analytical solutions can provide a quick estimation to gain an insight into a thermal problem to be solved. A few useful formulas are to be described below.

For one-dimensional (1-D) heat conduction through a component, for example, a plate, the thermal resistance is

$$R = \frac{L}{kA}$$

where L is the length of the component, A is the cross-sectional area of the component, and k is the heat conductivity of the component.

Similarly, for 1-D analysis, the thermal resistance corresponding to heat convection can be expressed as

$$R = \frac{1}{hA}$$

where A is the surface area subject to heat convection, and h is convection heat transfer coefficient. Typically, h can be assumed to be around 5 W/(m^{2}K) for natural air cooling and 20 W/(m^{2}K) for forced air cooling in a desktop personal computer (PC) environment.

When different 1-D components are thermally connected, a resistor network can be established to estimate their overall thermal performance. However, when two 1-D components with different cross-sections are connected, an additional thermal resistance, constriction resistance, needs to be considered. For instance, the additional thermal resistance for a circular heat source in contact with a heat spreader is

$$R = \frac{1}{2\sqrt{\pi} rk}$$

where k is the thermal conductivity of the thermal spreader, and r is the radius of the circular heat source. Examples of how to use these formulas to estimate thermal performance will be presented in the section entitled Case Study.

Plastic Packaging with Die Attachment. As stated by Pavio et al. (45), a plastic package enables source-to-ground assembly with semiconductor die. Thus, this arrangement supports the direct attachment of a transistor to the package heat sink (or actually a heat spreader). For the lower power devices (1 W to 2 W), the use of circuit board without additional heat spreading may be adequate. With increasing power levels, other options must be investigated. Figure 17 shows a die bonding to a conductive heat sink, for example, a Cu slug (42). Solder has to be used for thermally conductive die attachment, and the copper should be used for efficient heat spreading.

Ceramic Packaging with Die Attachment. Ceramics usually have a higher thermal conductivity compared with plastics

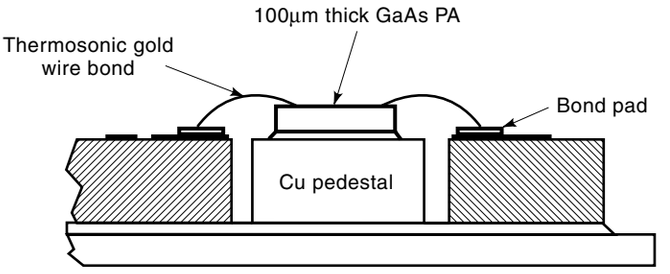


Figure 17. A typical packaging method for GaAs power amplifier chips using die bond to a heat sink and gold-gold wire bond. The heat sink connected to the copper (Cu) pedestal is used to extract heat divergently through the back of the power amplifier. (From Ref. 42, © IEEE 1989, reprinted with permission.)

and, in some conditions, can be directly used as heat sink. If the heat flux is very high, a more conductive heat spreader may be needed. For example, an AIN heat spreader can be inserted between a thinned GaAs chip and an alumina substrate, as shown in Fig. 18. More details on different materials for such heat spreading are to be discussed later on.

Flip-Chip Package. Flip-chip assembly is well known for its difficulty in removing heat from the chip. In fact, if the RF device is designed properly, the flip-chip assembly is thermally better than the wire bonded assembly. As shown by Gupta (42), the GaAs MESFET chips typically have a central active area of interdigitated source-gate-drain structures (Fig. 19), at which steady-state heat-dissipation densities of up to 300 W/cm^2 are encountered. The prevalent interconnect/packaging scheme for these power amplifier chips involves die bonding to a conductive heat sink, for example, a Cu slug (see Fig. 17). In order to remove intense heat through the die-bonded GaAs chip, additional care needs to be taken due to the poor thermal conductivity of GaAs. In order to extract heat divergently through the back of the power amplifier chip to the Cu pedestal on which it is die bonded, the die has to be thinned considerably (e.g., 50 μm) by back-grinding and chemical etching. Due to the brittleness of GaAs, this additional operation may involve yield loss after wafer fabrication.

Flip-chip interconnect is an alternative to the back-grinding of a GaAs chip. Because the active area of the GaAs chip is around the surface of the chip, flip-chip bumps can be used to directly remove the heat. In some conditions, where the power dissipated in the device is so high that the flip-chip

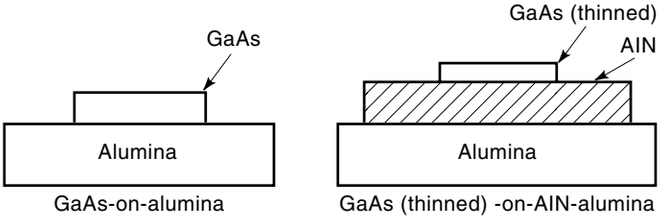


Figure 18. A high-conductivity AlN heat spreader used between thinned GaAs chip and alumina substrate to reduce thermal resistance. The AlN heat spreader has higher thermal conductivity and larger area than those of GaAs chip. Its insertion between the thinned GaAs and alumina reduces the thermal resistance between the heat source and heat sink.

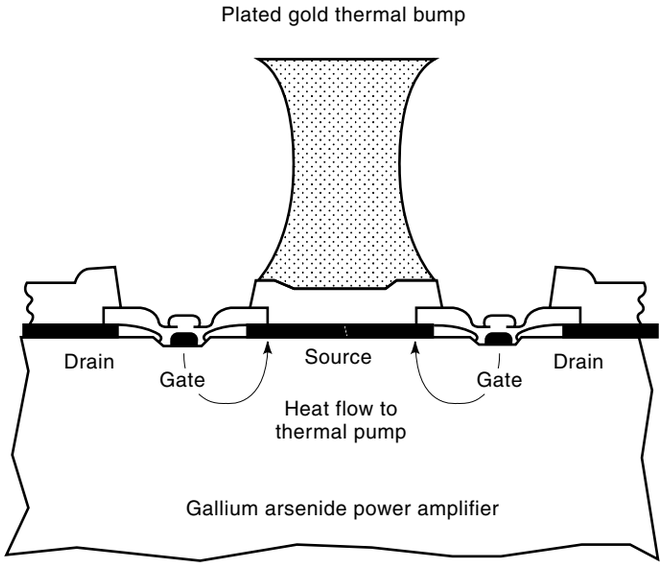


Figure 19. A gold-plated thermal bump on source fingers of a power amplifier. The thermal bump with high thermal conductivity is located close to the heat source and is directly connected to a heat sink. This bump greatly reduces the thermal resistance between the heat source and heat sink. (From Ref. 42 © IEEE 1989, reprinted with permission.)

bump may be not sufficient to remove the heat, a thermal bump has to be introduced to help remove the heat (Fig. 19). With a high thermal conductivity thermal bump (usually made by gold or silver), the thermal resistance from the GaAs chip to the heat sink substrate could be minimized.

Mechanical Integrity

Compared with microelectronic packaging, the mechanical integrity issues of RF packaging have the following unique features:

- The length scale of thermal mismatch is smaller. Typical sizes of RF chips and packages are smaller than those of microelectronic chips and packages. Therefore, thermal induced stresses/strains could be small.
- For efficient thermal management, mechanically poor materials have to be used for die attachment. For example, they may be highly conductive materials, such as solder, epoxy with added metal, or glass with added metal. In addition, any delamination could degrade heat conduction and increase temperature gradient across the die attachment. The increase could worsen the delamination and destroy the RF device.
- Mechanical solutions have to meet constraints demanded by the selection of materials and structures for low-loss RF performance, efficient thermal management, and cost. For example, underfill epoxy can enhance the fatigue life of flip-chip assembly using Duroid as the substrate (17). However, the epoxy could degrade the RF performance with additional losses. If these losses are not acceptable, an alumina substrate needs to be used for reliable assembly without the underfill epoxy.
- GaAs is the main RF device with poor mechanical properties: it is brittle and susceptible to cracking. With its poor thermal conductivity, a large temperature gradient in the device can result from high power dissipation and damage the device.

RF packages have different mechanical characteristics, as mentioned above. However, the trade-off design techniques are the same as those for microelectronic packaging. Delamination and fatigue are main concerns. These problems are well covered elsewhere, so only solder joint fatigue will be described briefly. Most discussions will focus on die cracking problem closely related to GaAs devices. The die cracking can occur at a die edge, at a via, and at a notch or a flaw due to stress concentration.

Solder Joint Fatigue. For a typical flip-chip assembly, the fatigue life of the solder joints is a major reliability concern. To estimate the solder fatigue life, numerical computation using finite element methods (FEM) is necessary. However, some simple formulas can be used to illustrate the fatigue problem and to quickly estimate the fatigue life. The Coffin-Manson relationship is popularly used to estimate the fatigue life of a solder joint in a flip-chip assembly with different thermal expansions of the chip and the substrate. It is expressed by

$$N_f = \frac{1}{2}\left(\frac{\Delta\gamma}{2\epsilon_{f'}}\right)^{-1/C}$$

where N_f is the fatigue life of the solder joint in terms of number of thermal cycles, $\Delta\gamma$ is total shear strain range, $\epsilon_{f'}$ is fatigue ductility coefficient (which is the maximum strain resulting in a failure in one cycle; it is approximately 0.325 for Sn/Pb eutectic solder), and C is fatigue ductility exponent (which is 0.442 for the eutectic solder). The shear strain range caused by mismatch of thermal expansions of the chip and the substrate can be estimated by

$$\Delta\gamma = \frac{L(\alpha_1 - \alpha_2)\Delta T}{h_C}$$

where L is the distance between the solder joint and the neutral point of the assembly, α_1 is the CTE (coefficient of thermal expansion) of the substrate, α_2 is the CTE of the chip, and h_C is the height of the solder joint.

From these formulas, it is clear that solder fatigue problem is caused by the mismatch between chip's and substrate's thermal expansions during thermal cycling with temperature changes. To avoid the reliability problem, there are typically three design approaches: (1) to choose a substrate with CTE matched to that of the chip, (2) to control the distance from the solder joint to the neutral position, or (3) to increase solder joint height. More details of the solder fatigue will be illustrated in the section entitled Case Study.

Cracking at a Die Edge. Solder is commonly used in RF die attachment because of its high thermal conductivity. Since the CTEs of die, solder, and substrate/heat sink are different, during thermal cycling, there is a large stress at the edge of the die. This stress, together with the imperfection of the die edge (caused by cutting), may result in a chip crack. Typi-

cally, there are vertical and horizontal cracks at the die edge. Vertical die cracks propagate under tensile stress and horizontal die cracks propagate under shear stresses at the edge. Horizontal edge cracks, developed from die-cutting damage, may propagate from the corner of the die to active chip elements and induce device failure. Or, it may propagate horizontally, causing the die to lift. Although die fracture is mainly governed by the size, shape, and defect locations in the die, voids in the attachment material or in the die-attach interface may also result in die fracture hyperturbing the thermal and stress transfer mechanisms (46). Lee and Matijasevic (47) developed a technique to produce void-free bonding between GaAs dice and alumina substrate using Au-Sn eutectic solder alloy, which reduced the possibility of chip crack greatly.

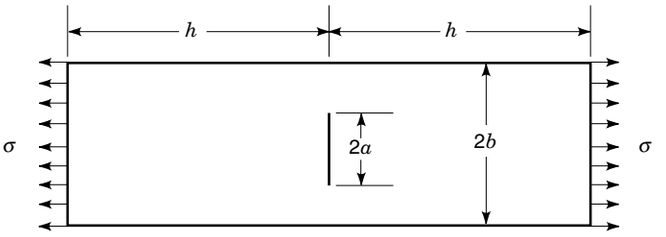


Figure 20. Plate of length $2h$, width $2b$, containing a central crack of length $2a$. Tensile stress σ acts in longitudinal direction and results in a stress intensity factor around the crack tip to be $K_0 = \sigma\sqrt{\pi a}$. When the stress intensity factor is higher than its critical value due to high stresses, the crack would propagate and break the plate.

Cracking at a Via. For the die attachment using solder, the capillary action causes the vias to fill with molten solder during reflow. Due to the thermal expansion mismatch between the Si/GaAs chip and solder, the chip may crack around vias during thermal cycling. The propagation of the crack could gradually damage the electrical performance of the device. Pavio (48) studied via cracking in a GaAs chip. The factors affecting the cracking are via size and shape. The problem can be eliminated by controlling the amount of solder which penetrates the via. A critical process window must be developed for each alloy to minimize the amount of solder filling the via, while maintaining sufficient coverage of solder die attachment for efficient thermal management. In addition, a small-size via can reduce the crack potential.

Cracking at a Notch or a Flaw on the Chip. Another cause for die cracking is the notches or the flaws on a chip. The fracture strength of brittle materials is dependent on several factors, the most important of which is the effect of stress concentration on notches and flaws. It is known from fracture mechanics that actual strengths for brittle materials will range 1/10 to 1/1000 of that predicted theoretically, because flaws act as stress concentrators. Fractures occur because a crack (flaw) propagates due to the decrease in stored elastic energy associated with crack extension, exceeding the increase in surface energy associated with the formation of new surface. The flaws on the chip are caused by wafer slicing and thinning, which can reduce the mechanical strength of the Si/GaAs chip. Hawkins et al. (49) and Vidano et al. (50) studied the fracture strength of Si and GaAs chip, respectively. They showed that mechanical thinning followed by chemical thinning (etching) can improve chip strength, because the size and population of flaws were reduced by the chemical thinning.

Notches are different from flaws. Notches are features of the design. For example, a sharp angle exists between any two bonded plates with different sizes. The sharp angle would cause stress concentration that could result in crack initiation in a brittle plate.

Crack Prediction. Cracking is a major concern when it comes to ensuring a RF package's mechanical integrity. Unfortunately, there is lack of knowledge of how to control this problem using a quantitative analysis. To characterize cracks initiated from flaws, the stress-intensity approach can be used. For the flaw shown in Fig. 20 the stress intensity factor is $K_0 = \sigma\sqrt{\pi a}$ (51).

For a notch as a designed feature, however, there is no well-established approach. Dunn et al. developed a new approach to characterize stress intensities in a notch for microelectromechanical systems (MEMSs) (52). Such an approach may be useful to understand cracks induced by stress concentration around a notch. In their study, they combined modeling, analysis, and experimental results to establish the crack criteria for a notch. They used the stress intensity factor K to study crack initiation. Cracks initiate for a given notch configuration when the stress intensity factor reaches a critical level K_{cr}. They found K_{cr} to be similar for a given notch angle and material regardless of other geometric factors. Their method may be used to predict crack initiation at flaws or notches.

CASE STUDY

This study illustrates a typical design procedure with a few key considerations for a RF package. The calculations are carried out using simple analytical solutions to get qualitative guidelines. Numerical computations may be needed for any quantitative designs.

Problem Definition

Figure 21 shows a flip-chip assembly with a GaAs chip soldered onto an alumina substrate. A metal wall encloses the assembly. CPW or microstrip lines can be used as the transmission lines on the substrate. Feedthrough is the transition from the substrate to the next level interconnects; it can be microstrip-stripline-microstrip or CPW-stripline-CPW. For CPW, there are three solder joints on each end of chip-to-substrate connection [see Fig. 11(a)]. For a microstrip line, there would be a single solder joint at each end [see Fig. 11(b)]. All the critical dimensions and material properties taken from Table 3 are listed below.

- Cavity enclosing the flip-chip package: the size is $a \times b \times d = 14.4 \times 6$ mm $\times$ 24 mm, where a, b, and d are housing dimensions in the x, y, and z direction, respectively.
- GaAs chip: thermal conductivity $k_{chip} = 48$ W/m°C, CTE (coefficient of thermal mismatch) $\alpha_{chip} = 6.1 \times 10^{-6}$ mm/

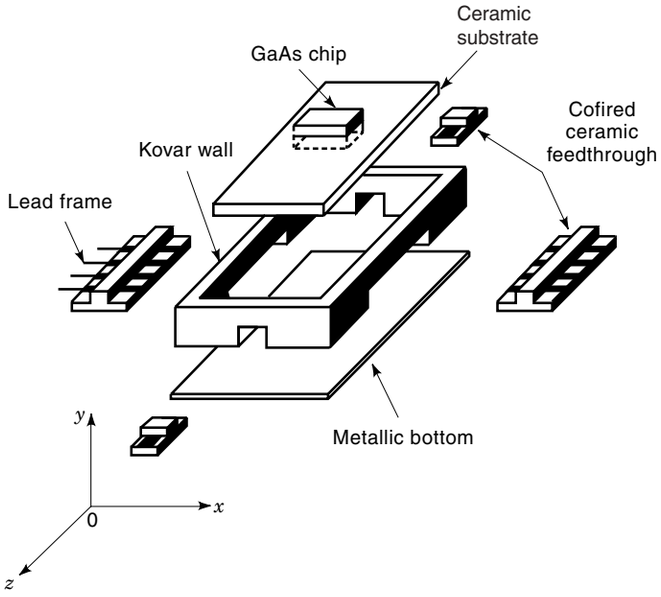


Figure 21. RF single chip package used in the case study. GaAs chip is flip-chip bounded on an alumina substrate with 6 solder joints for the case with a CPW and 2 solder joints for the case with a microstrip line. Feedthrough as shown is a microstrip-stripline-microstrip transition for RF signals. RF, thermal, and mechanical analyses are carried out in the case study to design the package.

mm°C, and size $L_{\text{chip}} \times W_{\text{chip}} \times t_{\text{chip}}$ = 4.7 mm × 1.13 mm × 0.625 mm.

- Ceramic substrate: $k_{\text{substrate}}$ = 20 W/m°C, $\alpha_{\text{substrate}}$ = 6.9 mm/mm°C, $L_{\text{substrate}} \times W_{\text{substrate}} \times t_{\text{substrate}}$ = 14.4 mm × 24 mm × 0.625 mm, dielectric constant ϵ_r = 9.8.
- Flip-chip solder joint: k_{joint} = 53 W/m°C, height H_{joint} = 75 μm, diameter of the circular pad d_{pad} = 150 μm (radius $r = d_{\text{pad}}/2$ = 75 μm), center-to-center distance of solder joints p_x = 4 mm and p_z = 0.46 mm.
- Air: k_{air} = 0.03 W/m°C.

A complete analysis would be very complicated since many packaging effects are coupled. RF, thermal, and mechanical designs are to be studied only to address the following questions: What are the RF losses of the interconnects for operating frequencies below 10 GHz? What is the lowest resonance frequency of the housing? What is the feedthrough design for smooth transition? What would be the junction temperature for the GaAs chip dissipating 0.8 W with the substrate cooled by air with the convection heat transfer coefficient h_{conv} = 20 W/m²°C and T_{air} = 25°C? What would be the fatigue life of the solder joints under thermal cycling from −25 to 125°C?

RF Design

Losses in Interconnect. From Fig. 9, the losses can be estimated for a CPW and its associated flip-chip solder joints. Using the same figure, the return loss is found to be less than 30 dB up to 8 GHz and the insertion loss could be found to be less than 1 dB. Such a loss is negligible if the GaAs chip has an amplifier with 10 dB gain.

Resonance Frequency of the Housing. The resonance frequency of the package housing can be calculated approximately by considering it as a rectangular waveguide cavity without a dielectric substrate. If dimensions shown in Fig. 22 are $b < a < d$, the dominant resonant mode (with lowest resonance frequency) is TE_{101}. Its corresponding resonance frequency can be calculated using the following formula taken from (23). For the dimensions: a = 14.4 mm, b = 6.0 mm, d = 24 mm, the resonance frequency for the lowest TE_{101} mode is about 12.1 GHz, which is calculated as below:

$$f_{\text{mnl}} = \frac{c}{2\pi}\sqrt{\left(\frac{m\pi}{a}\right)^2 + \left(\frac{n\pi}{b}\right)^2 + \left(\frac{l\pi}{d}\right)^2}$$

$$f_{101} = \frac{3 \times 10^8}{2 \times 3.1416}\sqrt{\left(\frac{3.1416}{14.4 \times 10^{-3}}\right)^2 + \left(\frac{3.1416}{24.0 \times 10^{-3}}\right)^2} = 12.1(\text{GHz})$$

where c is the speed of light, m, n, l are mode integers (1, 0, 1 for f_{101}).

However, with a dielectric substrate material located at the bottom of the housing, the resonance frequency should be modified. In this case, dielectric material is alumina with ϵ_r = 9.8 and thickness $t_{\text{substrate}}$ = 0.625 mm, the resonance frequency should be modified to be 11.5 GHz, which is calculated by using the following formula taken from (36):

$$f_r = f_c\left[1 - \frac{t_{\text{substrate}}}{b}\left(\frac{\epsilon_r - 1}{\epsilon_r}\right)\right]^{1/2}$$

$$f_r = f_{101}\left[1 - \frac{0.625}{6}\left(\frac{9.8 - 1}{9.8}\right)\right]^{1/2} = 11.5(\text{GHz})$$

where f_{101} is the frequency without the dielectric effect; b is the height of the cavity in y direction (see Fig. 21).

The dielectric substrate reduces the resonance frequency from 12.1 GHz to 11.5 GHz. In addition, the GaAs chip might cause another effect on the frequency. In this case, the chip is small compared with the housing, so the effect could be negligible. However, if the effect should be considered, for example, in the case of a multichip module, a full-wave simulation would have been conducted.

Feedthrough Design. A microstrip line is to be studied for this design consideration since it is the base transmission line for a feedthrough. For a CPW, it can be designed as a CPW-stripline-CPW transition (4) or CPW-shielded CPW-CPW transition (53). A full wave simulation is needed for CPW feedthrough structure design (53). A common feedthrough for a microstrip line is for the transition from a 50 Ω microstrip line to a 50 Ω stripline as shown in Fig. 16. To design a 50 Ω microstrip line on the alumina substrate with thickness $t_{\text{substrate}}$ = 0.625 mm and ϵ_r of 9.8, the width of the strip (W) can be calculated using a formula for $W/d < 2$ (23):

$$W = t_{\text{substrate}}\frac{8e^A}{e^{2A} - 2}$$

where

$$A = \frac{Z_o}{60}\sqrt{\frac{\epsilon_r + 1}{2}} + \frac{\epsilon_r - 1}{\epsilon_r + 1}\left(0.23 + \frac{0.11}{\epsilon_r}\right)$$

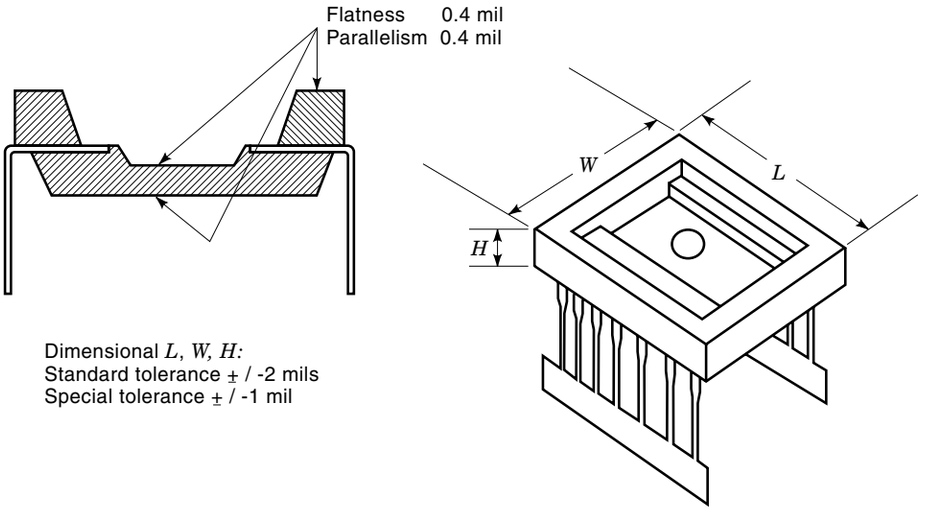


Figure 22. Premolded plastic package to increase applicable frequency. This package is different from typical injection-molded plastic packages with bond wires in air to control inductance variations. Bond wires are moved during the injection molding process; such movements are eliminated by the use of the premolded packages.

Hence, for this case:

$$A = \frac{50}{60}\sqrt{\frac{9.8+1}{2}} + \frac{9.8-1}{9.8+1}\left(0.23 + \frac{0.11}{9.8}\right) = 2.13$$

$$W = 0.625 \times \frac{8 \times e^{2.13}}{e^{2\times 2.13} - 2} = 0.61(\text{mm})$$

To design a 50 Ω stripline on the alumina substrate with the spacing between two ground planes $t_{\text{strip}} = 2t_{\text{substrate}} = 1.25$ mm and $\epsilon_r = 9.8$, the width of the strip (W) can be calculated as follows (23):

For $\epsilon_r Z_o > 120$

$$x = \frac{30\pi}{\sqrt{\epsilon_r} Z_o} - 0.441 = 0.16$$

$$W = t_{\text{strip}} \times (0.25 - \sqrt{0.6 - x}) = 0.23(\text{mm})$$

There is a clear mismatch between the width of the microstrip line (0.61 mm) and that of the stripline (0.23 mm). Typically, a taper section is used to connect these two transmission lines to decrease the return loss. The insertion loss of a typical feedthrough (a single microstrip-stripline-microstrip transition) can be less than 0.1 dB up to 20 GHz (4).

These three RF design considerations on interconnect losses, resonance frequency, and feedthrough are very critical to RF packaging. In addition, there are many other concerns that were discussed above. More general design methods are available in the literature (2,54–56).

Thermal Design

There are two approaches for thermal design. The simplest approach assumes no temperature gradients inside the GaAs chip. The substrate is cooled by air through convection heat transfer at the bottom surface; therefore, the main thermal path is from the chip to the bottom of the substrate through the solder joints. Its thermal resistance can be estimated using formulas described in the section on reliability/thermal management.

The thermal resistance of each solder joint is

$$R_{\text{joint}} = \frac{H_{\text{joint}}}{\pi r^2 k_{\text{joint}}}$$

For six joints, the thermal resistance is

$$R_{\text{joints}} = \frac{1}{6}R_{\text{joint}} = \frac{H_{\text{joint}}}{6\pi r^2 k_{\text{joint}}} = \frac{75 \times 10^{-6}}{6\pi(75 \times 10^{-6})^2 \times 53}$$
$$= 13(^\circ\text{C/W})$$

The thermal resistance of the air between the chip and the substrate is

$$R_{\text{air}} = \frac{H_{\text{joint}}}{(L_{\text{chip}} W_{\text{chip}} - 6\pi r^2) k_{\text{air}}}$$
$$= \frac{75 \times 10^{-6}}{(4.7 \times 10^{-3} \times 1.13 \times 10^{-3} - 6\pi(75 \times 10^{-6})^2) \times 0.03}$$
$$= 480(^\circ\text{C/W})$$

The thermal resistance of the substrate (as a heat spreader) is

$$R_{\text{substrate}} = R_{\text{constriction}} + R_{\text{conduction}} + R_{\text{convection}}$$
$$= \frac{1}{6}\frac{1}{2\sqrt{\pi} r k_{\text{substrate}}} + \frac{t_{\text{substrate}}}{L_{\text{substrate}} W_{\text{substrate}} k_{\text{substrate}}}$$
$$+ \frac{1}{h_{\text{conv}} L_{\text{substrate}} W_{\text{substrate}}}$$
$$= \frac{1}{12\sqrt{\pi} \times 75 \times 10^{-6} \times 20}$$
$$+ \frac{0.625 \times 10^{-3}}{14.4 \times 10^{-3} \times 24 \times 10^{-3} \times 20}$$
$$+ \frac{1}{20 \times 14.4 \times 10^{-3} \times 24 \times 10^{-3}}$$
$$= 31 + 0.09 + 145$$
$$\approx 176(^\circ\text{C/W})$$

So the total thermal resistance is

$$\begin{aligned} R_{\text{total}} &= \frac{1}{\dfrac{1}{R_{\text{joints}}} + \dfrac{1}{R_{\text{air}}}} + R_{\text{substrate}} \\ &= \frac{1}{\dfrac{1}{13} + \dfrac{1}{480}} + 176 \\ &= 12.7 + 176 \\ &\approx 189(^\circ\text{C/W}) \end{aligned}$$

With GaAs chip power dissipation at $Q = 0.8$ W,

$$\begin{aligned} T &= QR_{\text{total}} + T_{\text{air}} \\ &= 0.8 \times 189 + 25 \\ &= 176(^\circ\text{C}) \end{aligned}$$

The chip temperature is estimated to be 176°C with the air temperature at 25°C. This temperature is too high to be acceptable. To reduce the temperature, it is important to understand the roles of major thermal elements. The thermal resistance across the air gap (480°C/W) is very large compared with the resistance through the solder joint (13°C/W). For a GaAs chip without temperature gradients, that is, no heat conduction across the chip, the conduction through the air gap could be overlooked. On the other hand, the convection heat transfer results in a 145°C/W thermal resistance; it plays the dominant role for thermal design. The 20 W/(m^2°C) is a typical convection heat transfer coefficient for an air cooling system in a desktop personal computer (PC) environment. This value can be changed by using a heat sink, a different fan, or even different cooling medium such as liquid. If a small heat sink is added to double the surface area, it would reduce the chip temperature from 176°C to only 118°C, which may be acceptable for some applications. If this temperature is not acceptable or $T_{\text{air}} = 25$°C is not a good assumption because of higher inlet air temperature, additional thermal enhancement is needed. The enhancement can be accomplished by using a high thermal conductivity substrate to reduce the spreading resistance from 31°C/W to a lower value. Or, the convection can be further increased with more powerful air cooling or even liquid cooling.

The assumption of the chip without temperature gradients is reasonable for silicon chips; however, it may be unrealistic for a GaAs chip with a poor thermal conductivity. Let us calculate additional thermal resistance across the chip to understand this consideration. Assume the heat source is a line source dissipating at the center of the chip; the additional thermal resistance from the chip center to the solder joints can be roughly calculated as

$$\begin{aligned} R_{\text{chip}} &= \frac{1}{4}\frac{p_x/2}{t_{\text{chip}}(W_{\text{chip}}/2)k_{\text{chip}}} \\ &= \frac{4 \times 10^{-3}/2}{4 \times 0.625 \times 10^{-3} \times (1.13/2) \times 10^{-3} \times 48} \\ &= 30(^\circ\text{C/W}) \end{aligned}$$

where $P_x/2$ and $W_{chip}/2$ are for a quarter of the chip. The thickness t_{chip} of the GaAs is used to calculate the area for heat conduction. The $\frac{1}{4}$ is to convert the thermal resistance across a quarter of the chip into that across the entire chip. This additional thermal resistance is very large; it is the same as the spreading resistance in the substrate.

The corresponding total thermal resistance becomes

$$\begin{aligned} R_{\text{total}} &= 189 + 30 \\ &= 219(^\circ\text{C/W}) \end{aligned}$$

The highest temperature in the chip becomes

$$\begin{aligned} T &= QR_{\text{total}} + T_{\text{air}} \\ &= 0.8 \times 219 + 25 \\ &= 200(^\circ\text{C}) \end{aligned}$$

The junction temperature increases 24°C if poor GaAs conduction is considered. Of course, the above mentioned different enhancement schemes have to be adopted to reduce the junction temperature.

This simple calculation illustrates a key challenge to thermal design in RF packaging. GaAs is a poor thermal conductor, and concentrated heat sources in GaAs could cause a major thermal problem if they are located far from solder joints.

The calculation also shows how difficult it is to estimate an accurate junction temperature using one-dimensional formulas for a three-dimensional configuration. Sometimes, contributions of important thermal elements might be neglected by wrong assumptions. Numerical simulation is always preferred if accuracy is crucial.

Reliability Design

The formulas

$$\Delta\gamma = \frac{L(\alpha_1 - \alpha_2)\Delta T}{h_C}$$

and

$$N_f = \frac{1}{2}\left(\frac{\Delta\gamma}{2\epsilon_{f'}}\right)^{1/C}$$

are typically used to estimate the fatigue life of the flip-chip solder joints under thermal cycling. The life is strongly affected by the longest distance from the solder joints to the chip center (L), the mismatch between the chip's and the substrate's coefficients of thermal expansion (α_1–α_2), and the temperature change (ΔT) during thermal cycling. With the dimensions and properties given and the temperature changing from −25°C to 125°C, the shear strain is

$$\begin{aligned} \Delta\gamma &= \frac{\sqrt{\left(\dfrac{p_x}{2}\right)^2 + \left(\dfrac{p_y}{2}\right)^2}(\alpha_{\text{substrate}} - \alpha_{\text{chip}})\Delta T}{H_{\text{joint}}} \\ &= \frac{\sqrt{2^2 + 0.23^2} \times 10^{-3} \times (6.9 - 6.1) \times 10^{-6} \times [125 - (-25)]}{75 \times 10^{-6}} \\ &= 0.0032 \end{aligned}$$

The corresponding fatigue life the solder joint is

$$N_f = \frac{1}{2}\left(\frac{\Delta\gamma}{2\epsilon_{f'}}\right)^{1/C} = 0.5\left(\frac{0.0032}{2\times 0.325}\right)^{1/0.442} = 8.3\times 10^4\,(\text{cycles})$$

The fatigue life, that is, number of thermal cycles, is very high due to the very small mismatch between the chip and the substrate. However, it should be noted that the formula used might not be valid for the case studied. The formula is derived for a flip-chip assembly dominated by a global mismatch caused by a large CTE difference between the chip and the substrate. With a very small global mismatch of $6.9 - 6.1 = 0.8 \times 10^{-6}$ mm/mm°C in this assembly, the local mismatch between the solder and the GaAs chip may become the main failure cause. Unfortunately, there is no simple formula to estimate the fatigue life in a case strongly affected by a local mismatch. Numerical analysis is needed (57).

Although the 3.5×10^5 cycles predicted might not be accurate, the fatigue life is expected to be very high due to the very small global mismatch. If the substrate is changed to a polymer one, for example, Duroid (CTE = 14 mm/mm°C), the global mismatch is large and would reduce the fatigue life substantially. Under the same temperature range, the fatigue life with this large global mismatch can be estimated as follows:

The shear strain is

$$\begin{aligned}\Delta\gamma &= \frac{\sqrt{\left(\frac{p_x}{2}\right)^2 + \left(\frac{p_y}{2}\right)^2}(\alpha_{\text{substrate}} - \alpha_{\text{chip}})\Delta T}{H_{\text{joint}}} \\ &= \frac{\sqrt{2^2 + 0.23^2}\times 10^{-3}\times(14-6.1)\times 10^{-6}\times[125-(-25)]}{75\times 10^{-6}} \\ &= 0.032\end{aligned}$$

The corresponding fatigue life of the joint is

$$N_f = \frac{1}{2}\left(\frac{\Delta\gamma}{2\epsilon_{f'}}\right)^{1/C} = 0.5\left(\frac{0.032}{2\times 0.325}\right)^{1/0.442} = 450\,(\text{cycles})$$

The fatigue life is reduced substantially, and underfill epoxy might be used to enhance its reliability. However, underfill epoxy would affect RF performance due to the change of the effective dielectric constants of the surrounding materials. A RF design is needed to identify potential problems for this use. A good trade-off analysis can be found in (57).

The calculations were carried out using simple analytical solutions to review the basic design considerations. It is clear that qualitative guidelines could be obtained quickly. However, it is also clearly indicated that there are limitations of the formulas used. For a quantitative design, the designer must have a good background to select the right formulas for the estimation. Unfortunately, RF packaging involves many multidisciplinary considerations; it is very unusual to train a designer with such a background. Advanced CAD tool integrating RF, thermal, mechanical, and other considerations is critical to the design of RF package.

CAD ISSUES FOR RF PACKAGING

Two outstanding CAD issues in RF package design need to be addressed fully and resolved in the near future. The first one is the integration of the design of RF circuits with the design of the package used for housing the circuit. Design tools for RF and microwave circuits have reached a level of professional maturity in the past few years. However, the CAD tools for millimeter-wave circuit design (58) have yet to arrive at a similar level of maturity. Even for RF and microwave frequencies, at the current state-of-the-art, different approaches are used for simulation of circuits and for packages in which these circuits are housed. Network analysis–based software packages like Microwave Design System (MDS from HP) and Super Compact (from Compact Software Division of Ansoft Corp.) are used for circuit analysis. On the other hand, frequency-domain and time-domain electromagnetic simulation (EM) techniques (like HFSS and Momentum from HP, Em from Sonnet Software, Strata from Ansoft, and I3D from Zealand Software) are available for characterization of electronic packages at RF, microwave, and millimeter-wave frequencies. None of these approaches is, by itself, applicable for incorporating the effect of packages on performance of RF circuits, for designing of interconnects in the package assembly, or for design of passive embedded circuit functions in packages with multilayered dielectric substrates. Obviously, the network analysis approach, as such, cannot be applied to the RF package design; and three-dimensional field simulation approaches are not practical for analysis of complete RF circuit-package combinations because of impractical excessive computer memory and time requirements.

Two different approaches could possibly be used (and are being developed) for concurrent or integrated design of RF circuits and packages. The first one is based on network modeling of package effects (56,59–61). In this approach, the significant effects of the package on circuit performance are modeled in terms of equivalent network representations. Rigorous electromagnetic analysis (or approximate field analysis based evaluations) is used for these equivalent network model derivations. These equivalent network models are then used in RF network simulators for design of RF circuits incorporating the effect of package on circuit performance. An alternative to the equivalent network model is the derivation of artificial neural network (ANN) models for packages, trained by EM simulation of the package, that could be coupled to RF circuit design software tools. Use of ANN modeling has been successfully carried out for incorporating difficult-to-model circuit components in microwave design (62,63), but so far it has not been implemented for incorporating the effect of packages in RF circuit design. It is expected that the network or ANN modeling of package effects will be developed to a level appropriate for RF circuit designers to use it with commercially available RF circuit CAD tools.

The second approach for concurrent RF package and circuit design consists of using EM field simulators for package design and network simulators for circuit design (as is done separately now!) but linking the two simulators so that the design process can be carried out in an integrated manner. There have been some attempts (62–64) for interlinking diverse kinds of simulation tools. However, more of these have been directed toward analysis and design of integrated circuit–antenna modules. Design of integrated circuit–antenna modules is computationally similar to integrated package-circuit design. Just as package design needs to be based on EM field analysis (in contrast to the circuit design, which is based on network analysis), the design of antennas also needs EM

field analysis. Thus the computational techniques developed for concurrent circuit-antenna design (65) are conceptually applicable to integrated circuit-package design also.

The second issue in the design of RF packages is the need for integration of thermal and mechanical design considerations with the electrical design of packages. Incorporation of thermal vias in RF circuit chips can affect the RF performance. Shape and dimensions of flip-chip bumps in RF circuit affect both the mechanical reliability and RF performance (because of the inductance introduced by flip-chip bumps). Use of underfill epoxy in flip-chip modules can change the characteristic impedances and insertion losses of transmission lines of RF chips. These are a few of the examples illustrating how mechanical, thermal, and electrical issues can be interrelated in the design of RF packages. Thus the CAD of RF packages calls for some sort of functional integration of electrical, thermal, and mechanical design tools.

CAD of RF packages is a developing area of research and commercial implementation. We can look forward to the arrival of these CAD tools in the near future.

ADVANCED PACKAGING CONCEPTS

Trends in packaging may be described in categories based on combinations of power and frequency. Table 7 describes eight such regions from low RF/low power (A1) to millimeter-wave/high power (D2). These regions of applications will be used to discuss different advanced packaging concepts. New materials include high thermal conductivity and low-loss materials. New packaging approaches include premolded plastic package, packages with passive components, and flip-chip assembly. In addition, more challenging packaging technologies are being driven by new applications using active antennas, antenna arrays, RF photonics, RF microelectromechanical systems (MEMS), superconductors, and ferroelectric materials.

New Materials

High Thermal Conductivity Materials. There are instances where, although the total dissipation power requirement is low, devices have a heat concentrated area requiring local heat to be removed from a device surface. Thus aluminum nitride submounts with a surface-mount configuration might be suitable in this area. An AIN grade with lower conductivity around 75 W/mK can be used.

In the areas of high-power device packaging, thermal management is the predominant issue. The current heat-sinking materials have thermal conductivities between 150 W/mK (for AIN, CuW, and CuMoCu) to 350 W/mK (for Cu). Several studies are being pursued to investigate the development of diamondlike materials. Pure diamond has a thermal conductivity higher than 1000 W/mK. An alternative is to develop cost-effective solutions using composite materials. Composites with thermal conductivities over 400 W/mK are desirable.

Low-Loss Materials. Transmission loss, α_{total}, in high-frequency regions such as C1, D1, C2, and D2 is

$$\alpha_{\text{total}} = \alpha_r + \alpha_c + \alpha_d$$

where α_r is radiation loss dependent on package structure; α_c is conductor loss proportional to the length and inversely proportional to the square root of electrical conductivity; and α_d is dielectric loss proportional to loss tangent (tan δ). These loss components in packages become an issue in higher frequency regions such as C1 and D1 if the conducting path is long.

Materials development is required for ultra-low-loss tangent ceramics and plastics that are compatible with highly conductive line materials. Use of magnetic coupling to transfer electrical energy through dielectric materials without a conductive path can be used in the low-loss package solution in very-high-frequency regions such as C1, D1, C2, and D2.

New Packaging Approaches

Premolded Plastic Package. Currently, the plastic mold package is used in low-power regions at lower frequency (A1 and B1 regions). There are many attempts to increase the applicable frequency upward to the C1 region. Major issues in this area include wire bond inductance and control of the inductance. Thus the wire bonds must be in air, and this requires that a premold type of plastic should be used in this area, since it can create the necessary cavity structure in the package construction. An example of a premolded plastic package is shown in Fig. 22.

Flip-Chip Assembly. Various flip-chip applications are being developed, and flip-chip packaging is beginning to be utilized on the lower-power side. However, high-power applications demand new solutions. The flip-chip configuration has the disadvantage of taking heat out of the back side since heat dissipation is very limited through the solder-ball-bonded face. Without a proper design, thermal resistance could be very high. In addition, devices have to be redesigned. See the section on Reliability/Flip-Chip Package or Ref. 66 for details.

Package with Passive Components. For some RF packaging, the future trend is in integration of passive devices into the package. In regions A1 and B1 there are many functional integration schemes being used, such as integration of impedance matching and use of L, R and C filter functions within the package. The impedance-matching approach can reduce cost of the MMIC by fabricating matching circuits on the package instead of the MMIC. In some cases, the integration of passive components shown in Fig. 23 into the package

Table 7. Application Regions for RF Packaging

Frequency Range	Low RF 100 MHz–800 MHz	High RF 800 MHz–2 GHz	Microwave 2 GHz–30 GHz	Millimeter-Wave 30 GHz–100 GHz
Power low (mW–10 W)	A1	B1	C1	D1
Power high (>10 W)	A2	B2	C2	D2

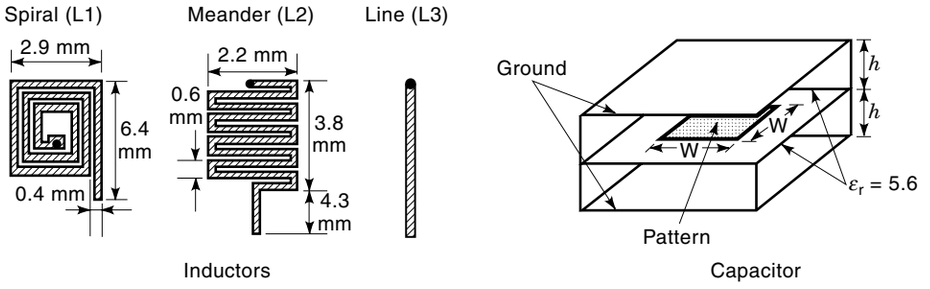


Figure 23. RF package with inductor and capacitor components integrated in a substrate. Such planar discrete components would reduce packaging costs. A large number of inductors and capacitors are commonly used as discrete components for RF modules. A high-density integration and batch processing of such planar components could result in a significant cost reduction.

could be easier and more cost-effective than integration into the active device.

New Applications

Active Antenna. As shown in Fig. 1, transmission lines interconnecting different RF devices are the limiting factors for RF performance. The trend for C1–D2 applications is to remove these lines by integrating RF devices and antennas into one active antenna. Figure 24 shows an active slot antenna modified from a design taken from Ref. 10. The package itself is the active antenna, requiring integrated considerations of antenna, electrical, thermal, and mechanical designs.

Antenna Arrays. For applications in D1 and D2, device efficiency is very poor, so power combining using a resonant antenna array is necessary. Figure 25 shows a design similar to a quasi-optical oscillator with frequency modulation obtained by a varactor array (67). In addition to power combining, new functionality can be created by manipulating phases of waves (68). Thousands of antenna elements are needed to achieve desirable functionality. The RF module is very complex and demands advanced MCM technologies.

RF Photonics. Another emerging area of integration is combination of optical and RF functions in devices and packages. RF characteristics of optoelectronic packages have already been identified as the major performance factors for gigahertz bandwidth. In addition, RF transceivers/optical transceivers can be integrated to form different module combinations for efficient transition between optical to wireless communication. Novel packaging concepts are being developed to accommodate this new challenging area.

RF Microelectromechanical Systems (MEMSs). MEMSs can be used to fabricate low-loss switches, high-Q tunable capacitor, integrated high-Q inductors, and microscale vibrating mechanical resonators (69–71). Through μm- or nm-level mechanical movements surrounded by air, the low-loss dielectric material, high-Q components could be designed and fabricated for applications in regions from C1–D2. Figure 26 shows RF switches using a thin diaphragm (1,69). In the mm-wave region, RF performance is very sensitive to μm-level movements. Such sensitivity used to be a major manufacturing problem. Using an MEMS, however, the sensitivity could be tuned for frequency-agile electronics (70). RF MEMSs are going to have an impact on low-cost, high-Q, frequency or phase adaptable filters, circulators, conformal and phased array antennas, oscillators, and phase shifters. For RF packaging involving MEMSs, there are new problems need to be overcome. For example, flip-chip assembly is the best approach to integrate MEMS with other RF devices and circuits;

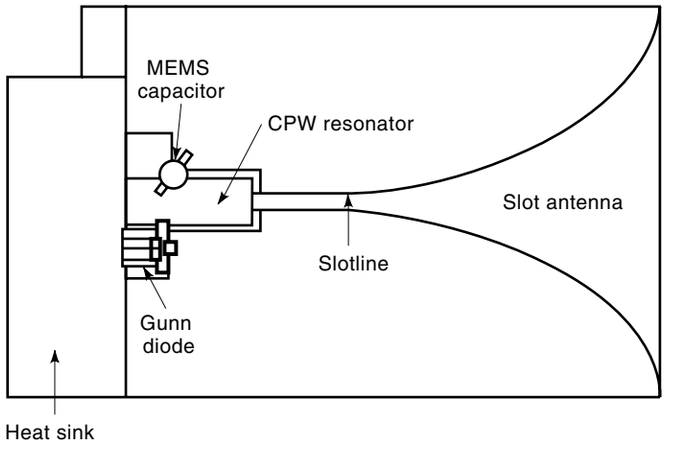


Figure 24. A tapered slot active antenna tuned by a variable capacitor. The device, transmission lines and antenna are integrated into a single module for high efficiency. The MEMS-based tunable capacitor could replace the varactor reported in Ref. 10 in order to enhance the quality factor (Q).

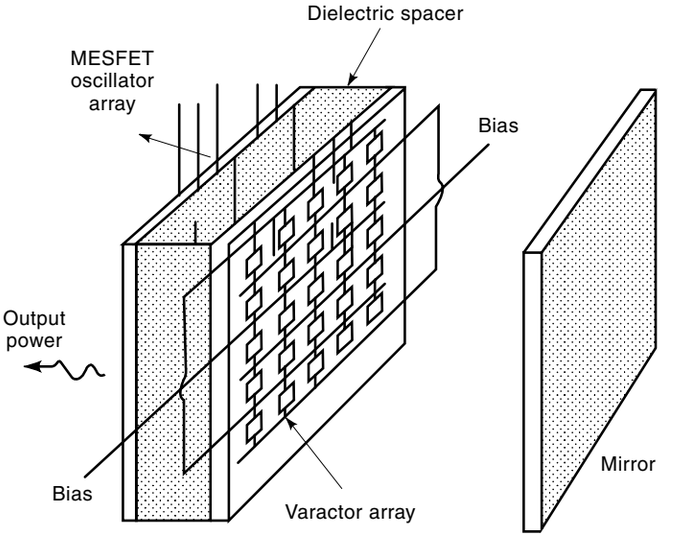


Figure 25. Quasi-optical oscillator with frequency modulation. This is an example to use an antenna array to enhance power transmission efficiency. The power transmission through grid resonance is an effective approach for power combining.

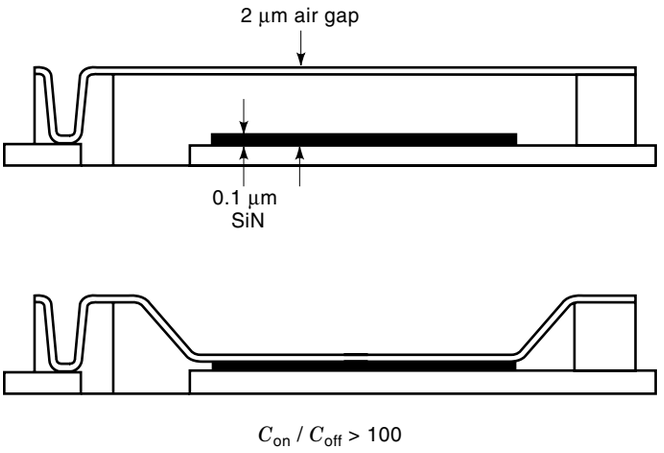


Figure 26. RF on/off switches using MEMS. The capacitance ratio between the air dielectric layer and the silicon nitride layer could reach 100. The switching is controlled by electrostatic forces. In addition to on/off switches, more complex MEMSs can be designed and fabricated for tunable capacitors, inductors and multiway switches. MEMS technologies can also be used to fabricate precise RF circuits and packages.

however, the silicon substrate used to fabricate MEMS has to be removed to achieve desirable RF performance (72).

Another interesting application of MEMS is the fabrication of RF circuits by silicon-based micromachining (73,74). In this application, bulk silicon can be used to fabricate waveguidelike circuit elements that simultaneously provide circuit function and package enclosures for MMIC and discrete components. Since silicon has good thermal conductivity, such structures are suitable for power devices. In addition, since air-filled cavities may be used to implement high-Q circuit elements, it is possible to fabricate many such circuits/packages out of an 8-inch (203 mm) wafer. This silicon-based micromachining technology is important to manufacture low-cost, precision circuits/packages for millimeter-wave applications.

Superconductor and Ferroelectric Materials. For very high-Q modules, superconductor and ferroelectric new materials can be used. The high-temperature superconductor makes it possible to build low-loss structure and the ferroelectric gives a voltage variable dielectric (75). The mixture of $Ba_{0.08}Sr_{0.92}TiO_3$ (BST) has shown to have both the desired large dielectric constant, for example, 17,000, and a large decrease in the dielectric constant, for example, 17,000 reduced to 6000, with an applied field of 25 kV/cm at 77 K. BST can be integrated with the superconductor $YBa_2Cu_3O_{7-x}$. (YBCO), because of the lattice match and chemical compatibility. The combinations have been used in a voltage-tunable oscillator, a phase shifter, and voltage-tunable phase array antenna system. In addition to typical issues for high-Q modules, the new materials and the new operation temperature at 77 K will demand very advanced RF packaging solutions.

SUMMARY

RF packaging is critical to the growth of applications of microwave and mm-wave modules and systems. The number of I/Os of RF packaging is not high; major packaging challenges result from two unique features:

1. Wide spectrum of operation frequencies ranging from kHz to hundreds of GHz
2. Packaging being a part of circuitry with strong effects on RF performance

This article reviews different RF single-chip and multichip packages, with an emphasis on their requirements that differed from those for microelectronics. It also discusses basic issues related to RF performance and package reliability in thermal management and mechanical integrity. To meet development needs, advanced packaging concepts are being created using new approaches and new materials. In addition, more challenging packaging technologies are being driven by new applications using active antenna, antenna arrays, RF photonics, RF microelectromechanical systems, superconductor, and ferroelectric materials.

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