J. Webster (ed.), *Wiley Encyclopedia of Electrical and Electronics Engineering*
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MULTICHIP MODULES

Today, it is practically impossible to spend a day without utilizing an electronic system, directly or indirectly. For example, electronic systems control the vast telecommunications network, and they also allow us to cook our food in a microwave oven. Microchips are connected together to form an electronic system. The electronic system is housed in a package. The electronic package provides support and protection to the system components. Moreover, the package provides means for signal distribution, heat dissipation, and power distribution to the internal components. The electronic package must be designed so that the system meets the specified quality, reliability, performance, and cost requirements (1,2).

A typical electronic system is made up of several levels of packaging, and each level of packaging has a distinctive type of interconnection technology. The interconnection hierarchy may be summarized as follows:

Level 0: Gate-to-gate interconnections on a single chip

Level 1: Die-to-chip package wires

Level 2: Printed wiring board (*PWB*) level of interconnection, where multiple packaged chips are connected together

Level 3: Connection between *PWB*s

Level 4: Connection between subassemblies to form a system

Level 5: Connection between systems, as in networks of computers

Each packaging level adds extra interconnection and interface circuitry. This introduces additional delay, thus degrading overall system performance. Furthermore, additional interconnections increase system power requirements and physical size (3,4).

Conventionally, bare die are packaged and then connected together on a *PWB*. Alternatively, bare die may be connected together on an interconnect substrate to form a multichip module (*MCM*). This bare-die–substrate module is then packaged and connected on to a *PWB*. The performance of an *MCM* may be much better than that of an equivalent system built from packaged chips connected on a *PWB*. The *MCM* derives its performance advantage by eliminating oversized drivers to support the chip–package pins and *PWB* wires, and by reducing signal propagation delay through using dense and high-performance interconnect substrates. The increased density and complexity in *MCM*s give rise to unique design, manufacturing, and test challenges.

This paper discusses various *MCM* types and design issues. In the next section, *MCM* types are discussed. The section after presents electrical design considerations. Then *MCM* thermal design and management are introduced. Finally, *MCM* test issues are covered.

Table 1. MCM Attributes

Attribute	MCM-L	MCM-C	MCM-D
Substrate	Printed wiring boards	Cofired ceramic, low-*E* ceramics	Low-*E* polymers, silicon on base
Material	Epoxy glass	Al_2O_3	Polyimide
Dielectric constant	2.8 to 4.5	4.5 to 10	2.6 to 4
Thermal dissipation	Poor	High	Moderate
Line width (μm)	75 to 750	90 to 125	12 to 50
I/O density	Low	Moderate	High
Cost	Low	Moderate	High

Types of Multichip Modules

*MCM*s are mainly differentiated by the interconnect substrate used to support and connect the bare die together. The four main types of *MCM* are *MCM-L*, *MCM-C*, *MCM-D*, and *MCM-V*. Table 1 lists several *MCM* attributes (5,6).

Multichip Module—Laminate (*MCM-L*). The *MCM-L* is essentially a laminated *PWB* scaled to meet *MCM* dimensions and requirements. The substrate is made from organic materials such as epoxy glass, on which copper conductors are formed on both sides; the resulting layers are laminated together. Interlayer electric contacts are provided by vias drilled prior to final lamination. The greatest advantage the *MCM-L* has is low cost due to existing infrastructure for high-volume *PWB* production. Furthermore, the technology has been in use for several years, and thus tested for its reliability. However, the *MCM-L* provides low routing density, poor thermal conductivity, high crosstalk, and moisture sensitivity.

Multichip Module—Ceramic (*MCM-C*). *MCM-C* technology utilizes ceramics, usually alumina, for the substrate, and multiple thick layers of screen-printed conductor pastes to provide signal interconnections. There are three main *MCM-C* technologies, namely, thick-film multilayer (*TFM*), high-temperature cofired ceramic (*HTCC*), and low-temperature cofired ceramic (*LTCC*).

In *TFM*, multiple levels of conductors are formed one layer at a time, separated by dielectric material. Interconnections are made using thick-film technology utilizing ink consisting of metal powder and organic binders that are screen-printed on ceramic substrates. Initial tooling costs for *TFM* are low, but the thick interconnects do not provide good density. In *HTCC*, individual layers are formed by screen-printing conductor material onto sheets of dielectric tape. Finally, the individual interconnect sheets are stacked, aligned, and laminated together under pressure and at elevated temperature. The finished module can have almost any number of layers, has good interconnect density, and has good thermal conductivity and low dielectric loss at high frequencies. In *LTCC*, sheets of dielectric are laminated to alumina substrates. The lower temperatures allow use of higher-conductivity interconnects such as gold, silver, and copper. However, the process is more expensive than that of *TFM* and *HTCC*.

Multichip Module—Deposit (*MCM-D*). *MCM-D* is fabricated by sequential deposition of conductor and dielectric substrate layers on a substrate base. The substrate base may be made of metal, ceramic, or silicon. The dielectric layer usually consists of silicon dioxide, a liquid polymer, or possibly a fluoropolymer. *MCM-D* provides low dielectric constants, dimensional accuracy, smallest feature sizes, lowest weight, and highest interconnect density. On the other hand, the process is expensive and is limited in the number of layers that can be deposited.

Multichip Module—Vertical (*MCM-V*). *MCM-V*, also known as 3-D interconnect, consists of chips stacked vertically (7). *PWB* and conventional *MCM* are 2-D entities, with chips or bare die connected together across an interconnect substrate. To further increase density, *MCM*s may be stacked on top of one another

with connections along the *Z* axis. 3-D stacking may involve stacked bare die, stacked packaged chips, stacked *MCM*s, or stacked wafers. Many vertical interconnection techniques are in use, and they are classified as:

Intrinsic interconnection by thin-film metallization
External interconnection:

- Leaded or leadless soldered edge conductors
- Glued with conductive epoxy
- Local connector
- Wiring

3-D packaging brings chips much closer together, thus reducing the interconnect length, which results in higher performance. Furthermore, reduced package size and weight are useful for many consumer and military applications. However, the increased density creates engineering challenges with respect to mechanical integrity and thermal management.

MCM-L, *MCM-C*, *MCM-D*, and *MCM-V* packaging are the four primary multichip packaging types. In practice, the differentiation between the types may not be so clear, and many hybrid variations exist. Designers must weigh cost against performance while meeting system requirements in order to select the proper *MCM* technology. *MCM* design requires many tradeoff studies (8). Often the primary goal is to maximize performance within given cost constraints. *MCM* electrical analysis aids in making overall performance predictions. The fundamental issues related to *MCM* electrical design are discussed in the next section.

Electrical Design

A multichip module consists of bare die connected together on an interconnect substrate. *MCM* package houses the die and substrate, and interfaces with the *PWB* through *MCM* package pins. Reduced dimensions and high density within a smaller area give *MCM* substrate interconnects a significant performance advantage. Superior interconnections and packaging allow *MCM*s to perform at higher frequency. However, increased performance also requires thorough understanding of electrical characteristics of the materials used and careful electrical design of the *MCM*. This section presents the fundamental elements involved in electrical design, phenomena affecting signals at high frequencies (such as transmission lines, skin effect and crosstalk), and finally issues related to power and ground (9,10,11).

Fundamental Considerations. Signals traveling in an ideal conductor can incorporate arbitrary frequencies without losing their strength or integrity. However, chip, *MCM*, and *PWB* interconnects use materials that are good but not perfect conductors. Interconnect parasitic properties that degrade the electrical signal are modeled as resistors, capacitors and inductors (12,13).

Current flow in conventional metals results from electron flow due to an applied electric field. However, the electrons do not travel unimpeded, because of resistance. The resistance R is given as a function of voltage V and current I by

$$R = V/I \qquad (\Omega) \tag{1}$$

The ohm (Ω) is the unit of resistance.

The resistance of an extended conductor is given by

$$R = \rho L/A \tag{2}$$

Table 2. Resistivity of Metals

Metal	Resistivity ($10^{-6}\Omega \cdot$cm)
Aluminum	2.73
Copper	1.73
Gold	2.27
Silver	1.63

where ρ is the resistivity of the material, L is the length of the conductor, and A is its cross-sectional area. Table 2 lists the resistivities of a few commonly used metals.

Capacitance is the charge-storing capacity of two conductors when voltage is applied between them. The farad (F), the unit of capacitance, represents the ability to store one coulomb of charge at a potential of one volt. Capacitance is defined in terms of the charge Q and the potential V between two conductors by

$$C = Q/V \qquad \text{(F)} \tag{3}$$

Interconnect capacitance is determined by interconnect dimensions, insulator dielectric constant, and insulator thickness. To first order the relationship for interconnect capacitance is

$$C = \varepsilon_0 \varepsilon_r wl/d \tag{4}$$

Where w is the interconnect width, d is the insulator thickness between interconnect and ground plane, l is the interconnect length, ϵ_r is relative dielectric constant of the insulator, and ϵ_0 is the permittivity of free space.

Inductance, in henrys (H), is defined as the ratio of the voltage across a conductor to the rate of change of current through it:

$$L = \frac{V}{di/dt} \qquad \text{(H)} \tag{5}$$

where V is the voltage, i is the current, and t is time. The inductance due to power and ground planes with currents of equal magnitude in opposite directions is given by

$$L = \mu_0 \, l \, h/w \qquad \text{(H)} \tag{6}$$

where l is the plane length, h is the separation between planes, w is the plane width, and μ_0 is the permeability.

The parasitic resistance and capacitance introduce signal delays. In *MCM*s, interconnect dimensions are small and the interconnect density is large, resulting in large parasitic capacitance. The signal propagation delay introduced by the parasitic resistance and capacitance is known as *RC* signal delay. At high frequencies, interconnects cannot be modeled by a simple *RC* delay model. Instead, they must be treated as transmission lines.

Transmission Lines, Skin Effect, and Crosstalk. Electromagnetic signals in the form of voltage and current travel along interconnections at roughly the speed of light reduced by a factor of the square root of the relative dielectric constant of the medium between the conductors. At low frequencies all parts of the conductor are approximately at the same voltage. However, at high frequencies, because of the finite speed of transmission, the voltages at different conductor locations will differ significantly. When the propagation time

of the signal becomes comparable to or greater than its rise time, the transmission-line effects become very important (14).

The circuit behavior is analyzed by treating the line as a series cascade of many segments, each short enough to be modeled as a simple lumped circuit element. For small interconnect length increment dx, the voltage $V(x)$ and current $I(x)$ along the line are given by the coupled transmission-line equations

$$dV/dx = -(i\omega L + R)I \tag{7}$$

$$dI/dx = -(i\omega C + G)V \tag{8}$$

where L, R, C, and G are the inductance, resistance, capacitance, and conductance per unit length, respectively. Here, ω is the angular frequency ($\omega = 2\pi f$). The resulting voltage waves are described by

$$V = V_{\mathrm{A}} e^{i(\omega t - kx)} + V_{\mathrm{B}} e^{i(\omega t + kx)} \tag{9}$$

where V_{A} is the amplitude of a wave traveling in the positive x direction and V_{B} is the amplitude of a wave traveling in the opposite direction. The *propagation constant* K is defined by

$$K = [-(i\omega L + R)\ (i\omega C + G)]^{1/2} \tag{10}$$

The current along the transmission line obeys a similar relationship. The *characteristic impedance* is given by

$$Z_0 = V_{\mathrm{A}}/I_{\mathrm{A}} = [(i\omega L + R)\ (i\omega C + G)]^{1/2} = -V_{\mathrm{A}}/I_{\mathrm{A}} \tag{11}$$

Characteristic impedance is not real impedance in the sense of resistance. A signal on a transmission line may have components at many frequencies traveling in both directions. Characteristic impedance describes a relationship that exists between those signal components. All the components are superimposed to make up the actual signal. The approximate propagation velocity of a signal along a transmission line is

$$V_{\mathrm{p}} = \omega/\mathrm{Re}\ K \tag{12}$$

In an *MCM* interconnect L, R, C, and G are nonzero. An imaginary component in the propagation constant means that signals can be transmitted for only a limited distance before their energy is dissipated. A frequency-dependent propagation velocity means that different Fourier components of the signal travel at different speeds and don't arrive at the destination in synchrony; this results in distorted signals.

The line resistance per unit length is mainly a function of the metal used for the line and its cross-sectional dimensions. The dielectric conductance per unit length is mainly determined by the insulation that isolates the line. A metal line is lossy if R is nonzero. The dielectric is lossy if G is nonzero. To maximize performance, the *MCM* interconnections should have the same characteristic impedance as the system-level interconnections.

At high frequencies, current concentrates in the skin of a conductor, the current density decreasing with increasing distance from the outer surface. The skin depth is defined as the depth at which the current density is 37% of the current density at the conductor surface. It is given approximately by

$$\delta = (\rho/\pi\mu f)^{1/2} \tag{13}$$

Table 3. Metal Skin Depths at 10 GHz

Metal	Skin Depth (μm)
Aluminum	0.81
Copper	0.66
Gold	0.79
Silver	0.64

where ρ is the conductor's resistivity, μ is its magnetic permeability, and f is the signal frequency. The skin effect generally becomes important at frequencies where $\delta \leq 0.3t$, where t is the conductor thickness. Table 3 lists δ at 10 GHz for commonly used conductors.

Mutual inductance and capacitance between signal conductors can cause crosstalk. Crosstalk is the electrical noise caused by a signal on a neighboring interconnect. If not controlled, crosstalk can create false signals on an interconnect, leading to system error. The maximum crosstalk allowed determines the minimum spacing between conductors, which in turn affects the *MCM* interconnect density. All parasitic elements and their effects discussed above directly influence the power supply distribution on an *MCM*.

Power and Ground. Multiple die are connected together on an interconnect substrate to build an *MCM*. Power and ground signals are brought in through the *MCM* pins attached to the *PWB*. The power and ground must be distributed on the *MCM* so that each chip, at all times, receives a steady current supply at a constant voltage. However, parasitics and nonuniform circuit switching make it very difficult to distribute power and ground for ideal voltage and current supply. In designing the die and interconnect substrate, issues like power dissipation, *IR* drop, current variation, coupling, and power distribution must be considered (15,16,17).

The average power dissipated by an *MCM* is given by

$$P_{\text{mcm}} = V^2 C f \tag{14}$$

where V is the supply voltage, C is the total capacitance, and f is the operation frequency. Power is distributed on the *MCM* and on the die through metal wires, which have finite resistance. Hence, the voltage (*IR*) drop will not be uniform across the *MCM* unless care is taken to ensure that all parts of the die and *MCM* are adequately connected to the VDD and VSS lines. However, not all circuits switch simultaneously and uniformly at all times. The current drawn from the supply will fluctuate from cycle to cycle and will vary across the *MCM*. Consequently, the VDD and VSS lines must be distributed so that each device receives a steady current supply with negligible *IR* drop. A common solution is to provide reference planes on the interconnect substrate. Reference planes are VDD and VSS plates across the complete interconnect substrate. The reference planes provide inductive and capacitive decoupling to reduce crosstalk and provide an excellent current return path, which minimizes inductive noise caused by signal switching. In addition, decoupling capacitors are added to the power supply lines on the *MCM* substrate to reduce current fluctuations.

To predict and meet performance goals, *MCM* electrical analysis must be done early in the design cycle. Materials used to build interconnect and devices are not ideal conductors, semiconductors, or insulators. Thus, the parasitics are modeled as resistors, capacitors, and inductors. At high frequencies, the parasitic device behavior becomes increasingly complex. Interconnects must be modeled as transmission lines. Skin effect and crosstalk also become prominent at high frequencies. Adequate *MCM* package pins and interconnect substrate wires must be appropriate to VDD and VSS to ensure that all *MCM* dies receive a steady and uniform power supply at all times.

Increased device and interconnect density and high frequency drastically increase the average power dissipated by the *MCM*. Excess power is diffused in the form of heat. The next section discusses issues related to thermal management on *MCM*s.

Thermal Management

Technological advances have reduced transistor sizes drastically, thus reducing the heat dissipated per transistor. However, application demands have increased the device density enormously. Consequently, the heat dissipated per unit area by a system has increased to levels where special methods are required to remove it. In *MCM*s the problem is further compounded because the device density per unit area is further increased, and miniaturization makes it more difficult to manage thermal flow. This section discusses the fundamentals of heat production and transfer and introduces selected methods to manage thermal flow (18,19,20,21).

A significant source of heat is the power supply used in systems where ac voltage is converted to various dc voltage levels. The I^2R losses in on-chip and substrate wiring generate heat. In each chip, energy is generated within 25 μm of the top surface. The heat flux averaged over time and chip surface area varies from 5 to 250 W/cm^2.

Increased temperatures can cause a variety of deleterious effects. The reverse saturation current of a *p–n* junction is directly proportional to temperature. Increased temperatures accelerate electromigration, corrosion, and interfacial diffusion, which lead to premature failures in metallization and bonded interfaces. The mean time to failure is decreased by a factor of 2 with 10% increase in temperature. Therefore, it is important to select proper materials and cooling techniques to meet *MCM*s' high power dissipation requirements.

Heat transfer is the movement of energy due to a temperature difference. Three modes of heat transfer are conduction, convection, and radiation. Conduction occurs within a continuous, stationary medium, solid or liquid. Convection occurs when surface is in contact with a fluid (liquid or gas). Radiation occurs when energy is exchanged in the form of electromagnetic waves.

A figure of merit (*FOM*) is used to compare the thermal efficiency of various *MCM* package and cooling strategies. The most commonly used *FOM* is the junction-to-ambient thermal resistance

$$\theta_{\mathrm{ja}} = \frac{T_{\mathrm{j}} - T_{\mathrm{a}}}{P_{\mathrm{c}}} \tag{15}$$

where T_{j} is the device junction temperature, T_{a} is the ambient temperature, and P_{c} is the chip power dissipation. A more realistic *FOM* normalizes θ_{ja} to the area packaging density of chips on the module:

$$\theta_{\mathrm{jaapd}} = \frac{T_{\mathrm{i}} - T_{\mathrm{a}}}{P_{\mathrm{c}}\ (A_{\mathrm{mod}}/N)} \tag{16}$$

where A_{mod} is the projected module area and N is the number of chips.

The principal cooling techniques are air cooling and liquid cooling. Air cooling is the most natural and common method of heat transfer. However, it effects are limited. Natural air flow may provide heat fluxes of roughly 0.05 W/cm^2 at 100°C; forced air using fans may increase it to 1 W/cm^2 at 100°C. Advanced forced convection methods involving finned sinks can achieve 1.5 W/cm^2 at 100°C.

Liquid cooling may be either single-phase or two-phase. *Single-phase* cooling is called *direct* if the liquid is in direct contact with the circuitry. *Indirect* liquid cooling involves liquid being separated from the circuitry,

which may result in loss of thermal efficiency due to the separation and additional material between liquid and circuit. In *two-phase* liquid cooling the method of delivery may be immersing the circuit in a pool of evaporating liquid, or forcing the flow of liquid over the heat-producing surfaces, or spraying liquid directly onto the heat source.

The thermal management problem is further aggravated in *MCM* by the increased circuit density per package. Innovative methods must be devised to remove heat from the active circuitry. Otherwise, excessive operating temperatures degrade circuit performance and may cause physical damage to the circuitry and the package. Therefore, in addition to cooling methods, *MCM* designers must design the circuits so that chip power dissipation is minimized.

Testing and Design for Testability

Chip and interconnect substrate fabrication are sophisticated processes involving many steps. A tiny defect in any step may cause the system to fail. A manufacturer must assure that the final system will operate flawlessly for many years. Thus, in order to screen defective parts, the chip, the interconnect substrate, and the final packaged *MCM* must be tested at several stages (22). This section discusses the issues involved in *MCM* testing, and the subsections cover the following topics: test cost, yield and defect level, electrical tests, faults and defects, and design for testability.

Test Cost. Ideally, every faulty component is identified and discarded before shipping it to a customer. However, given the complexity of multimillion-device *MCM*s, exhaustive testing within reasonable limits of time and cost is impossible. Therefore, test strategies must be developed that maximize the final system quality with acceptable cost. The cost of detecting a fault in an electronic component increases by a factor of ten at each level of system assembly (23). For example, if the cost of detecting a fault in an integrated circuit chip is $\$X$, then the cost of detecting that fault after the chip has been mounted on a board is $\$10X$, the cost of detecting it after the board has been installed in a system is $\$100X$, and the cost of detecting it after the system has been deployed in the field is $\$1000X$. Moreover, an undetected fault causing system failure may cause a fatal accident. To be cost-effective, testing must be considered from the beginning of the *MCM* design process and throughout the design cycle (24). Probability and statistics are employed to gauge the final system quality.

Yield and Defect Level. The *process yield* is the number of parts accepted as good after completing the process divided by the number of parts that entered the process and is given by

$$Y = P \times 100\% \tag{17}$$

where P is the probability that the part is defect-free. *MCM* yields depend on defects in the dies, the interconnect substrate, and the final assembly. Thus, the *MCM* yield is given by

$$Y_{\mathrm{mcm}} = Y_{\mathrm{c}}^{n} Y_{\mathrm{s}} Y_{\mathrm{i}}^{m} Y_{\mathrm{a}} \tag{18}$$

where n is the number of chips on the substrate, Y_{c} is the individual chip yield, Y_{s} is the substrate yield, m is the number of interconnects per substrate, Y_{i} is the interconnect yield, and Y_{a} is the assembly yield.

The bare dies are the most complex entities on the *MCM*. Conventionally, for *PWB* systems, the dies are packaged before they undergo thorough testing. The packaged pins provide adequate controllability and observability to allow acceptable testing. However, in an *MCM* the bare dies are not packaged, thus compounding test complexity. Consequently, extra care must be taken to ensure a *known good die* (*KGD*) (25).

The *quality* of a product is the probability that it is fault-free. Parts cannot be tested exhaustively; therefore, faults may escape undetected. The *defect level* (*DL*) is the fraction of defective parts escaping into the field:

$$\mathrm{DL} = \frac{\text{faulty parts passing test}}{\text{total parts passing test}} \tag{19}$$

A common expression to estimate an *MCM*'s defect level is

$$\mathrm{DL}_{\mathrm{mcm}} = 1 - Y_{\mathrm{mcm}}(1 - \mathrm{FC}) \tag{20}$$

where Y_{mcm} is the *MCM* process yield, and FC is the fault coverage of the tests applied (26,27). The first step towards achieving high fault coverage is identifying all types of defect that may occur in an *MCM*. Secondly, techniques to stimulate the parts so that the defects manifest themselves must be developed.

Electrical Tests. The basic types of electrical test methods are dc parametric, ac parametric, and functional.

Dc parametric tests verify the non-time-varying analog voltage and current values at the device electrical connections. These tests are applied at various conditions of electrical loading, temperature, and power supply voltage to verify device operation over the full operating range.

Ac parametric tests measure device signal timing relationships and values. Among these, *propagation delay tests* measure the time interval required for a signal to travel from an input to a specified output. *Setup tests* verify that a specified input signal is valid at a certain time before asserting a second signal. *Hold tests* verify that a specified signal output remains valid until after an input signal is asserted. Ac tests also measure pulse width and frequency.

Functional testing verifies that the device performs its intended function. *Static tests* check the circuit logic at lower than rated operating speed. *Dynamic tests* verify the circuit logic and the signal timing. However, dynamic tests are not performed at speed. *At-speed tests* verify the circuit at the rated device operating speed.

When not switching, CMOS circuits draw negligible leakage current. However, certain defects may cause CMOS devices to draw measurable quiescent current flow. I_{DDQ} testing is performed by measuring the current after the inputs have changed state and prior to the next input change.

Fault Models. Physical defects can be modeled as logical faults whose effects approximate the effects of common actual faults. These fault models are used to specify well-defined representations of faulty circuits that can be simulated (28,29). Fault models are also used to generate test patterns. Typical faults in circuits are stuck-at faults, opens, and shorts. The *fault coverage* of a set of patterns is its ability to reveal the modeled faults.

A fault causing a path in a circuit to be stuck at logical 1 or logical 0 is termed a *stuck-at fault*. To make test generation computationally tractable, the *single-stuck-at-fault* model assumes that a circuit can only have a single fault. *Short circuits* are modeled as bridging faults. Bridging-fault models assume that the effect of a short is to create a logical AND or a logical OR. Sometimes, bridging faults can convert a combinatorial circuit into a sequential one. A delay fault causes signals to propagate slower than normally. The fault may manifest when the path is sensitized and the output cannot keep up with the clock rate. A fault is detected by stimulating the part inputs and observing the resulting behavior.

Thus, to achieve high fault coverage, an *MCM* must have excellent controllability and observability. However, given submicrometer device and interconnect feature sizes, it is necessary to add circuitry to make the part more testable.

Design for Testability. Test generation, fault coverage estimation, test vector count, test time, and test equipment resolution affect overall *MCM* testability. To enhance a circuit's controllability and observability,

additional features such as a scan path, built-in self-test, boundary scan, and test access ports are included in the *MCM* die (30,31).

The circuit memory elements are configured into a shift register to form a scan path. This allows a sequential circuit to be partitioned into combinatorial subcircuits. Test patterns are shifted into the scan path, and for a single cycle the stimulus is allowed to ripple through the combinatorial subcircuit, and the results are captured by the memory elements at the subcircuit output. The results are then shifted out via the scan path and examined externally by the tester. Built-in self-test (*BIST*) employs circuits such as linear feedback shift registers (*LFSR*s) to generate test vectors on the chip itself. The results are fed into another on-chip *LFSR*, and the final signature at the end of the test should match a predetermined pattern (32). Using *BIST*, subcircuits on chip may be tested at speed.

Boundary scan cells are memory elements placed at the chip I/O. They can also be connected together to form a shift register to scan in test vectors and to scan out the results. Using the boundary scan register, the connections between the *MCM* dies may be tested. Test access ports (*TAP*s) such as the IEEE 1149.1 standard provide access and control of all test circuitry on a chip. Furthermore, the *TAP* provides a standard test interface between the dies on the *MCM* and the external test equipment (33,34).

Design for testing (*DFT*) features provide excellent controllability and observability, which facilitate testing to achieve high fault coverage. However, the test circuitry requires additional hardware, causing the die size, and hence the total *MCM* cost, to increase. In addition, the test circuitry adds delay to the circuit paths, causing slight performance degradation. Therefore, tradeoff studies must be made to provide maximum test coverage within given cost and performance constraints.

As device feature sizes drop, chip complexity increases. Consequently, test complexity also increases. In *MCM* the use of bare dies compounds the problem by reducing controllability and observability. The application requirements will drive the test cost. However, strict process control can maximize the process yield and hence reduce the defect level for a given fault coverage. To achieve high fault coverage it is necessary to understand all defect types, model the defects, generate efficient test vectors, and use *DFT* to maximize controllability and observability.

In summary, the dense interconnects and bare-die connections provide superior *MCM* performance and reduced size in comparison with *PWB* designs. The interconnect substrate material defines the *MCM* type. Increased density and high frequency of operation require thorough electrical design. Issues such as transmission-line effects, skin effect, crosstalk, and power–ground distribution must be given careful consideration. In an *MCM*, increased complexity within reduced area drastically increases the heat dissipated per unit area. Improper heat dissipation may adversely affect system reliability and may degrade performance. Therefore, thermal management is a critical issue in *MCM*s.

Before field use, an electronic system must be defect-free. Thus, an *MCM* must be thoroughly tested within the cost constraints.

Finally, use of bare dies and dense interconnect substrates reduces overall *MCM* testability due to inadequate controllability and observability. Therefore, *DFT* circuits are added to improve fault coverage.

BIBLIOGRAPHY

1. W. D. Brown (ed.) *Advanced Electronic Packaging*, New York: IEEE Press, 1999.
2. R. R. Tummla E. J. Rymaszewski A. G. Klopfenstein *Microelectronics Packaging Handbook Part I*, New York: Chapman & Hall, 1997.
3. P. E. Garrou I. Turlik (eds.) *Multichip Module Technology Handbook*, New York: McGraw-Hill, 1998.
4. D. P. Seraphim R. Lasky C.-Y. Li *Principles of Electronic Packaging*, New York: McGraw-Hill, 1989.
5. D. A. Doane P. D. Franzon (eds.) *Multichip Module Technologies and Alternatives: The Basics*, New York: Van Nostrand Reinhold, 1993.

6. A. Iqbal et al. Design tradeoffs among *MCM-C*, *MCM-D* and MCM-D/C Technologies, *IEEE Trans. Compon. Packag. Manuf. Technol. B, Adv. Packag.*, **17**(1): 22–29, 1994.
7. S. F. Al-Sarawi D. Abbott P. D. Franzon A review of 3-D packaging, *IEEE Trans. Compon. Packag. Manuf. Technol. B, Adv. Packag.*, **21** (2): 2–12, 1998.
8. G. A. Katopis W. D. Becker S/390 cost performance considerations for *MCM* packaging choices, *IEEE Trans. Compon. Packag. Manuf. Technol. B, Adv. Packag.*, **21** (8): 286–297, 1998.
9. H. B. Bakoglu *Circuits, Interconnections and Packaging for VLSI*, Reading, MA: Addison-Wesley, 1990.
10. A. Deutsch Electrical characteristics of interconnections for high-performance systems, *Proc. IEEE*, **86** (2): 315–357, 1998.
11. R. R. Tummala Multichip packaging—a tutorial, *Proc. IEEE*, **80** (12): 1955–1964, 1992.
12. C. S. Chang Resistive signal line wiring net designs in multichip modules, *IEEE Trans. Compon. Packag. Manuf. Technol. B, Adv. Packag*, **16** (8): 909–918, 1993.
13. C. T. Tsai Package inductance characterization at high frequencies, *IEEE Trans. Compon. Packag. Manuf. Technol. B, Adv. Packag.*, **17** (2): 175–181, 1994.
14. C. W. Davidson *Transmission Lines for Communications*, London: Macmillan, 1978.
15. G. A. Katopis Delta-I specification for high performance computing machine, *Proc. IEEE*, **73** (9): 1403–1415, 1985.
16. R. Senthinathan J. L. Prince Simultaneously switching ground noise calculation for packaged CMOS devices, *IEEE J. Solid-State Circuits*, **26** (11): 1724–1726, 1991.
17. R. Downing P. Gebler G. Katopis Decoupling capacitor effects on switching noise, *IEEE Trans. Compon. Hybrids Manuf. Technol.*, **16** (5): 484–489, 1993.
18. A. D. Kraus A. Bar-Cohen *Thermal Analysis and Control of Electronic Equipment*, New York: McGraw-Hill, 1983.
19. R. Darveaux, et al. Thermal stress analysis of a multichip package design, *IEEE Trans. Compon. Hybrids Manuf. Technol.*, **12** (4): 663–671, 1989.
20. M. Mahalingam Thermal management in semiconductor device packaging, *Proc. IEEE*, **73** (9): 1396–1404, 1985.
21. A. Bar-Cohen Thermal management of air- and liquid-cooled multichip modules, *IEEE Trans. Compon. Hybrids Manuf. Technol.*, **10** (2): 159–169, 1987.
22. M. Abramovici M. A. Bruer A. D. Friedman *Digital Systems Testing and Testable Design*, New York: Computer Science, 1990.
23. P. Singh D. L. Landis Test cost vs quality: Cost effective testing in electronic systems and subsystems, *ISSAT Proc. Int. Conf. on Reliability and Quality in Design*, 1994, pp. 389–393.
24. M. Abadir Economic modeling of multichip modules testing strategies, *IEEE Trans. Compon. Packag. Manuf. Technol. B, Adv. Packag.*, **21** (11): 360–370, 1998.
25. J. Hagge R. Wagner High yield assembly of multichip modules through known good IC's and effective test strategies, *Proc. IEEE*, **80**: 1965–1994, 1992.
26. T. W. Williams N. C. Brown Defect level as a function of fault coverage, *IEEE Trans. Comput.*, **30** (12): 987–988, 1981.
27. P. Singh D. L. Landis Optimal chip sizing for *MCM*, *IEEE Trans. Compon. Packag. Manuf. Technol. B, Adv. Packag.*, **17** (3): 369–375, 1994.
28. K. M. Butler M. R. Mercer *Assessing Fault Model and Test Quality*, Norwell, MA: Kluwer, 1992.
29. W. Maly Tutorial: Realistic fault modeling for VLSI testing, *Proc. 24th Design Automation Conf.*, 1987, pp. 173–180.
30. T. W. Williams K. P. Parker Design for Testability—A Survey, *IEEE Trans. Comput.*, **31** (1): 2–15, 1982.
31. K. Posse A design-for-testability architecture for multichip modules, *Proc. IEEE Int. Test Conf.*, 1991, pp. 113–121.
32. E. J. McCluskey Built in self test techniques, *IEEE J. Design Test Comput.*, **2** (2): 21–28, 1985.
33. Anon, *IEEE Standard Test Access Port and Boundary-Scan Architecture*, IEEE Standard 1149.1-1990, New York: IEEE Standards Board, 1990.
34. D. L. Landis P. Singh Optimal placement of IEEE 1149.1 test port and boundary scan resources for wafer scale integration, *Proc. IEEE Int. Test Conf.*, 1990, pp. 120–126.