PACKAGING RELIABILITY, CHIP-SCALE SEMICONDUCTOR

Portable communication products are currently being driven towards smaller and lighter form factors; one of the thrust areas has been smaller packaging. Assembly-level reliability characterization of a few such chip-scale packages [including the flex-substrate ball–grid array (BGA), elastomer-on-flex package, and overmolded partial-array BGA] is discussed in this article.

PACKAGE ARCHITECTURE—AN OVERVIEW

Flex-Substrate Ball–Grid Array Packages

The flex-substrate BGA is a chip-scale package that consists of a chip wirebonded to a single-sided flex-polyimide substrate

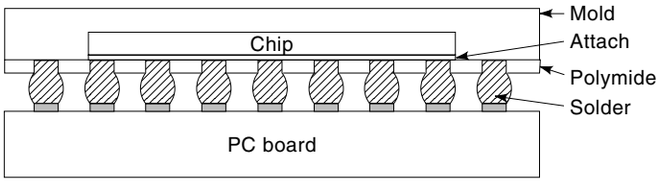

Figure 1. Schematic of a flex-substrate BGA cross section.

(75 μm thick). The wirebonded assembly is overmolded. All the package inputs and outputs (I/Os) that communicate with the board are routed to pads on the chip side of the polyimide substrate. The package-to-board connections are made with 63% Sn–37% Pb solder balls, which go through holes in the substrate and connect to the solder pads on the chip side of the polyimide substrate (Fig. 1). The flex-substrate BGA has 0.45 mm solder balls at 0.8 mm pitch.

Elastomer-on-Flex Packages

The elastomer-on-flex package is a BGA format chip-scale package. The package consists of a chip flipped onto an elastomeric substrate. All the I/Os of the chip are routed to a single-sided flexible circuit, which is bonded to the other side of the elastomeric substrate by beam leads (gold, 18 μm thick). The beam leads are extensions of the printed circuit on the flexible circuit, which are connected to 63% Sn–37% Pb solder balls. The package is exactly the size of the chip, is 80% smaller than a comparable 40-lead thin-small outline package (TSOP) and is 17% thinner, measuring just 1 mm in thickness. The elastomer-on-flex 48-I/O package has 0.3 mm (11.81 mil) diameter solder balls at 0.65 mm pitch (Fig. 2). Two versions of the elastomer-on-flex interposer CSP (from a single source) have been characterized in this study—the 48-pin and the 40-pin. Both the 40-bump and 48-bump versions have 0.3 mm (11.81 mils) diameter solder balls at 0.75 mm pitch (Figs. 2 to 5).

Rigid-Interposer Flip-Chip Packages

Figure 6 is a schematic of a Motorola SLICC (or Motorola JACS-Pak) package mounted to a main printed circuit board (PCB); Table 1 gives typical characteristics. An IC with high-lead solder bumps (e.g., 97% Pb–3% Sn or 95% Pb–5% Sn) is reflowed to a BT–epoxy (Bismaleimide Triazine) PCB interposer substrate 0.2 mm to 0.3 mm (8 to 12 mils) thick and underfilled using conventional flip-chip processes. Active I/Os are routed, through PTHs (plated-thru hole), to an array of solder pads on the underside of the package, as in pad array

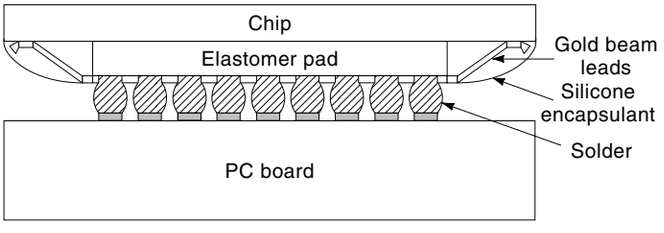

Figure 2. Schematic of an elastomer-on-flex package cross section.

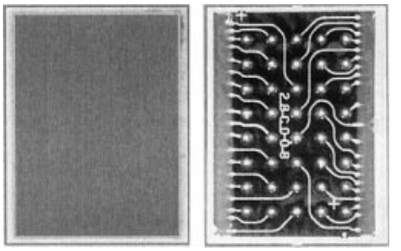

Figure 3. 40-pin elastomer-on-flex interposer chip-scale package.

carriers such as the plastic ball-grid array (PBGA) package (Figs. 6, 7). The SLICC bottom-side package solder-joint pad pitch is 32 mils (0.8 mm). These pads are bumped with solder spheres of 22.2 mil (0.564 mm) diameter. SLICC packaging has extended the existing pad array carrier technology limits both in pad-pitch and in solder-sphere size. SLICCs for ICs with I/O counts in the range from 40 to 150 can be made about 0.060 in. to 0.100 in. (0.15 cm to 0.25 cm) larger than the IC on a side. The area efficiency is greatly enhanced for the SLICC package over wirebonded packages [OMPAC, Quad-Flat Package (QFP) etc.] because of the increased area that is available to route the runners under the IC. This area underneath the IC is critical to routing the I/Os from the IC to the bottom side in the most efficient manner. As PCB technologies lend themselves to finer lines and spaces, smaller plated vias, and better tolerances, this approach can result in carriers that can theoretically be the same size as the IC in the x and y dimensions.

The flip chip is assembled to the interposer board via alignment on the C4 bump cell and subsequent reflow soldering in a convection reflow process. The low-temperature solder on the board reflows and forms the interconnect between the chip and the board. The high-temperature solder on the chip is not reflowed, and the presence of this solder bump helps maintain the standoff between the chip and the board. The C4 bonded chip is then underfilled. The package solder-joint bumping is done using the conventional BGA bumping process.

Chip bonding consists of four substeps: (a) chip alignment, (b) flux dispense, (c) chip placement, (d) reflow. Prior to any processing, the interposer substrate is fixtured into a specially designed pallet to prevent substrate warpage after chip placement. The chips are flipped face down in the waffle

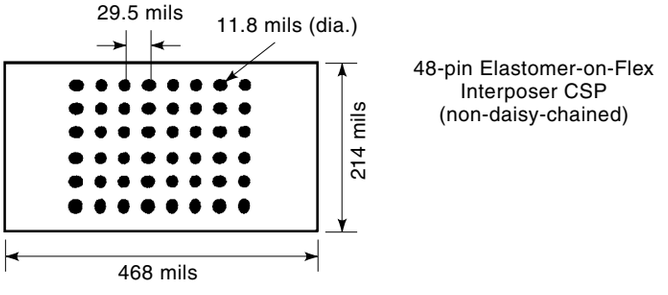

Figure 4. Non-daisy-chained 48-pin version of the elastomer-on-flex interposer chip-scale package.

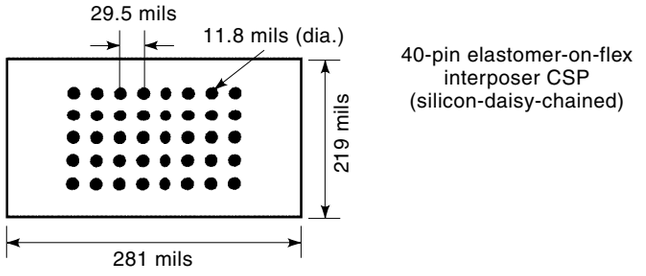

Figure 5. Daisy-chained 40-pin version of the elastomer-on-flex interposer chip-scale package.

packs prior to mounting the waffle packs for chip placement. The chips are picked from the waffle packs and visually aligned (using the imaging system on the C4 bump cell) so that the pads on the interposer substrate overlap the bumps on the chip. Flux is then dispensed at the bonding site on the interposer substrate. The chip is placed immediately after dispense, before the flux dries up. This is very important, since the flux contains a tacky medium that holds the chip in place during population of the interposer substrate and transfer to the convection furnace, and in the convection furnace prior to reflow. After the chips have been placed on the interposer substrate, the pallet is fed into the reflow oven to form the C4 joints. The low-temperature solder on the interposer wicks up and forms a joint with the high-temperature solder on the chip.

Underfilling is carried out by dispensing underfill material around all of the chip and the material is pulled in by subjecting the assembly to cyclic application of vacuum and air pressure for two or three cycles. Acoustic microscopy has been used to verify the complete underfilling of the chip by vacuum infiltration (Fig. 8). For the underfill to be effective at all, it is extremely important for the material to engulf the solder joints and have maximum adhesion in the peripheral region. The risk to the integrity of the device with some trapped voids in the center is minimal.

The BGA ball-bumping process involves dispensing flux on each of the C5 pads and placing solder spheres. After the array has been populated with solder spheres, it is then reflowed. The array is then singulated by sawing, using precision sawing equipment.

Table 1. SLICC Characteristics

Size of carrier (in.)	0.028–0.100 larger than IC edge
Thickness of substrate (in.)	0.008–0.012
Substrate materials	FR4, BT-Epoxy
Thickness of topside solder mask (in.)	0.0008–0.001
Height of topside pad finish	0.0008–0.0015
PTH metal	0.0005-in.-thick Cu (typical), plugged
Minimum line widths/spacings (in.)	0.004/0.004
Bottom-side pad finish	Au flash over Cu–Ni
Bottom-side pad pitch[a] (in.)	0.032
Bottom-side pad diameter (in.)	0.020
Bottom-side ball diameter (in.)	0.0222

[a] Center to center.

THERMAL FATIGUE RELIABILITY

Nonlinear Finite-Element Model Predictions

Thermal fatigue reliability has been predicted using nonlinear finite-element models under both accelerated test conditions and field-use conditions for all the chip-scale packages.

Solder Constitutive Behavior. Constitutive behavior of the solder has been modeled using a sinh–viscoplastic law (1),

$$d^{\mathrm{p}} = Ae^{-Q/RT} \sinh\left(\xi \frac{\sigma}{s}\right)^{1/m} \tag{1}$$

where the dynamic hardening is represented by

$$\frac{ds}{dt} = \left[h_0 \left|1 - \frac{s}{s^*}\right|^a \operatorname{sign}\left(1 - \frac{s}{s^*}\right)\right] d^{\mathrm{p}} \tag{2}$$

and

$$s^* = \tilde{s}\left(\frac{d^{\mathrm{p}}}{A} e^{Q/RT}\right) \tag{3}$$

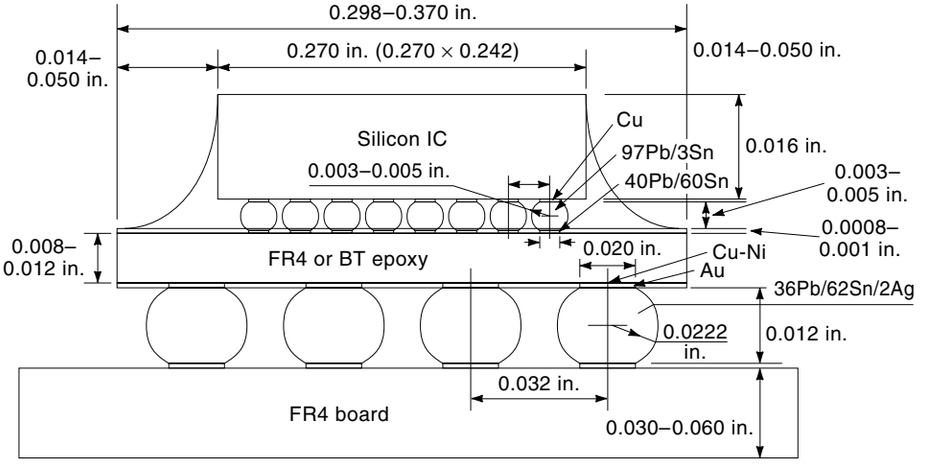

Figure 6. Schematic of a SLICC package.

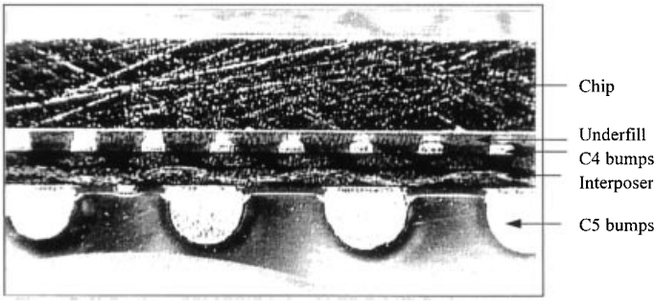

Figure 7. Cross section of SLICC (JACS-Pak) package.

where d^p is the effective inelastic deformation resistance, σ is the effective Cauchy stress, s is the deformation resistance, s^* is the saturation value of the deformation resistance, $\tilde{s}$ is the saturation value of the coefficient of deformation resistance, A is the preexponential, Q is the activation energy, m is the strain-rate sensitivity, h_0 is the constant rate of thermal hardening, and T is the absolute temperature. The deformation resistance represents the isotropic resistance to inelastic flow of the material. The material parameters in this constitutive equation, A, Q, m, x, h_0, $\tilde{s}$, and a, are assumed to be temperature-independent in the temperature and strain range of interest (Table 2).

The solder-joint reliability has been predicted based on the following approach: If R_1, R_2, R_3, R_4, . . ., R_q represent the reliabilities of individual joints, calculated from nonlinear finite-element simulations, then the component reliability can be calculated as follows (series system):

$$R_c = R_1 R_2 R_3 R_4 \cdots R_q \tag{4}$$

Ideally, since all the joints are equidistant from the neutral point of the package, the reliabilities (or inversely the probabilities of failure) should be equal for all the joints. Then Eq. (4) can be reexpressed as follows:

$$R_c = R_i^q \tag{5}$$

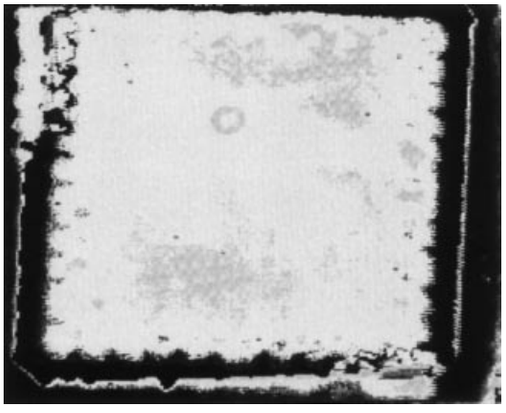

Figure 8. Acoustic microscope image of SLICC package after underfill.

The accelerated test data on the thermal fatigue solder-joint failure distribution have been fitted with a Weibull distribution with a cumulative failure distribution given by

$$F(t) = 1 - \exp\left[-\left(\frac{t - t_0}{\eta}\right)^{\beta}\right] \tag{6}$$

The reliability is inversely given by $R(t) = 1 - F(t)$. Taking the natural logarithm of Eq. (5) and substituting for joint reliability from Eq. (6), we obtain

$$\frac{\ln R_c}{q} = -\left(\frac{t - t_0}{\eta}\right)^{\beta} \tag{7}$$

Thus, the failure-free life, or B1 life, for the component (the time to failure of 1% of the component population) can be calculated from

$$t_{f,c} = t_0 + \eta\left(\frac{-\ln R_c}{q}\right)^{1/\beta} \tag{8}$$

where $t_{f,c}$ represents the component time to failure. The predicted component life derived using Eq. (8) is independent of any assumption of a component statistical distribution. The damage relationships used for correlating damage to life are (2)

$$\begin{aligned} N &= 7860(\Delta W)^{-1.00} \\ \frac{da}{dN} &= (4.96 \times 10^{-8})[(\Delta W)^{1.13}] \end{aligned} \tag{9}$$

$$\alpha_w = N_{i,s} + \frac{a - (N_{i,s} - N_{i,p})\dfrac{da_p}{dN}}{\dfrac{da_s}{dN} + \dfrac{da_p}{dN}} \tag{10}$$

where ΔW is the plastic work per cycle, a is the crack length, N is the number of cycles, α_w is the characteristic life, and the subscripts p and s represent the primary and secondary regions. The interested reader is referred to Ref. 3 for a more detailed discussion of failure mechanisms in microelectronic devices.

Flex-Substrate Ball–Grid Array. A nonlinear finite-element model has been developed for the flex-substrate BGA package (Fig. 9). Major geometry and architecture variables affecting reliability were identified and incorporated in the model, including:

1. `xpklen`, `ypklen`, `pkhgt`: the package length, width, and thickness
2. `chlnx`, `chlny`, `chthk`: chip length, width, and thickness
3. `njt`: number of solder joints
4. `jheight`: solder-joint height
5. `rjbase`, `rjtop`, `rjint`; `jtheta`; `jskang`: joint radius at the base, at the top, and at user-specified intermediate locations; joint vertical inclination (perfectly vertical joint has zero inclination); joint horizontal skew angle
6. `nclm`, `nrow`: numbers of rows and columns of solder joints
7. `xstagr`, `ystagr`, `xskew`, `yskew`; `xmrgn`, `ymrgn`: latitudinal staggers and longitudinal skews between succes-

Table 2. Constants for the Anand Viscoplastic Formulation as a Function of Strain Rate and Assembly Stiffness

Imposed Strain $1/K$	Assembly Stiffness	S_0 (psi)	A (s^{-1})	ξ	m	h_o (psi)	$\hat{S}$ (psi)	n	a
1e−4	1e+6	1.8e+3	4e+6	1.5	0.303	2e+5	2.00e+3	0.07	1.3
	1e+7			1.6	0.29		2.16e+3		1.5
	1e+8			1.7	0.28		2.32e+3		1.6
	1e+9			1.8	0.27		2.55e+3		1.7
1e−3	1e+5	1.8e+3	4e+6	1.2	0.22	2e+5	1.8e+3	0.02	1.5
	1e+6			1.5	0.24		2.0e+3		

sive rows and columns of the array; x and y margins between the edge of the package and the first row or column

8. `xpitch`, `ypitch`: x and y pitches of the solder-joint array
9. `rghtk`: polymide-flex substrate thickness
10. `bdthk`: PC board thickness
11. `dtthk`: die attach thickness

Figure 10 shows the viscoplastic strain energy density distribution in the solder joints during liquid–liquid temperature shock (LLTS) from −55° to 125°C, 5.8 cycles per hour (c/h). The primary crack propagation site is at the package-to-solder-joint interface, and the secondary crack propagation site is at the solder-to-board interface. Model predictions indicate a viscoplastic strain energy density of 76.6 psi · in./in. (528 kPa · m/m) in the primary region and 66.7 psi · in./in. (460 kPa · m/m) in the secondary region. The time to first failure has been predicted based on crack-propagation dynamics, statistical distribution of solder-joint thermal fatigue failures, and Monte Carlo simulations. The package time to first failure is in the neighborhood of 598 cycles. Table 3 shows the effect of ball size on the reliability of the flex-substrate BGA. Model predictions indicate an increase in the time to first failure from 125 cycles to 600 cycles of LLTS from −55° to 125°C, 5.8 c/h, with increase in the ball diameter from 0.3 mm to 0.45 mm.

Table 4 shows the effect of board thickness on the reliability of the flex-substrate BGA. Model predictions indicate a decrease in the time to first failure from 600 cycles to 550 cycles of LLTS from −55° to 125°C, 5.8 c/h, with increase in the board thickness from 0.032 in. (0.081 cm) to 0.062 in. (0.157 cm). The 48-I/O, 0.8 mm pitch flex-substrate BGA packages were soldered onto a 0.8 mm thick, immersion-Ni–Au-finish PC board. The board assemblies were subjected to LLTS, −55° to 125°C, 5.8 c/h. The failures were determined by resistively probing the parts. The accelerated test data were fitted with a Weibull distribution. Each of the data points represents probit data. Both the distributions showed Weibull slopes in the neighborhood of 2.6 to 4.0 for unaged (β = 3.935) and aged (β = 2.637) flex-substrate BGAs. These shape parameter values are characteristic of solder-joint fatigue. The characteristic life [time to failure (TTF) of 63.2% of the population] for the unaged solder joints is in the neighborhood of 970 cycles, and for the aged joints is in the neighborhood of 713 cycles. The time to first failure for the unaged parts is in the neighborhood of 550 cycles, and that for the aged parts is in the neighborhood of 300 cycles. Figure 11 shows a cross section of an 48-I/O, 0.8 mm pitch flex-substrate BGA after thermal fatigue failure—notice the primary crack propagation region at the package-to-solder interface. This correlates very well with the nonlinear finite-element prediction from Fig. 10 (model prediction TTF = 598 cycles).

Partial-Array Ball–Grid Array, 0.5 mm Pitch, 48-I/O Package. Nonlinear finite-element simulations have been used to evaluate the effect of package and board material properties on the thermal fatigue reliability of the 48-I/O, 0.5 mm pitch package. A quarter-symmetry nonlinear model has been developed to model the package. Quarter symmetry was used because that is the symmetry of the geometry, loading, and boundary conditions. The input material properties variables include board thickness, board coefficient of thermal expansion [CTE, (μm/m)/°C], organic-substrate CTE [(μm/m)/°C],

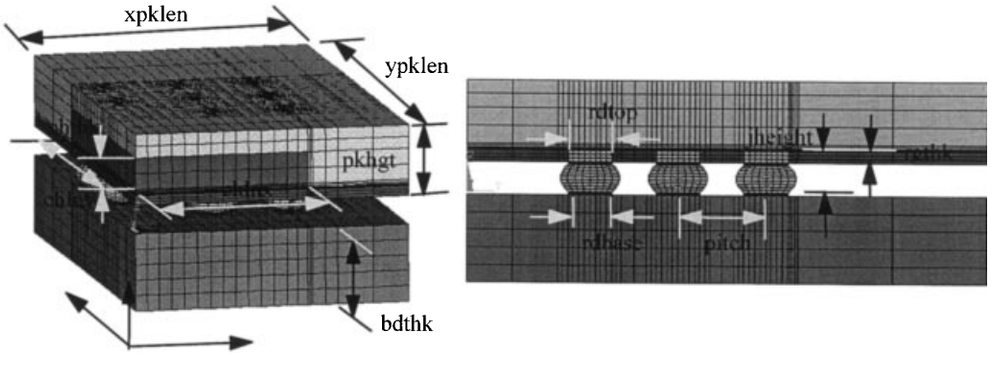

Figure 9. Nonlinear finite-element model for the flex-substrate BGA package.

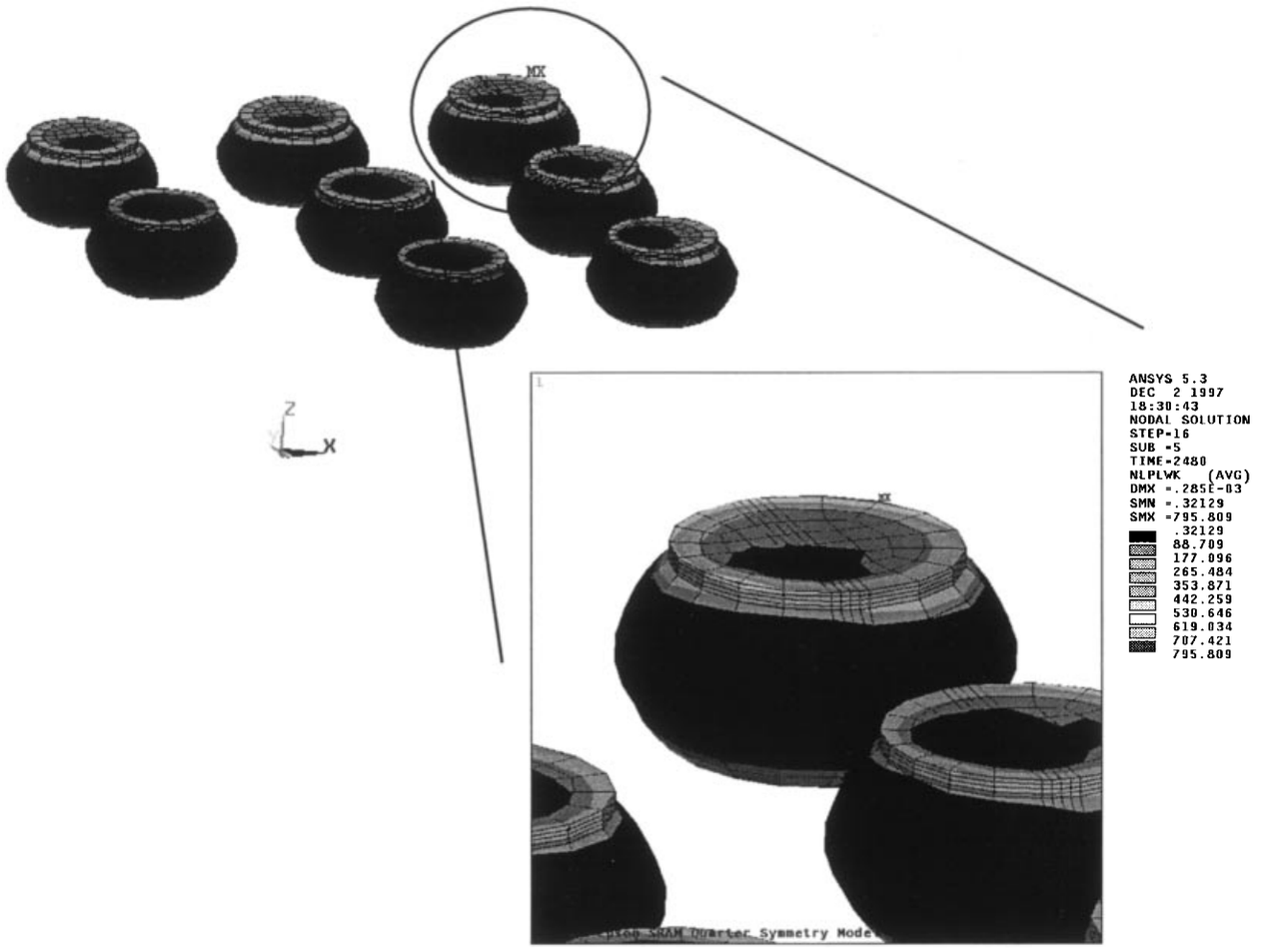

Figure 10. Viscoplastic strain energy distribution in the solder joints of flex-substrate BGA during thermal shock.

and organic-substrate elastic modulus (psi); Table 5 shows the input deck for each for the variables. The board thickness variation reflects a range of 7 mils (0.2 mm) on a nominal thickness of 48 mils (1.2 mm). The board CTE variations reflect the range of measured CTEs. Nonlinear finite-element simulations have been run to evaluate the effect of material property variations on the thermal fatigue reliability during LLTS from −55 to 125°C, 5.8 c/h. Figure 12 shows the location of the maximum viscoplastic strain energy density in the solder joints at the two temperature extremes. The location of the maximum strain energy density in all the cases was at the package–solder-joint interface. Table 6 shows the package time to first failure based on crack-propagation dynamics, statistical distribution of solder-joint thermal fatigue failures, and Monte Carlo simulations. The package time to first failure shows a range of 125 cycles to 1025 cycles, depending on the package and board material properties. Simulation case 2 reflects the daisy-chained test board; the predicted 1025 cycles correlates well with the first failure in the neighborhood of 1000 cycles.

The 48-I/O, 0.5 mm pitch partial-array BGAs were soldered to a 1.2 mm thick, OPC-finish PC board and subjected

Table 3. Effect of Ball Diameter on the Time to First Failure for the Flex-Substrate BGA Package[a]

Ball Size (mm)	Predicted Time to First Failure (cycles)
0.3	125
0.45	600

[a] The package reliability decreases with decrease in ball diameter.

Table 4. Effect of Board Thickness on the Time to First Failure for the Flex-Substrate BGA Package[a]

Board Thickness (in.)	Predicted Time to First Failure (cycles)
0.032	598
0.048	565
0.062	550

[a] The package reliability decreases with increase in board thickness.

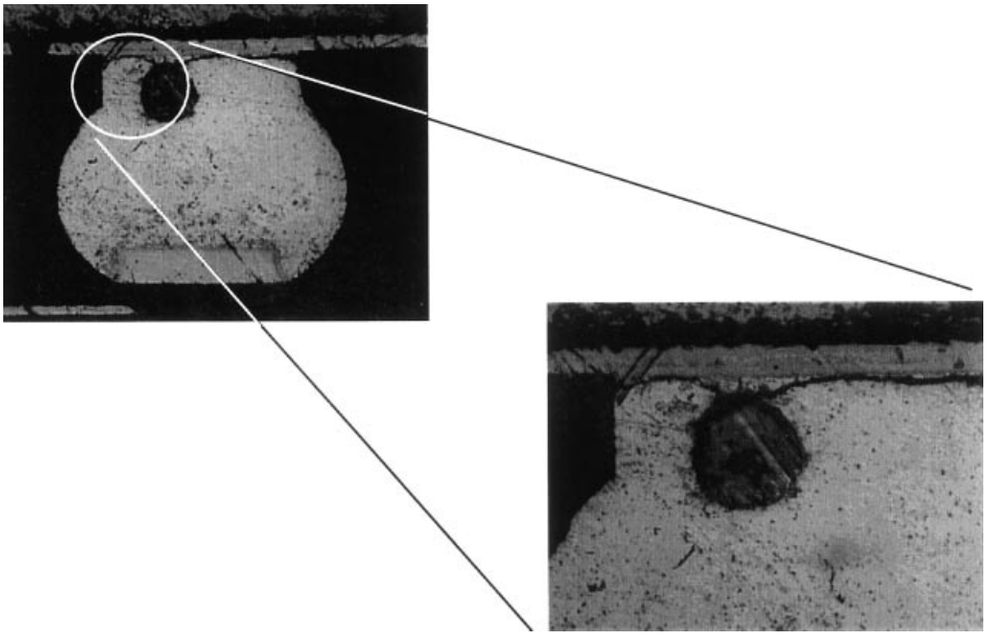

Figure 11. Cross section of flex-substrate BGA thermal fatigue failure. The primary crack propagation site is at the solder-joint-to-package interface.

to LLTS, −55° to 125°C, 5.8 c/h. A second population of the parts was thermally aged at 170°C for 144 h and subjected to LLTS. The failures were determined by resistively probing the parts. The accelerated test data were fitted with a Weibull distribution. Each of the data points represents probit data. Weibull distributions for both the aged and the unaged parts showed slopes in the neighborhood of 2.6 to 4.0 for unaged (β = 4.218) and aged (β = 2.875) partial-array BGAs. These shape parameter values are characteristic of solder-joint fatigue. The characteristic life (TTF of 63.2% of the population) for the unaged solder joints is in the neighborhood of 1980 cycles, and the characteristic life for the aged joints is in the neighborhood of 1063 cycles. Note the horizontal shift in the accelerated life distributions of the unaged and the aged parts, which indicates that the mechanism has not changed, but the life has decreased by a factor of 1.9. The time to first failure for the unaged parts is in the neighborhood of 1000 cycles, and that for the aged parts is in the neighborhood of 500 cycles. Figure 13 shows a cross section of a partial-array BGA package (48 I/Os, 0.5 mm pitch) after thermal fatigue failure—notice the primary crack propagation region at the package-to-solder interface. This correlates very well with the nonlinear finite-element prediction from Figure 12 and Table 6—the daisy-chained test configuration corresponds to simulation case 2 (model prediction TTF = 1025 cycles). The model predictions thus show good agreement with experimental data.

Rigid-Interposer Flip-Chip Packages, 0.8 mm Pitch, 68-I/O Package. A 3D-slice parametric finite-element model has been developed for the SLICC package (Fig. 14). Model variables include the user-specified number of solder joints (both underfill and package-level solder joints); the user-specified joint geometry, including incline, pitch, shape (hourglass to barrel), in-plane skew, and pad misalignment; the chip length, width, and thickness; the underfill of the end fillet; the interposer thickness; and the board thickness.

Bar samples of the underfill material 0.5 mm to 0.7 mm thick, 6 mm to 7 mm wide, and 1 in. (2.5 cm) long were constructed and subjected to a cantilever deflection test at different temperatures and at two different cure conditions: 30 min at 150°C, and 15 min wait plus 60 min at 155°C. The elastic modulus versus temperature is shown in Fig. 15. The CTE

Table 5. Package and Board Material Properties Used for Various Simulation Runs

Simulation	Board Thickness (in.)	Board Coefficients of Thermal Expansion (μm/m)		Solder-Joint Height (in.)	Organic-Substrate Coefficients of Thermal Expansion (μm/m)		Molding-Compound Elastic Modulus (10^6 psi)
		α_x	α_y		α_x	α_y	
1	0.042	16.0	16.0	0.007	9.9	10.2	1.42
2	0.042	15.2	18.2	0.007	13.0	13.0	1.42
3	0.055	21.8	21.8	0.007	9.9	9.9	3.42

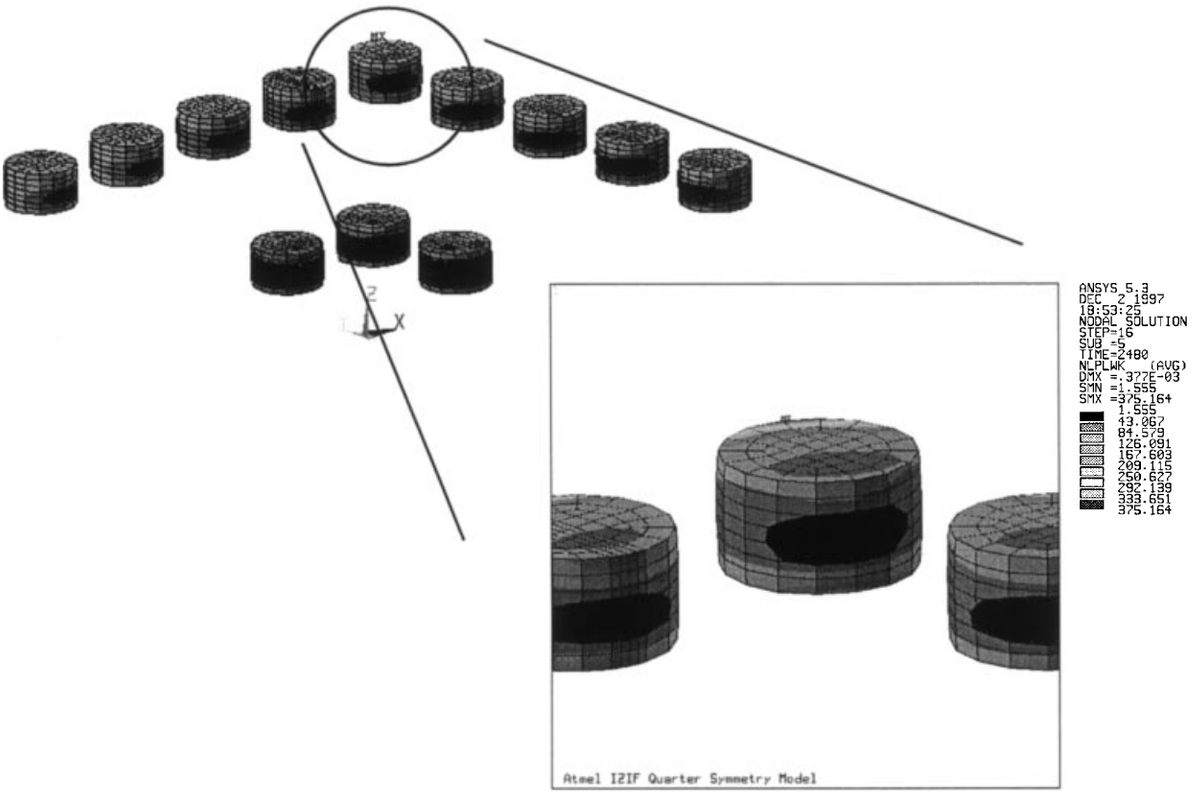

Figure 12. Viscoplastic strain energy density in the solder joints during liquid–liquid temperature shock—fifth cycle.

does not change with cure condition and stays at 20 (μm/m)/°C up to the glass-transition temperature (T_g).

Several combinations of wait time, cure time, and cure temperature were investigated for the underfilling process. From the results of the LLTS test (−55° to 125°C), it was found that the wait time during underfill cure had little or no effect on the life t_{50} of the chip–underfill interface. Only two cure conditions (30 min at 150°C, and 15 min wait plus 60 min at 155°C) were examined for thermal fatigue modeling purposes. The packages were examined under an acoustic microscope and subjected to electrical test to check for solder-joint failures after 100, 200, 300, 500, 700, 1000, and 1300 cycles.

The failure data have been fitted with a Weibull distribution in Fig. 16. The circles in the graph indicate the number cycles to initiation of delamination at the chip–underfill interface. Typically this is the first interface to fail in thermal fatigue in underfilled packages. After the initial delamination, the crack propagates at the chip–underfill interface until the underfill is completely detached from the chip. At that point, the C4 solder joints fail in no more than a few cycles (shown with squares in Fig. 16). This is demonstrated by the almost parallel lines of initial delamination and solder-joint failures for both the cure conditions.

LLTS of the SLICC packages was also simulated. The model predictions of the von Mises stress at the chip–

Table 6. Model Predictions for the Various Property Data Sets

	Viscoplastic Strain Energy Density (psi · in./in.)		
Simulation	Primary Region	Secondary Region	Package Time to First Failure (cycles)
1	95.25	62.29	540
2	53.20	39.97	1025
3	320.875	284.73	125

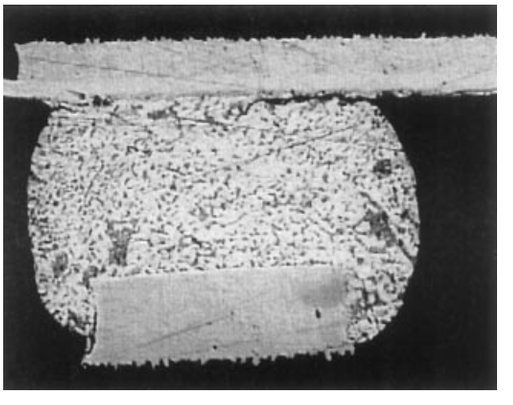

Figure 13. Cross section of 0.5 mm pitch package after thermal fatigue failure. Notice the crack propagation at the package-to-solder interface.

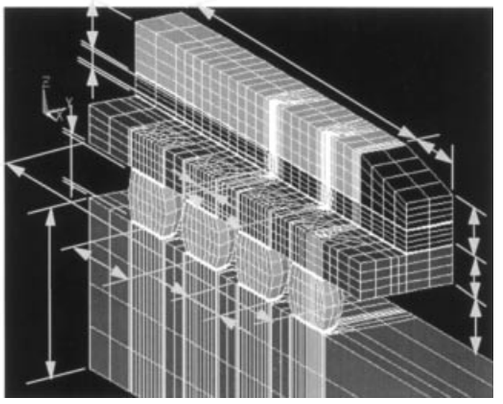

Figure 14. SLICC package primitive.

underfill interface are plotted in Fig. 17. The crack initiation site is typically at the edge of the chip at the chip–underfill interface, which is also the site of maximum von Mises stress concentration, both at the hot and at the cold end of the shock test. From Fig. 16, it can be seen that the cure for 30 min at 150°C gives a characteristic life (≈ 289 cycles) that is $\frac{1}{6}$ of the characteristic life from the cure condition of 15 min wait plus 60 min at 155°C (≈ 1759 cycles). Simulations were run to evaluate the reason for the difference in fatigue life. Elastic properties for the underfill, which were measured using a Rheometrics DMA, were used for simulation purposes. From the simulation results, it was seen that the mean von Mises stresses for the two cure conditions were 1574 psi and 1831.5 psi respectively [Fig. 18(a,b,c,d)]. The von Mises stress is chosen as the failure indicator for interfacial delamination for the chip–underfill interface because delamination is actuated by the differential shear between the chip and the underfill. The underfill material becomes more compliant with increase in cure time from 30 min to 60 min at 150°C, which means an increase in fatigue life. It is unclear at this point how the interface properties change with cure time. Experiments are underway to decouple the effect of interface properties from that of the properties of the underfill.

Predictions from thermal fatigue simulations indicate that for SLICC package solder joints, the plastic work per cycle in the primary region is in the neighborhood of 12 psi · in./in. (82 kPa · m/m), and in the secondary region is in the neighborhood of 2.03 psi · in./in. (14.0 kPa · m/m). The predictions have been done for a SLICC package on an FR4 board [15 (μm/m)/°C, 1.40 cm (55 mils) thick]. In Fig. 19, showing the distribution of plastic work in package solder joints, the primary region is the top right and the secondary region is the bottom left. The primary region is the area of largest plastic work in the joint and is typically closer to the package side, creating a crack from the outside periphery of the joint inwards along the joint–chip interface. The secondary region is closer to the board side of the package solder joint and creates a crack from the inside periphery of the joint outward along the joint–board interface. The plastic work per cycle predicted for the SLICC translates to more than 655 cycles to crack initiation in primary region and 3930 in the secondary region of package solder joints.

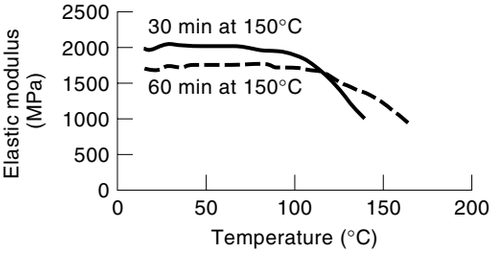

Figure 15. Elastic modulus of underfill versus temperature.

The predicted characteristic life required for complete failure of the package solder joints is predicted to be in excess of 10,000 cycles. This prediction is consistent with the data in that no package solder-joint failures have been seen in accelerated tests. Similar estimates have been obtained for the C4 joints in a substrate SLICC package 27 mils (0.69 mm) thick. The plastic work distribution inside the C4 solder joints is plotted in Fig. 20. The predicted numbers of cycles to failure initiation in the primary and secondary regions are in the neighborhood of 413 and 1357 respectively. The predicted characteristic life for complete failure of the C4 joints is in the neighborhood of 8000 cycles (assuming no delamination of the chip–underfill interface). This agrees with the experimental data in that the C4 joints fail only after the chip–underfill interface delaminates.

Direct Chip Attach Versus SLICC in Thermal Fatigue. Simulations were run to evaluate the stresses in the chip and the underfill for direct chip attach (DCA) versus the SLICC package. The principal chip stresses at the hot and the cold ends of the thermal shock cycle are shown in Fig. 21 for both DCA and SLICC. The mean principal stress for DCA is in the neighborhood of 7690 psi (53.0 MPa), which is higher than the mean principal stress for SLICC, in the neighborhood of 5805.4 psi (40.02 MPa). The mean principal stress was chosen because in brittle material, such as silicon, the crack propagation is perpendicular to the maximum principal stress direction. The mean principal stress is lower than the fracture strength of silicon, which is in the neighborhood of 53,669 psi (370.0 MPa). The mean von Mises shear stress at the chip–underfill interface for DCA is 1822.5 psi (12.57 MPa), which is higher than that for the SLICC, which is 1574 psi (10.85 MPa; see Fig. 22).

Elastomer-on-Flex Package, 0.65 mm Pitch, 48-I/O Package. The solder-joint reliability of the package was modeled. A quarter-symmetry finite-element model was built for reliability evaluation of the elastomer-on-flex interposer CSP (Fig. 23). The model incorporates the geometry and architecture of the various package elements, including the chip, copper beam leads internal to the package, chip metallization, elastomer, encapsulant, polyimide, polyimide metallization, solder bumps, and board. The geometric variables incorporated in the model include:

- *Package.* Permits modeling any package shape, from rectangular to square. First-order parameters include length (pklen), width (pkwdt), thickness (pkthk), and margin (pkmgn).
- *Elastomer.* The low-modulus material located between the die and the polymide tape. The model permits evalu-

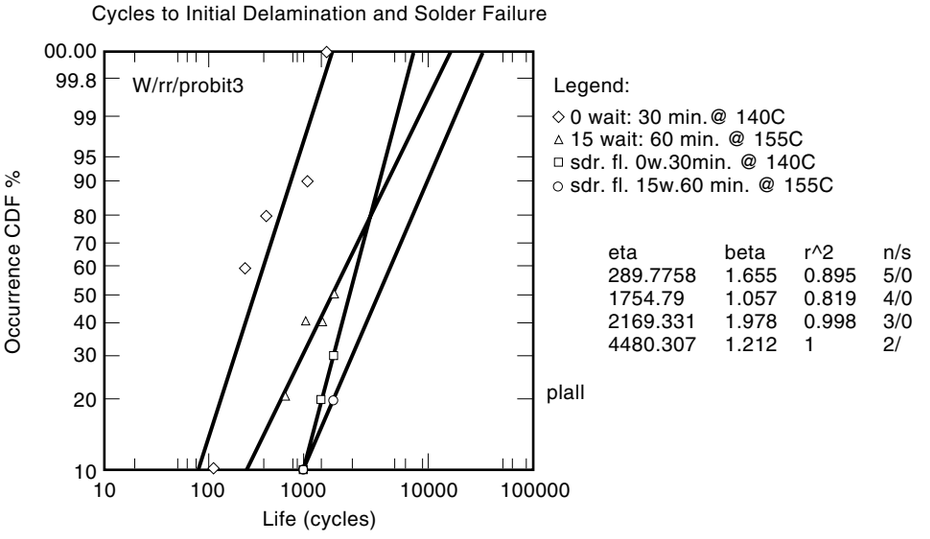

Figure 16. Weibull plot of the number of cycles to crack initiation and solder failure for cure conditions of 30 min at 150°C and of 15 min wait followed by 60 min at 155°C.

ation of any elastomer thickness, user-specified shape from rectangular to square, and user-specified percentage of package area coverage. First-order parameters include length (etlen), width (etwdt), and thickness (eehk).

- *Encapsulant.* The encapsulant is dispensed around the periphery of the package and around the elastomer, to provide mechanical protection to the beam leads. The model supports a user-specified encapsulant thickness, width-in-package margin, and fillet radius. First-order parameters include width (mdwdt) and radius (mdrad).
- *Polymide Tape.* The interposer substrate between the chip and the board. The model permits evaluation of any polymide shape from rectangular to square, and user-specified length, width, thickness, and percentage area coverage of the chip. First-order parameters include length (tplen), width (tpwdt), and thickness (tpthk).
- *Solder Joint.* The model incorporates the solder wicking in the through holes on the bottom of the polymide to the copper pads on top of the polymide. The model permits evaluation of user-specified C5 solder-joint shape, height, in-plane skew, out-of-plane incline, and misalignment. First-order parameters include height (jheight), diameters (rdbase, rdtop), skews (xskew, yskew), misalignments (xmst, ymst), and shape (hourglass to barrel).
- *Beam Leads.* The model permits evaluation of user-specified lead shape, lead thickness, lead width, lead pitch, lead angle, lead bonded length, and lead height. First-order parameters include thickness (ldthk), length

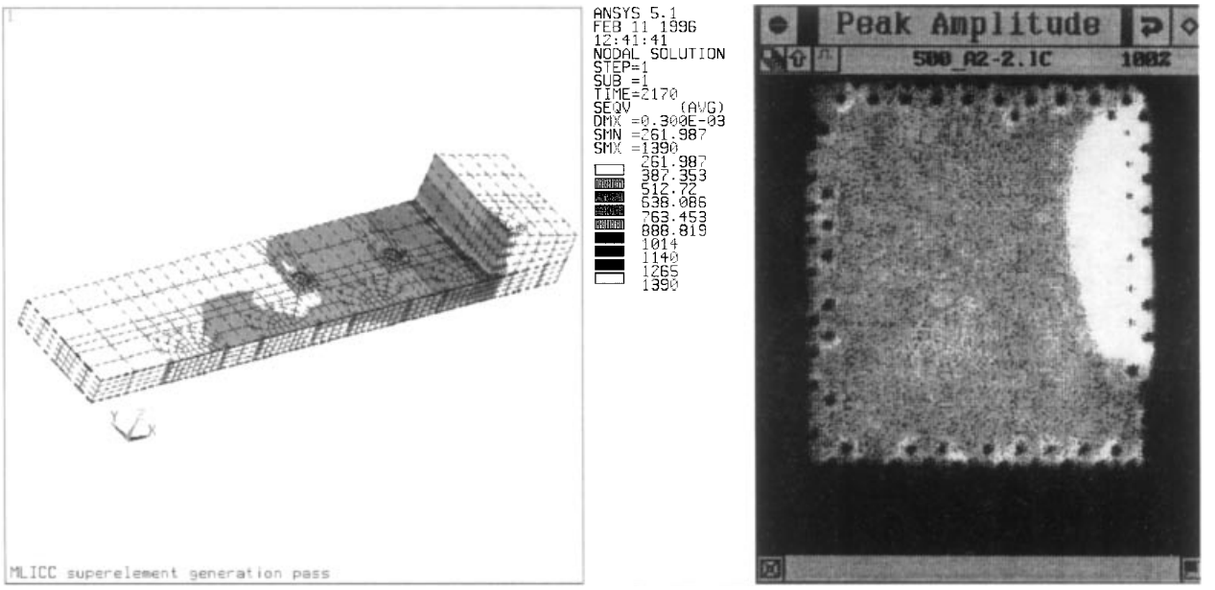

Figure 17. (left) Model prediction of the von Mises stress at the chip–underfill interface during liquid–liquid thermal shock. (right) Acoustic microscope image of delamination at the chip–underfill interface after 500 cycles of liquid–liquid thermal shock.

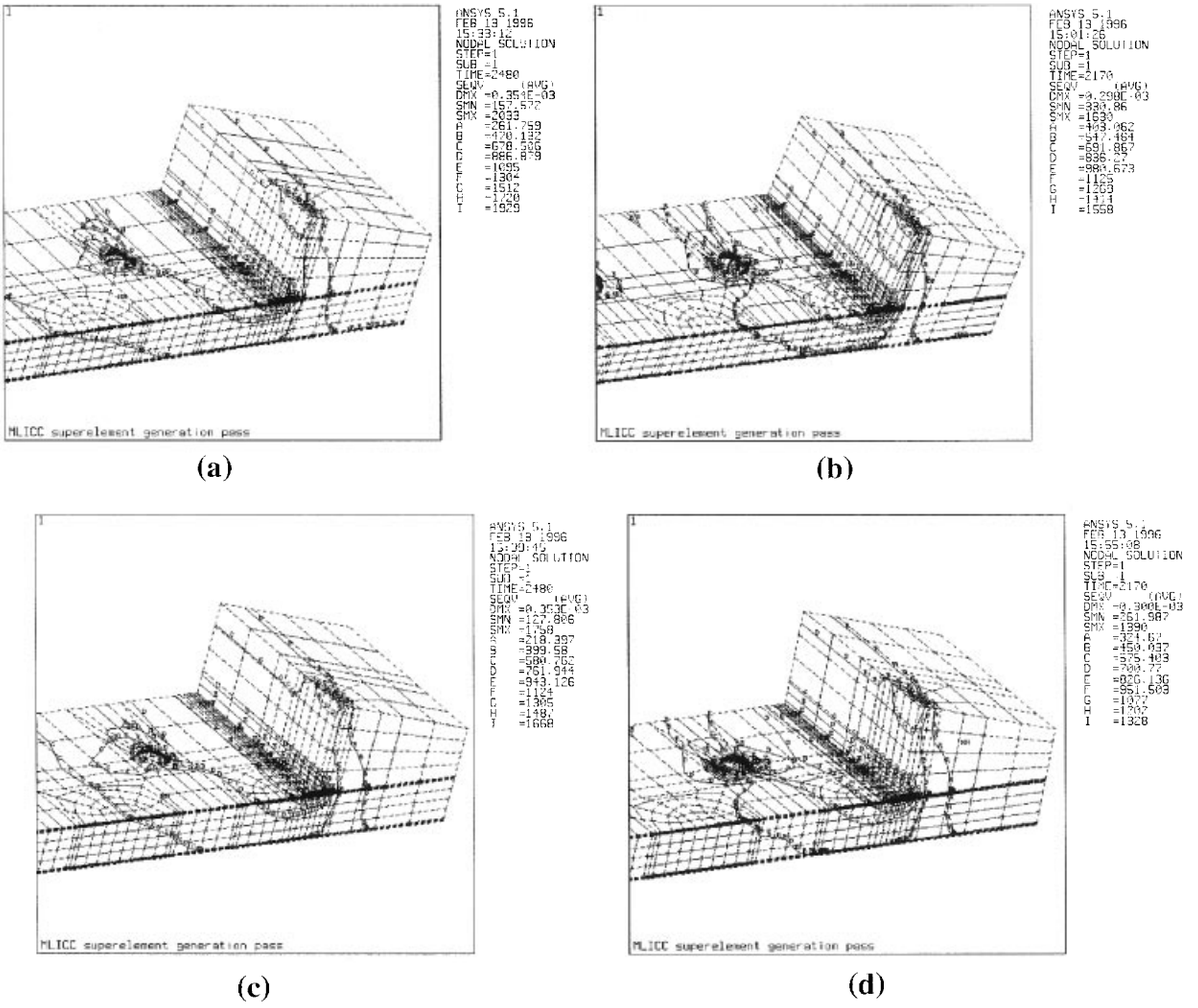

Figure 18. Von Mises stress at the chip–underfill interface: (a) at 125°C after cure for 30 min at 150°C; (b) at −55°C after cure for 30 min at 150°C; (c) at 125°C after cure of 15 min wait followed by 60 min at 155°C; (d) at −55°C after cure of 15 min wait followed by 60 min at 155°C.

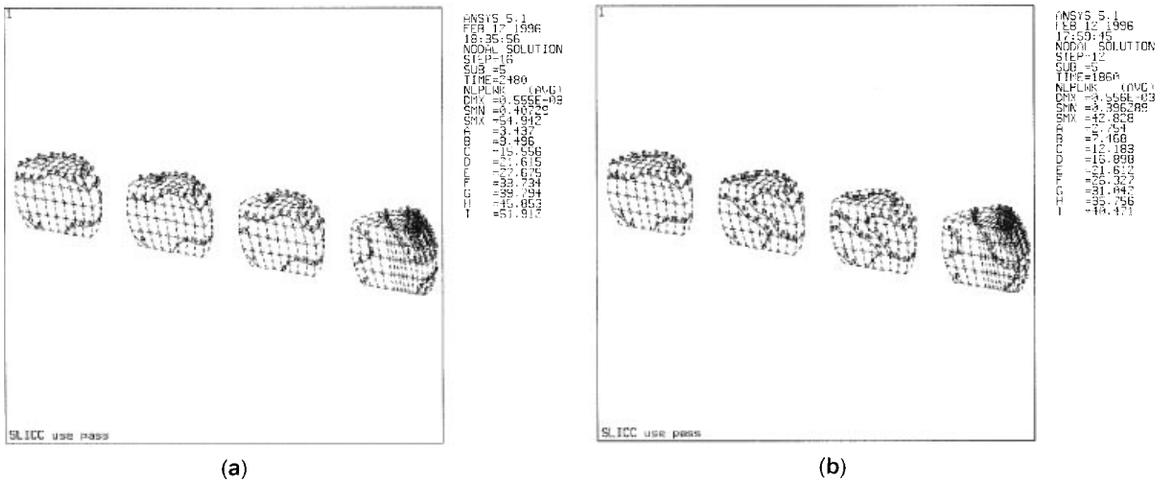

Figure 19. Plastic work in C5 solder joints during thermal shock: (a) hot end at 125°C; (b) cold end at −55°C.

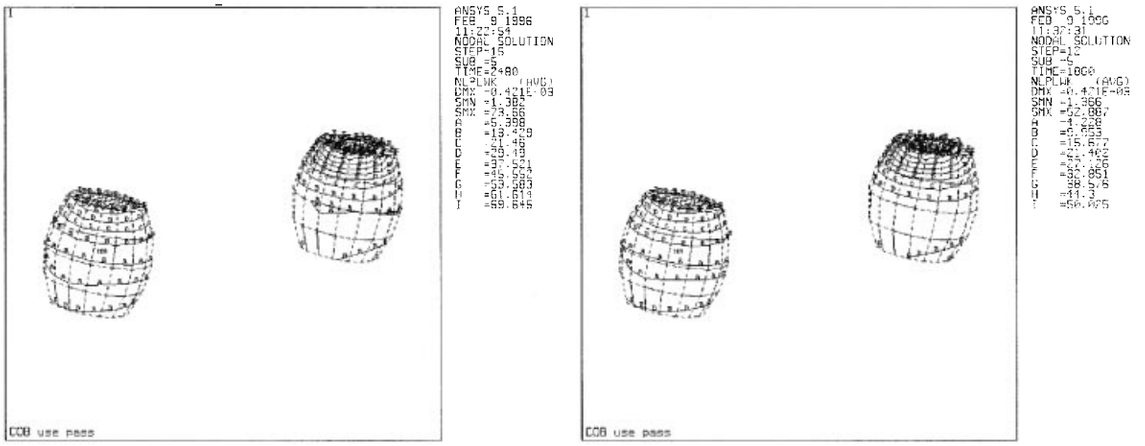

Figure 20. Plastic work in the C4 solder joints during thermal shock: (a) hot end at 125°C; (b) cold end at −55°C.

(ldlnt), width (ldwdt), height (ldhgt), pitch (ldpitch), angle (ldang), and bonded length (ldx1).

- *Copper Traces on Flex.* The model supports user-specified copper-trace width on top of the polymide tape interposer substrate, and user-specified copper-pad diameter and shape (circular to square). First-order parameters include pad diameter (pdrad), copper thickness (pdthk), and pad shape (pd_shape_indx).
- *Chip Metallization.* The model permits evaluation of user-specified chip metallization thickness, length, and width. First-order parameters include pad length (pdclnt), pad width (pdcwdt), and thickness (pdcthk).
- *Board Thickness.*

The elastomer-on-flex interposer CSPs were soldered onto FR-4 PC boards 55 mils (1.4 mm) thick and subjected to LLTS from −55° to 125°C, 5.8 c/h. The packages were CSAMed (C-mode Scanning Acoustic Microscopy) every hundred cycles to evaluate any delamination at the chip–elastomer interface and at the flex–elastomer interface. Two versions of the device were used in reliability characterization—40-pin daisy-chained, and 48-pin non-daisy-chained. The daisy-chained devices were used to evaluate the beam-lead reliability, and the non-daisy-chained devices were used to evaluate the reliability of the solder joints. The resistance the daisy-chained devices was monitored every 100 cycles to determine any failures internal to the package. Three conditions of the packages were tested: (a) unaged virgin parts, (b) thermally aged at 170°C for 144 h, and (c) humidity aged at 85°C and 85% relative humidity (RH) for 168 h. Three dominant failure modes were evaluated during thermal fatigue reliability evaluation: (a) solder-joint failure, (b) beam-lead failure, and (c) chip cracking. Each of the failure modes is discussed in more detail in this section. Readers interested in understanding the physics of the failure mechanisms should refer to Ref. 4.

Failure Mechanisms

Chip Cracking. Several of the elastomer-on-flex interposer CSPs failed due to chip cracking during accelerated tests. The failure is however mechanical in nature and is a result of the lack of any protection on the chip. Only the 48-pin elastomer-on-flex interposer CSP showed this failure mode. The 40-pin one did not do so, because the low-modulus silicone gel that encapsulates the beam leads extends beyond the edge of the chip and covers all the edges of the chip.

Solder-Joint Reliability. Figure 24 shows the finite-element model's predictions of viscoplastic strain energy density in the solder joints, due to thermal fatigue, versus the distance form the center of the package. Figure 24(a) shows the plastic work in the solder at the flex–solder interface, and Fig. 24(b) shows it at the solder–board interface. Each of the curves indicates

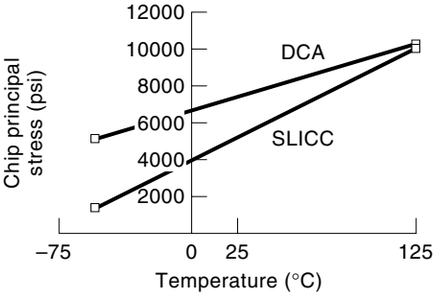

Figure 21. Principal chip stress for chip on board versus SLICC during LLTS thermal shock.

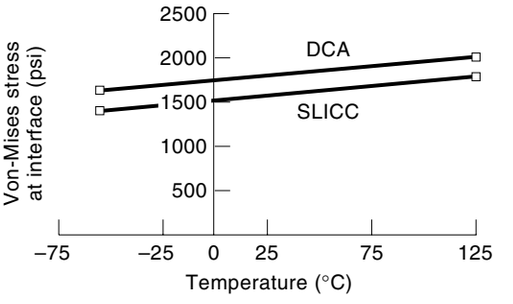

Figure 22. Von Mises stress at chip–underfill interface for chip on board versus SLICC during LLTS thermal shock.

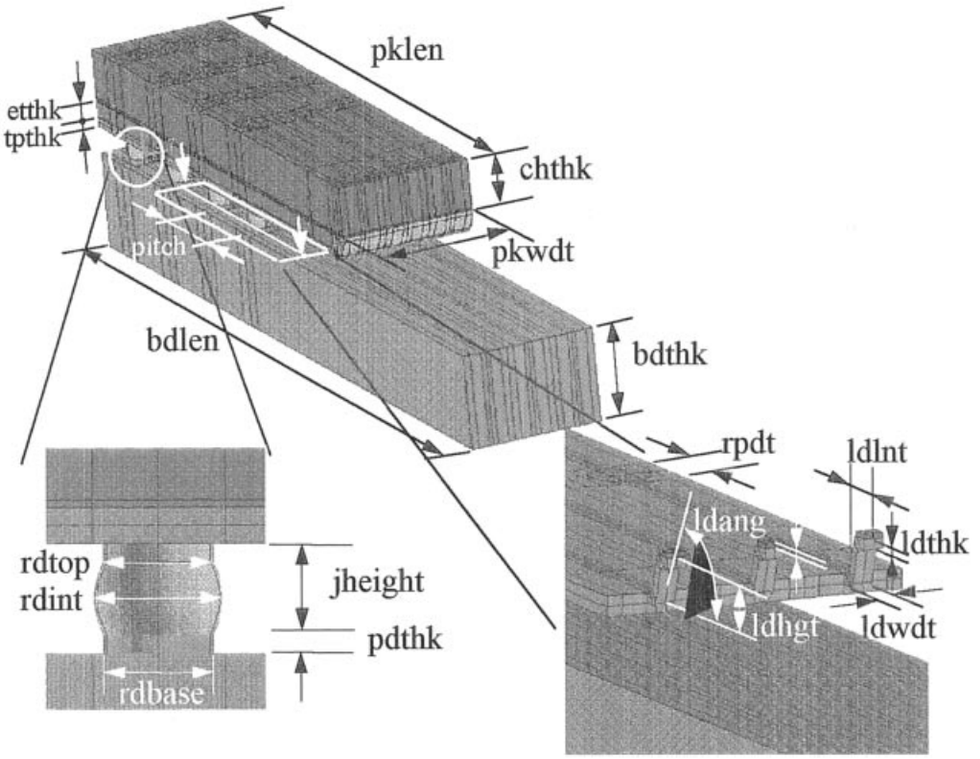

Figure 23. Primitive for the elastomer-on-flex interposer CSP.

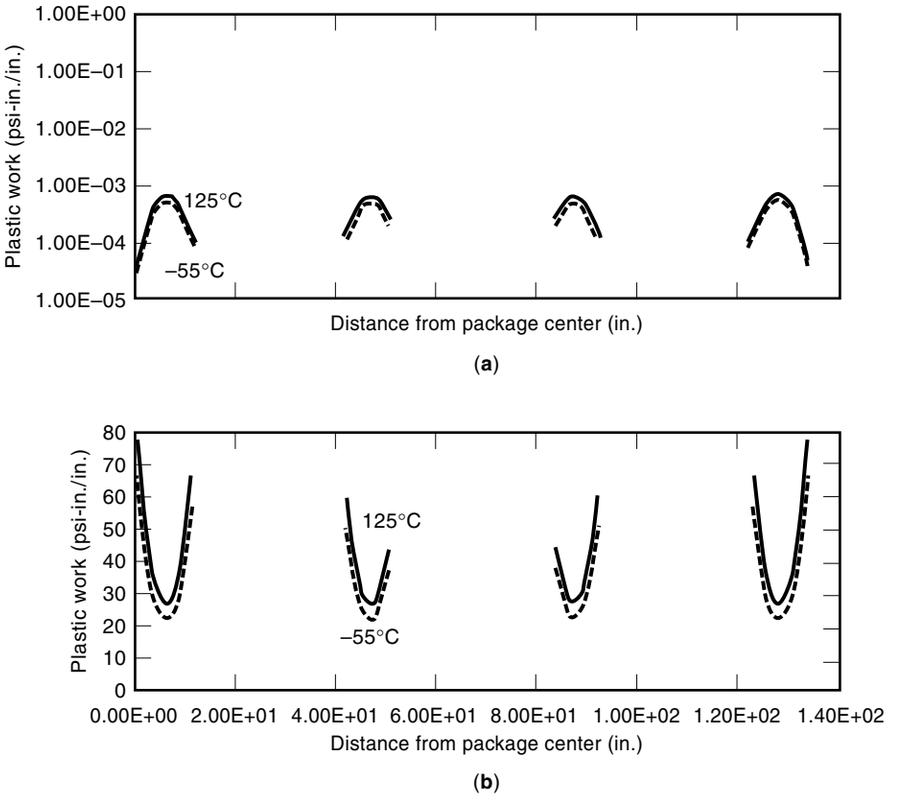

Figure 24. Viscoplastic strain energy density in the solder joints versus distance from the center of the package.

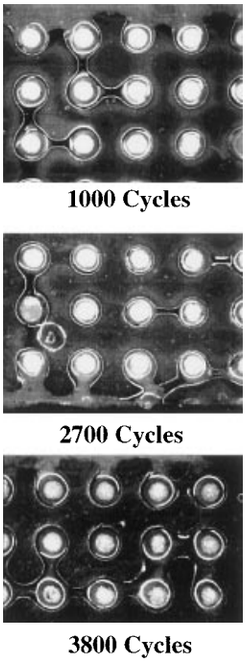

Figure 25. Red-dye-tested virgin non-daisy-chained 48-pin elastomer-on flex interposer CSPs after 3800 cycles of LLTS, −55° to 125°C, 5.8 c/h.

the location of the solder joints with respect to the center of the package. The upper set of curves in each figure indicate the viscoplastic strain energy density at 125°C, and the lower set at −55°C. The average difference between the two curves in each figure indicates the plastic work per cycle. The average magnitude of the plastic work at the flex-solder interface is in the neighborhood of 10^{-4} psi · in./in. (10^{-3} kPa · /m). The average plastic work per cycle at the solder–board interface is in the neighborhood of 6.9 psi · in./in. (48 kPa · m/m). The predicted time to first failure for solder-joint thermal fatigue is in the neighborhood of 23,430 cycles.

Red-dye test of the elastomer-on-flex interposer CSPs (virgin unaged, 48-pin, non-daisy-chained) to identify any cracks in the solder joints revealed no cracking after 1000, 2700, and 3800 cycles of LLTS, −55° to 125°C, 5.8 c/h. Figure 25 shows the red-dye-tested packages; failed joints typically show up as stained red (or dark in the picture). Only one corner of the packages is shown, because typically solder joints directly under the outermost edge of the chip are the first to fail in plastic BGA packages. No crack propagation has been detected after 3800 cycles.

Table 7 shows the failure distribution of the elastomer-on-flex interposer CSPs during LLTS; the failure cause was identified using an identifier. Most of the package failures were due to chip cracking as a result of mechanical damage during test.

Beam-Lead Reliability. Figure 26 shows the parametrization of the beam lead for purposes of reliability simulations, using a length parameter ξ. The parametrization was done to evaluate the stress amplitude and the mean stress in the beam lead during temperature cycling. The stresses have been evaluated on the chip-adjacent layer and the solder-adjacent layer of the beam leads. Four sections of the lead are identified as A, B, C, and D, where A is the length of the lead projecting from the edge of the flex, B is the flex-fillet length of the lead at the flex bend, C is the diagonal length of the lead from the flex fillet to the chip fillet, and D is the chip-fillet length. The stress state predicted from nonlinear finite-element simulations has been used to evaluate the axial stresses along both chip-adjacent layer and the solder-adjacent layer of the beam leads. Table 8 shows the parametric length (ξ) of each of the sections of the beam lead along the chip-adjacent layer and the solder-adjacent layer. The value of ξ at the beginning and end of each section has been indicated versus section and layer name.

The following equations show the transformation relations used to evaluate the maximum stresses along ξ at each layer of the beam lead:

$$\begin{aligned}
\sigma(L_\mathrm{i}, \phi, T) &= \frac{\sigma_x(L_\mathrm{i}, T) + \sigma_z(L_\mathrm{i}, T)}{2} \\
&\quad + \frac{\sigma_x(L_\mathrm{i}, T) - \sigma_z(L_\mathrm{i}, T)}{2} \cos 2\phi \\
&\quad + \tau_{xz}(L_i, T) \sin 2\phi \\
\tau(L_\mathrm{i}, \phi, T) &= \frac{\sigma_x(L_\mathrm{i}, T) - \sigma_z(L_\mathrm{i}, T)}{2} \sin 2\phi \\
&\quad + \tau_{xz}(L_\mathrm{i}, T) \cos 2\phi \\
L_\mathrm{i} &= \mathrm{sa}, \mathrm{ca} \\
\phi &= \phi_1, \phi_2, \phi_3 \\
T &= -55^\circ \text{ to } 125^\circ\mathrm{C}
\end{aligned} \tag{11}$$

where σ_x, σ_z are the stresses perpendicular to the x and z faces, σ_{xz} is the shear stress on the x face in the z direction, σ_{zx} is the shear stress on the z face in the x direction, ϕ is the angle between the lead section and the x axis, T is the temperature, and L_i is the layer parameter (indicating the solder–interface layer and the chip–interface layer). The stress

Table 7. Distribution of Failure Modes during LLTS for a 48-pin Elastomer-on-Flex CSP[a]

	Failure Distribution[b]		
No. of Cycles	Unaged	170°C for 144 h	85°C at 85% RH for 168 h
100–1000	0/7[c]	0/8	0/8
1300	n/e	0/8	n/e
1600	0/6[d]	n/e	0/8
1800	n/e	0/7[d]	n/e
1900	n/e	n/e	0/8
2100	0/6	0/7	n/e
2200	n/e	n/e	0/8
2400	0/6	0/7	0/8
2600	n/e	n/e	0/8
2700	0/5[c]	0/7	0/6[d]
2900	0/5	0/7	0/6
3000	0/5	0/6[d]	0/6
3200	0/5	0/6	
3800	0/4[c]		

[a] −55° to 125°C, 5.8 c/h.
[b] Not evaluated.
[c] Red-dye test.
[d] Chip cracking.

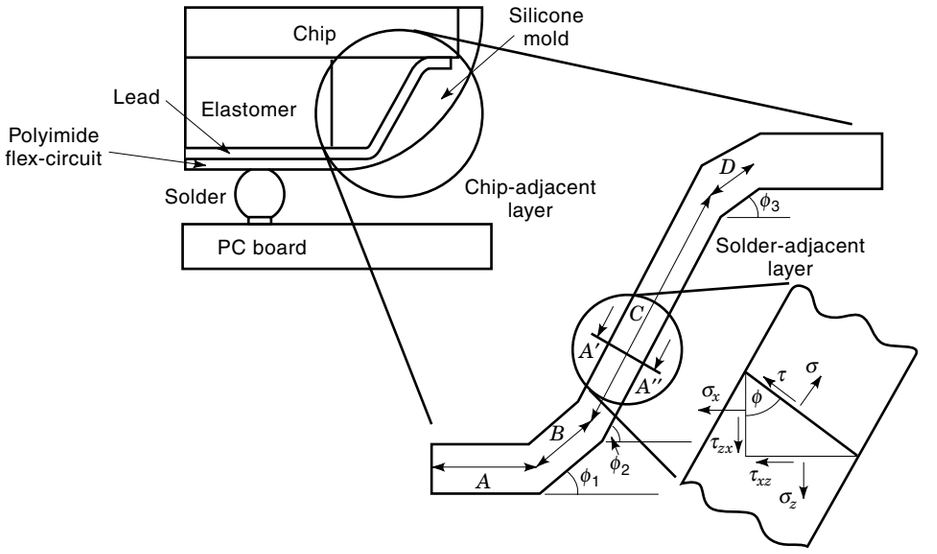

Figure 26. Parametrization of the beam lead for reliability simulation (using the length parameter ξ).

amplitude along each layer is then determined by the following relations,

$$\sigma_a = \frac{\sigma(L_i, \phi, 125^\circ\text{C}) - \sigma(L_i, \phi, -55^\circ\text{C})}{2}$$
$$\sigma_m = \frac{\sigma(L_i, \phi, 125^\circ\text{C}) + \sigma(L_i, \phi, -55^\circ\text{C})}{2} \quad (12)$$

where σ_a, σ_m are the amplitude and the mean stress, and σ is the stress determined from Eq. (11).

Figure 27 shows the model predictions of stress amplitude versus lead length parameter (ξ). The stress amplitude is maximum at the section B—that is, the flex-fillet length of the lead at the flex bend. The maximum stress amplitude is in the neighborhood of 14 ksi to 17 ksi (96.52 MPa to 117.2 MPa). The stress amplitude peaks occur at both the chip-adjacent layer and the solder-adjacent layer of the beam lead. The stress amplitude at the chip-fillet end of the chip-adjacent layer is in the neighborhood of 9 ksi (60 MPa).

Figure 28 shows the model predictions of σ_a/σ_m versus the lead length parameter ξ. This ratio has been examined because an increase or decrease in it results in an increase or decrease in the allowable stress amplitude below the endurance limit, respectively. Further, a negative value of σ_a/σ_m indicates a mean compressive stress, and a positive value indicates a mean tensile stress. Figure 28 shows that along the chip-adjacent layer σ_a/σ_m is in the range of -8 to $+8$, which indicates a very low mean stress (slightly tensile or compressive) and a large stress amplitude over most of the length of the beam lead. This layer is the predicted site of crack propagation during temperature cycling.

Table 8. Parametric Lengths ξ of the Chip-Adjacent Layer and Solder-Adjacent Layer for the Beam Leads

	Parametric Length (in.)			
	Chip-Adjacent Layer		Solder-Adjacent Layer	
Section	Begin	End	Begin	End
A	0	0.0016946	0	0.0030959
B	0.0016946	0.002181	0.0030959	0.00358
C	0.002181	0.0098619	0.00358	0.011262
D	0.0098619	0.103471	0.011262	0.011748

The lead is susceptible to fatigue failure as a result of the reverse bending seen during temperature cycling. The time-to-failure predictions are obtained from the modified Goodman diagram and the S–N diagram. The σ_a/σ_m of 10 to 16 indicates a ϕ of 82° to 87°, which indicates a low allowable mean stress (<6.894 ksi-7 MPa) and a high allowable stress amplitude (endurance limit S_e) for the safe operating region (Fig. 29). The stress amplitude in this case lies outside the safe operating region. The value of the peak stress amplitude is used in the S–N diagram for copper to calculate the fatigue life for the beam lead, which is in the neighborhood of 400 cycles (Fig. 30).

The daisy-chained 40-pin elastomer-on-flex interposer CSPs (single-sourced) were subjected to LLTS with three sets of preconditioning: (a) unaged, (b) thermal aging at 170°C for 144 h, and (c) humid aging at 85°C and 85% RH for 168 h. Figure 31 shows the cross section of an elastomer-on-flex interposer CSP after failure at 500 cycles of LLTS (−55° to 125°C, 5.8 c/h). Table 9 shows the failure distribution of elastomer-on-flex interposer CSPs after LLTS.

Figure 32 shows the solder-joint locations that showed resistance increase when the package was probed after the LLTS test. However, the solder joints did not fail, because the package continued to show an increased resistance after it was removed from the board. Several of the packages showed inner-joint resistance opens before any of the corner joints showed any resistance increase—this is not typical of solder-joint fatigue failures. The solder joints were traced to the beam leads. It was found that noncorner solder joints connect to corner beam lead locations. Figure 33 shows the lead locations that failed after LLTS test.

Comparison of Thermal Fatigue Reliability: CSP versus 1.5 mm Pitch OMPAC

Figure 34 shows the thermal fatigue reliability for the partial-array BGA (0.5 mm pitch, 48 I/O), elastomer-on-flex package (0.65 mm pitch, 48 I/O), and flex-substrate BGA (0.8 mm

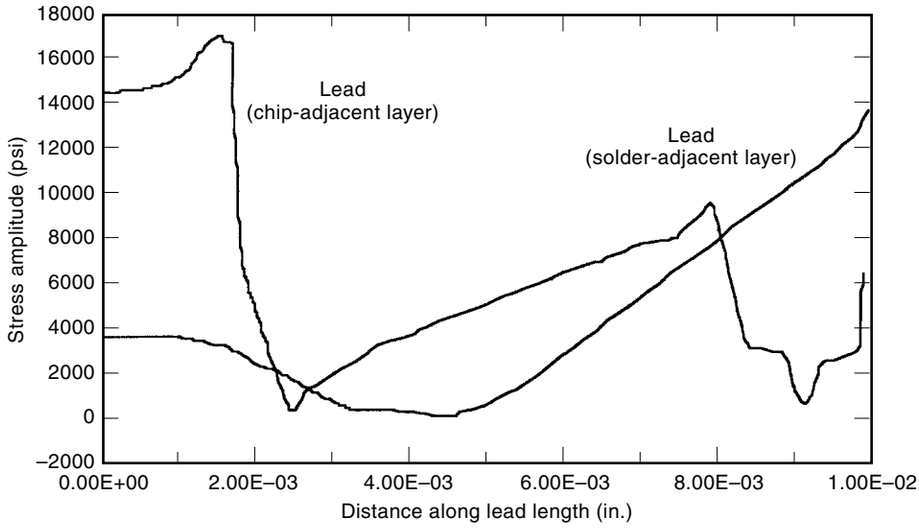

Figure 27. Stress amplitude at the chip-adjacent and solder-adjacent layers versus lead parametric length ξ.

pitch, 48 I/O). The Weibull distribution distinguishes between failure mechanisms by difference in the slopes of the distributions. The similarity in the slopes of the flex-substrate BGA and the partial-array BGA packages is because of similarity in the mechanisms of failure—solder-joint fatigue. The difference in the slope of the elastomer-on-flex package is because of a different failure mechanism—beam-lead failure. Figure 35 shows the normalized accelerated-test time to first failure of the packages (LLTS, −55° to 125°C, 5.8 c/h) versus package type.

The glob-top BGA (1 mm pitch, 196 I/O) has a TTF 1.6 times that of the OMPAC (1.5 mm pitch, 68 I/O). The partial-array BGA (0.5 mm pitch, 48 I/O) has a TTF 0.88 times that of the OMPAC. The elastomer-on-flex package (0.65 mm pitch, 48I/O) has a TTF 0.68 times that of the OMPAC. The dominant failure mechanism for the elastomer-on-flex package is different than for the OMPAC—the former fails by lead fatigue internal to the package. The flex-substrate BGA (0.8 mm pitch, 48 I/O) has a TTF 0.48 times that of the OMPAC (1.5 mm pitch, 68 I/O). Its cominant failure mechanism is similar to that of the OMPAC: solder-joint fatigue at the package-to-solder-joint interface.

Acceleration Transforms

An acceleration transform is a relationship between accelerated test life of a product and its field life. An environmental usage profile has been developed, based on the usage profile of a handheld portable product (e.g. cellular phone), typical environmental extremes, and the measured thermal behavior of the radio. The profiles (Fig. 36) have been developed for two distinct environmental conditions—extreme heat and cold. Nonlinear finite-element simulations have been run to evaluate the field life and correlate LLTS cycles with years of field life.

Acceleration transforms have been derived based on nonlinear finite-element model predictions. An acceleration transform quantifies the acceleration factor for an accelerated test environment by comparison with actual field use environments. The acceleration transform is in turn determined by

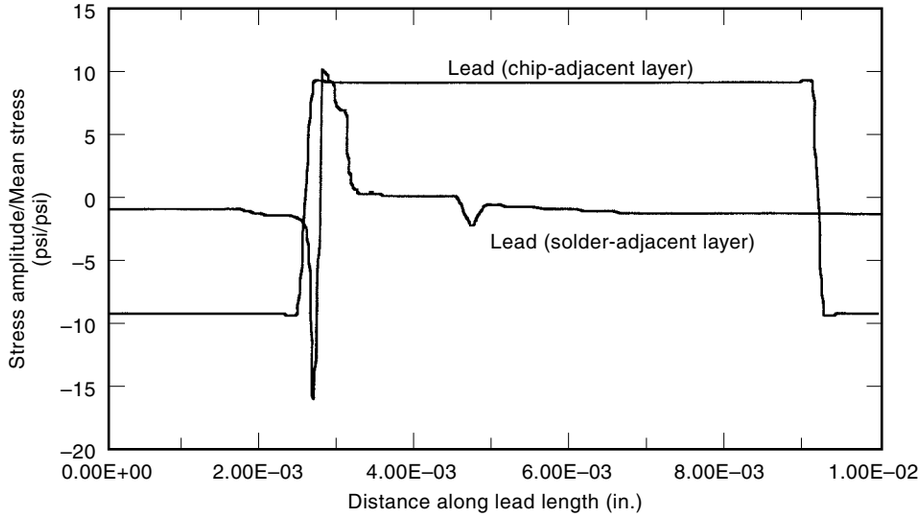

Figure 28. (Stress amplitude)/(mean stress) versus lead length parameter x.

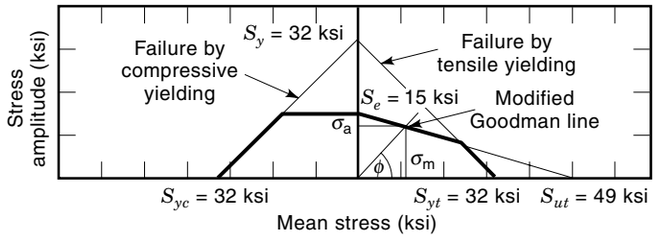

Figure 29. Modified Goodman diagram for copper beam lead.

several variables, including the component and board geometry, materials, and architecture and (most importantly) the field profile. Ideally, one would like to have one acceleration transform that could be used to evaluate the field life once the life in accelerated test has been found.

Unfortunately, there is no universal acceleration transform; further, there can be no such relationship. The reason is that the variables that influence the acceleration transform vary from component to component and thus can be derived only for a class of components (e.g., plastic BGAs, ceramic BGAs, TSOPs, or pendulums) in specific product architectures. Care has to be exercised in using such a simplification of the damage mechanics as the acceleration transform.

The acceleration transform lumps into itself several geometry and architecture variables integral to the component, the solder-joint geometry, and the assumed field profile. If any of the variables change, the acceleration transform must change. For this reason, acceleration transforms make sense only for a particular set of conditions and for particular components. The field profile is the temperature–time plot of the field environment for a radio. The acceleration transform represents the relationship between accelerated test life and field life for a particular accelerated test and a particular field profile. Solder is viscoplastic in nature, which means that it is sensitive to the absolute temperature, temperature ramp rate, and time spent at a given temperature. Changes in either the field profile or accelerated-test conditions change the damage sustained in solder and thus the joint reliability. For this reason, the acceleration transforms presented in this subsection are valid only for the accelerated-test conditions and environmental profiles for which they have been derived.

Figure 37 shows the acceleration transforms for the 0.5 mm pitch, 48-I/O package and the flex-substrate BGA 0.8 mm pitch, 48-I/O package. The vertical bars indicate the time to first failure for the package in each environment. The acceleration transforms can be used to calculate the accelerated test requirement for each package or, inversely, predict the field life in any field use environment, or a combination of the two. It is known from Miner's superposition rule that

$$\sum_{i=1}^{m} \frac{n_i}{N_i} = 1 \tag{13}$$

where n_i is the number of cycles in a particular environment i, and N_i is the number of cycles to failure in the same environment, Miner's superposition rule states that the cumulative damage at end of life will be equal to 1. For example, the accelerated test requirement for a 10 year field life can be calculated, based on Fig. 37 and Miner's superposition, as follows: n_i = 10 years; N_i = 15 years for an extremely hot environment (m = 1); and N_i = 1025 for the accelerated-test environment. We find

$$n_i = \frac{10}{15} \times 1025 = 684 \,\text{cycles} \tag{14}$$

Thus, 684 cycles of LLTS are required for the 0.5 mm pitch, 48-I/O package to guarantee a 5 year life in extreme heat.

The above method can also be used to calculate the accelerated test requirement for any combination of the above environments. For example, we may want to calculate the accelerated-test requirement for a product that will be in extreme heat for 6 years and in extreme cold for 4 years. Then n_1 = 6 years, N_1 = 15 years for the extremely hot environment; n_2 = 4 years, N_2 = 25 years for the extremely cold environment; and N_i = 1025 for the accelerated-test environment. We find

$$n_i = \left(\frac{6}{15} + \frac{4}{25}\right) \times 1025 = 574 \,\text{cycles} \tag{15}$$

Thus, 574 cycles of LLTS are required for the 0.5 mm pitch, 48-I/O package to guarantee a 10 year life (6 years in extreme heat and 4 years in extreme cold).

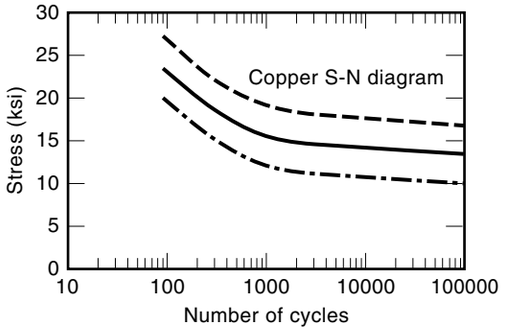

Figure 30. *S–N* diagram for copper (data from *Mark's Handbook for Mechanical Engineers; ASM Metals Handbook*).

Popcorn Susceptibility of the Elastomer-on-Flex Interposer CSPs

The popcorn susceptibility for the 40-pin elastomer-on-flex CSPs was characterized by aging the packages at 85°C and 85% RH for 168 h. The packages were then subjected to two reflows and CSAMed after each reflow. CSAM images show no delamination at the chip–elastomer interface (Fig. 38). The packages used in the study were daisy-chained through the chip. The packages showed no increase in resistance compared to virgin packages.

Moisture and Thermal Sensitivity of Elastomer-on-Flex Interposer CSPs

Figure 39 shows the red-dye test of 48-pin elastomer-on-flex interposer CSPs that were subjected to (a) 85°C and 85% RH for 168 h followed by LLTS, −55° to 125°C, 5.8 c/h, and (b) 170°C for 144 h, followed by LLTS, −55° to 125°C, 5.8 c/h. None of the packages show any crack propagation after 3800 cycles of LLTS. The 40-pin elastomer-on-flex interposer CSPs were subjected to the same preconditioning as in (a) and (b) above, and then subjected to LLTS, −55° to 125°C, 5.8 c/h. The packages were examined under an acoustic microscope to detect any delamination at the chip–elastomer interface and

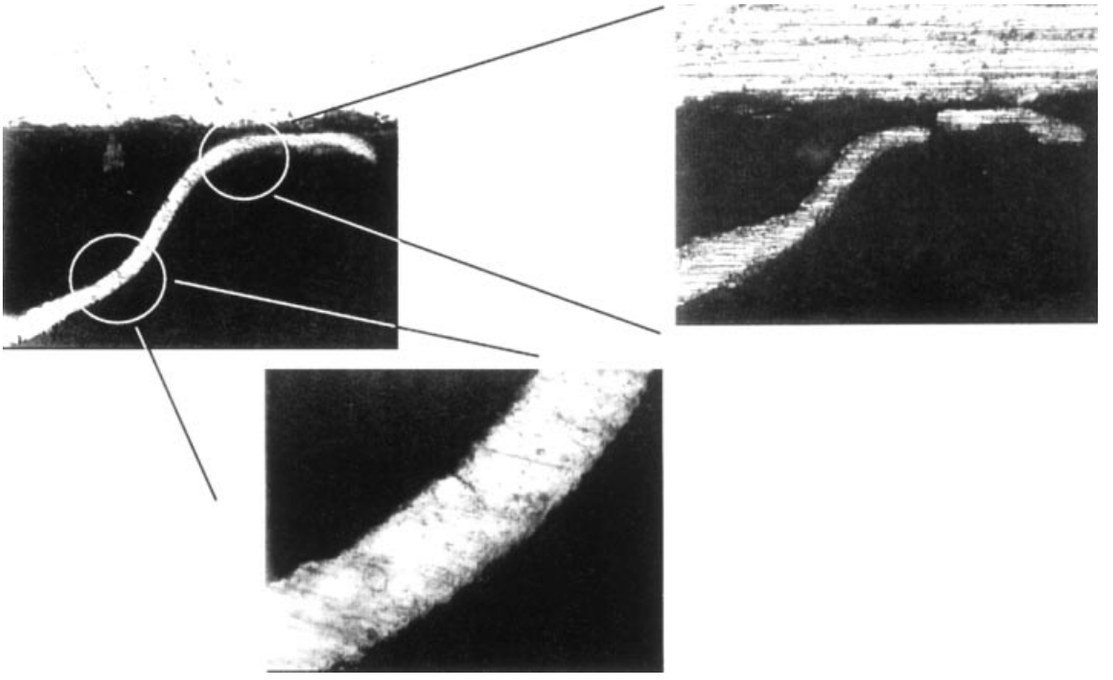

Figure 31. Cross section of 40-pin elastomer-on-flex interposer CSP, showing fracture of copper lead after 500 cycles of LLTS (−55° to 125°C, 5.8 c/h).

at the flex–elastomer interface. No delamination was observed at any of the interfaces after 100 cycles of LLTS.

Out-of-Plane Deformation Reliability

Interface Strength and Simulation. Two configurations of sandwich specimens were constructed to evaluate the strength of the chip–elastomer interface and the solder–flex interface: (a) a chip–elastomer sandwich specimen, and (b) a package-board sandwich specimen. The two configurations were pull-tested and the load at failure measured. Figure 40 shows the stress at failure for the interfaces measured. The elastomer–chip interface showed a mean stress at failure of 397.48 psi (2.704 MPa), and the solder–package interface showed a mean stress at failure of 3049.92 psi (21.0291 MPa). This correlates well with the out-of-plane deformation model predictions, which show an average stress of 3212 psi (22.15 MPa) in the outermost joint at failure.

Solder-Joint Reliability. The packages were soldered onto daisy-chained test boards for out-of-plane deformation reliability assessment in the following configurations (Table 10): (a) glob-top BGA (0.8 mm thick, 196 I/O) on 0.8 mm thick Ni–Au finish board; (b) elastomer-on-flex packages (48 I/O, 0.65 mm pitch) on 0.8 mm thick Ni–Au finish board; 9c) flex-substrate BGA (48 I/O, 0.8 mm pitch) on 0.8 mm thick Ni–Au finish board; (d) partial-array BGA (48 I/O, 0.5 mm pitch) on

Table 9. Failure Distribution of 40-pin Elastomer-on-Flex Interposer CSPs during LLTS[a]

No. of Cycles	Failure Distribution		
	Unaged	170°C for 144 h	85°C at 85% RH for 168 h
100	0/8	0/8	0/6
200	0/8	0/8	0/6
300	0/8	0/8	0/6
400	0/8	0/8	0/6
500	1/8[b]	1/8[b]	1/8[b]
600	3/8[b]	3/8[b]	2/8[b]
700	4/8[b]	3/8[b]	2/8[b]
800	4/8		
900	7/8[b]		
1000	8/8[b]		

[a] −55° to 125°C, 5.8 c/h.
[b] Resistance change.

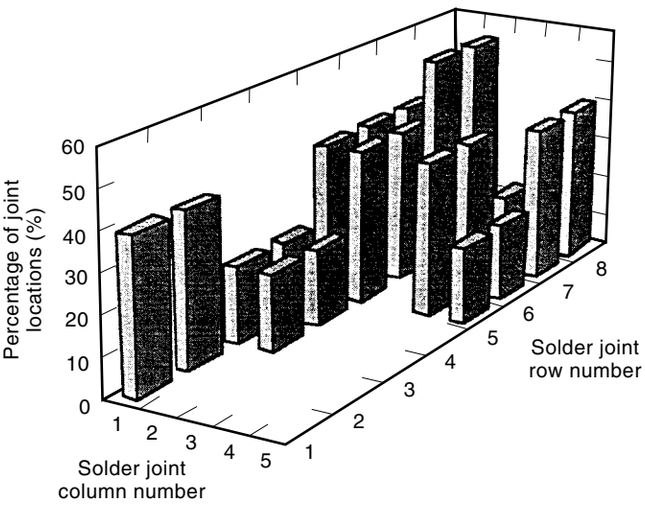

Figure 32. Solder-joint locations showing a resistance increase when probed after LLTS test.

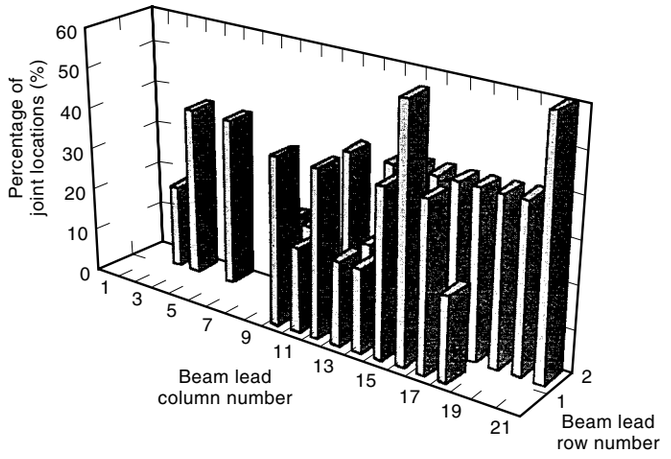

Figure 33. Beam-lead locations showing a resistance increase when probed after LLTS test.

a 1.2 mm thick OPC-finish board; (e) PBGA (48 I/O, 0.8 mm pitch) on a 1.2 mm thick organic protective coating (OPC) finish board. The data were benchmarked versus 1.5 mm pitch OMPAC on a OPC-finish board. The boards were tested on a 1 in. (2.5 cm) span, using an instron at a crosshead speed of 1 mil/s (25 μm/s). The force–displacement behavior was recorded. The resistance of the parts was measured in situ, and the first occurrence of high resistance was treated as a failure. A smaller value of the radius of curvature indicates a tighter bend radius and thus is more desirable.

Figure 41 shows the radius of curvature at failure versus package type in a three-point bend test for an elastomer-on-flex package (D), a 196-I/O glob-top BGA (B), a 68-I/O OMPAC (A), and a flex-substrate BGA (C). (All packages were on PC boards with immersion Ni–Au finish.) The data were benchmarked against 68-I/O OMPAC packages on PC boards of 55 mil (1.4 mm) thickness with OPC finish. The straight lines connecting the failure loads at the two conditions indicate the change in means, the vertical bars are the error bars, the rectangular boxes are the quantiles (horizontal lines show the 10th, 25th, 75th, and 90th quantiles), the diamonds indicate the 95% confidence interval and the group mean, and the horizontal dashed line indicates the standard deviation. The elastomer-on-flex packages (D) had a mean radius of curvature at failure in the neighborhood of 1.58 in. (4.01 cm), which is statistically different from the 68-I/O, 1.5 mm pitch OMPAC (A) (indicated by the nonoverlapping circles from the Student's t test and the Tukey–Kramer test). The flex-substrate BGA (C) had a mean radius of curvature in the neighborhood of 2.17 in. (5.51 cm), which is also statistically different from the 68-I/O, 1.5 mm pitch OMPAC (A). However, there is no significant difference between the elastomer-on-flex package and the flex-substrate BGA. The glob-top BGA (B) failed at a mean radius of curvature in neighborhood of 7.21 in. (18.3 cm), which is at least 3 times larger than for either the elastomer-on-flex package (D) or the flex-substrate BGA (C).

Figure 42 shows the radius of curvature at failure versus package type in a three-point bend test for packages on 1.2 mm thick PC boards with OPC finish. The 0.8 mm pitch, 48-I/O PBGA package (G) showed a mean radius of curvature at failure in the neighborhood of 1.38 in. (3.51 cm), which is 0.44 times that for an OMPAC (A). The 0.5 mm pitch, 48-I/O package (F) showed a mean radius of curvature at failure in the neighborhood of 1.16 in. (2.95 cm), which is 0.37 times that for an OMPAC (A). The 0.8 mm pitch, 48-I/O elastomer-on-flex package (E) showed a mean radius of curvature in the neighborhood of 1.55 in. (3.94 cm), which is 0.49 times that for an OMPAC (A). There was no statistically significant difference in mean radius of curvature between the elastomer-on-flex packages (E), partial-array BGAs (F), and 0.8 mm pitch PBGAs (G).

Aging was performed to simulate the effect of long-term field operation at high temperature and to evaluate the effect of decrease in out-of-plane deformation reliability due to ex-

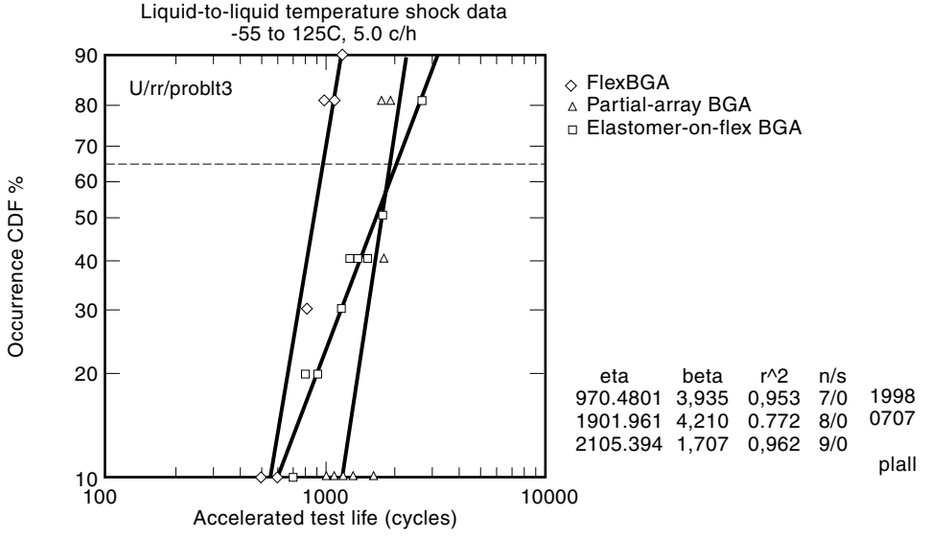

Figure 34. Weibull distributions for the flex-substrate BGA package, elastomer-on-flex package, and partial-array BGA package subjected to LLTS, −55° to 125°C, 5.8 c/h.

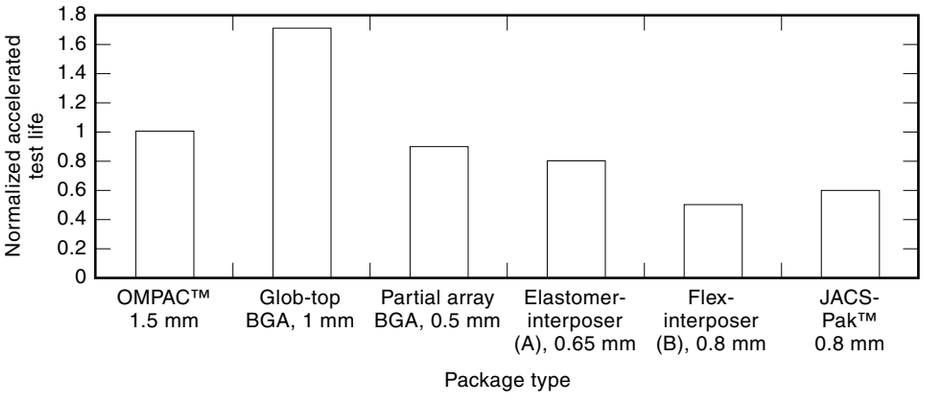

Figure 35. Comparison of the thermal fatigue reliability for the partial-array BGA (0.5 mm pitch, 48 I/O), elastomer-on-flex package (0.65 mm pitch, 48 I/O), flex-substrate BGA (0.8 mm pitch, 48 I/O), and glob-top BGA (1 mm pitch, 196 I/O) versus OMPAC (1.5 mm pitch, 68 I/O).

cessive intermetallics. Intermetallic formation follows an exponential dependence on temperature and a parabolic dependence on time:

$$D = D_0 e^{Q_a/RT}$$
$$x = \sqrt{Dt} \tag{16}$$

where D is the diffusivity of the metals at the solder-joint interface (m^2/h), D_0 is the diffusion coefficient (1.336 m^2/h), x is the intermetallic layer thickness (m), R is the universal gas constant (8.31 J/mol K), Q_a is the activation energy for intermetallic formation (112 kJ/mol, which is the worst-case value reported in the literature), t is the time (hs), and T is the temperature (K).

Figure 43 shows the effect of aging on the mean radius of curvature at failure versus package type in a three-point bend test on 1.2 mm thick PC boards with Ni–Au finish, after aging. All packages were tested on PC boards with OPC finish. In general, all the packages showed an increase in the mean radius of curvature; the largest increases were noticed in the glob-top GBA 196-I/O and the OMPAC 68-I/O packages. The relative trend between the radius of curvature at failure for the packages remained more or less the same as before aging. The aged 0.8 mm pitch, 48-I/O PBGA package showed a mean radius of curvature at failure in the neighborhood of 2.26 in. (5.74 cm), which is 0.3 times that of an aged OMPAC. The aged 0.5 mm pitch, 48-I/O package showed a mean radius of curvature at failure in the neighborhood of 1.34 in. (3.40 cm), which is 0.18 times that for an aged OMPAC. The 0.8 mm pitch, 48-I/O elastomer-on-flex package showed a mean radius of curvature in the neighborhood of 2.05 in. (5.21 cm), which is 0.28 times that of aged OMPAC. The difference between the aged OMPAC and both the aged PBGA packages is statistically significant. There is, however, no significant difference between the aged elastomer-on-flex and the aged PBGA packages.

Figure 44 shows the cross section of an aged elastomer-on-flex interposer CSP soldered on 1.2 mm thick PC boards with OPC finish, after a three-point bend test. Notice the growth of intermetallic at the board pad–solder interface, which causes the interface to fail preferentially. The three-point-bend radius of curvature increases from a mean of 1.55 in the unaged packages to 2.33 in the aged packages. There is a statistically significant difference between the three-point-bend failure radius of curvature for the aged and unaged 48-pin elastomer-on-flex interposer CSPs.

Figure 45 shows the radius of curvature (R_c) at failure versus package type in a three-point bend test, after aging, for packages soldered on a 0.8 mm thick Ni–Au finish board. The largest effect of aging was noticed on the OMPAC and the flex-substrate BGA packages. The aged elastomer-on-flex packages had R_c at failure in the neighborhood of 2.34 in. (5.94 cm), which is statistically different from that of the aged 1.5 mm pitch, 68-I/O OMPAC. The aged flex-substrate BGA had R_c in the neighborhood of 4.79 in. (12.2 cm), which is also statistically different from that of the aged 1.5 mm pitch 68-

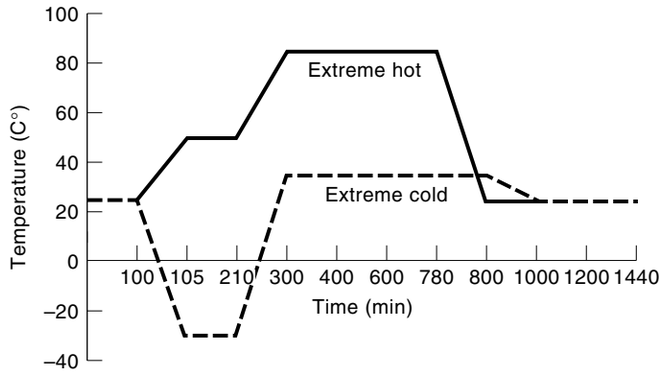

Figure 36. Schematic of temperature profile for extremely hot and extremely cold environments.

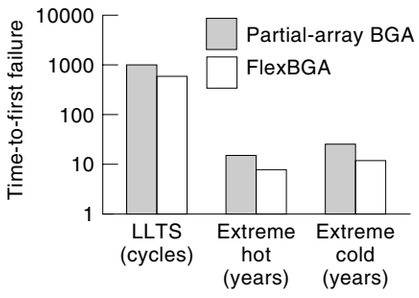

Figure 37. Acceleration transforms for partial-array BGA (0.5 mm pitch, 48-I/O package) and flex-substrate BGA (0.8 mm pitch, 48-I/O package) subjected to thermal fatigue.

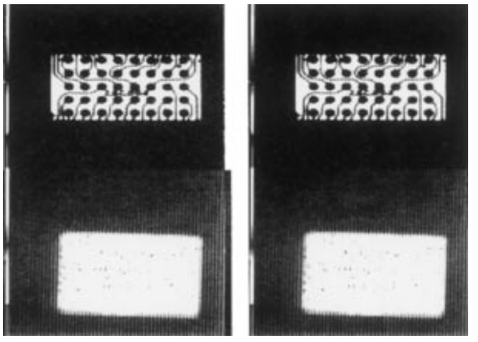

Figure 38. CSAM images of the chip–elastomer interface after (a) 85°C at 85% RH for 168 h and one reflow, (b) 85°C at 85% RH for 168 h and 2 reflows.

I/O OMPAC. Unlike the unaged samples, there is a statistically significant difference between the elastomer-on-flex package and the flex-substrate BGA. The aged glob-top BGA failed at a mean radius of curvature in the neighborhood of 6.14 in. (15.6 cm), which is at least 2 times larger than that of the aged elastomer-on-flex package and 1.5 times larger than that of the aged flex-substrate BGA. Comparison of R_c at failure for unaged versus aged packages reveals a higher R_c for the aged samples, indicating a decrease in the interface strength due to intermetallic growth. The lower R_c for aged glob-top BGA packages is attributed to the decrease in dielectric strength after aging.

Modeling Out-of-Plane Deformation. The out-of-plane deformation of the SLICC package has been modeled. Figure 46 shows the deformed and the undeformed shape of a SLICC package soldered onto a board 30 mil (0.76 mm) thick under an out-of-plane board deformation of 50 mils (1.2 mm), about 2.5 times the board thickness. The force–deflection characteristics from experiment and modeling were found to match closely. The effective in-plane modulus of the bare board was measured from the force–deflection characteristics and used for modeling instead of the bulk modulus of the board material. The reason is that the effective modulus of the board is determined by its layer composition, which can differ by a factor of 4 from the modulus of the bulk material. While an estimate for the effective modulus can be included in the model according to classical laminate plate theory (CLPT), for now, the modulus for modeling purposes was measured experimentally for each board layer composition. Finite Element (FE) models were successfully run for three crosshead rates, for SLICC packages soldered onto boards 55 mil (1.4 mm) thick. For model verification, the effective modulus of three different board thicknesses [31 mils (0.78 mm), 47 mils (1.19 mm), and 59 mils (1.50 mm), double-sided] was measured from the force–deflection characteristics on the Instron. The resulting data will be used in place of the bulk modulus for the board material.

Figure 39. Humidity-aged and thermally aged 48-pin elastomer-on-flex interposer CSPs after red-dye test at 3800 cycles of LLTS, −55° to 125°C, 5.8 c/h.

The outermost package solder joins show maximum plastic deformation. The stress σ_z in the package and underfill solder joints is shown in Fig. 47. In general the area of maximum σ_z for all the joints is on the periphery of the solder joints. The outermost joint shows the maximum stress, which is concentrated at the inner top and the outer bottom of the package solder joint. Under a 50 mil (1.3 mm) out-of-plane deformation, the solder shows a maximum σ_z of $\approx$ 19.8 ksi (136 MPa). The smaller underfill solder joints show approximately one-third the σ_z in package solder joints, $\approx$ 5.3 ksi (37 MPa). Von Mises inelastic strains in the package solder joints were in the neighborhood of 0.6 to 0.7, and the bulk of the solder is in an inelastic range, $>$ 0.3 to 0.4. The underfill solder joints, however, show inelastic strains in the neighborhood of 0.4×10^{-4}, which is consistent with the motivation for the underfill process. From experimental observations, the strain at onset of failure for 62% Sn–36% Sn–2% Ag joints has been noted to be in the range of 0.2 to 0.4, which indicates that for this package geometry, pitch (32 mils, 0.81 mm), solder-joint size (diameter 22.2 mils = 0.564 mm), board thickness (30 mils = 0.76 mm), board size (3 times the package size), and crosshead rate (5 mils/s = 0.12 mm/s), a deformation of 50 (1.2 mm) describes the limit at which the outermost joint would fail in this out-of-plane deformation mode. This translates to a bend radius of 1.94 in. (4.82 cm). The predicted radius of curvature from three-point bend tests for the SLICC package is in the neighborhood of the reported radius of curvature for the 1.0 mm pitch OMPAC package: 1.96 in. (4.98 cm) (5). This makes sense intuitively, because the SLICC package is slightly smaller than the 1.0 mm pitch OMPAC. While extensive testing with a National Instruments LabView setup for the SLICC package is underway, coarse tests done by three-point bending of the package to a predetermined radius of curvature and a subsequent red-dye test have demonstrated that the radius of curvature is in the neighborhood of 2 in. (5 cm). (The red-dye test involves dispensing red dye under the package and removing the package to look for stained solder-joint cross sections, which indicate the presence of cracks.) The maximum inelastic strain value occurs at the outer surface of the outermost solder joints, which is consistent with experimental observations. The stress in the chip is much lower than the modulus of rupture of silicon. The force–deflection characteristics from the instron match the simulation results, and the solder failure location from three-point bend tests matches the finite-element prediction (Figs. 47, 48). Simulations results are consistent with experience that

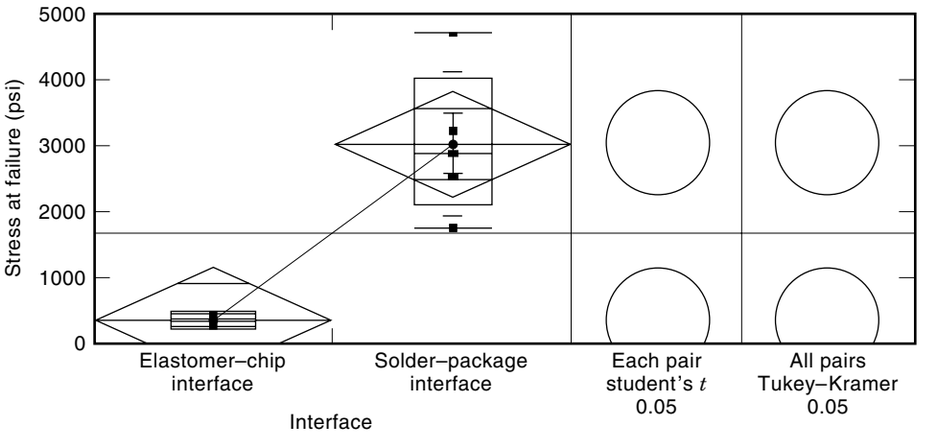

Figure 40. Stress at failure in tensile test for the elastomer-chip interface and the solder-package interface in the elastomer-on-flex interposer CSPs.

increasing board assembly stiffness will reduce stress on solder joints. Simulations also show that either very high board stiffness or very low board stiffness will reduce BGA failure due to out-of-plane deformation.

A thicker board is beneficial mainly because it requires a larger force to produce the same out-of-plane deformation as a thinner board; however, for the same out-of-plane deflection a board with greater stiffness (e.g., a thicker board) will result in larger viscoplastic strain energy density, that is, larger damage to the package solder joints. The resultant of these two opposing factors will determine the design window. While lower strain rates result in more strain being absorbed by the solder, higher board stiffnesses result in larger shear strain in solder for the same out-of-plane deformation. Higher board stiffnesses result in lower stresses but larger strains in the solder joints; higher strain rates result in higher stresses, and in lower strain at a given stress. The result of these effects is that the plot of plastic work per unit volume versus deformation remains more or less same for the different strain rates. Thus, the dominant factor is the board stiffness.

Low-Frequency Repeated Bending

A test fixture has been designed to evaluate the package solder-joint reliability in low-frequency repeated bending (LFRB). LFRB is often experienced by devices during keypad pushes when the user dials a phone number or a radio number. The test setup has been used to acquire data on the 0.8 mm pitch, 48-I/O flex-substrate BGA package and the 196-I/O glob-top BGA assembled on PC boards with a Ni–Au finish. The occurrence of a crack or a failure is indicated by a large voltage drop—during the LFRB, the crack in the solder joint opens and closes, causing the resistance and thus the voltage drop to increase and then drop to near zero. After a few thousand cycles of crack propagation, the crack does not close completely, producing a significant voltage drop at no displacement. Figure 49 shows the number of cycles to failure in LFRB versus package type on a PC board 32 mils (0.81 mm) thick with Ni–Au finish. All the data were acquired at 1 in. (2.5 cm) span in the x and y dimensions with an out-of-plane displacement of 0.25 mm. The glob-top BGA showed a mean number of cycles to failure in the neighborhood of 109,361. The flex-substrate BGA showed a mean number in the neighborhood of 4105.

Figure 50 shows the number of cycles to failure versus board displacement for a 196-I/O glob-top BGA on a PC board 55 mils (1.40 mm) thick with OPC finish subjected to LFRB. The mean number of cycles to failure decreases from 20,000 at 10 mils (0.25 mm) of displacement to 2000 at 20 mils (0.51 mm) of displacement. The number of cycles to failure on a thicker, 55 mil (1.40 mm) board is much lower than on a 32 mil (0.81 mm) PC board because a thicker board requires a larger force to produce the same deflection, but for the same displacement, a thicker board produces more plastic work than a thinner board. Figure 51 shows the cross section of a 196-I/O glob-top BGA subjected to LFRB. The failure is at the package-to-solder interface.

Table 10. Three-Point-Bend Test Configuration

Package	Pitch (mm)	No. of I/Os	Board Thickness (mm)	Finish
Glob-top BGA	1	196	0.8	Ni-Au
Elastomer-on-flex package	0.65	48	0.8	Ni-Au
Flex-substrate BGA	0.8	48	0.8	Ni-Au
Partial-array BGA	0.5	48	1.2	OPC
BGA	0.8	48	1.2	OPC
BGA	1.5	68	1.4	OPC

Optimizing CSP Reliability and Assembly Processes

Often the process and reliability requirements do not point to a unique solution. For example, taller BGA solder joints improve reliability but at the same time are less conducive to stable second-side (the part hanging down) reflow; more solder volume, desirable for enhanced reliability, often also increases the probability of shorts; and so on. The approach developed enables the attainment of the true optimum solder joint design. The tradeoff between the maximum weight of the component that can be supported by the BGA joint during second-side reflow and reliability can thus be assessed early in the design phase, and the design optimized for a desired joint height. This methodology is limited to prediction of the equilibrium solder shape after reflow and does not deal with

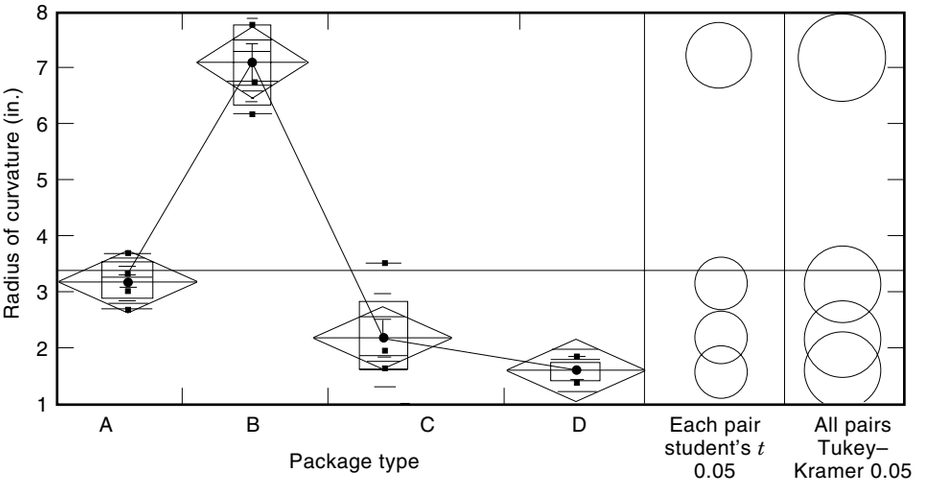

Figure 41. Radius of curvature at failure (in.) versus package type in a three-point bend test. A, OMPAC, 1.5 mm pitch, 68 I/O; B, glob-top BGA, 1 mm pitch, 196 I/O; C, flex-substrate BGA, 0.8 mm pitch, 48 I/O; D, elastomer-on-flex package, 0.65 mm pitch, 48 I/O. All packages on 0.8 mm thick PC boards with Immersion Ni–Au finish.

issues like solder wetting or nonwetting due to contaminants on the pad and the like. It has been developed in response to falloff of a first-side heavy part during second-side reflow. The package is a heavy BGA-format package weighing about 3.394 g. This problem does not exist for typical PBGA and CBGA devices weighing in the neighborhood of 0.5 g to 1.2 g. The packages were carefully examined and showed almost hemispherical solder balls on both the package and the board. This indicated that the problem was not related to wetting and was more likely related to the package design.

Simulation Methodology. The approach addresses the problem of deriving the set of acceptable solutions based on a user-specified set of process and reliability requirements. The process requirements typically include the solder-joint characteristics, including force–joint-height characteristics, solder-joint shape and stability during reflow, and equilibrium joint height after first and second reflow. The reliability requirements typically include field and accelerated-test life. The unique set of acceptable solutions will thus satisfy both the process and reliability requirements (Figs. 52, 53).

Surface Evolver (code from the University of Minnesota) was used to predict the final shape of the BGA joints after reflow, given the pad size, solder volume, and weight of the package. Surface Evolver (6,7) is an interactive program written by Ken Brakke of Susquehanna University for studying surface-tension-defined shapes. Given an initial surface, the program evolves the shape towards a minimum-energy configuration. It uses a gradient descent method to find the local minimum of the energy functional. For the BGA solder-joint simulations, the energy functional consists of potential energy and surface energy terms. A parametric model has been created to simulate joint collapse during reflow, using Surface Evolver parametric language and C language code. The model variables include (Fig. 53) (a) solder volume, (b) pad radius [the initial joint height prior to reflow is calculated from this

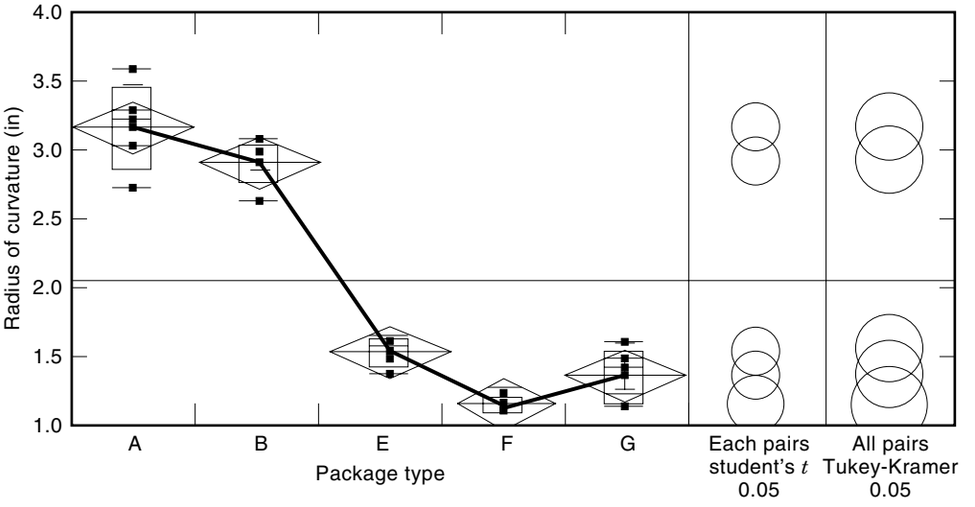

Figure 42. Radius of curvature at failure (in.) versus package type in a three-point bend test. A, OMPAC, 1.5 mm pitch, 68 I/O; B, glob-top BGA, 1 mm pitch, 196 I/O; E, elastomer-on-flex package, 0.75 mm pitch, 48 I/O; F, partial-array BGA, 0.5 mm pitch, 48 I/O; G, PBGA, 0.8 mm pitch, 48 I/O. All packages on 1.2 mm thick PC boards with OPC finish.

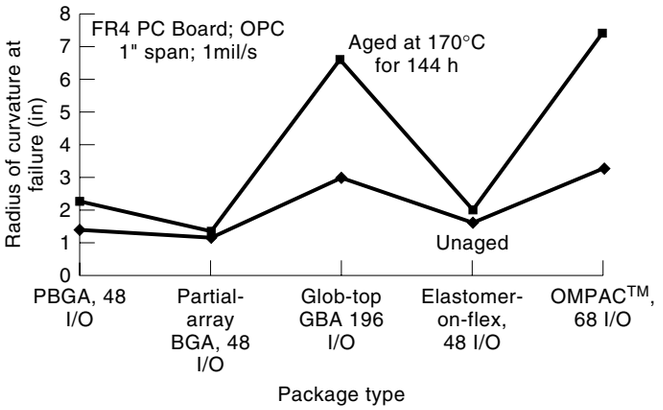

Figure 43. Radius of curvature at failure (in.) versus package type in a three-point bend test (after aging). A, OMPAC, 1.5 mm pitch, 68 I/O; B, glob-top BGA, 1 mm pitch, 196 I/O; E, elastomer-on-flex package, 0.75 mm pitch, 48 I/O; F, partial-array BGA, 0.5 mm pitch, 48 I/O; G, PBGA, 0.8 mm pitch, 48 I/O. All packages on 1.2 mm thick PC boards with OPC finish.

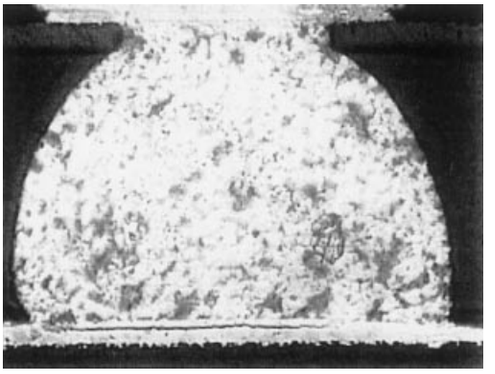

Figure 45. Radius of curvature at failure (in.) versus package type in a three-point bend test (after aging). A, OMPAC, 1.5 mm pitch, 68 I/O; B, glob-top BGA, 1 mm pitch, 196 I/O; C, flex-substrate BGA, 0.8 mm pitch, 48 I/O; D, elastomer-on-flex package, 0.65 mm pitch, 48 I/O. All packages on 0.8 mm thick PC boards with Ni–Au finish.

and (a)], (c) liquid–gas surface energy of the solder, (d) liquid–solid surface energy of the solder–copper interface, (e) density of the solder, (f) weight of the chip, (g) ball diameter, (h) package-to-board misalignment. Based on the user-defined inputs, the model is able to predict the maximum weight of the part that the solder can support.

To simulate the spreading during wetting of the pads, the surface constraints are mapped from an area to the curve surrounding that area. This is done to prevent a minimization of the surface area at the constraints that results in an unstable solution. The function map is done using Stokes's theorem as follows:

$$\begin{aligned} \iint_s \boldsymbol{n} \cdot (\nabla \times \boldsymbol{w})\, ds &= \oint_c \boldsymbol{w} \cdot d\boldsymbol{l} \\ \nabla \times \boldsymbol{w} &= T\hat{\boldsymbol{k}} \\ \boldsymbol{w} &= -Ty\hat{\boldsymbol{i}} \text{ or } Tx\hat{\boldsymbol{j}} \end{aligned} \tag{17}$$

where $\boldsymbol{w}$ is some function describing the constraint, s is the surface area at the constraint, c is the curve bounding the area, and T is the surface tension at the surface. Figure 54 shows how the surface constraints for the BGA joints have been modeled: A_1 is the area of the pad, of which A_2 has been wetted by the solder, and A_3 is the free surface of liquid solder. The energy functional consists of surface energy and potential energy terms:

$$E = \iint_{A_3} \gamma_l\, dA + \iint_{A_2} \gamma_{ls}\, dA + \iint_{A_1 - A_2} \gamma_s\, dA + \iiint_{\Omega} \rho g z\, dV \tag{18}$$

$$= \iint_{A_3} \gamma_l\, dA + \oint_{C_2} (\gamma_{ls} y\hat{\boldsymbol{i}} - \gamma_s y\hat{\boldsymbol{i}}) \cdot d\boldsymbol{l} + \oint_{C_1} \gamma_s y\hat{\boldsymbol{i}} \cdot d\boldsymbol{l} + \iiint_{\Omega} \rho g z\, dV \tag{19}$$

The first three terms in Eq. (18) represent the surface energies of liquid solder, solder–pad interface, and pad surface. The fourth term represents the potential energy of solder. Stokes's theorem has been used to transform the area terms in the energy equation to closed integrals around curves bounding the area. From Eq. (19), it is obvious that at the constraint, the third term is a constant (assuming a completely wet pad, typical of BGA solder joints). Thus, only the

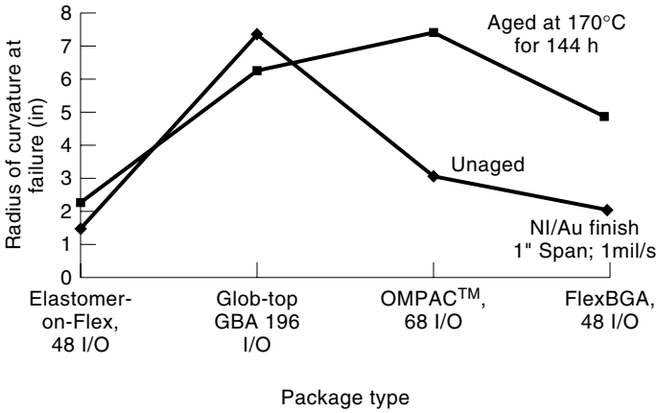

Figure 44. Cross section of aged 48-pin elastomer-on-flex interposer CSPs after three-point bend test.

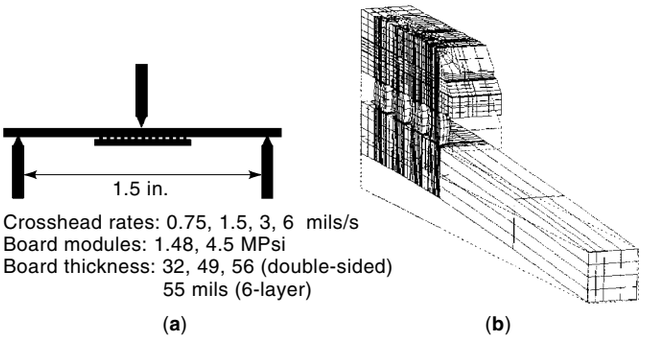

Figure 46. (a) Test setup for the three-point bend test. (b) Package and board geometry before and after out-of-plane deformation of the board.

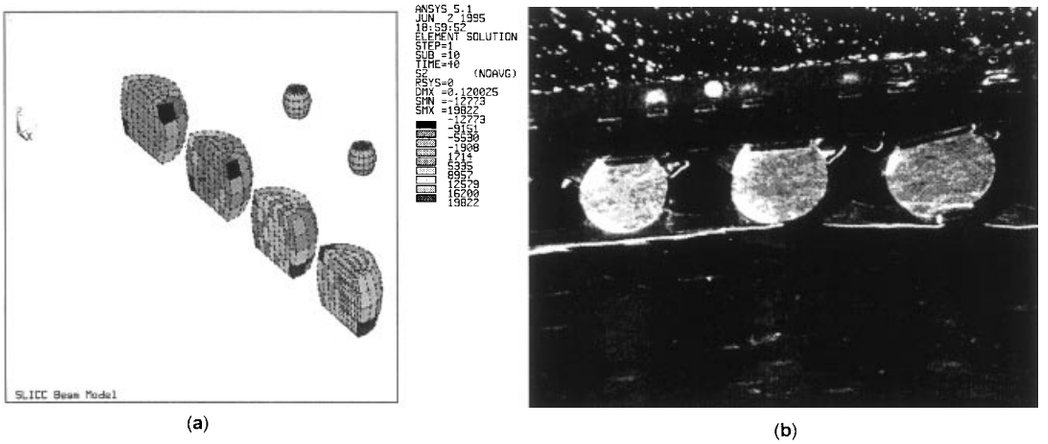

Figure 47. (a) Inelastic σ_z distribution in the solder for the underfill solder joints (smaller joints) and the package solder joints. (b) Cross section of SLICC after three-point bend test.

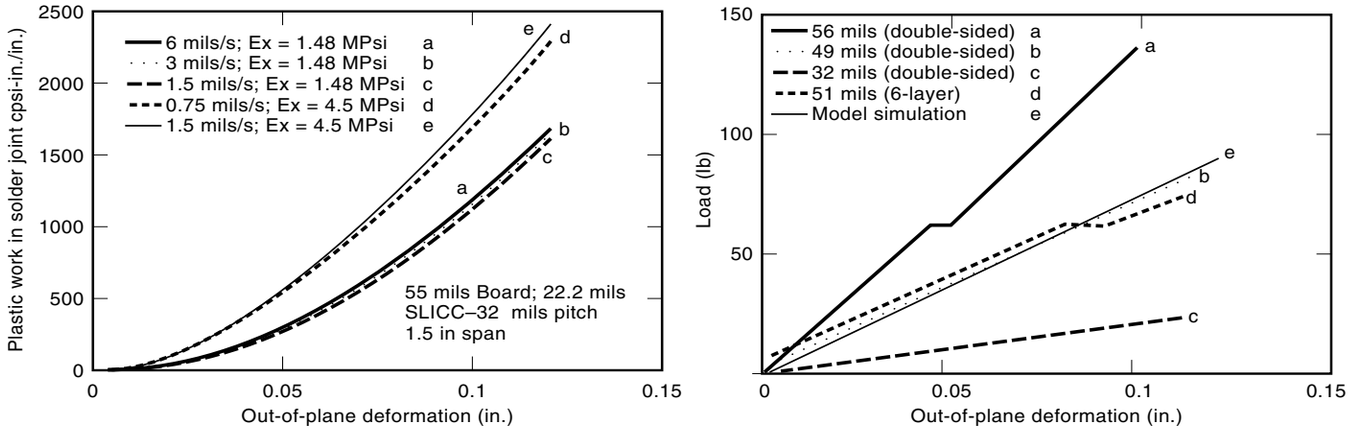

Figure 48. (left) Plastic work in solder joints versus out-of-plane deformation for three-point bend test. (right) Load-versus-deflection characteristics for various board thicknesses and stiffnesses. Predicted force–deflection characteristic is plotted as a dashed line on the graph. Model prediction agrees with experimental data.

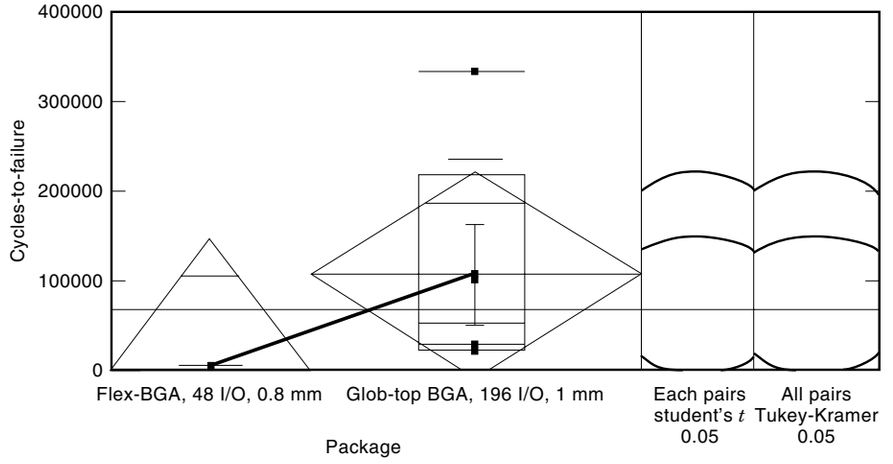

Figure 49. Number of cycles to failure in low-frequency repeated bending versus package type. All the data were acquired at 1 in. (2.5 cm) span in the x and y dimensions with a out-of-plane displacement of 0.25 mm.

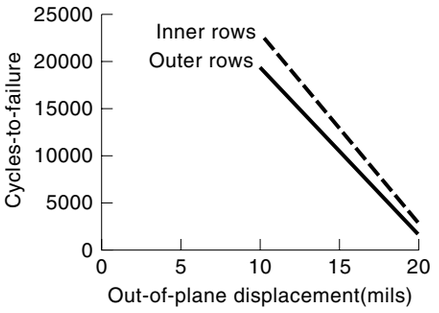

Figure 50. Number of cycles to failure versus board displacement for a 196-I/O glob-top BGA in low-frequency repeated bending.

remaining three terms need to be considered for minimization of the energy functional. The effective surface tension at the constraint is the represented by the second term in Eq. (19).

Translation Interface: Surface Evolver to ANSYS. A translation interface from Surface Evolver to ANSYS has been written to translate models seamlessly for reliability simulations (Fig. 55). Typically Surface Evolver models consist of vertices, edges, and facets. Vertices are joined with straight lines to form edges, three edges form a triangular area called a facet, and facets enclose a volume. All vertex, edge, and facet information is preserved during translation. The translated model can be readily tet-meshed for linear FE analysis. This interface is completely generic and is not specific to the BGA solder-joint model. Typically the user has control over the initial vertex, edge, and facet information inside Surface Evolver. The energy minimization scheme of Surface Evolver requires continual refinement of the surface areas so that the facets can conform accurately to the minimal-energy surface. The final evolved shape (Fig. 56) thus may often consist of hundreds of vertices, edges, and facets. The interface enables the translation of the evolved shape into a commercial finite-element code for nonlinear finite-element simulations for reliability assessment.

Translating a Tet-Meshed Model to a Brick-Meshed Model. Translation subroutines have been written to translate a tet-meshed geometry to an equivalent brick-meshed geometry (Fig. 57). The main reason is that viscoplastic elements used to characterize the time-dependent behavior of solder are much too stiff for tetrahedral-element formulation in large deformation.

Integration into Finite-Element Models for Life Prediction. The translated model has been embedded into component finite-element models in ANSYS (Fig. 58). The major motivation behind this approach is that the solder-joint geometry does not have to be measured from cross sections of the part or nominal values assumed for simulation of reliability. Stresses, strains, displacement, and plastic work (where applicable) are calculated from environmental loads such as the thermal cycle, thermal shock, and out-of-plane deformation.

Model Predictions. Figures 59 and 60 show the net vertical force and energy for the joint as a function of joint height. The equilibrium joint shape without the chip corresponds to the point of minimum energy—this is shown by the plot of energy versus force per joint. The condition of minimum en-

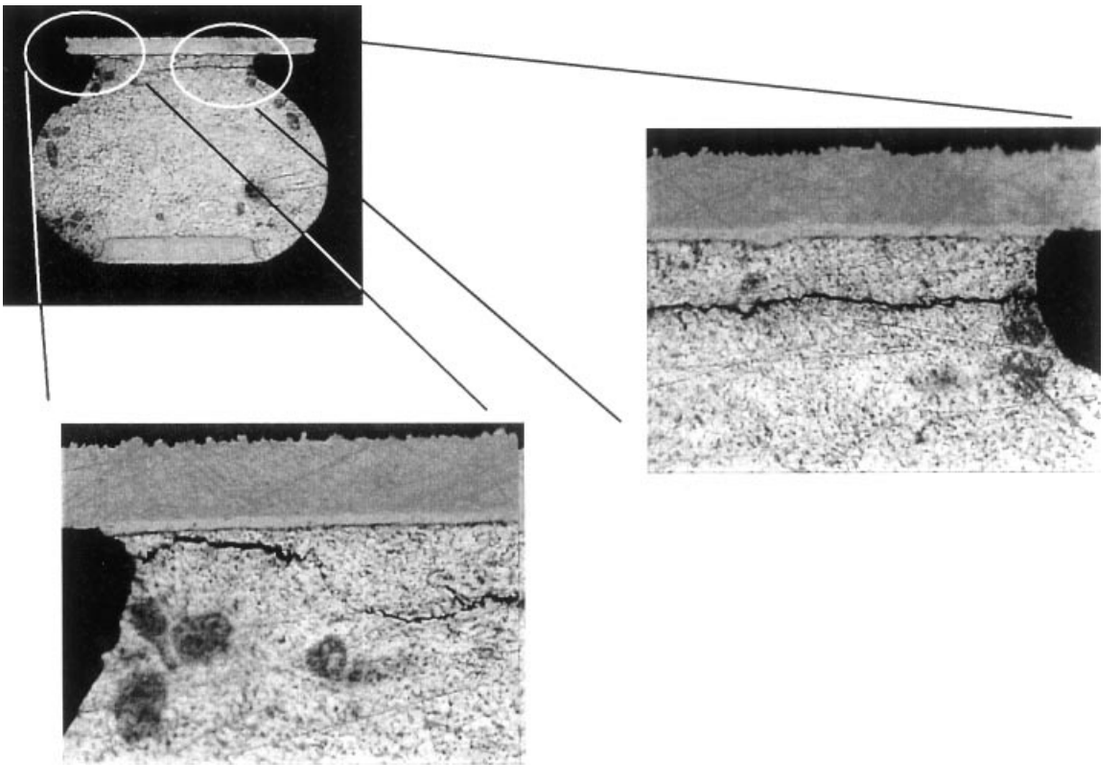

Figure 51. Cross section of a 196-I/O glob-top BGA subjected to low-frequency repeated bending.

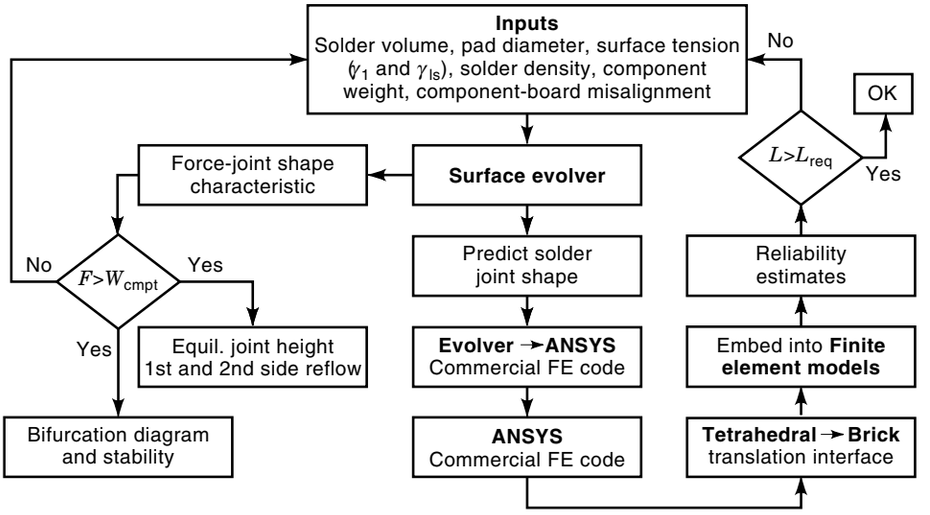

Figure 52. Methodology for optimal design based on process and reliability requirements.

ergy for the equilibrium holds for any chip weight, because the force is determined as the negative gradient of energy with respect to displacement along that direction: mathematically,

$$F = -\frac{\partial E}{\partial h} \tag{20}$$

where F is the force, E is the energy, and h is the displacement along the direction of F. Simulation variables include: (a) ball diameter: 25 mils (0.63 mm, 1.3407×10^{-10} m^3), 30 mils (0.76 mm, 2.3167×10^{-10} m^3), or 35 mils (0.89 mm, 3.6788×10^{-10} m^3); (b) pad diameter: 25 mils (0.63 mm, 3.175×10^{-4} m^2), 30 mils (0.76 mm, 3.81×10^{-4} m^2), or 35 mils (0.89 mm, 4.445×10^{-4} m^2).

Figure 59 shows the predictions of force per joint (N) versus joint height (m) obtained from the simulations for pad diameters including the above values, for constant solder volume corresponding to 30 mil ball diameter. The chip weight per joint is shown as a solid line with the $\pm 3\sigma$ shown by the dashed lines. To prevent the chip from falling, the force per joint has to be larger than the chip weight per joint. Predictions of force–displacement characteristic for the present configuration (30 mil ball on 30 mil pad) indicate that during second-side reflow, even though the retention force per joint is larger than the chip weight per joint, any movement or mishandling resulting in an increase in joint height will cause the part to fall off. The reason is that the force per joint does not increase with any further increase in joint height, so that the configuration is unstable with respect to additional loads from vibration and handling (Figs. 59 and 60). Predictions indicate that an increase in the pad diameter from 30 mils to 35 mils will increase the force per joint during second-side reflow. A decrease in the pad diameter from 30 mils to 25 mils will reduce the force per joint and is thus not desirable. A positive value of the retention force in Figs. 59 and 60 indicates an opposing tensile force exerted by the joint (as in the part hanging from the board during second-side reflow), and a negative value of the retention force indicates an opposing compressive force exerted by the joint (as in the part sitting on the board during first-side reflow).

Figure 60 shows the predictions of force per joint (N) versus joint height (m) obtained from the simulations for ball diameters including 25 mils, 30 mils, and 35 mils, for constant pad diameter of 30 mils. Predictions from the simulations indicate that using a smaller ball size (25 mils) will increase the force per joint during second-side reflow by 1.5 times over the present configuration (30 mil ball diameter). Using a larger ball diameter (35 mils ball diameter) will reduce the force per joint and is thus not desirable. Figure 61

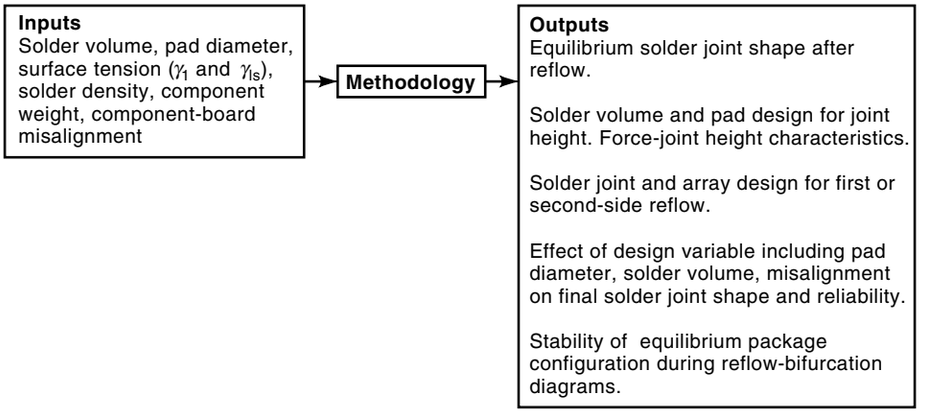

Figure 53. Inputs to and outputs from the methodology.

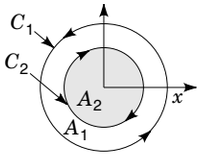

Figure 54. Transformation from area to curve on constraints.

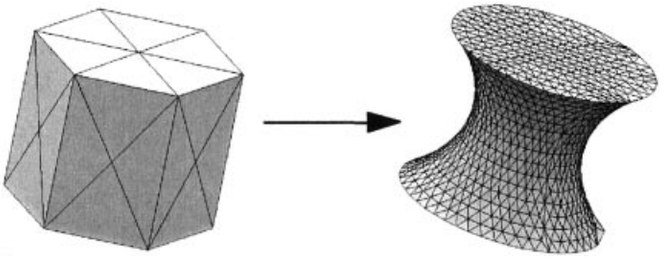

Figure 55. Surface evolver-to-ANSYS interface.

shows the predicted equilibrium joint height for first and second reflow versus pad diameter and ball diameter. It can be seen that smaller ball diameter and larger pad diameter increase the stiffness of the solder system and thus reduce the increase in solder-joint height from first to second reflow.

Closed-Form Solution. A closed-form solution based on Heinrich's approach (8) has been used to predict the force–joint-height characteristic; the numerical solution is limited to joints without any misalignment. The method involves calculating the normalized solder volume (V_n) and the truncated solder volume (V_t), given by

$$V_n = \frac{V}{h^3} \tag{21}$$

$$V_t = \frac{\pi}{3}\frac{\rho_s^3 - \rho_c^3}{\rho_s - \rho_c} \tag{22}$$

where ρ_s is the normalized pad radius at the substrate ($= r_s/h$), ρ_c is the normalized pad radius at the BGA part ($= r_c/h$), V is the volume of solder, and h is the height of the solder joint. If normalized solder volume (V_n) is greater than the truncated solder volume (V_t), then the solder joint is barrel-shaped; if V_n is smaller than V_t, then the solder joint is hourglass-shaped. The radius of curvature ($\overline{R}$) of the solder joint is then calculated iteratively so that the calculated volume V_c of solder matches the normalized solder volume V_n, where

$$\overline{R} = \tfrac{1}{2}[(\rho_s + \rho_c)^2 + 1] \tag{23}$$

$$V_c = \pi\{R^2 - \zeta_0^2 + \zeta_0 - \tfrac{1}{3} + \rho_0[\rho_c + \zeta_0(\rho_s - \rho_c)]\} \pm \rho_0\overline{R}^2\left[\cos^{-1}\left(\frac{1-\zeta_0}{\overline{R}}\right) - \cos^{-1}\left(-\frac{\zeta_0}{\overline{R}}\right)\right] \tag{24}$$

and ρ_0 and ζ_0 are the normalized coordinates of the center of curvature of the solder arc. The force exerted by the joint is represented by

$$\overline{F} = \frac{\pi\rho_0}{2\overline{R}}\left(\mp(\rho_1 + \rho_2) - \sqrt{\frac{4\overline{R}^2}{(\rho_1 + \rho_2)^2 + 1} - 1}\right) \tag{25}$$

where λ is the surface tension of molten solder (0.376 J/m^2) in the presence of flux and nitrogen atmosphere, and F is the compressive force—that is, a positive value of F corresponds to a compressive force, meaning that a concave solder joint pulls on the component.

The closed-form solution is however not as generic as the numerical solution based on Surface Evolver. The assumptions for it include: (a) the molten solder bump has attained static equilibrium shape when solidification occurs; (b) the contact pads on the components and the substrate are circular and are aligned at the time of solder solidification; (c) the

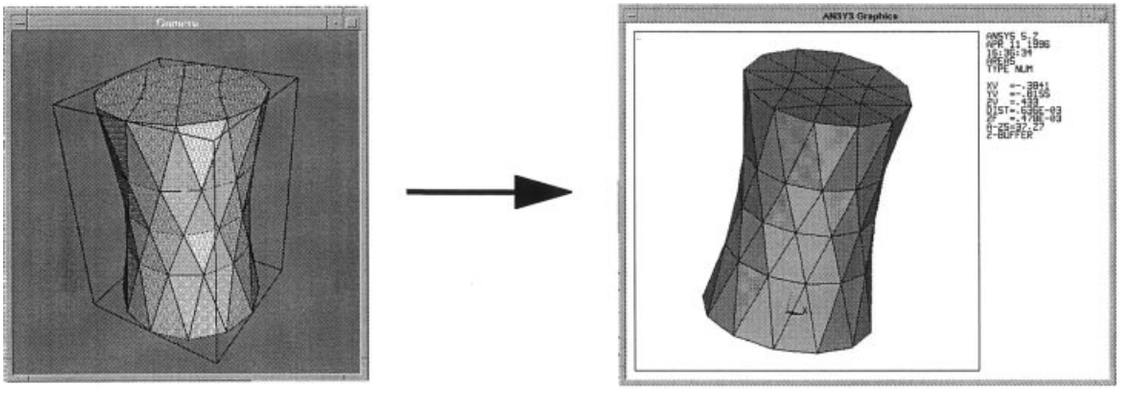

Figure 56. Evolution of solder-joint shape.

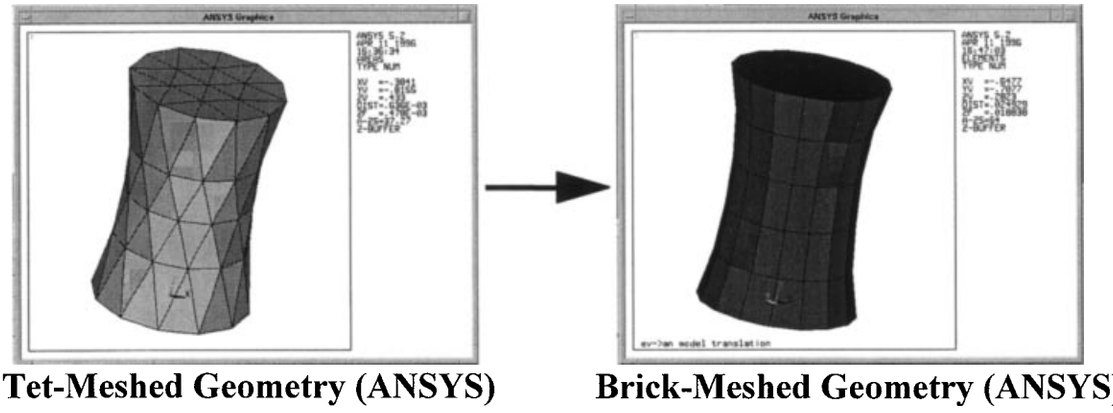

Figure 57. Translation of a tet-meshed geometry to a brick-meshed geometry.

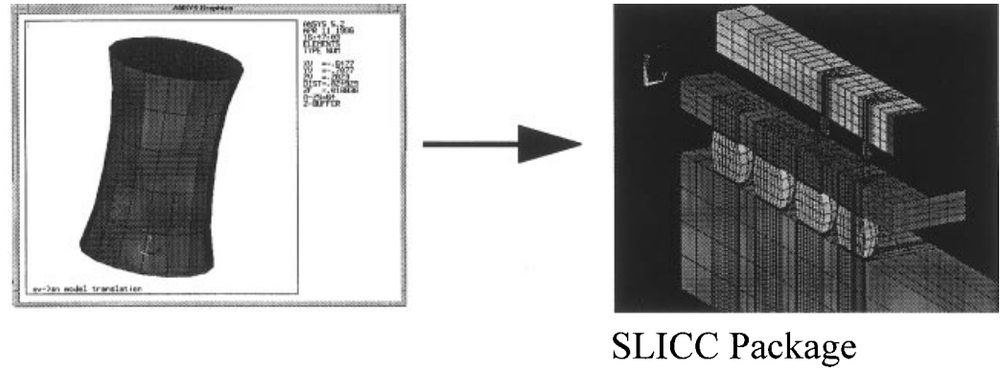

Figure 58. Translated solder-joint geometry has been embedded into the finite-element models for life prediction.

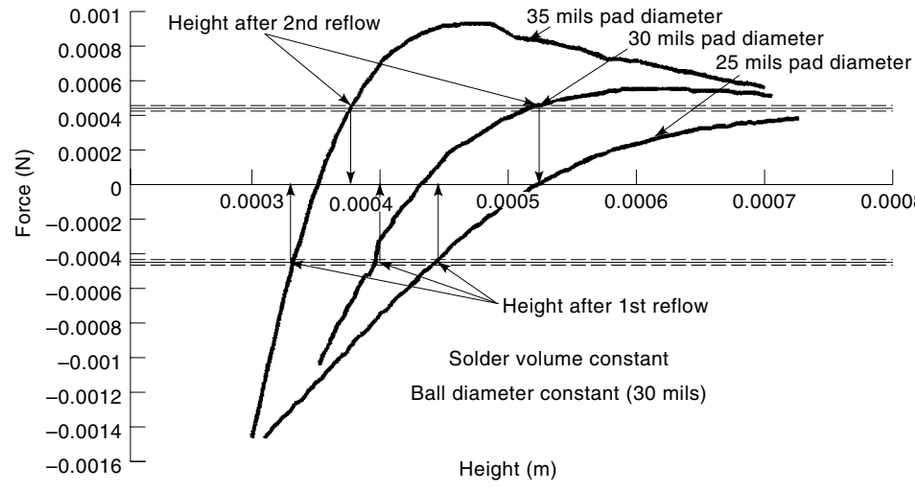

Figure 59. Predicted force-versus-joint-height characteristic for various pad diameters. The solder volume is held constant (ball diameter 30 mils) for the simulations.

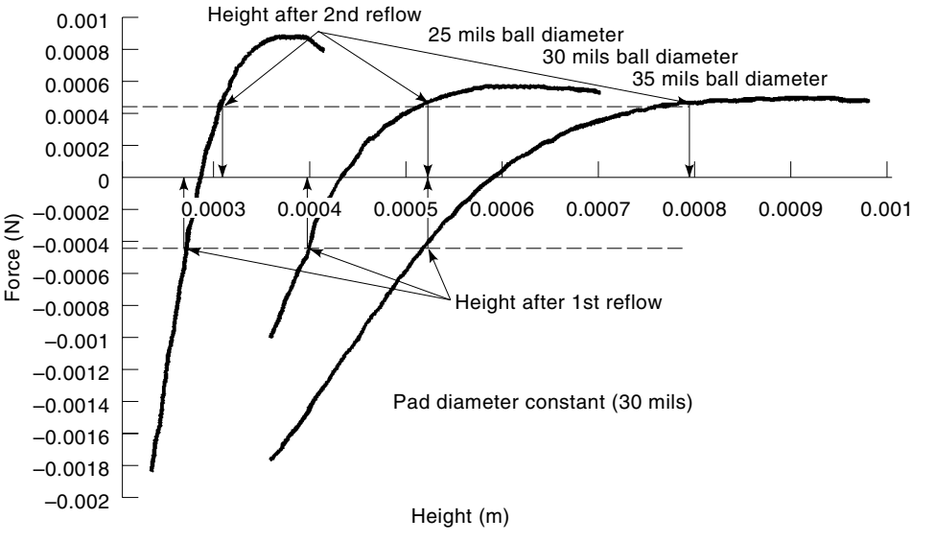

Figure 60. Predicted force-versus-joint-height characteristic for various ball diameters. The pad diameter is held constant at 30 mils for the simulations.

free surface of the molten solder joint is axisymmetric; (d) the meridian defining the solder-joint free surface is approximated by a circular arc; (e) the center of gravity of the component is aligned with the center of the array; (f) there are no spacers used to actively control the height.

The correlation between the two solutions is good (Fig. 62). The numerical solution slightly overpredicts the force-versus-joint-height characteristic compared to the Surface Evolver solution. The numerical solution is applicable for a subset of the cases that the Surface Evolver solution can address and contains several approximations.

Model Validation Setup and Results. Samples of packages soldered on the PC board were obtained. These packages are different from the present package in that they are subjected to a single face-up reflow. The idea was to use the data to validate the model prediction for the joint height after single reflow. The samples were cross-sectioned and the ball heights measured. Table 11 shows the ball heights after single reflow. The predicted height for the above configuration is 15.74 mils (0.400 mm), which is in the neighborhood of the observed mean height 13.34 mils (0.339 mm) and within the $\mu \pm 3\sigma$ bounds of 9.815 mils (0.249 mm) and 16.865 mils (0.428 mm).

To validate the model predictions of the dynamic force–joint-height characteristic during reflow, BGA samples for different pad geometries and ball sizes 25, 30, and 35 mils have been obtained. A 2 lb (0.9 kg) instron load cell was used for the experiments. The load cell has been tested for accuracy in the load range of interest (1 g to 10 g) by hanging a dead weight from the load cell. Figure 63 shows the test configuration. Ceramic sandwiches with different ball and pad geometries were used for the test. Each sandwich was placed on a hot plate, and the top part of the sandwich was pulled to obtain the normal force. The bottom of the sandwich was adhesively bonded to a heavy steel stud.

The model has been validated and predicts with sufficient confidence how to solve the problem that the part falls off in second-side reflow because its weight is barely supported by the solder. Model predictions of height after first-side and second-side reflow have been verified from cross sections of the part. Tests on 25 mil balls on 30 mil pads showed force–displacement characteristic similar to that predicted by the simulations (Fig. 64). The predicted stiffness (force per unit displacement) for 25 mil ball diameter was ≈15.84 N/m, and that for 30 mil ball diameter was ≈8.20 N/m. The predicted stiffness agrees with the measured mean stiffness (Table 12). The mean measured stiffness for the 25 mil ball was ≈17.96 N/m, and that for the 30 mil ball was ≈8.38 N/m.

The model predictions of the process margin [(peak load for 25 mil ball)/(peak load for 30 mil ball) ≈2.45] agree with the measured process margin of 1.8. The model however underpredicts the peak load at failure. The ratio of the measured to the predicted peak load at failure is in the neighborhood of 1.6 to 2.2 in both cases. The actual mean peak load at failure can thus be calculated from the predicted value by multiplying the latter by 1.9. This factor is needed only to calculate the peak load at failure. For the most part, the joint height for any chip weight (force per joint) is predicted accu-

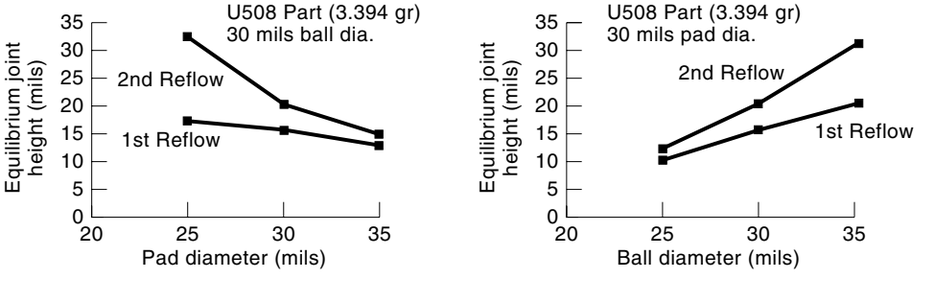

Figure 61. Predicted equilibrium joint height versus ball diameter and pad diameter for the CBGA.

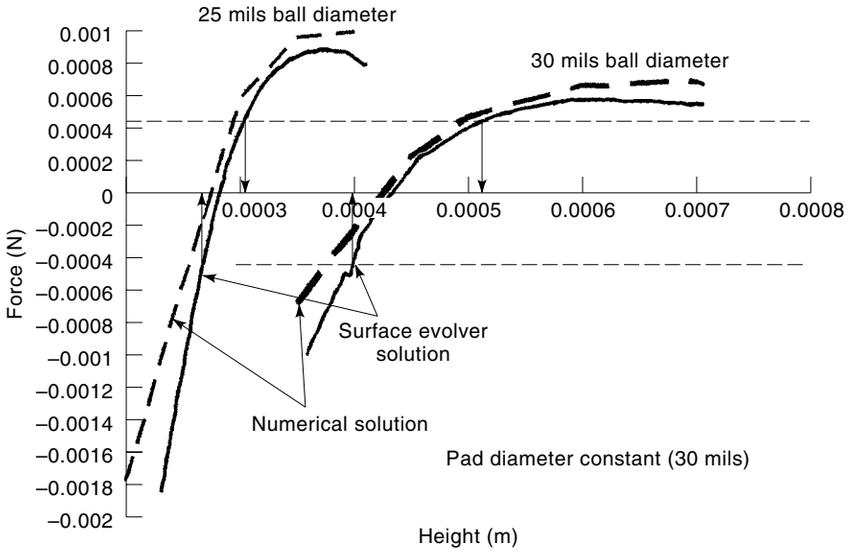

Figure 62. Correlation between closed-form and surface evolver solution.

rately, as can be seen by the good correlation between the measured and predicted values of slopes of the force–displacement curve (Fig. 64).

The reason for the difference between the prediction and experimental data is yet to be investigated. Three possible sources of error are (a) a drop of the bulk solder temperature towards the end of the test as the specimen is being elongated to failure, (b) neglect of necking effects during solder separation at load drop, and (c) crusting of flux and oxidation of solder. The predicted and measured values support the theory that the package in its present configuration is likely to fall off because of vibration and mishandling. The reason is that the force per joint does not increase with any further increase in joint height, so that the package is unstable under additional loads from vibration and handling. Prediction from the simulations indicates that using a smaller ball size or a larger pad size will increase the force per joint during second-side reflow by a factor of 1.8 to 2.2 over the present configuration. Predictions indicate that an increase in the pad diameter from 30 to 35 mils will increase the force per joint during second-side reflow. In the present configuration, the lower bound ($\mu - 3\sigma$) on the experimental value of peak load is $\approx 0.42 \times 10^{-3}$ N, which is barely larger than the weight of the package per joint, $\approx 0.35 \times 10^{-3}$ N. Reducing the ball size from 30 mils to 25 mils increases the peak load for failure for each joint $\approx 1.1 \times 10^{-3}$ N ($\mu - 3\sigma$).

Reliability Modeling. To evaluate the reliability of the solder-joint configurations that satisfied the process requirements, the solder-joint geometry from Surface Evolver was translated to ANSYS. The translated solder-joint geometry was then embedded into a CBGA finite-element model.

Table 11. Correlation between Predicted and Measured Heights after Single Reflow for Part on PC Board

Experimental height (mils)	13.34 ± 3.51
Predicted height (mils)	15.74
Error w.r.t. mean (%)	15.2

The Ceramic BGA finite-element model was then used to simulate reliability in LLTS from −55° to 125°C (5.8 c/h). The location of maximum damage coincides with the site of crack propagation observed using red-dye tests on parts subjected to LLTS (Fig. 65). The predicted characteristic life reduces by a factor of 0.55 for a change in joint height from 19 mils (0.48 mm) to 15 mils (0.38 mm) in LLTS. The model prediction agrees with the LLTS results from a 750 × 750 mil (19 × 19 mm) ceramic BGA with 60 mil (1.5 mm) pitch and 25 mil (0.63 mm) ball diameter, ceramic BGA which showed sufficient crack propagation towards the end of the predicted life. Even though the life has been reduced, it is still greater than the required field life (Fig. 66).

Modeling an Out-of-Plane Package Tilt. If the package weight is nonuniformly distributed or the array configuration is not symmetric about the center of gravity of the package or all the array pads are not the same diameter, finite-element modeling (in the present case ANSYS), along with the spring stiffness from Table 12 and Figs. 59 and 60, can be used to model the out-of-plane tilt of the package during second-side reflow. The package is modeled as `SOLID45` elements, with actual mass densities assigned to individual package elements, to approximate the actual weight of the package. The

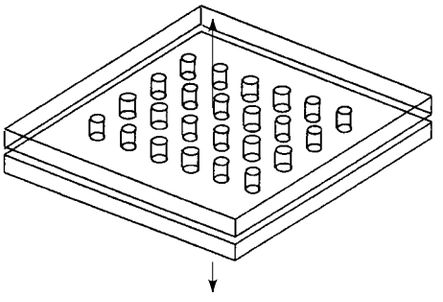

Figure 63. Test configuration for validating force prediction from Surface Evolver. The configuration consists of a ceramic sandwich with balls in the middle, placed on a hot plate.

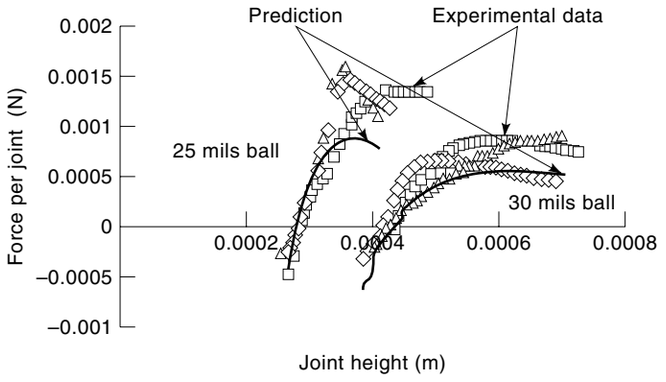

Figure 64. Correlation between force–displacement characteristic from experimental data and from simulations based on energy minimization for 25 mil balls on 30 mil pads. Solid line indicates simulation results, and plot symbols indicate experimental data.

package is supported by nonlinear springs (COMBIN39—a nonlinear generalized force–deflection element in ANSYS) at the joint locations (Fig. 67). The element has one degree of freedom per node. The location of each spring element corresponds to the center of the solder joint. One end of the spring is attached to the package, and the other end is fixed. The force–deflection characteristic may be derived by using the stiffness (spring constant) in Table 12 for each joint configuration, or alternatively the nonlinear force–displacement curves for the springs from Figs. 59 and 60 can be used to model the spring behavior.

SUMMARY

The thermal fatigue reliability has been characterized for three CSPs, including elastomer-on-flex packages, flex-substrate BGA packages, and partial-array BGA packages. The dominant failure mechanisms have been isolated using nonlinear finite-element modeling and accelerated-test data. The dominant failure mechanism for the elastomer-on-flex packages is beam-lead failure, while solder-joint failure dominates in the flex-substrate BGA and the partial-array BGA packages. Good correlation was obtained between the model predictions and the accelerated-test data for all the CSPs.

Table 12. Correlation between Experimental and Predicted Values of Peak Load and Solder Stiffness

Ball Diameter (mils)	Attribute	Experiment $\mu \pm 3\sigma$	Predicted	Error Factor
25	Peak load (10^{-3} N)	1.43 ± 0.33	0.86	0.4
	Stiffness (N/m)	17.96 ± 9.36	15.84	0.12
30	Peak Load (10^{-3} N)	0.79 ± 0.37	0.35	0.55
	Stiffness (N/m)	8.38 ± 5.67	8.20	0.02
	Process margin	1.8	2.45	

Packages were tested on 0.8 mm thick Ni–Au-finish and 1.2 mm thick OPC-finish PC boards using three-point bending on a 1-in. (2.5-cm) span. In both cases, there was no statistically significant difference between the out-of-plane deformation reliability of the elastomer-on-flex packages, flex-substrate BGA packages, and partial-array BGA packages. There was however, a statistically significant difference between the three CSPs and both the 1.5 mm pitch OMPAC and the 1 mm pitch glob-top BGA packages. The CSPs in general were more reliable in out-of-plane deformation than the OMPAC and the glob-top BGA. Aging has a large effect on the OMPAC, glob-top BGA, and flex BGA packages, and a minimal effect on the partial-array BGA and the elastomer-on-flex packages.

Low-frequency repeated bend (LFRB) tests show a mean number of cycles to failure in the neighborhood 110,000 for the 196-I/O glob-top BGA and 4000 for the flex-substrate BGA at 10 mil (0.25 mm) deflection. Most of the data are spread over a big range of 20,000 cycles to 330,000 cycles for the glob-top BGA. The LFRB reliability has been character-

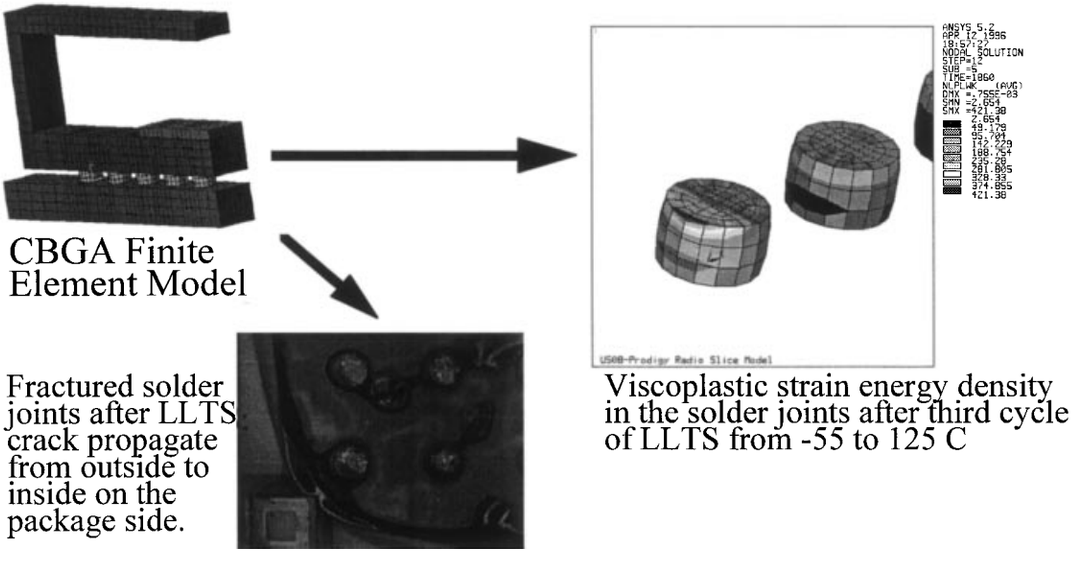

Figure 65. Reliability prediction of site for maximum damage coincides with the crack propagation site during liquid–liquid thermal shock.

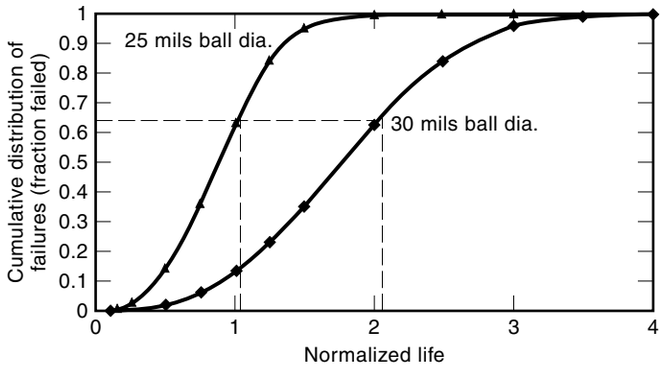

Figure 66. Predicted solder-joint fatigue life in liquid–liquid thermal shock versus joint height.

ized as a function of the out-of-plane displacement. The 48-I/O flex-substrate BGA showed much poorer LFRB reliability than the 196-I/O glob-top BGA.

A methodology has been developed and validated for the optimal design of BGA solder joints based on process and reliability requirements. Model predictions have been validated, including the validation of the final joint height versus package weight and the predicted force–displacement characteristic during collapse and elongation of the BGA solder joint. The force–joint-height characteristics have been measured for different ball diameters. Model predictions of height after first and second reflow have been verified from cross sections of the part. Tests on 25 mil balls on 30 mil pads showed force–displacement characteristic similar to that predicted by the simulations. The predicted stiffness and peak load at failure agree with model predictions.

- The methodology can be used to predict the equilibrium shape of BGA solder joints, their force–displacement characteristics during reflow, and the stability of their final equilibrium shape. Based on the primary information above, BGA solder joints can be designed for a particular shape (hourglass, barrel, etc.) and a desired standoff.
- To evaluate the reliability requirements in solder-joint design, a translation interface from Surface Evolver to ANSYS has been written to translate models seamlessly for reliability simulations. All the vertex, edge, and facet information is preserved during translation. The translated model is however tet-meshed. Another translation interface has been written to translate the tet-meshed model into a brick-meshed model. The parametric nature of the models allows the user to evaluate the influence of various variables, including solder volume, misalignment, pad radius, solder surface tension, and surface tension of the solder–pad finish interface, on the final solder joint shape after reflow.
- The translated BGA solder-joint models from Surface Evolver have been embedded in component finite-element models for predicting reliability.

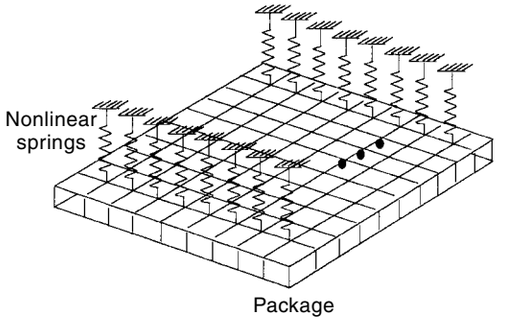

Figure 67. Nonlinear springs used to model the out-of-plane tilt of the package during second-side reflow.

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