NONLINEAR CIRCUIT SYNTHESIS USING INTEGRATED CIRCUITS

Integrated circuit (IC) components are intrinsically nonlinear, as are all circuits built by interconnecting them. In some applications, such as amplification and filtering, nonlinearities are sought as error sources, and the designer employs design techniques to reduce their influence. In others, such as modulation, power measurement, sensor linearization, and signal shaping, the objective is not to attenuate the components' nonlinearities but to use them to perform nonlinear processing tasks.

Nonlinear IC synthesis can be informally defined as a constructive procedure to interconnect IC primitive components and to assign values to their parameters to realize specified nonlinear relationships among electrical variables. This consists of several methodological steps:

1. Identify the *intrinsic* nonlinearities availables at the IC primitives.
2. Construct nonlinear basic building blocks to realize *elementary* nonlinear operations such as logarithm, exponent, squaring, and sign.
3. Interconnect these blocks and the primitives themselves to realize nonlinear *functions* such as multiplication, division, and absolute value.
4. Realize *nonlinear tasks* through the proper interconnection of all the circuit blocks.

This article presents principles and design techniques to cover the first three steps above using bipolar junction transistors (BJTs) and metal oxide semiconductor transistors (MOSTs)—the basic primitives of most commonly used IC technologies (1–3). Considerations related to the fourth step are found elsewhere (4–10).

OUTLINE OF INTRINSIC PRIMITIVE NONLINEARITIES

The nonlinear behaviors exhibited by BJTs and MOSTs may be classified for design purposes into two groups: *continuous* (exponential functions, power functions, etc.) and *piecewise* (abrupt transitions between conducting and blocked states). These behaviors, and their associated characteristic equations, are outlined in Table 1. It is worth noting that these equations are first-order models and, as such, give only rough approximations to actual behaviors. As a consequence, nonlinear circuit designs based on these expressions will only approximate the intended functionality. Detailed analysis of second-order phenomena can be found in the references listed at the end of this article.

According to the preceding classification for the intrinsic primitive nonlinearities, the circuits used to realize the elementary nonlinear operations and the nonlinear functions are also classified in two different groups: continuous and piecewise. They are covered separately in the rest of the article.

BASIC CONTINUOUS OPERATIONS

Three basic continuous operations exploitable for nonlinear synthesis can be identified, namely: (a) linearly controlled transconductances, (b) exponentials and logarithms, and (c) squaring and square-rooting.

Only those realizations based on the intrinsic primitives nonlinearities outlined in Table 1 will be considered, although they can be implemented by other means. For instance, logarithmic amplifiers can be realized using switched-capacitor techniques (6) or approximated with parallel combinations of MOST source-coupled pairs (11–13). Similarly, squarers can be easily implemented using multipliers with identical input signals, or via piecewise linear (PWL) approximation. Exceptionally, the section entitled "Squaring and Square Rooting" will show circuit solutions for the synthesis of the squaring and square rooting operations based on the translinear principle (covered in the next section) (14,15) as an illustration of this important technique for function generation.

Linearly Controlled Transconductances

Table 1 shows that the small-signal *transconductance* of BJTs biased in the forward active region depends linearly on the collector current I_c. A similar dependence is observed for MOSTs biased in the weak inversion region. Correspondingly, the transconductance of MOSTs biased in the saturation strong-inversion region is a linear function of the gate-source voltage overdrive $V_p - V_s$. These linear dependences are at the very heart of the *translinear* principle (14,15), which allows the analysis and synthesis of current-mode circuits able to generate algebraic transformations in an essentially exact and temperature-insensitive manner. The translinear principle can be formulated for BJTs and MOSTs as follows. Consider a loop of n BJTs biased into forward active region (correspondingly, MOSTs operated in forward saturation under strong inversion) such that their base–emitter junctions (correspondingly, their gate–source voltages) are connected in series. Assume that there are equal numbers of transistors arranged clockwise and counterclockwise. Then, the product (sum) of the collector current densities (square root of the drain current densities) in the clockwise direction is equal to the product (sum) of the collector current densities (square root of the drain current densities) in the counterclockwise direction. Mathematically, this can be expressed as

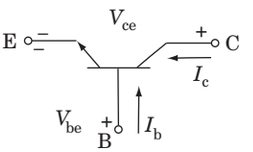
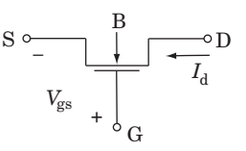
$$\begin{aligned} &\text{BJTs} \quad \prod_{\text{CW}} \left(\frac{I_{\text{ck}}}{A_{\text{k}}}\right) = \prod_{\text{CCW}} \left(\frac{I_{\text{ck}}}{A_{\text{k}}}\right) \\ &\text{MOSTs} \quad \sum_{\text{CW}} \sqrt{\frac{I_{\text{dk}}}{(W/L)_{\text{k}}}} = \sum_{\text{CCW}} \sqrt{\frac{I_{\text{dk}}}{(W/L)_{\text{k}}}} \end{aligned} \tag{1}$$

where A_k represent emitter areas of BJTs; and $(W/L)_k$ aspect ratios of MOSTs. Throughout this article, an extensive use of the translinear principle will be made. For a more throughout study of this essential principle for nonlinear synthesis, readers are referred to Refs. 14 and 15.

Exponentials and Logarithms

These operations can be easily implemented by taking advantage of the exponential large-signal characteristic of BJTs (and MOSTs in weak inversion). Focusing on BJTs,

Table 1. Intrinsic Primitive Nonlinearities

BJT	**MOST**
	
Continuous	
Exponential I–V characteristic of BJTs in the *forward active region* ($V_{be} > 0$, $V_{bc} > 0$), and the corresponding logarithmic transresistance V–I characteristics.[a] $$I_c = I_S \exp\left(\frac{V_{be}}{U_t}\right)\left[1 + \frac{V_{ce}}{V_A}\right]$$ $$I_b = \frac{I_c}{\beta}$$	Square-law characteristic[b] of MOSTs in the forward saturation region under *strong* inversion.[c] $$I_d = n\beta(V_p - V_s)^2\left[1 + \frac{V_d - V_p}{V_A}\right]; V_s < V_p < V_d$$ Product characteristic of a MOST operating in the conduction (ohmic) region under *strong* inversion $$I_d = 2n\beta\left[V_p - \frac{1}{2}(V_d + V_s)\right](V_d - V_s); V_s, V_d < V_p$$ Exponential characteristic of a MOST operating in the forward saturation region under *weak* inversion.[d] $$I_d = I_{D0}\exp\left(\frac{V_p - V_s}{U_t}\right)\left[1 + \frac{V_d - V_p}{V_A}\right]; V_s, V_d > V_p$$ Small-signal transconductance of a MOST in saturation and strong inversion as a linear function of the gate voltage. $$g_m = 2\sqrt{\frac{\beta I_d}{n}} = 2\beta(V_p - V_s)$$ Small-signal self-conductance of a MOST in ohmic region as a linear function of the gate voltage. $$g_{ds} = 2n\beta(V_p - V_s)$$
Small-signal transconductance of a BJT in the forward active region as a linear function of the collector current. $$g_m = \left.\frac{\partial I_c}{\partial V_{be}}\right|_{\text{Quiescent Point}} = \frac{I_c}{U_t}$$	
Piecewise	
Negligible output current for $V_{be} < 4U_t$.	Negligible output current for $V_s > V_p + 4U_t$ and $V_d > V_p + 4U_t$.

[a] $U_t = kT/q$ is the thermal voltage (26 mV at 300 K); I_S is the collector saturation current (proportional to the emitter–base junction area); V_A is the Early voltage (typically from 50 V to 200 V); and β is the forward base–collector current gain (typical values are between 50 to 200).
[b] MOST voltages are referred to the bulk (local substrate) terminal, B.
[c] $\beta = (W/L)\mu C_{ox}/2$ is the transconductance parameter (usually from 10 μA/V^2 to 50 μA/V^2 for $W = L$); n is a slope factor usually smaller than 2, which tends to 1 for large values of V_g; $V_p = (V_g - V_{T0})/n$ is the pinch-off voltage; V_{T0} is the threshold voltage; and V_A is the equivalent Early voltage (proportional to the transistor length).
[d] I_{D0} is the specific current of the transistor (typically from 20 nA to 200 nA for $W = L$), and it is proportional to the transconductance parameter β.

if the base–emitter junction of the transistor is driven by a voltage, V_{be}, the resulting collector current, I_c, is roughly proportional to an exponential function of V_{be}. Reciprocally, if the transistor is forced to accommodate a given collector current, I_c, the resulting V_{be} is approximately proportional to the logarithm of I_c. Figure 1(a,b) shows simple logarithmic [Fig. 1(a)] and exponential [Fig. 1(b)] voltage amplifiers based on these principles. These circuits exploit the virtual ground of the opamp to obtain $I_i = V_i/R$ [Fig. 1(a)] and $V_o = I_iR$ [Fig. 1(b)].

The circuits of Fig. 1(a,b) are seldom used in practice because of some important nonidealities. For instance, Fig. 1(a) has a notorious tendency to oscillate because of the nonlinear feedback around the opamp. To ensure stability, a frequency compensation circuit must be added to this feedback loop (5). Another drawback is caused by their dependence on temperature, through both I_s and U_t (see Table 1). The circuits in Fig. 1(c,d) compensate the former by using common-emitter differential pairs instead of single transistors. In this way, the dependence of the amplifiers output voltages with the saturation currents disappears to a first approximation, as shown in the insets of Fig. 1(c,d). These expressions show that V_o in both amplifiers still depend on temperature via U_t. This can be compensated by implementing R_2 with a temperature-dependent resistor having the same temperature characteristic as U_t (5).

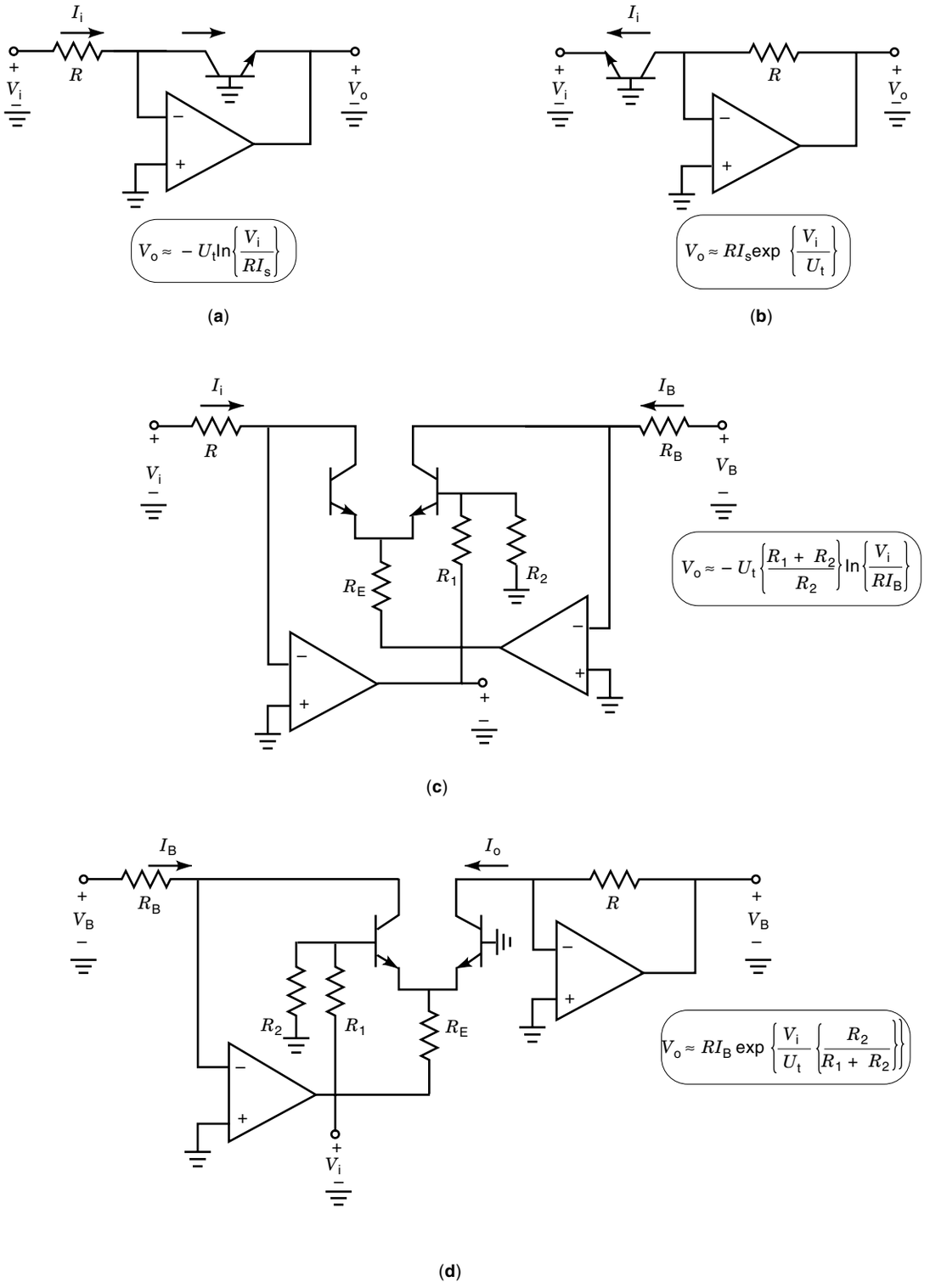
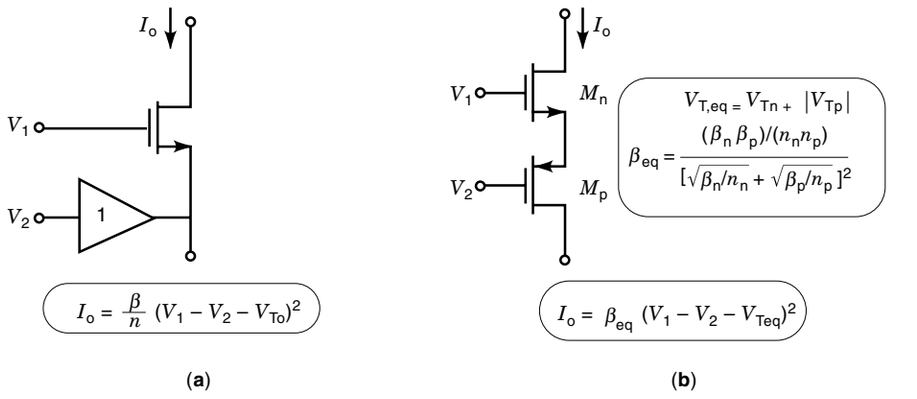


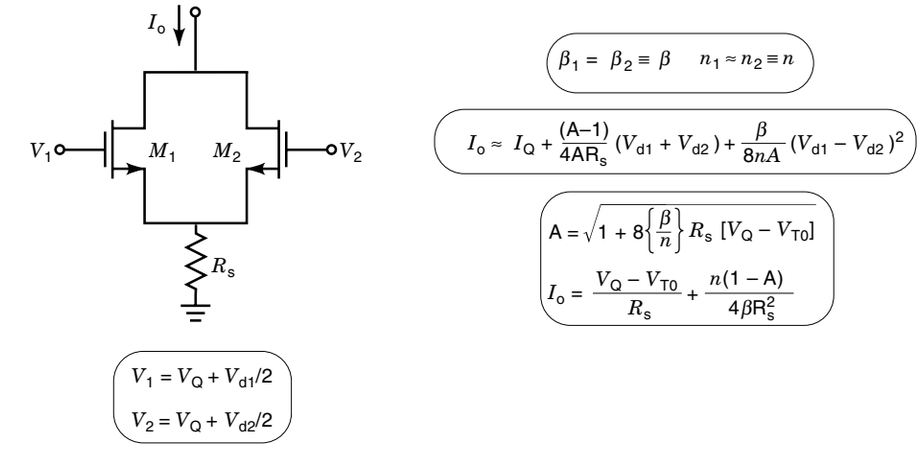
Figure 1. Logarithmic (a) and exponential (b) amplifiers based on a single *npn* BJT. Logarithmic (c) and exponential (d) amplifiers using matched pairs of *npn* BJTs to cancel out the dependence with the collector saturation current.

Squaring and Square Rooting

These operations can be synthesized by exploiting MOST's strong inversion saturation region. If two voltages (with identical common-mode values) are applied, respectively, to the gate and source of a MOST in the saturation region, the drain current contains a term proportional to the square of the difference of the two voltages. Reciprocally, if the transistor is forced to accommodate a given drain current I_d (this requires application of feedback as occurs at the input stage of MOST current mirrors), the resulting V_{gs} contains a term roughly proportional to the square root of I_d. However, these operations are adversely affected by the nonzero threshold voltage: When a MOST is operated as a squaring device, its drain current contains other undesired terms together with the difference-squared component; and reciprocally, when a MOST is configured as a square-rooting device, its gate–source voltage includes an offset term.

Figure 2(a–c) shows some squaring circuit blocks together with their transfer characteristics assuming no body effect (MOSTs source terminals are connected to their local substrates). Figure 2(a) uses a single MOST and a voltage buffer to maintain the gate–source voltage independent of the current flowing through the device; this buffer is needed because the source terminal is a low-impedance node. The buffer can be implemented using voltage followers (16), shunt feedback





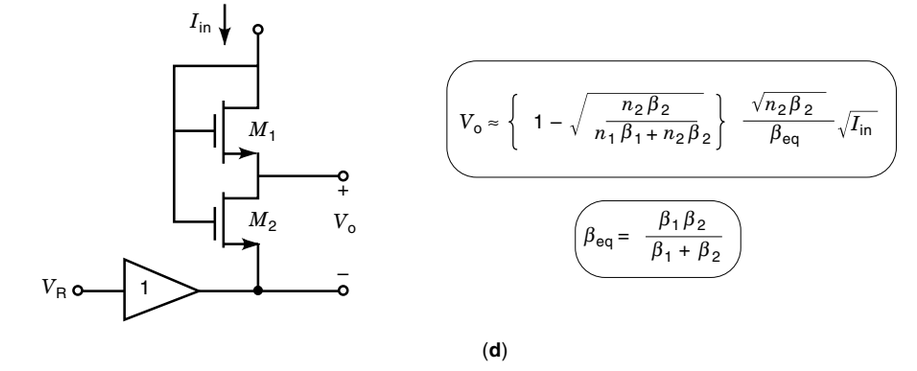


Figure 2. Squaring and square-rooting circuits based on the large signal characteristic of MOSTs. (a) Squaring circuit using a single MOST with source buffering; (b) squaring circuit based on a CMOS composite pair; (c) squaring circuit using a source degenerated differential pair; (d) nested connection of two MOSTs for squaring or square-rooting operations.

amplifiers (17), or opamp-based inverters (18). The squaring block of Fig. 2(b) avoids the buffering stage by using a CMOS *composite* pair (19). This circuit can be seen as an *n*- or *p*-channel MOST, operating in the saturation region, with the parameters $V_{T,eq}$ and β_{eq} shown in the inset, but with high impedance gate and source nodes. Finally, Fig. 2(c) uses a source degenerated differential pair (20), whose large-signal transconductance characteristic contains a term proportional to the square of the difference of the two gate voltages. In practice, the resistor can be implemented with another MOST operating in the ohmic region.

Figure 2(d) shows a nested connection of two MOSTs which, depending on the attachment, can perform either as a square rooting of the input current [configuration in Fig. 2(d)] or as a squaring of the input voltage (21). Interestingly enough, both operations are free from other undesired terms provided that the transistors have the same threshold voltage. However, the internal node of this nested connection cannot be directly loaded but must be sensed or driven through a high-impedance node (21).

As previously stated, another possibility to implement the squaring and square-rooting operations relies on the translinear principle. Circuit solutions exist for both the BJT (14,15) and MOST (22) version of this principle, but we will restrict to the latter. Figure 3(a,b) shows two possible realizations of a MOST translinear current-mode squarer (22). Applying the translinear principle [see Eq. (1)] on the loops formed by the gate-source paths of transistors M_1–M_4 in the circuits of Fig. 3(a,b), obtains the expression,

$$\sqrt{\frac{I_{d1}}{\beta_1}} + \sqrt{\frac{I_{d3}}{\beta_3}} = \sqrt{\frac{I_{d2}}{\beta_2}} + \sqrt{\frac{I_{d4}}{\beta_4}} \tag{2}$$

where I_{di} and β_i represent the drain current and transconductance factor of transistor M_i, respectively. If the currents I_{d1} and I_{d3} are each forced to be equal to a bias current I_Q; the difference of I_{d4} and I_{d2} is defined by the input signal, I_{in}; and the current $I_{d2} + I_{d4}$ is taken as the output of the circuit, Eq. (2) becomes

$$I_o = I_Q + \frac{I_{in}^2}{4I_Q} \tag{3}$$

where the aspect ratios of the transistors are such that $\beta_1 = \beta_3 \equiv 2\beta$ and $\beta_2 = \beta_4 \equiv \beta$. Note that the offset term in Eq. (3)

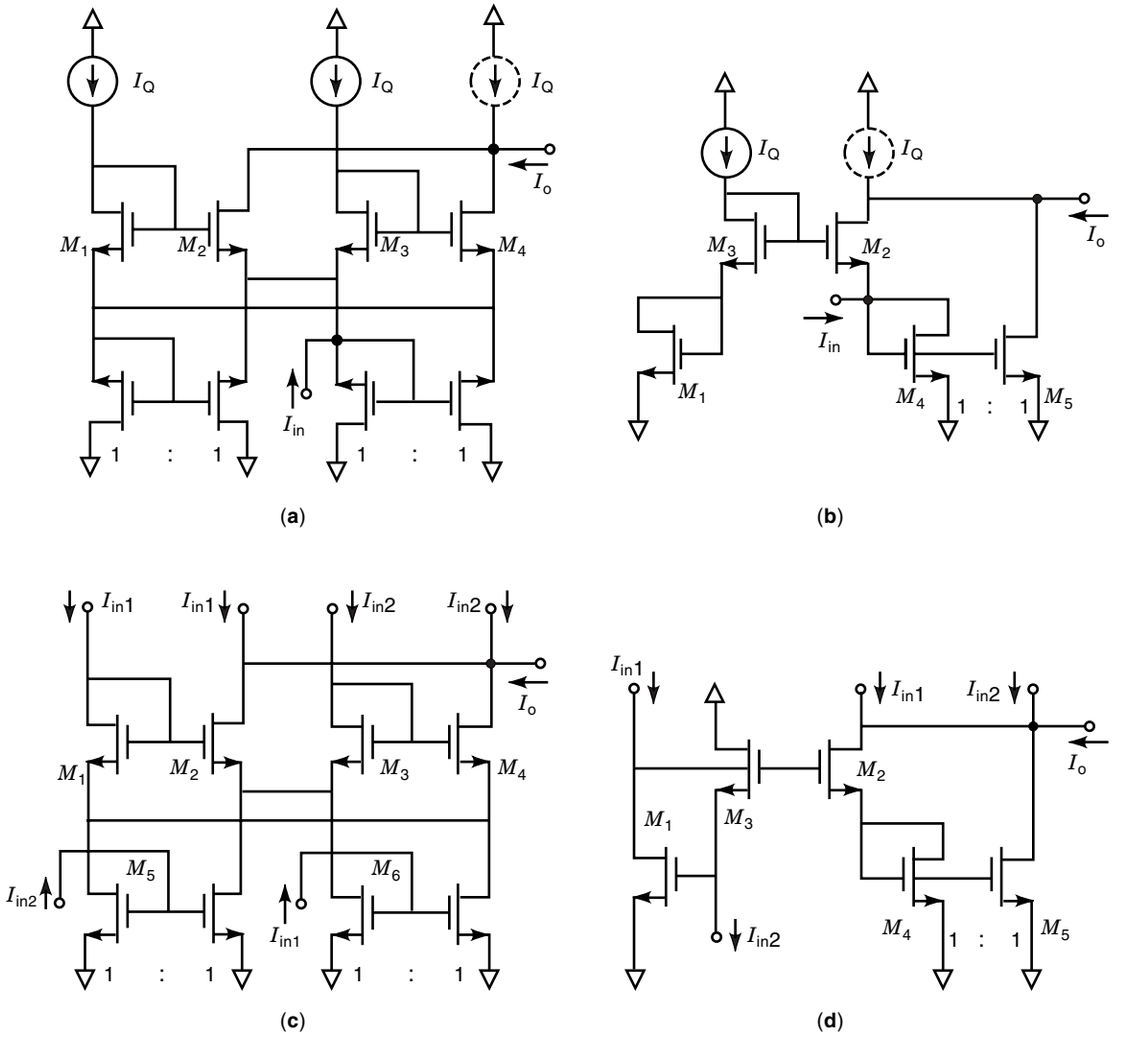


Figure 3. MOST translinear current-mode circuits: (a,b) squarers; (c,d) geometric mean operators.

can be eliminated by inserting another replica of the bias current [dashed sources in Figs. 3(a,b)] at the output node. Valid operation range is guaranteed when all transistors operate in the saturation regime, which leads to $|I_{in}| < 2I_Q$.

Schematics similar to those in Fig. 3(a,b) enable to realize the square-rooting operator (or more exactly, the geometric mean operator). These are shown in Fig. 3(c,d). The synthesis strategy is to take I_{d1} and I_{d3} as the input signals (I_{in1} and I_{in2}, respectively); I_{d4} and I_{d2} are made equal, and the current $I_{d2} + I_{d4}$ is again considered as the output of the circuit. Assuming $\beta_1 = \beta_3 \equiv \beta$ and $\beta_2 = \beta_4 \equiv 2\beta$, the following characteristic is obtained:

$$I_o = I_{in1} + I_{in2} + 2\sqrt{I_{in1}I_{in2}} \tag{4}$$

which includes a term proportional to the geometric mean of I_{in1} and I_{in2}. Obviously, if one of the input currents is regarded constant, such term becomes proportional to the square root of the other input signal. Once again, the undesired terms in the expression may be eliminated by applying a compensating source at the output node, in this case $I_{in1} + I_{in2}$. Correct performance of the circuits is ensured whenever I_{in1} and I_{in2} are positive.

BASIC PIECEWISE NONLINEAR OPERATIONS

Three basic discontinuous nonlinear operations can be identified, namely: (a) comparison, (b) rectification, and (c) controlled switching.

Comparison

A voltage comparator produces an output binary voltage y to codify the polarity of an analog input voltage x with respect to a reference value E,

$$y = \begin{cases} V_{OH}, & x > E \\ V_{OL}, & x < E \end{cases} \tag{5}$$

where V_{OL} and V_{OH} are voltage levels associated to the low and high logical states, respectively.

The simplest way to realize Eq. (5) is employing a *one-stage* voltage amplifier. Figure 4(a) shows three possible CMOS implementations of this concept: two are unilateral (reference voltage is set by the transistor threshold voltages); the third is differential (reference voltage set by an external source). Similar implementations can be made with BJTs.

The behavior of one-stage voltage comparators can be approximated to a first-order by the circuit model shown in the inset of Fig. 4(a). This model captures three nonideal features: input offset voltage (E_{os}), finite dc gain ($A_v = g_m R_o$), and time constant ($\tau = R_o C_o$). It models also the amplifier output voltage saturations. Assuming that a small positive voltage step $\Delta = x - E$ is applied at $t = 0$, the output voltage evolution in the linear region is calculated as

$$y(t) = (\Delta - E_{os})A_v\left(1 - e^{-t/\tau}\right) \tag{6}$$

A similar equation is found for negative input steps. From Eq. (6) two major drawbacks of this comparator structure can be identified. On the one hand, the input *sensitivity* (i.e., the minimum Δ needed for the output to reach the logical levels) is limited by the input offset voltage and the finite dc gain; the larger E_{os} the larger the Δ needed to obtain a positive output, and the smaller A_v the larger the Δ needed to reach $y = V_{OH}$. On the other hand, the output transient evolution is dominated by a rather large time constant τ. [The maximum speed capability of Fig. 4(a) is set by the time constant $\tau_u = C_o/g_m$. However, the time constant of the one-stge comparator is reduced by the dc gain (i.e., $\tau = \tau_u/A_o$.] To raise the operation speed and increase the gain of the one-stage comparator, two nonexclusive strategies can be adopted (23): using *multistage* amplifiers [Fig. 4(b)], and using positive feedback to obtain *regenerative* amplification [Fig. 4(c)]. This latter implies synchronous operation. On the other hand, to cancel the comparator offset, *autozeroing* techniques, where the offset is periodically sensed, stored, and added to the input in such a way as to cancel itself, are commonly used—also involving synchronous operation [Fig. 4(d)].

Consider now that the input and the reference are currents. They can be compared by first injecting both into a sensing block to convert their difference in an intermediate voltage and then using this voltage to drive a voltage-mode comparator. Figure 5(a) shows the concept (24). The resistive part of the current sensing device is such that the equivalent resistance is large for low currents (R_s) and small for large currents (R_s^*). This enables us to combine very low current detection capability with reduced input voltage excursion. Figure 5 shows two practical CMOS implementations of this concept. The circuit of Fig. 5(b) uses the nonlinear resistor formed by transistors M_n and M_p. In many practical applications, a simple CMOS inverter can be used in place of the voltage-mode comparator (24), thus leading to very compact realizations. An important drawback of Fig. 5(b) is that the transient behavior is largely dominated by the overlapping capacitance C_f, which connects input and output terminals of the voltage amplifier. The circuit in Fig. 5(c) overcomes this drawback by decoupling the input and output nodes of the amplifier (24).

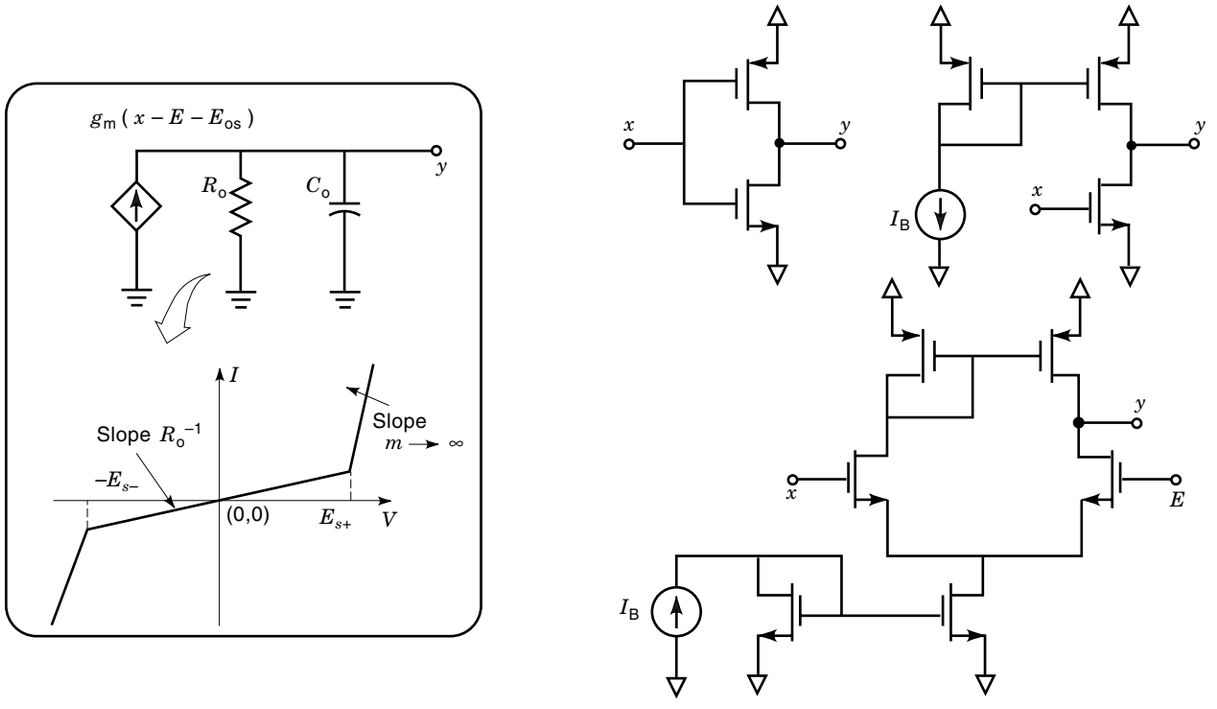
Rectification

The two most basic rectification operators are the so-called positive and negative half-wave rectifiers, which are defined as (represented at the top of Fig. 6)

$$y = u_+(x) = \begin{cases} x, & x \geq 0 \\ 0, & \text{otherwise} \end{cases} \qquad y = u_-(x) = \begin{cases} x, & x \leq 0 \\ 0, & \text{otherwise} \end{cases} \tag{7}$$

where variables x and y can be in the form of currents or voltages. The relevance of these operators comes from the fact that they are basic building blocks for the realization of any elementary piecewise linear function, as will be shown in the section entitled "Derived Piecewise Nonlinear Operations."

The basic rectification mechanism is the controlled transition between the blocked and conducting states of either diode or diode-connected transistors, and leads to implementations of Eq. (7) with input and output current [see Fig. 6(a)]. A drawback of these circuits is the current-dependent nonzero voltage drop in the conducting state. It can be reduced by using feedback to create superdiodes, shown in Fig. 6(b) for the grounded case and Fig. 6(c) for the floating case (exempli-



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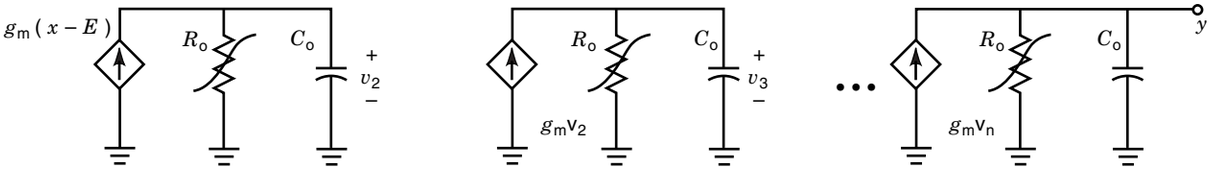

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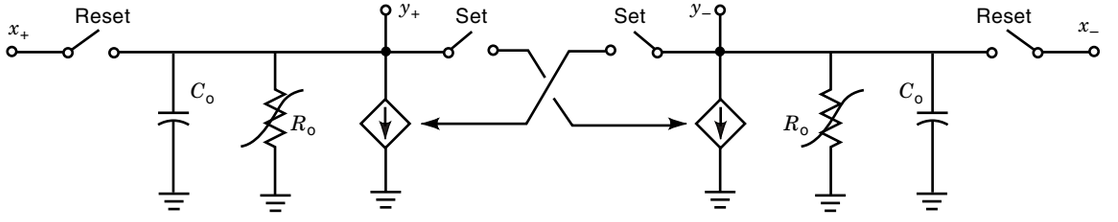

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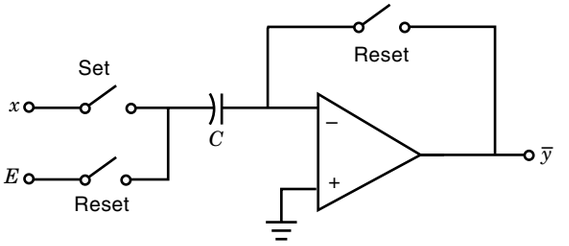


(**d**)

Figure 4. Voltage-mode comparators: (a) based on one-stage voltage amplifiers; (b) using multistage amplifiers; (c) via regenerative amplification; (d) with offset cancellation.

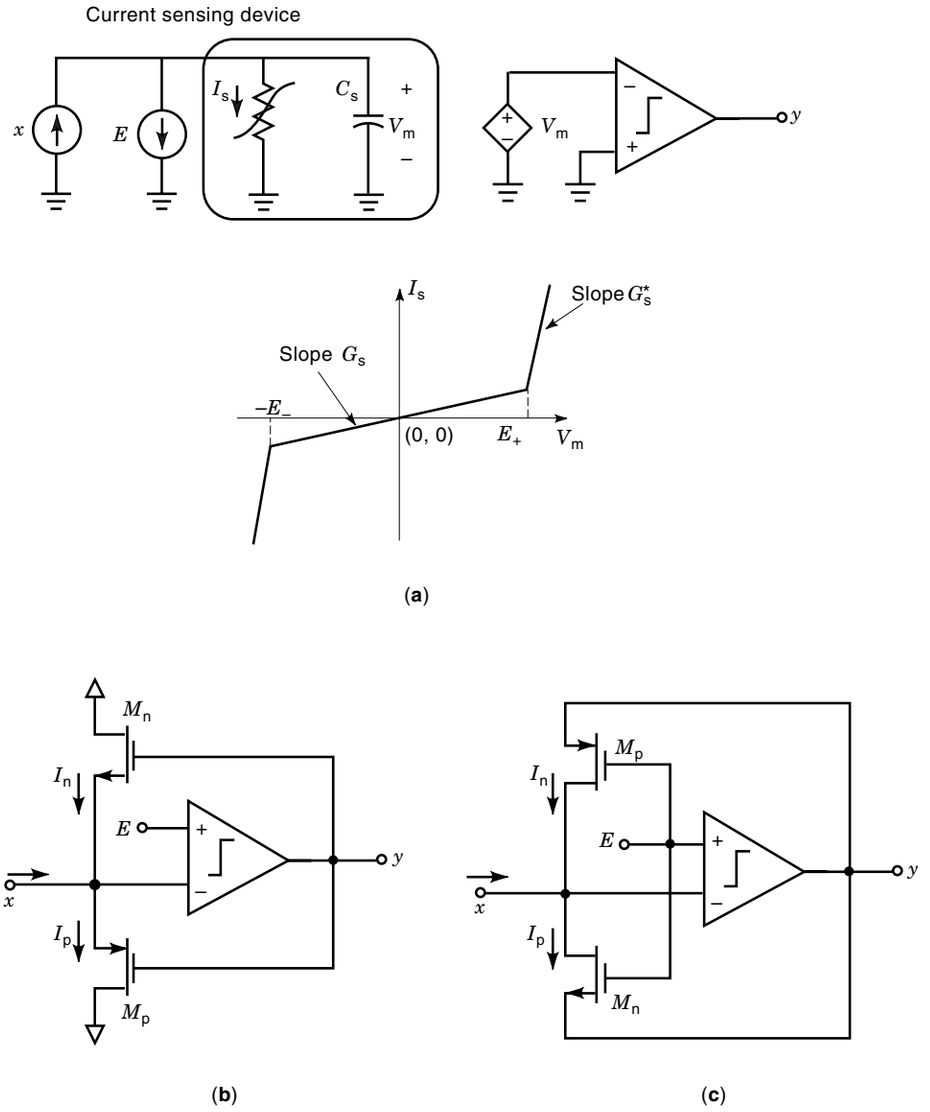


Figure 5. (a) Current-mode comparator based on voltage amplification. (b) Current sensing device made of transistors M_n and M_p; (c) Current steering configuration.

fied with a MOST). In both cases, the reduction of the forward voltage drop is proportional to the dc gain of the amplifier.

Another building block widely used for current rectification is the current mirror. Figure 7 shows the rectifying characteristics of very simple current mirrors using *n*-channel [Fig. 7(a)] and *p*-channel [Fig. 7(b)] MOSTs with bias-shifting. For both cases, we assume that the aspect ratio W/L of the output transistor is m times larger than that of the input. The transfer characteristic of the circuit in Fig. 7(a) can be easily derived taking into account that the input transistor enters the cut-off region for values of I_{in} below $-I_{B1}$, for which the input voltage becomes lower than the threshold voltage V_{Ton}. Similar analysis also applies for the circuit in Fig. 7(b). Dashed lines in Fig. 7(a,b) show the transfer characteristics for zero I_{B1} and I_{B2}. In this situation, the breakpoints of the characteristics are at the origin, and the output current is given by $I_o = -mu_+(I_{in})$ for the circuit in Fig. 7(a), and $I_o = -mu_-(I_{in})$ for the circuit in Fig. 7(b). BJTs can also be used for rectification based on the current mirror concept.

The most important limiting factor of using current mirrors for rectification is the delay time required to discharge the input capacitance in the transition from cut-off to conduction. To improve this, class AB configurations can be used (25). The reason is that in class AB circuits there is always a low-impedance path for the input current to flow and thus the voltage at the input node remains limited. Figure 8(a) shows an example of a class AB current rectifier. The output currents I_{o1} and I_{o2}, assuming matched devices and saturated operation, can be described by

$$I_{o1} = m\frac{(4I_B + I_{in})^2}{16I_B} \quad \text{and} \quad I_{o2} = -m\frac{(4I_B - I_{in})^2}{16I_B} \tag{8}$$

for $|I_{in}| \leq 4I_B$. When the input current magnitude exceeds $4I_B$, Eq. (8) no longer holds because one of the output mirrors now takes virtually all the current, the other one being effectively switched off. This means that proper rectification occurs only for large enough input currents. Another class AB

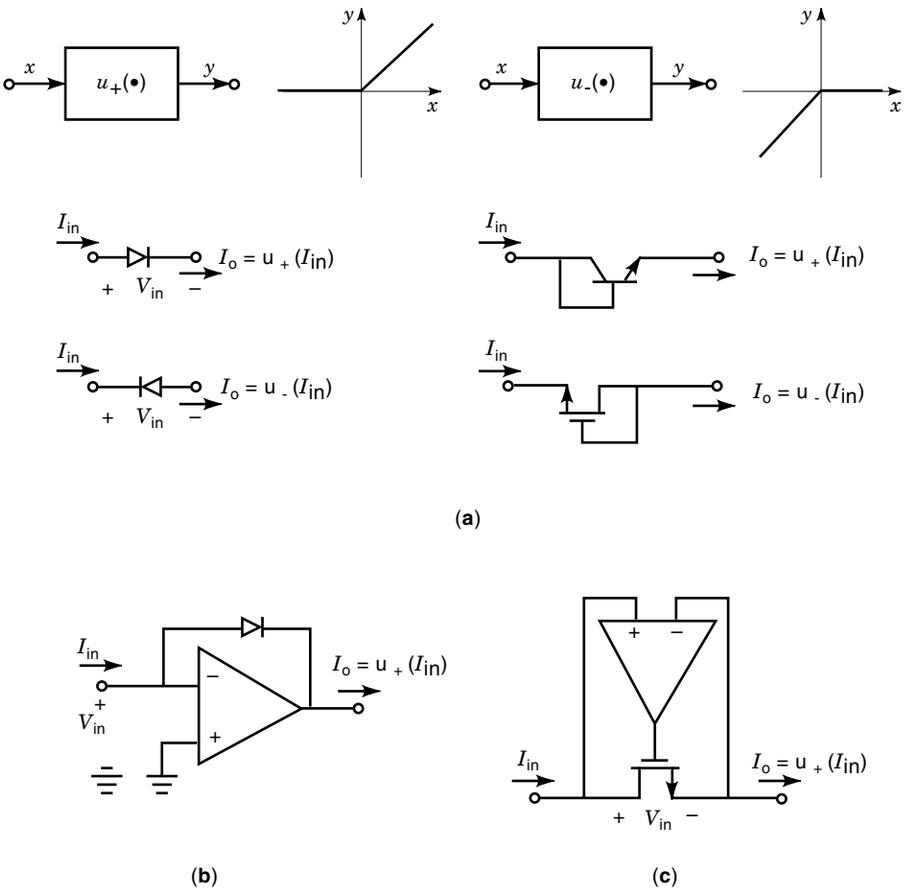


Figure 6. (a) Diode and diode-connected transistors for current rectification; (b,c) super-diodes.

configuration which avoids this lack of accuracy at low currents is shown in Fig. 8(b), and it is based on the rectification properties of the nonlinear feedback current comparator of Fig. 5(b). Any positive input current increases the input voltage, turning the bottom device, M_p, ON. Because both devices share the input voltage, the top device, M_n, becomes OFF. Similarly, the input voltage decreases for negative input currents, so that M_n becomes ON and M_p, OFF. In sum, positive input currents are drawn to the bottom device, whereas negative currents are drawn to the top device, thus achieving nearly perfect rectification. Furthermore, the circuit is insensitive to transistor mismatch; hence, it can be realized through minimum size devices. Proper routing and scaling of the drain currents passing through transistors M_n and M_p obtain the concave and convex basic characteristics, as shown at the bottom of Fig. 8 (24–26).

Controlled Switching

Switches, often operated by comparators, are used locally in nonlinear circuitry to establish new conditions when a threshold on a given variable has been crossed (27). For instance, they may change a gain, reverse a polarity, or initiate a new mode of operation, thus producing an overall nonlinear response. Signal processing multipliers, covered in the section entitled "Multiplication," represent an application example of the controlled switching operation for nonlinear synthesis.

Figure 9 shows three common analog switches used in practice (23). Figure 9(a) is the most simple realization and consists of a single MOST with its gate voltage controlling the resistance between its drain and source. As shown in Table 1, when the MOST operates in the linear region, this resistance can be expressed as

$$R_{on} = \frac{1}{2\beta(V_G - V_{T0} - nV_s)} \tag{9}$$

and when the device turns blocked, this resistance (R_{off}) becomes virtually infinite. In order to extend the input swing of the single MOST switch and further reduce the on resistance in Eq. (9), the complementary structure of Fig. 9(b) is used instead. It is formed by an NMOS and a PMOS device, whose gates are controlled with complementary logical levels so that the two devices turn on and off simultaneously. In pure bipolar technologies, where MOSTs are not available, controlled switching is performed by diode bridges, illustrated in Fig. 9(c).

DERIVED CONTINUOUS NONLINEAR OPERATIONS

Here we include (a) sigmoid transfer characteristics, (b) bell-like transfer characteristics, (c) multiplication, (d) division, (e) vector magnitude calculation, (f) normalization, and (g) maximum and minimum.

Sigmoid Characteristic

IC implementation of arbitrary nonlinear functions is possible using universal representation techniques as, for instance,

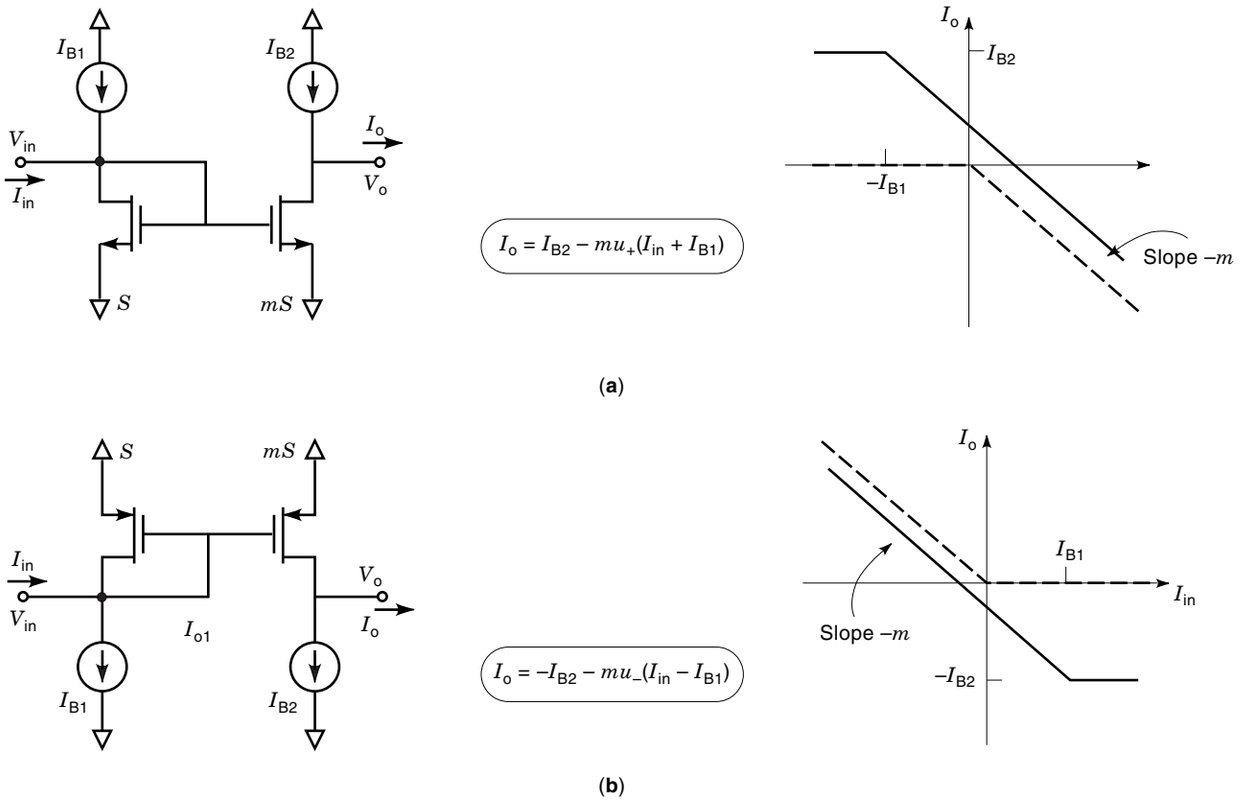
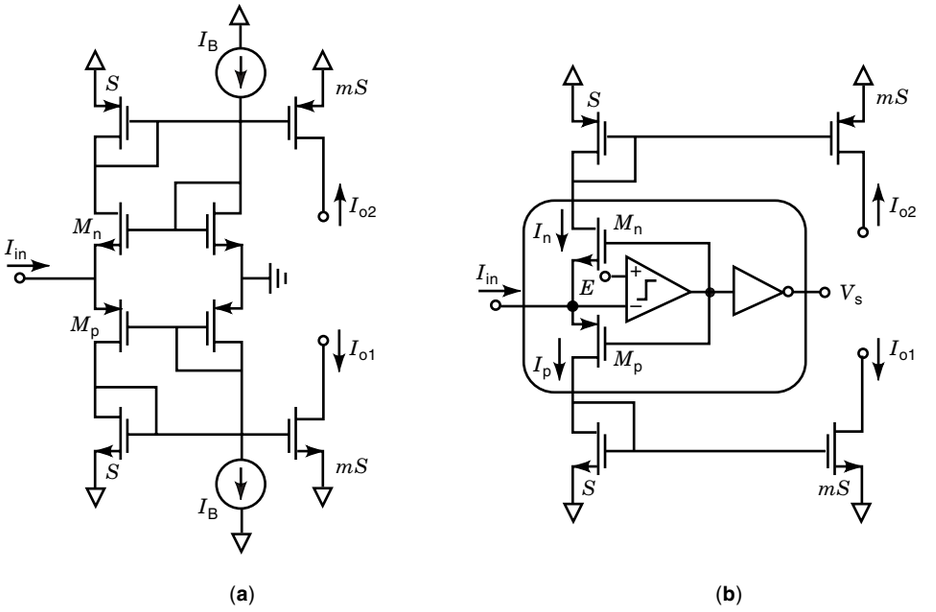


Figure 7. Rectifying characteristics of current mirrors using (a) *n*-channel and (b) *p*-channel MOSTs with bias-shifting as basic transconductors.

multilayer perceptrons, for which elementary computational units realize sigmoidal functions. Figure 10 depicts two sigmoidal shapes used in practice. Figure 10(a), the hard limiter, has an inner piece of large (ideally infinite) slope, whereas for Fig. 10(b), the soft limiter, this slope is smaller and can be used as a fitting parameter. Hard-limiter characteristics can be easily achieved using the comparison operators discussed in the previous section entitled "Comparison." On the other hand, soft-sigmoid characteristics can be easily synthesized by exploiting the global transfer characteristics of basic differential amplifiers (11,28) or using simple CMOS inverters (10). Here, we will restrict ourselves to the first approach.

Figure 11 shows the expressions for the large-signal output current of a basic differential pair implemented with saturated MOSTs (top expression) and with bipolar transistors (bottom expression). In the first case, the sigmoid characteristic exhibits a quadratic dependence with the input voltage and saturates at $+I_B$ and $-I_B$. In the second case, identical saturation levels hold, but dependence with the input voltage is now exponential. In both cases, transfer function presents a continuous derivative $G_m(I_B)$, which is tunable through the biasing current of the differential pair. Circuits in Fig. 11 have been widely used in neural network implementations and function synthesis hardware. For instance, Fattaruso and Meyer (11) use arrays of MOS differential pairs in the saturation region as analog function synthesizers and propose a biasing strategy that allows independence to temperature and processing variations. On the other hand, MOS differential pairs operated in weak inversion have become one of the basic elements in the implementation of feedforward neural networks and other massively parallel computation paradigms as a result of their low power consumption and high integration density (7).

A problem arising with basic differential pairs for function synthesis is that the tuning of the biasing current implies not only a variation on the slope of the sigmoid characteristic but also a shift of the saturation levels. Several techniques have been proposed to overcome this problem. A first approach consists on truncating the output current of the differential pair so that the saturation levels remain always between $+I_B$ and $-I_B$ for any value of the transconductance. This truncation operation is implemented in the current domain by loading the differential pair with adequate rectifying or maximum/minimum operators. A second strategy to control the slope of the sigmoidal characteristic without affecting the saturation levels relies on input voltage scaling (13). In this way, if V_{in} is linearly preamplified by a factor k at the input of the differential pair, the slope of the sigmoid becomes $kG_m(I_B)$ and can be tuned by controlling the voltage gain k. A third approach is based on degenerating the source/emitter of the differential pair through a voltage-controlled resistor so that the transconductance of the amplifier turns dependent on the equivalent degenerative resistance (29). A last approach to achieve continuous and electrically tunable changes in the slope of the sigmoid characteristic uses compound transistors (28). These compound transistors have the same signal terminals as con-



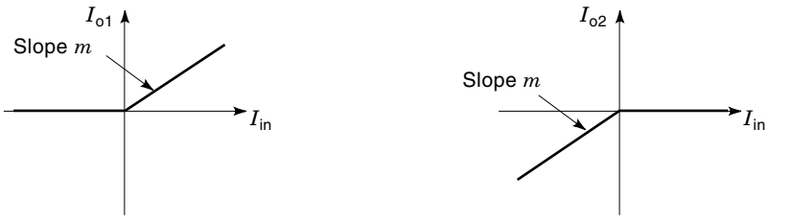


Figure 8. Class AB current mirrors with positive and negative rectifying outputs: (a) using a second-generation current conveyor; (b) using a feedback current comparator.

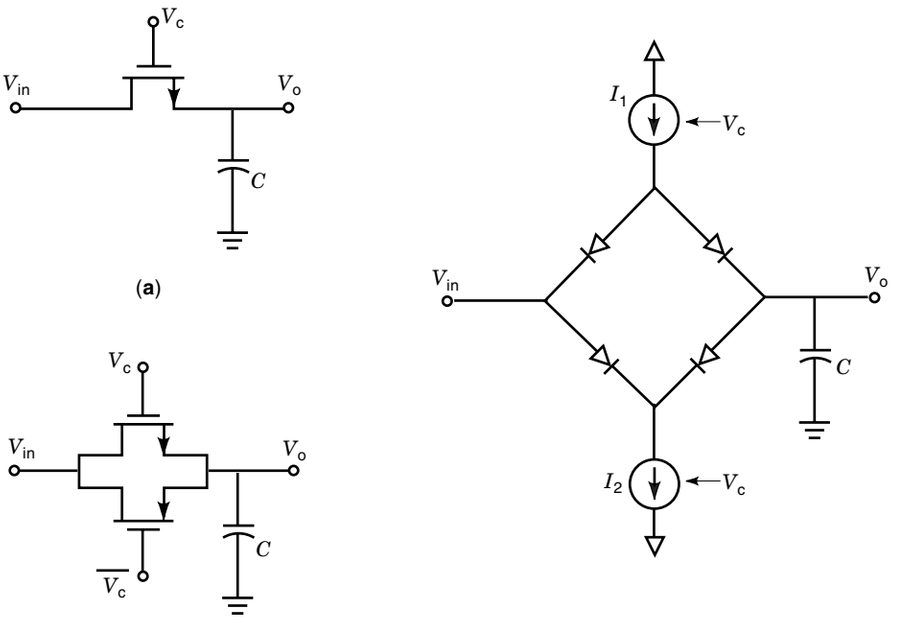


Figure 9. Basic switches: (a) single MOST; (b) complementary MOS; (c) diode bridge.

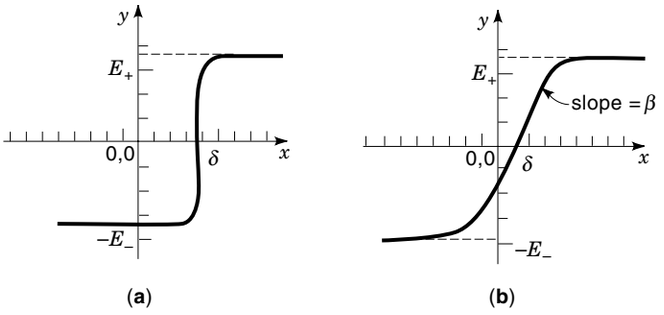


Figure 10. Typical sigmoidal shapes: (a) hard limiter; (b) soft limiter.

ventional transistors in Fig. 11, but their transconductance is controllable through a parameter associated to either a digital word or a control voltage.

Bell-Like Function

Several bell-shaped functions have been proposed as interpolation operators in the framework of radial basis networks and neuro/fuzzy controllers (9). Among these operators, the polynomial and Gaussian basis functions, represented in Fig. 12(a,b), respectively, are the most widely found in the literature. The electronic realization of these characteristics involves the interconnection of squarers, power computation blocks, and exponential operators. However, these exact shapes are not required in many applications and can be approximated using simpler circuits.

One possibility to approximate the polynomial bell-shaped characteristic shown in Fig. 12(a) is to combine two differential pairs as indicated in Fig. 13, where rectangular blocks can be replaced by MOSTs, BJTs, or other compounds devices (13,28). In this circuit, $V_{\delta 1}$ and $V_{\delta 2}$ are used to adjust the width of the bell-like function, and the voltage amplifier with gain parameter k is used to change the slope of the transconductance characteristic. In Fig. 13, some of the current components generated by the circuit are also shown. The differential output current of the block I_o is obtained as the sum of the individual differential output currents of the two source/emitter coupled pairs and is always comprised in $[0, 2I_B]$ regardless of the devices replacing the rectangular blocks. The width and center of the bell are given, respectively, by

$$2\sigma = V_{\delta 2} - V_{\delta 1} \qquad \delta = \frac{V_{\delta 2} + V_{\delta 1}}{2} \tag{10}$$

which are controlled by the designer. On the other hand, the slope of the bell at the crossover points depends on the transconductance of the differential amplifiers and the gain k of the input voltage amplifier. If the rectangular blocks are replaced by MOSTs in the saturation region, the slope at the crossover points S and the width of the rise or fall edges Δ are given by

$$S = k\sqrt{\frac{2\beta I_B}{n}} \qquad \Delta = \sqrt{\frac{2nI_B}{\beta k^2}} \tag{11}$$

assuming that the width of the bell is larger than $(2\sigma)_{min} = 2(nI_B/\beta)^{1/2}$. If the rectangular blocks are replaced by bipolar transistors, S and Δ take the form

$$S = \frac{kI_B}{2U_t} \qquad \Delta = \frac{4U_t}{k} \tag{12}$$

where it should be noted that Δ is now independent of the bias current I_B.

With regard to the Gaussian radial basis function, Fig. 14 shows a circuit implementation based on MOS differential pairs in the saturation region (10). Contrary to the circuit in Fig. 13, the input signal is in differential form. The center of the bell is defined by the voltage difference $V_{\delta A} - V_{\delta B}$, and the standard deviation of the Gaussian function can be varied by changing the sizes of the transistors in the input differential pairs using digitally programmed structures (30). On the other hand, parameters a and b can be chosen to better approximate the ideal Gaussian curve.

Multiplication

Analog multipliers implementation has long been an important topic in electronic research. Besides their suitability for function synthesis, analog multipliers also find a wide range

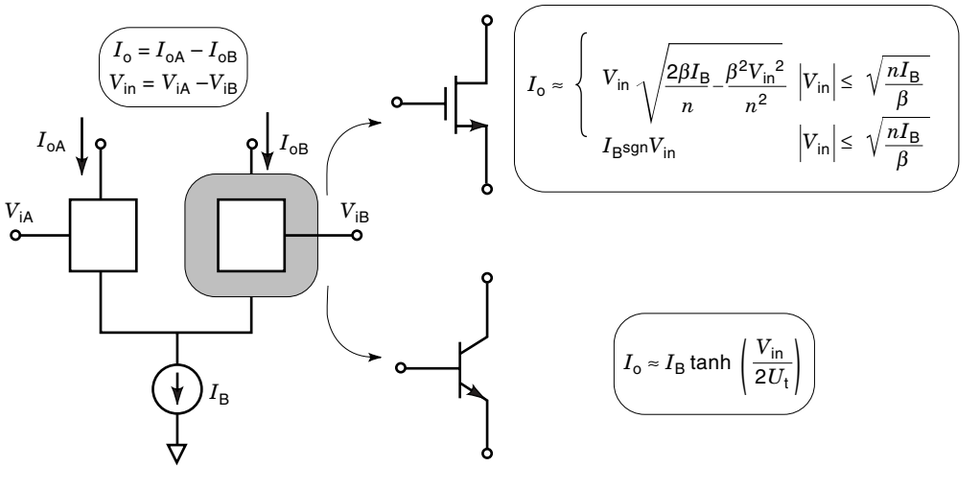


Figure 11. Differential amplifiers and their associated large-signal characteristics.

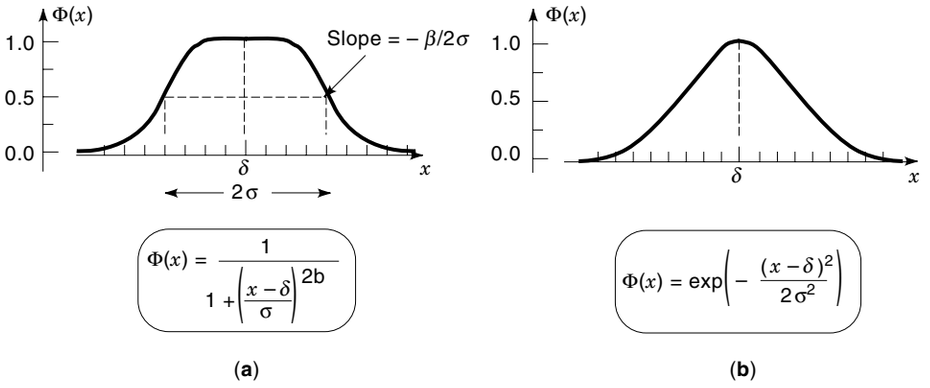


Figure 12. Basic interpolation functions: (a) polynomial; (b) Gaussian.

of applications in signal processing systems, including communication and instrumentation systems, wave generation, modulation, dynamic gain setting, power measurement, and computational circuits, as well as in artificial neural networks. There are two basic strategies to realize multiplication circuitry,

- using signal processing, and
- exploiting some nonlinear mechanism of the primitive components.

In the following sections, we intend to provide a brief overview of both approaches.

Signal Processing Multipliers. The most popular signal processing multiplier is the so-called *pulse-modulation* multiplier. It relies on the principle that the area under a rectangular pulse equals to the product of its amplitude and duration. Thus, if the amplitude of a pulsed signal is made proportional to one multiplicand, and the duty cycle proportional to the other multiplicand, the area under the pulse-train becomes proportional to the multiplication operation. Figure 15(a) shows a voltage domain implementation of this concept based on *averaging*. This is performed by a low-pass filter whose input is a pulse-train V_t with amplitude proportional to V_x and duty cycle proportional to V_y. This latter proportionality is achieved through nonlinear sampling, by comparing V_y with a time reference triangular (or saw-tooth) signal φ with period T and amplitude V_α. If the variation rate of V_y is much less than the averaging frequency $f = 1/T$, then the duty cycle of the control signal V_c and, therefore, of the pulse train V_t, results in $\tau/T = V_y/V_\alpha$. As a consequence, if the low-pass filter has unity gain, the average output voltage of the filter reads as

$$V_z = \frac{V_x V_y}{V_\alpha} \tag{13}$$

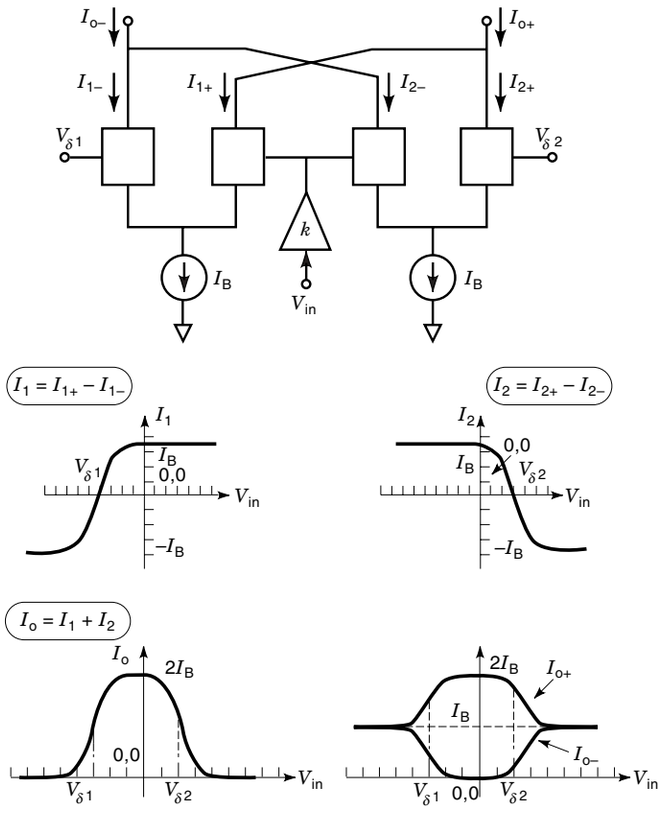


Figure 13. Transconductance circuits for bell-shaped function.

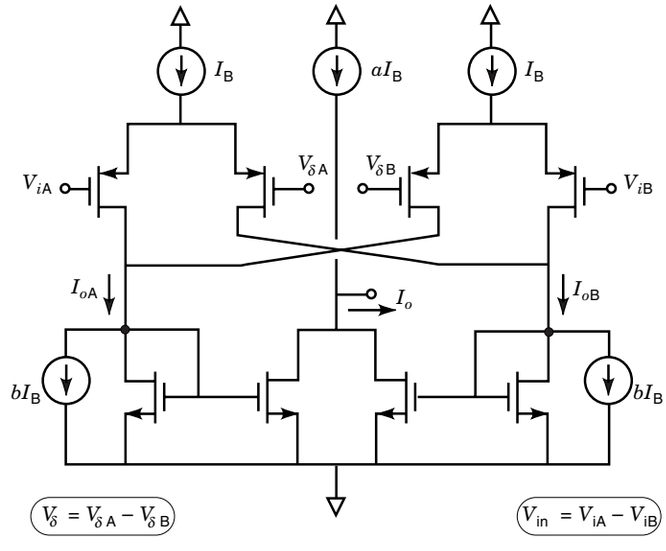


Figure 14. Gaussian function circuit with differential input.

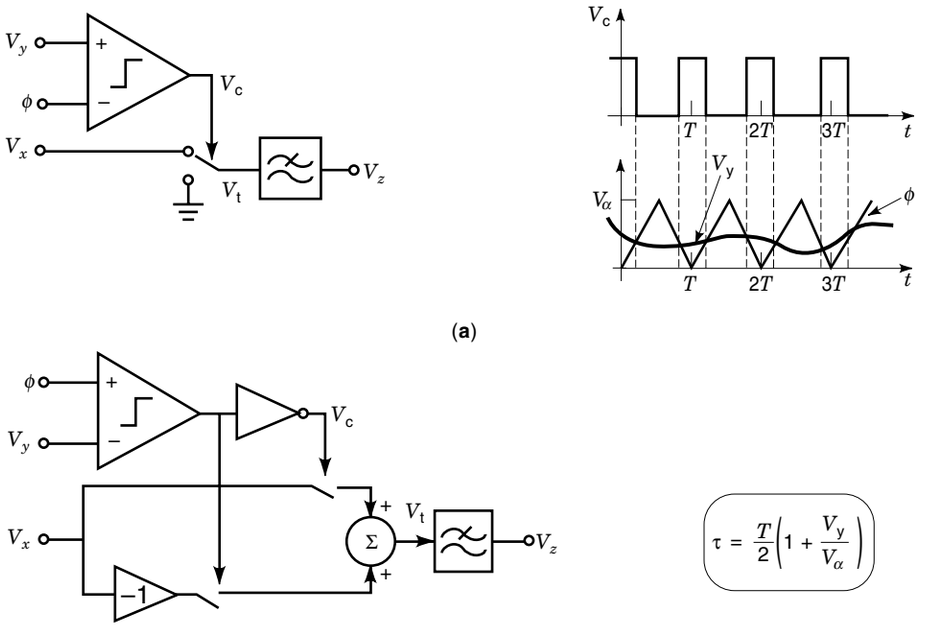


Figure 15. Pulse-modulation multipliers: (a) two-quadrant and (b) four-quadrant realizations.

Note that the V_x multiplicand can be either positive or negative, but voltage V_y is limited to positive values, since the duty cycle τ/T cannot be negative. Thus, the circuit in Fig. 15(a) realizes two-quadrant multiplication. To extend its operation to four-quadrant multiplication, a bipolar triangular waveform oscillating between $-V_\alpha$ and V_α must be used (this makes a zero V_y input corresponds to a 50% duty cycle), and signal V_x must be sampled in balanced form, as shown in Fig. 15(b). Further details on the performance of pulse-modulation multipliers are discussed in classical texts on analog computation (5). Also in Ref. 6, several configurations using switched capacitor (SC) techniques are reported. In particular, some designs that avoid the use of external waveform references by applying feedback around the voltage comparator are presented.

Figure 16(a) shows an alternative signal processing multiplier based on the transient evolution of linear circuits. For reasons that will become apparent soon, this technique is referred to as *temporal shaping.* Again, voltage-mode operation is assumed. The circuit in Fig. 16(a) uses two linear blocks with normalized unit step response given by $h_1(t)$ and $h_2(t)$. The last is driven by level V_x to obtain

$$V_t(t) = V_x h_2(t),\ 0 \le t < \tau \tag{14}$$

where τ denotes the amplitude of the time interval during which the switch S remains closed. The other is driven by a reference level V_α to render τ given by

$$\tau = h_1^{-1}\left(\frac{V_y}{V_\alpha}\right) \tag{15}$$

While switch S is closed, the output voltage V_z follows the signal V_t. At $t = \tau$, that switch opens, and V_z is held to $V_t(\tau)$.

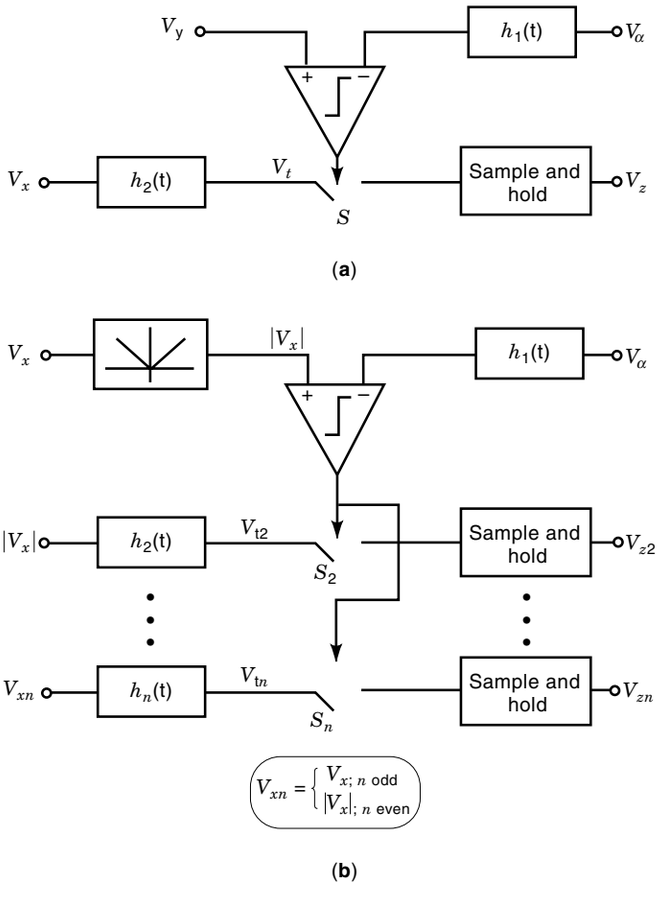


Figure 16. Signal processing multipliers by shaping in time domain.

Thus, assuming both linear blocks are identical and the time function invertible, one obtains

$$V_z = \frac{V_x V_y}{V_\alpha} \tag{16}$$

in the steady state situation. The simplest implementation of Fig. 16(a) uses integrators [i.e., $h_j(t) = t$] as linear blocks (31). Another possibility uses exponential ramp generators with a normalized unit step response given by $h_j(t) = \exp(-t/T_j)$.

Interestingly enough, the principle can be extended to the generation of powers of an input signal by higher-order shaping in time domain. This is illustrated in Fig. 16(b). In this case, the linear blocks are selected to fulfill the condition,

$$h_j(t) = h_1^{j-1}(t);\ j = 2, \ldots, n \tag{17}$$

where $h_j(\cdot)$ denotes the normalized unit step response of the jth linear block. On the other hand, signals $V_{tj}(t)$ take the form

$$V_{tj}(t) = \begin{cases} V_x h_j(t); & j \text{ odd} \\ |V_x| h_j(t); & j \text{ even} \end{cases} \tag{18}$$

for $0 \le t < \tau$, and the time internal during which switches S_j

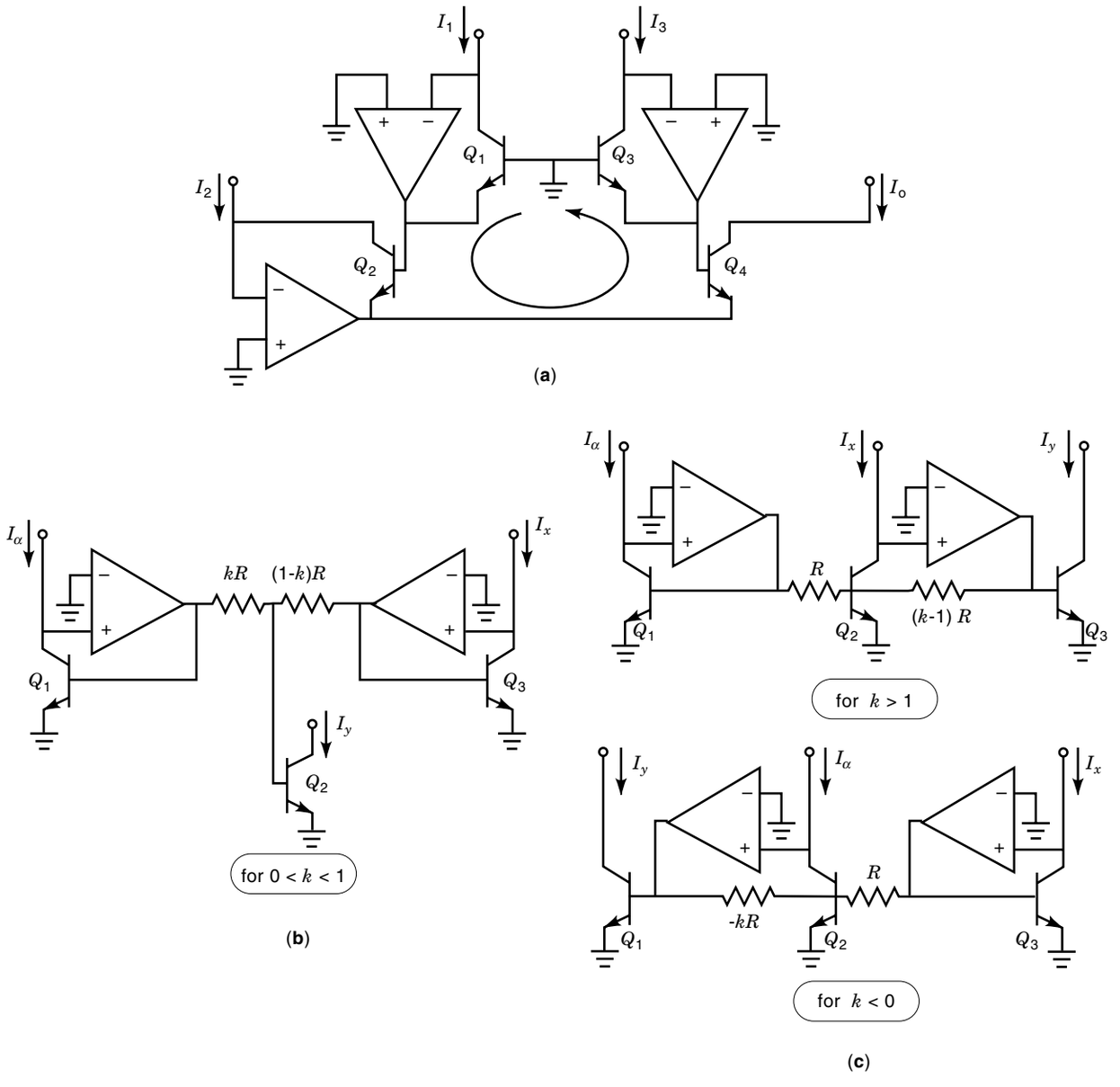


Figure 17. (a) Core block of a log–antilog multiplier; (b), (c) circuits to elevate to a power.

($j = 2, \ldots, n$) are closed is defined as

$$\tau = h_1^{-1}\left(\frac{|V_y|}{V_\alpha}\right) \tag{19}$$

Combining the last three equations, the steady state value of the output signals V_{zj} results in

$$\frac{V_{zj}}{V_\alpha} = \left(\frac{V_x}{V_\alpha}\right)^j ;\ j = 2, \ldots, n \tag{20}$$

There are various alternatives for the design of the linear blocks under the restriction Eq. (17). One of them obtains the linear block with unit step response $h_j(t)$ as a cascade of $j - 1$ integrators (31). Another alternative relies on the use of time exponentials with scaled time constants, $T_j = T_1/(j - 1)$ for $j = 2, \ldots, n$. Realizations suitable for integrated circuits of these time-function generators can be found in Refs. 6 and 32.

Another type of signal processing multiplier that operates in the voltage-charge domain has been proposed in Ref. 33. Its operation principle shares some properties from the aforementioned pulse modulation and temporal shaping concepts. Instead of controlling the amplitude and duty cycle of a pulse-train, the multiplier modulates the amplitude σ and decay time τ of a single-sided exponential current pulse. The integral charge delivered by such a pulse is proportional to the product of the peak amplitude and the decay time constant; in other words,

$$Q_z = \int_0^\infty \sigma \exp\left(-\frac{t}{\tau}\right) u(t)\, dt = \tau\sigma \tag{21}$$

where Q_z is the charge delivered. Thus, if the amplitude of the exponential pulse is made proportional to one multiplicand, V_x, and the decaying time constant is modulated by the other multiplicand, V_y, the integral charge is proportional to $V_x \cdot V_y$. An important feature of the multiplier in Ref. 33 is its low device complexity and large modularity, which renders its usage very well suited for the implementation of neural network paradigms.

Other signal processing multipliers are based on the operation of the generalized integrator, which is an electronic circuit capable of integration with respect to a dependent variable. In the most general case, its functionality is described by the integral

$$z(t) = z_0 + \int_{x_0}^{x(t)} \frac{y(t)}{\alpha(t)}\, d[x(t)] \tag{22}$$

where $x(t)$, $y(t)$, $\alpha(t) > 0$, and $z(t)$ are time-dependent signals and x_0 and z_0 denote initial values at $t = 0$. Proper usage of generalized integrators allows the synthesis of any nonlinear multivariate function $z = f(v_1, v_2, \ldots, v_n)$, including multiplication (6). The method simply consists of expressing the function (assumed real and analytic) as a closed set of ordinary differential equations. These equations can be easily obtained by successively differentiating $f(\cdot)$ as follows:

$$dz = \sum_{i=1}^{N} z_i dv_i \quad dz_i = \sum_{j=1}^{N} z_{ij} dv_j \quad dz_{ij} = \sum_{k=1}^{N} z_{ijk} dv_k \quad \ldots \tag{23}$$

where

$$z_i = \frac{\partial f}{\partial v_i} \quad z_{ij} = \frac{\partial^2 f}{\partial v_i \partial v_j} \quad z_{ijk} = \frac{\partial^3 f}{\partial v_i \partial v_j \partial v_k} \quad \ldots \tag{24}$$

Because the terms on the right-hand side of the equations in Eq. (23) have the same functional form as the integrand in Eq. (23), function $f(\cdot)$ can be implemented as a network of layered generalized integrators. In Ref. 6, different approaches for the design of generalized integrators using SC techniques are reported. Also, in this reference, experimental results from a four-quadrant multiplier built upon generalized integrators are presented.

Multipliers Based on Primitive Components. The intrinsic continuous nonlinearities listed in Table 1 of the primitive components display several mechanisms that are exploitable to realize analog multipliers. In the following sections, we will briefly discuss four different techniques for analog multiplication, each one exploiting a particular device functionality from those listed in Table 1.

Log–Antilog Multipliers. The log–antilog class of multiplying structures is based on the exponential large signal transconductances of the BJT and MOST, this last either in the subthreshold or bipolar region (8). The principle arises from the following basic relationships:

$$\begin{aligned} \ln(xy) &= \ln(x) + \ln(y) \\ \exp[\ln(xy)] &= xy \end{aligned} \tag{25}$$

which can be realized as shown in Fig. 17(a) for the bipolar case (5). This circuit operates on positive terminal currents (one-quadrant multiplication) to obtain $I_o = (I_1 I_2)/I_3$, which can be understood from translinear circuit principles, by noting that the four base-to-emitter voltages define a *translinear loop* which verifies

$$\ln\left(\frac{I_1}{I_s}\right) + \ln\left(\frac{I_2}{I_s}\right) = \ln\left(\frac{I_3}{I_s}\right) + \ln\left(\frac{I_o}{I_s}\right) \tag{26}$$

The same circuit can be made to operate in four-quadrant mode, though restricted to currents larger than $-I_B$, by driving each terminal with a bias current source of value I_B. Note that the circuit of Fig. 17(a) operates in current-mode. Voltage-to-current transformation can be achieved using linear resistors and exploiting the virtual ground property of operational amplifiers. Applying this transformation, the circuit of

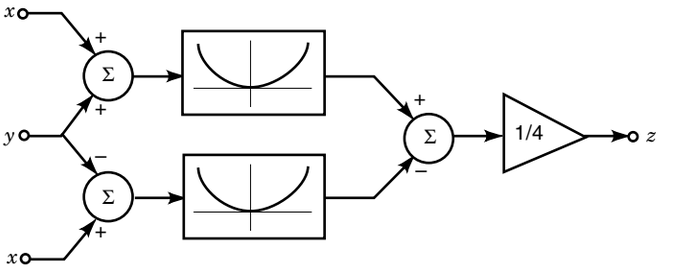
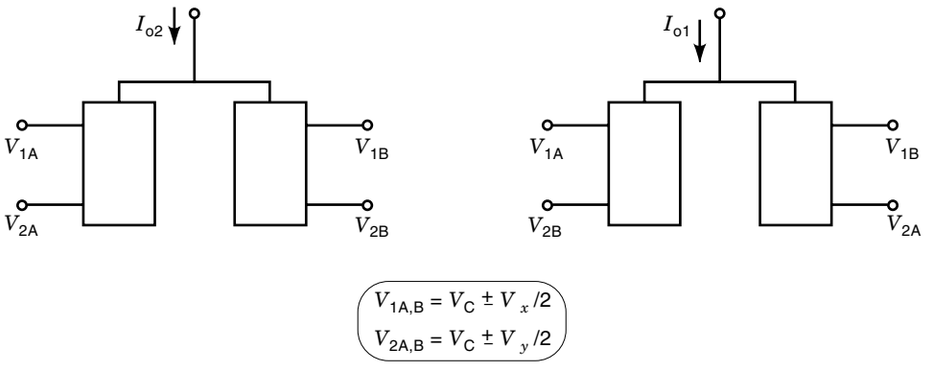


Figure 18. Conceptual block diagram of the quarter-square multiplier.



Squarer	I_{o1}	I_{o2}	$I_o = I_{o1} - I_{o2}$
Fig.2(a)	$\frac{\beta}{n}[(V_x + V_y)^2/2 + 2V_T^2]$	$\frac{\beta}{n}[(V_x - V_y)^2/2 + 2V_T^2]$	$4\frac{\beta}{n}V_xV_y$
Fig.2(b)	$\beta_{eq}[(V_x + V_y)^2/2 + 2V_{T,eq}^2]$	$\beta_{eq}[(V_x - V_y)^2/2 + 2V_{T,eq}^2]$	$4\beta_{eq}V_xV_y$
Fig.2(c)	$2I_Q + \frac{\beta}{4nA}(V_x + V_y)^2$	$2I_Q + \frac{\beta}{4nA}(V_x - V_y)^2$	$\frac{\beta}{nA}V_xV_y$

Figure 19. Quarter-square multipliers.

Fig. 17(a) can be understood as the connection of three logarithmic amplifiers like that in Fig. 1(a) (those comprising transistors Q_1, Q_2, and Q_3), and one exponential amplifier like that in Fig. 1(b) (comprising transistor Q_4). Extension of this circuit structure to generate arbitrary powers is discussed in Ref. 15. Figure 17(b) uses similar techniques by introducing scaling factors in the translinear loop (34). If the resistor values are low enough to neglect the voltage drop caused by the base current of transistor Q_2 in the three configurations, and all the transistors are identical, the functionality of the circuits results in

$$\frac{I_y}{I_\alpha} = \left(\frac{I_x}{I_\alpha}\right)^k \tag{27}$$

Square-Law Multipliers. A second class of multiplying structures is based on the quadratic large-signal law governing MOSTs in strong inversion and saturation. Most of the multipliers exploiting this quadratic law use the *quarter-square* technique, which is derived from the following relationship:

$$z = \frac{1}{4}[(x+y)^2 - (x-y)^2] = xy \tag{28}$$

The block diagram associated with this algebraic identity is conceptually shown in Fig. 18. As can be seen, multiplication is performed in three steps. First, the sum and differences of the two input signals are formed. Then, these variables are squared. Finally, the difference of the squared values is obtained and scaled to get the desired result.

Any of the squaring blocks of Figs. 2(a–c) and 3 can be used to implement the concept of Fig. 18. Quarter-square multipliers based on the current mode squarers of Fig. 3 can be synthesized in a straightforward manner, by exploiting the Kirchhoff's current law (KCL) to obtain the sums and differences of the signals. Examples can be found in Ref. 22. Regarding the squarers in Figs. 2(a–c), it must be noted that their associated output currents contain other undesired terms, together with the difference-squared component, which must be cancelled out in order to apply the quarter-square technique. This can be done using *cross-coupled* topologies and *fully balanced* input voltages, as shown schematically in Fig. 19. In this figure, the black boxes are symbols for the squarers of Figs. 2(a–c), and the output currents I_{o1} and I_{o2} of the corresponding multipliers are indicated in the attached table. Note that these currents are also balanced. They can be subsequently transformed into an output voltage by applying a symmetric resistive load to the multiplier block or into a single-ended output current I_o (see the fourth column of the table in Fig. 19) by using current mirrors. These transformations realize, indeed, the difference and scaling operations on the right-hand side of the block diagram in Fig. 18.

Technical literature contains several examples meeting the general architecture of Fig. 19. Examples are in Refs. 16–18 and 35. In all cases, the valid operation range of the multipliers is dictated by the need to keep all the transistors of the squaring blocks properly biased in the saturation region. For

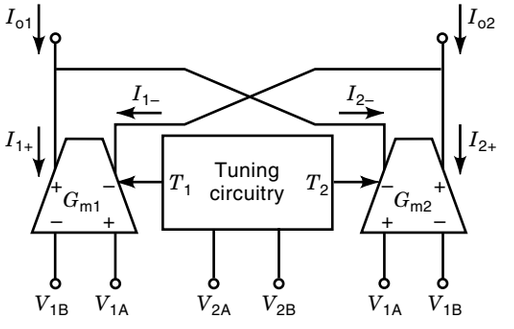


Figure 20. Concept of the variable transconductance multiplier.

instance, if the squarer of Fig. 2(a) is used, it can be shown that the multiplier input voltages must verify $|V_x| + |V_y| > 2V_T$, and similarly, for the squarer of Fig. 2(b), the operation range reads $|V_x| + |V_y| > 2V_{T,eq}$. In applications where this operation range must be further extended, active attenuators or level shifters can be used.

Transconductance Multipliers. A direct, straightforward technique to realize the four-quadrant multiplication function exploits the possibility of tuning the gain of differential-input transconductors through an electrical variable (current or voltage). Although this feature is exhibited also by single-ended transconductors, most practical realizations use differential-input blocks to reduce offset problems and enhance linearity (2). Figure 20 shows the general concept of the variable transconductance multipliers. It consists of two identical cross-coupled transconductor cells, driven by the input signals V_{1A} and V_{1B}, such that

$$\begin{aligned} I_{m1} &= I_{1+} - I_{1-} = G_{m1}(V_{1A} - V_{1B}) \\ I_{m2} &= I_{2+} - I_{2-} = G_{m2}(V_{1A} - V_{1B}) \end{aligned} \tag{29}$$

and a tuning circuit, controlled by the voltages V_{2A} and V_{2B}, which defines the transconductance gains G_{mj} ($j = 1, 2$) in Eq. (29) through the associated variables T_j. Usually, the transconductance gains G_{mj} takes the form,

$$G_{mj} = k_m g(T_j) \tag{30}$$

where k_m is a scaling factor; and $g(\cdot)$ is a real positive-definite, positive-valued invertible function whose argument is the tuning variable T_j. Thus, for multiplication purposes, the tuning circuitry must provide either of the two following output signal pairs:

$$\begin{aligned} T_1 &= g^{-1}[k_g(V_B + V_{2A})] \\ T_2 &= g^{-1}[k_g(V_B + V_{2B})] \end{aligned} \tag{31}$$

or

$$\begin{aligned} T_1 &= g^{-1}[k_g(V_B + V_{2A} - V_{2B})] \\ T_2 &= g^{-1}[k_g(V_B + V_{2B} - V_{2A})] \end{aligned} \tag{32}$$

where $g^{-1}(\cdot)$ is the (positive definite) inverse function of $g(\cdot)$; k_g is another scaling factor; and V_B is a bias voltage that can be implicitly contained in the common-mode value of V_{2A} and V_{2B}. Taking into account the role of control signals V_{2A} and V_{2B} in the argument of the function $g^{-1}(\cdot)$, the tuning circuitry defined by Eq. (31) will be referred to as *separable,* whereas that described by Eq. (32), as *nonseparable.* These mathematical definitions have a direct physical counterpart, since separable tuning circuits, contrary to the nonseparable ones, are built in practice using separate blocks.

For the separable tuning circuit, substituting Eq. (31) into Eq. (30), and considering the characteristics in Eq. (29), the differential output current of the block in Fig. 20, takes the form

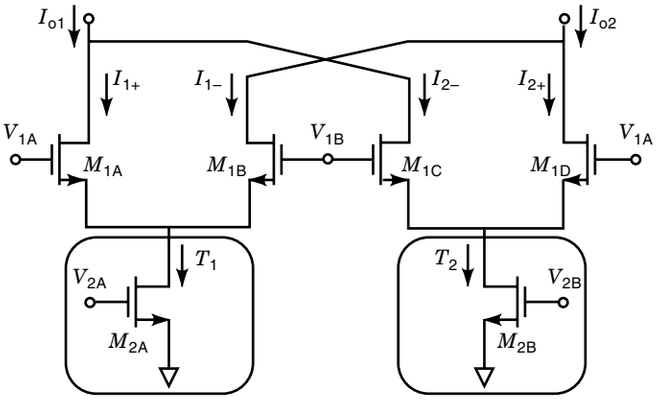
$$I_o = I_{o1} - I_{o2} = I_{m1} - I_{m2} = k_m k_g (V_{1A} - V_{1B})(V_{2A} - V_{2B}) \tag{33}$$

and, similarly, for the nonseparable tuning circuitry

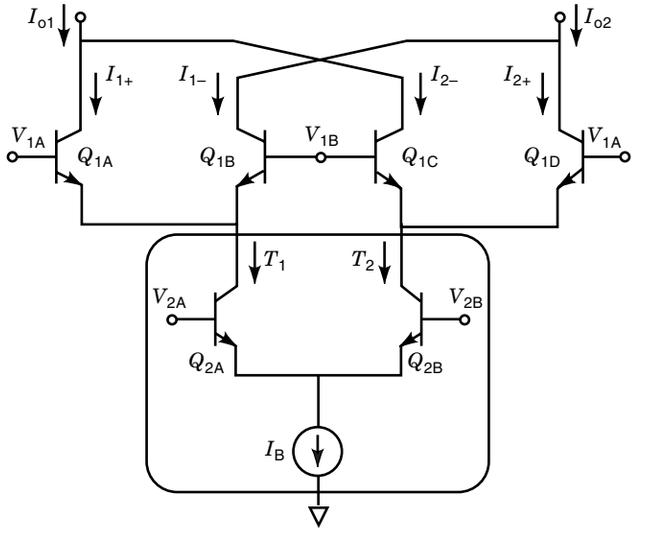
$$I_o = I_{o1} - I_{o2} = I_{m1} - I_{m2} = 2k_m k_g (V_{1A} - V_{1B})(V_{2A} - V_{2B}) \tag{34}$$

Observe that in both cases, I_o is proportional to the product of the differential input voltages $V_1 = V_{1A} - V_{1B}$ and $V_2 = V_{2A} - V_{2B}$, thus leading to four-quadrant multiplication. Also, it is worth noting that, for separable tuning circuits, the block in Fig. 20 can be seen as a cross-coupled connection of a pair of two-quadrant multipliers because $g(\cdot)$ is positive definite, and the sign of the output current is uniquely determined by the differential voltage V_1.

Figure 21(a) shows an example of MOST separable tuning variable transconductance multiplier where variables T_1 and T_2 are in the form of currents (a similar bipolar counterpart can be found in Ref. 2). If the input signal V_1 is small as compared to $\sqrt{n_1 T_1/\beta_1}$ and $\sqrt{n_1 T_2/\beta_1}$, then the differential output currents I_{mj} ($j = 1, 2$) of the cross-coupled differential pairs



(a)



(b)

Figure 21. (a) MOS separable tuning variable transconductance multiplier; (b) bipolar nonseparable tuning variable transconductance multiplier.

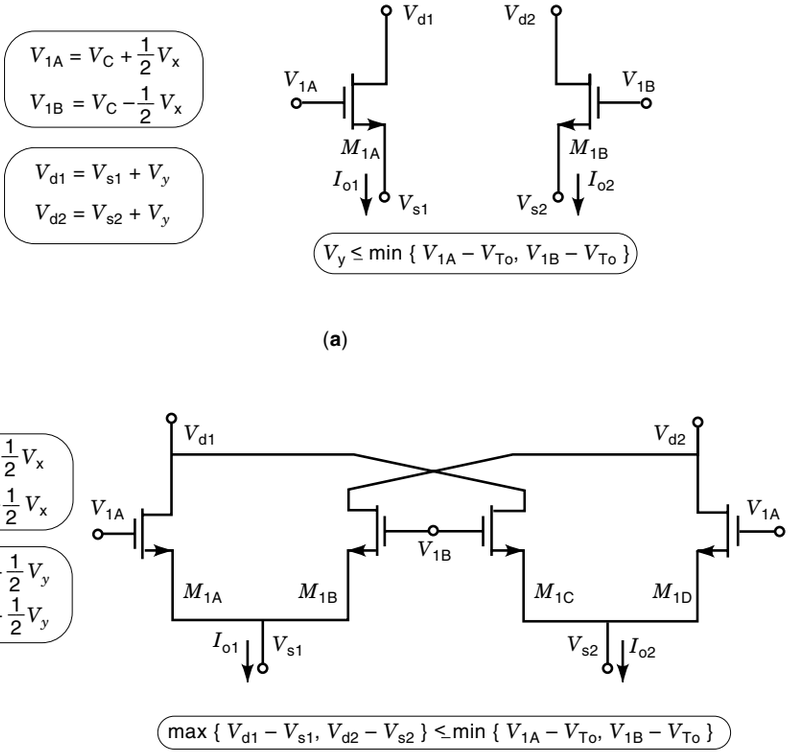


Figure 22. Four-quadrant multiplier cores using MOS transistors in the ohmic region. (a) Basic differential architecture; (b) cross-coupled quad configuration.

can be approximated as

$$I_{mj} = I_{j+} - I_{j-} = \sqrt{\frac{2\beta_1 T_j}{n_1}}\,(V_{1A} - V_{1B}) \tag{35}$$

Comparing Eqs. (30) and (35), it is clear that function $g(\cdot)$ is the square root operator. As was previously shown, its inverse function (i.e., the squaring operator) can be implemented by simply exploiting the quadratic law of MOSTs in the saturation region. Consequently, the tuning circuit may consist of two voltage driven MOSTs as shown in Fig. 21(a). This gives the following values for the biasing currents T_1 and T_2,

$$\begin{aligned} T_1 &= \frac{\beta_2}{n_2}\,(V_{2A} - V_{SS} - V_{To})^2 \\ T_2 &= \frac{\beta_2}{n_2}\,(V_{2B} - V_{SS} - V_{To})^2 \end{aligned} \tag{36}$$

which when compared to Eq. (31), gives $V_B = -(V_{SS} + V_{To})$ and $k_g = \sqrt{\beta_2/n_2}$. Therefore, taking into account Eq. (33), the differential output current of the multiplier is given by

$$I_o = I_{m1} - I_{m2} = \sqrt{2\frac{\beta_1\beta_2}{n_1 n_2}}\,(V_{1A} - V_{1B})(V_{2A} - V_{2B}) \tag{37}$$

Figure 21(b) shows a bipolar transconductance multiplier using a nonseparable tuning circuit (indicated by the shaded areas). This multiplier architecture is commonly known as *Gilbert cell* or *Gilbert multiplier core* (15). Observe that the tuning mechanism is provided by a third differential pair with a constant bias current. Assuming that the differential output currents of the emitter-coupled pairs in Fig. 21(b) are defined as shown in Fig. 11, the output current of the multiplier core reads as (2)

$$I_o = I_B \tanh\left(\frac{V_{1A} - V_{1B}}{2U_t}\right) \tanh\left(\frac{V_{2A} - V_{2B}}{2U_t}\right) \tag{38}$$

thus, an approximately linear response is obtained whenever the input signals V_1 and V_2 are small as compared to $2U_t$. Bipolar-like Gilbert cells have been also implemented in complementary metal oxide semiconductor (CMOS) technologies using MOST operated in the weak inversion region (7), and using compatible lateral bipolar transistors (36). An inconvenience of the Gilbert cell, particularly stressing in the MOST version, is the high supply voltage requirements to bias the stacked differential pairs, which render the structure poorly suited for low-voltage applications. This can be solved by using folded circuits (37).

A major drawback of the circuits in Fig. 21 is the rather small multiplication range. This makes the circuits only suitable for low-resolution applications as in artificial neural networks (38). In order to improve the linearity performance, several strategies have been proposed, usually employing Gilbert cells. One technique consists of using differential active attenuators at the input of the multiplier core to increase signal swing capabilities (39). Most often, a predistortion nonlinearity in series with the input signals are used in order to achieve an ideal four-quadrant multiplier. This is, for instance, the approach followed in the classical Gilbert multi-

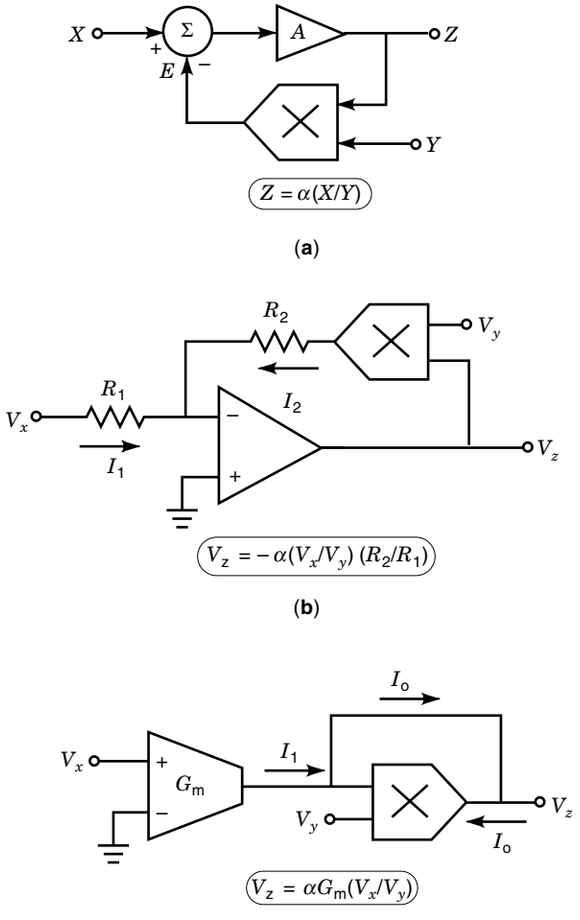


Figure 23. Division operator using a feedback multiplier: (a) concept; (b) with voltage multiplier and opamp; (c) with transconductance multiplier and amplifier.

plier (2), where a bipolar Gilbert cell is linearized by using $\tanh^{-1}$ type predistortion. Application of this approach to MOST Gilbert cells can be found in Ref. 40. A third technique to increase the multiplier linearity consists on using linearized transconductors instead of basic differential pairs. For instance, in Ref. 37 the upper differential pairs of a MOST Gilbert cell have been replaced with adaptively biased MOST saturated transconductors. The proposals in Refs. 19 and 41 substitute all the three differential pairs of a MOST Gilbert cell with source-coupled linearized stages. Finally, the separable MOST transconductance multiplier of Fig. 21(a) can be improved by replacing the basic differential pairs with voltage-biased common-source differential pairs so that the difference between their respective tail voltages is proportional to V_2 (42).

Ohmic Region Multipliers. A fourth class of analog multipliers exploits the large-signal transfer characteristic of MOST in the ohmic region, which contains a term proportional to the product of the gate voltage and the drain-to-source voltage drop. As usual, remaining terms can be cancelled out by using differential structures.

The most simple triode multiplier capable of four-quadrant operation consists of two matched MOSTs with identical drain-to-source potential and driven by fully balanced gate voltages. The circuit is shown in Fig. 22(a). One of the multiplicands (that controlling the drain-to-source voltage drop) is single-ended, while the other (controlling the gate voltages) is differential. Taking into account Table 1 and assuming $V_{s1} = V_{s2}$, the differential output current of the cell results in

$$I_o = I_{o1} - I_{o2} = 2\beta_1 V_x V_y \tag{39}$$

thus achieving linear multiplication. The valid operation range is indicated in the inset of Fig. 22(a). Practical usage of this circuit requires some extra circuitry to properly define the voltages at the source and drain terminals, regardless of the currents flowing through the transistors. The most simple alternative is by using low output impedance unity-gain buffers at the drain terminals of transistors M_{1A} and M_{1B}, as well as, at the source nodes. This is, for instance, the approach followed in Ref. 43 where the voltage follower action of the buffers is enhanced using local feedback. To keep the drain

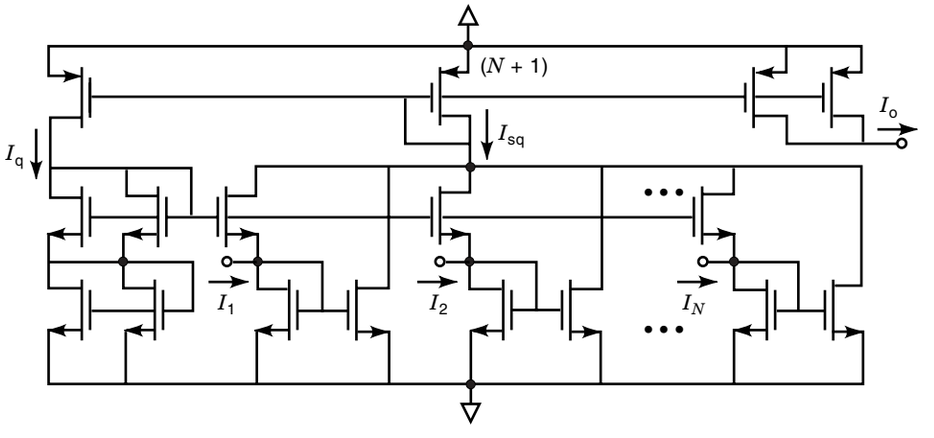
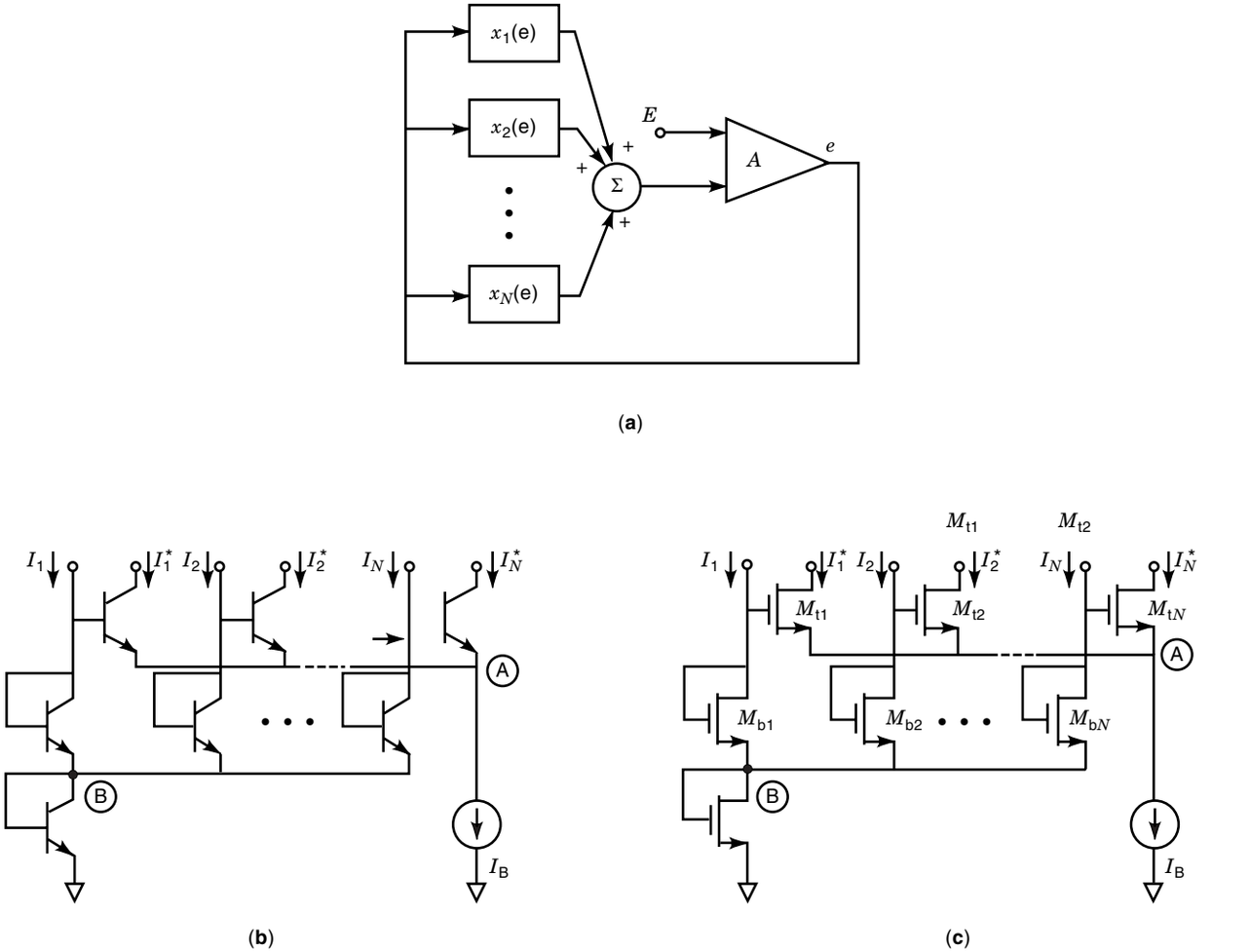


Figure 24. CMOS self-biased Euclidean distance circuit.



(**a**)

(**b**)

(**c**)

Figure 25. Current-mode normalization circuits: (a) feedback concept; (b) BJT; (c) CMOS.

terminals equipotential, corresponding buffers must be driven by the same voltage. Another approach to obtain a virtual short between the drain terminals exploits the virtual ground between the input nodes of voltage-mode opamps (44).

A main disadvantage of the multiplier in Fig. 22(a) is that the magnitude of the differential output current given by Eq. (39) will generally be small as compared to the individual current values of I_{o1} and I_{o2}. As a consequence, the processing circuitry driven by the multiplier (either a subtraction stage or a common-mode cancellation structure) will suffer from appreciable errors, the larger as the common-mode to differential mode output current ratio increases. An alternative triode multiplier, for which the magnitude of the differential signal components are comparable to their common-mode value, is shown in Fig. 22(b) (45–47). This multiplier can be seen as a cross-coupled connection of two circuits like those in Fig. 22(a), but with fully balanced drain-to-source voltage drops. Assuming $V_{s1} = V_{s2}$, the differential output current of the multiplier in Fig. 22(b) is given by

$$I_o = I_{o1} - I_{o2} = 2\beta_1 V_x V_y \tag{40}$$

with the valid operation range indicated in the figure. Again, the accuracy of the fully differential multiplier in Fig. 22(b) strongly depends on the availability of low-impedance loading stages to sink the output currents of the triode transistors. A common strategy consists on using cascade devices with very large transconductance on top of the ohmic transistors. Some circuit solutions following this approach can be found in Refs. 48 and 49. Another possibility is to exploit the virtual ground property of operational amplifiers, as proposed in Refs. 45 and 50. Interestingly enough, the circuit in Ref. 50 is able to perform several algebraic operations (multiplication, division, square rooting, and voltage amplification) without the use of any external dedicated circuitry.

Division

Most of the divider solutions found in the literature are based on the multiplication circuitry presented in the previous section. In some cases, application is straightforward since the scale factor of the multiplication is inversely proportional to a third variable, which acts as the dividend. This occurs, for instance, in the signal processing multipliers of Figs. 15 and 16, which can be employed for division by making the reference level V_α variable, or in the log–antilog multiplier of Fig. 17(a), by making the current I_3 to represent the denominator of the divider.

In cases where there is no explicit electrical variable to be used as dividend, analog division can still be realized by applying feedback around a multiplier—a similar strategy to that applied for the obtention of the logarithmic and square rooting operators. The concept is illustrated in Fig. 23(a); the multiplier obtains $E = (ZY)/\alpha$, and, for $A \to \infty$, the feedback forces $X = E$. Thus, if $Y \neq 0$, the circuit obtains $Z = \alpha(X/Y)$. This concept of division is applicable regardless of the physical nature of the variables involved. In the special case where E and X are current and Z is a voltage, the division can be accomplished using KCL to yield $X = E$. Figure 23(b) shows a circuit for the case where the multiplication is in voltage domain, and Fig. 23(c) is for the case where multiplication is performed in transconductance domain. The transconductance gain for input Z of this latter case must be negative to guarantee stability (51).

Collective Computation Circuitry

Radial basis functions and fuzzy inference require multidimensional operators to calculate radial distances in the case of radial basis functions and to normalize vectors and calculate T-norms in the case of fuzzy inference. These operators can be expressed as the interconnection of the nonlinear blocks discussed previously or realized in simpler manner through dedicated collective computation circuitry. Most of these circuits operate intrinsically in current domain and are worth mentioning because their simplicity and relevance for parallel information processing systems.

Vector Magnitude. Figure 24 (52) shows a CMOS circuit to compute the magnitude of an N-dimensional vector with current components I_k, which is based on the translinear current squarer of Fig. 3(b). The configuration of transistors M_2, M_4, and M_5 of Fig. 3(b) is repeated N times with the N input currents to produce the total current I_{sq}

$$I_{sq} = NI_q + \frac{1}{4I_q} \sum_{k=1..N} I_k^2 \tag{41}$$

This current is used to self-bias the structure of Fig. 24 by imposing, through the weighted p-channel current mirrors:

$$I_q = \frac{I_o}{2} = \frac{I_{sq}}{N+1} \tag{42}$$

which yields, by introducing Eq. (41),

$$I_o = \sqrt{\sum_{k=1..N} I_k^2} \tag{43}$$

If the current I_k at each terminal is shifted through a bias current of value δ_k, the circuit serves to compute the Euclidean distance between the vector of input currents and the vector δ.

Normalization Operation. The normalization circuit operation can be summarized by the following two expressions:

$$x_k^* = F(\boldsymbol{x}), \quad x_k^* = \kappa x_k \tag{44}$$

$$|\boldsymbol{x}^*| = \sum_{k=1..N} x_k^* = E \tag{45}$$

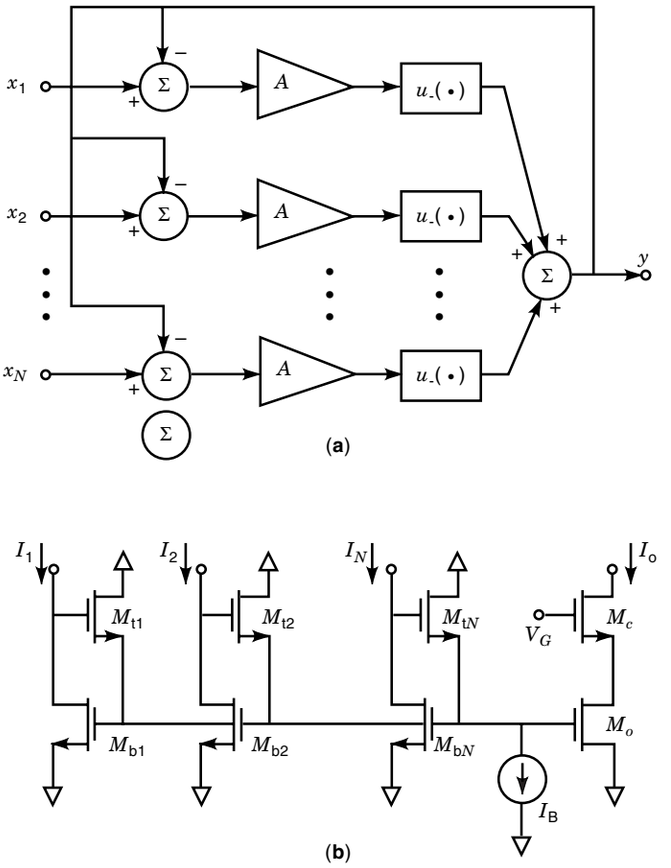


Figure 26. Concept for (a) maximum operator and (b) current-mode realization.

where $F(\cdot)$ is an increasing monotonic function of x_k, for $1 \leq k \leq N$; E is a reference level; and κ is a scale factor. An elegant strategy to achieve Eqs. (44) and (45) uses feedback to maintain constant the sum of components of vector $\boldsymbol{x}^*$ (53). Figure 25(a) illustrates the concept. Every x_k, $1 \leq k \leq N$, is controlled by the error signal, e, at the differential amplifier

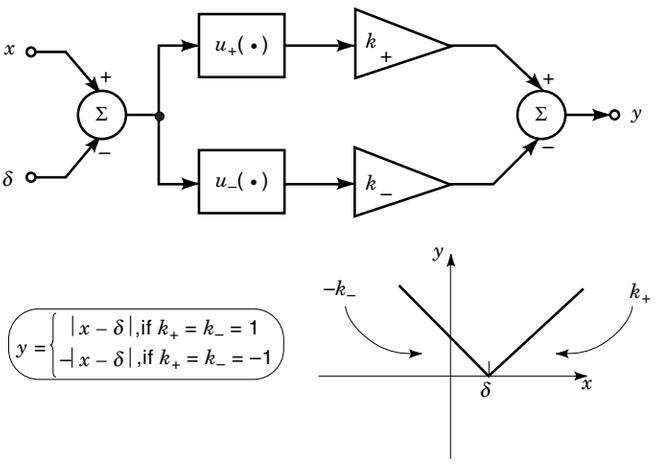


Figure 27. Generic full-wave rectifier. Positive and negative absolute value functions can be implemented as shown in the inset.

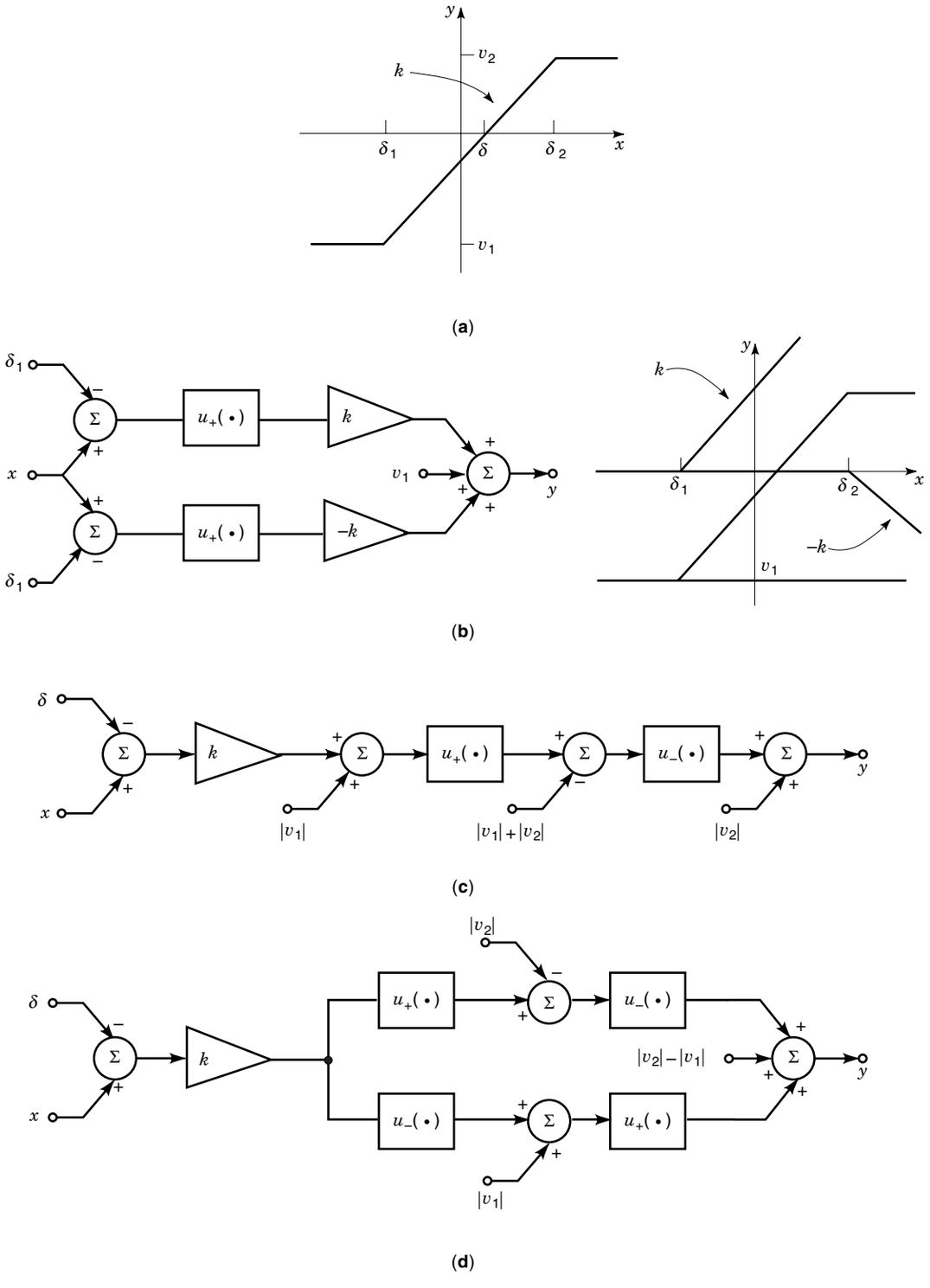


Figure 28. (a)–(d) PWL soft-sigmoid function realizations.

output. If the open-loop gain is large enough and the loop stable, feedback forces the differential amplifier input to zero, and consequently $\sum x_k^*(e^*) = 1$, where e^* is the steady-state value of the differential amplifier output. Unfortunately, the transient response of this normalization scheme is rather poor—a negative consequence of feedback.

Figure 25(b,c) show circuit solutions, for the BJT (15) and CMOS (28) case, respectively, which normalize an input current vector, $\boldsymbol{I}$, without explicit feedback, and hence yield much better transient response than the previous proposal. Their operation is based on the translinear principle. Let us consider the BJT case. Assuming that all transistors are identi-

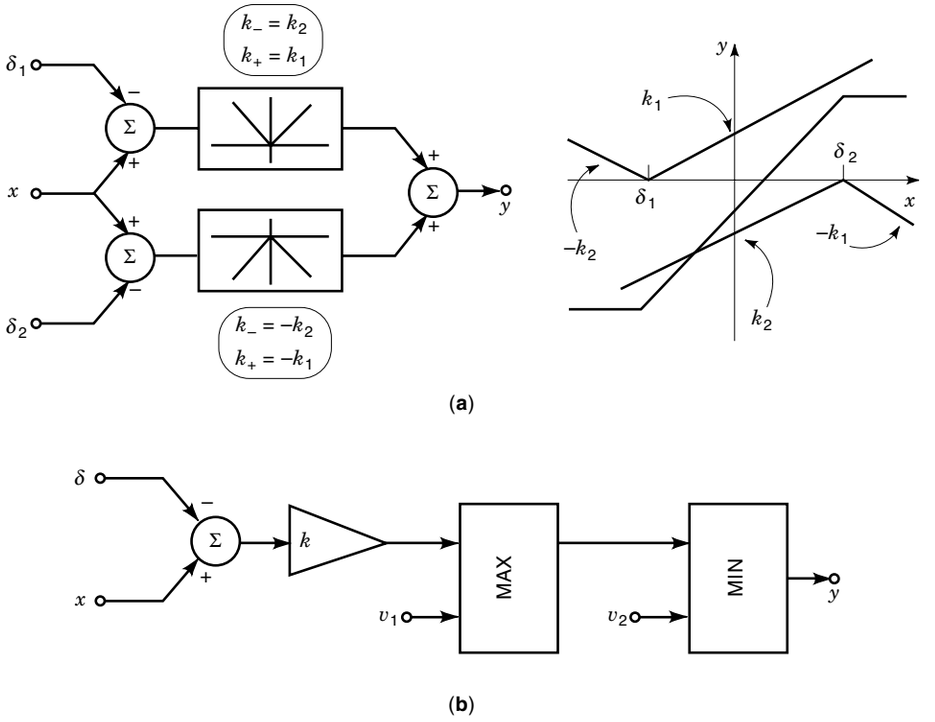


Figure 29. PWL soft-sigmoid function realizations based on (a) full-wave rectifiers; (b) max-min operators.

cal, the voltage drop between the common emitter nodes A and B verifies

$$V_A - V_B = kT \ln\left[\frac{I_k^*}{I_s}\right] - kT \ln\left[\frac{I_k}{I_s}\right] = kT \ln\left[\frac{I_k^*}{I_k}\right] \tag{46}$$

for $1 \leq k \leq N$. Since this voltage drop is the same for all transistor pairs, Eq. (44) is met. Simultaneously, KCL forces the sum of all the output vector components to be equal to the bias current I_B (ignoring base currents), and thus we have

$$I_k^* = \frac{I_k}{\sum_{j=1,N} I_j} \tag{47}$$

which is the intended operation. For the MOST circuit of Fig. 25(c), the translinear principle gives

$$V_A - V_B = \sqrt{\frac{I_k^*}{\beta_t}} - \sqrt{\frac{I_k}{\beta_b}} \tag{48}$$

which yields

$$I_k^* = \frac{\beta_t}{\beta_b} I_k \left[1 + \sqrt{\frac{\beta_b}{I_k}} (V_A - V_B)\right]^2 \tag{49}$$

Summing for all k, as in Eq. (45), and after some algebra, the following expression is obtained for $F(\cdot)$:

$$I_k^* = F(\boldsymbol{I}) = \frac{\beta_t}{\beta_b} I_k \left[1 + \frac{\eta(\boldsymbol{I})}{\sqrt{I_k}}\right]^2 \tag{50}$$

with,

$$\eta(\boldsymbol{I}) = \frac{\sum_{k=1,N} \sqrt{I_k}}{N} \left[\sqrt{1 + \frac{N\left[\frac{\beta_b}{\beta_t} I_B - \sum_{k=1,N} I_k\right]}{\left[\sum_{k=1,N} \sqrt{I_k}\right]^2}} - 1\right] \tag{51}$$

Note that Eq. (45) is always fulfilled because $|\boldsymbol{I}^*| = I_B$; however, Eq. (44) is only verified if the quotient $\eta(\boldsymbol{I})/\sqrt{I_k}$ in Eq. (50) is the same for all k. This occurs only if the input currents are already normalized; we have $\sum I_k = (\beta_b/\beta_t)I_B$ and then $\eta(\boldsymbol{I}) = 0$. Otherwise, depending on how $\sum I_k$ differs from $(\beta_b/\beta_t)I_B$, the proportionality constant κ becomes more and more k-dependent and deviations from Eq. (44) increase. Nevertheless, proper design obtains quasilinear transformation of I_k into I_k^*, which can be tolerated in most neurofuzzy systems, where nonlinearities are corrected through adaptation.

Minimum and Maximum Operators. The calculation of the minimum of an input vector $\boldsymbol{x}$ is functionally equivalent to obtaining the complement of the maximum of the complements of its components. Thus, only maximum operators will be considered hereafter. Figure 26(a) illustrates a classical approach used in analog computation to calculate the maximum of an input vector $\boldsymbol{x}$. It is based on the following steady state equation (4):

$$-y + \sum_{k=1,N} u_-[A(x_k - y)] = 0 \tag{52}$$

where A is large and function $u_-(\cdot)$ is defined in Eq. (5). This concept can be realized in practice using operational trans-

conductance amplifiers (OTAs) or opamps, and diodes. Both of these have voltage input and output. An alternative maximum/propagate concept realizes the following equation:

$$-y + \sum_{k=1,N} x_k u_o(x_k - y) = 0 \tag{53}$$

where $u_o(\cdot)$ is the threshold operator (Heaviside function), which can be easily implemented in the current domain by using current comparators (28). Unfortunately, both approaches exhibit a rather slow transient response as a consequence of the feedback mechanism used.

Another solution, which avoids this lack of operation speed, is shown conceptually in Fig. 26(b). It is based on the winner-take-all circuit of Lazzaro et al. (28,54) and exploits the characteristics of MOSTs operating in ohmic region; in particular, the possibility to reduce its current density by driving it with small drain-to-source voltages. The operation of the circuit is as follows. First, note that all transistors M_{bk}, for $k = 1, \ldots, N$, have the same gate-to-source voltage V_{gs}, which is also shared by the output transistor M_o. The steady state value of this voltage is set by the largest input current $I_{k,\max}$ as

$$V_{gs} = V_{To} + \sqrt{\frac{nI_{k,\max}}{\beta_b}} \tag{54}$$

where β_b is the transconductance factor of transistors M_{bk}. All bottom transistors are driven by this common voltage to draw the maximum current $I_{k,\max}$, while the externally applied current may be smaller than $I_{k,\max}$. Thus, the gate of each top transistor, M_{tk}, becomes an error-sensitive node that detects differences between corresponding external current and the maximum current. If $I_k < I_{k,\max}$, the error current $I_k - I_{k,\max}$ is integrated in the gate-to-source capacitor of transistor M_{tk}, the corresponding voltage drop decreases and consequently, the drain-to-source voltage of the associated bottom transistor M_{bk} decreases until the transistor enters in ohmic region and the error current becomes null.

DERIVED PIECEWISE NONLINEAR OPERATIONS

As previously stated, the rectifier blocks devised in the section entitled "Rectification" can serve as basic building blocks for the realization of many elementary piecewise linear functions. Synthesis strategies for the implementation of the most common PWL nonlinearities (absolute value, saturation, basis functions, etc.) are detailed in the following.

Regarding the absolute value function, Fig. 27 shows a general realization that allows one to control the slopes of the characteristic, as well as, the position along the x axis. If an offset value along the y axis is also required, a constant contribution must be added to the rightmost summer. This kind of circuit is commonly known as a full-wave rectifier. Figure 28 shows some implementations of the PWL soft-sigmoid function represented in Fig. 28(a). These circuits are also known as signal limiters. The circuit in Fig. 28(b) is built upon the characteristic decomposition shown at the right of the figure, based on the extension operator formulation. An inconvenience of this architecture is the need for input signal replication to drive the half-wave rectifiers, which require additional circuitry if x is in current form. This can be solved by using the circuit of Fig. 28(c) which uses nested rectifications. Observe that the circuit achieves the intended functionality with a minimum number of block elements and, in this sense, it can be regarded as canonical. The circuit in Fig. 28(d) is also based on nested rectifications, but it is not canonical. Anyway, because its symmetry, it leads to very modular implementations particularly using current-mode techniques.

Other signal limiter realizations employ building blocks other than the basic rectifier circuits defined in Eq. (7). Some examples are shown in Fig. 29. That in Fig. 29(a) obtains the PWL soft-sigmoid function by adding the output signals of two shifted odd-symmetric full-wave rectifiers. According to Fig. 28(a) and the characteristic decomposition at the right of Fig. 29(a), the slope of the central piece of the sigmoid is given by $k = k_1 + k_2$. The circuit of Fig. 29(b) are based on the maximum and minimum operators described in the previous section.

Figure 30(b,c) shows two simple block diagrams, based on the full-wave rectifiers devised in Fig. 27, for the Hermite linear basis functions represented in Fig. 30(a). In both cases, the desired characteristic is obtained by shifting the full-wave rectification map along the y axis by an amount equal to the

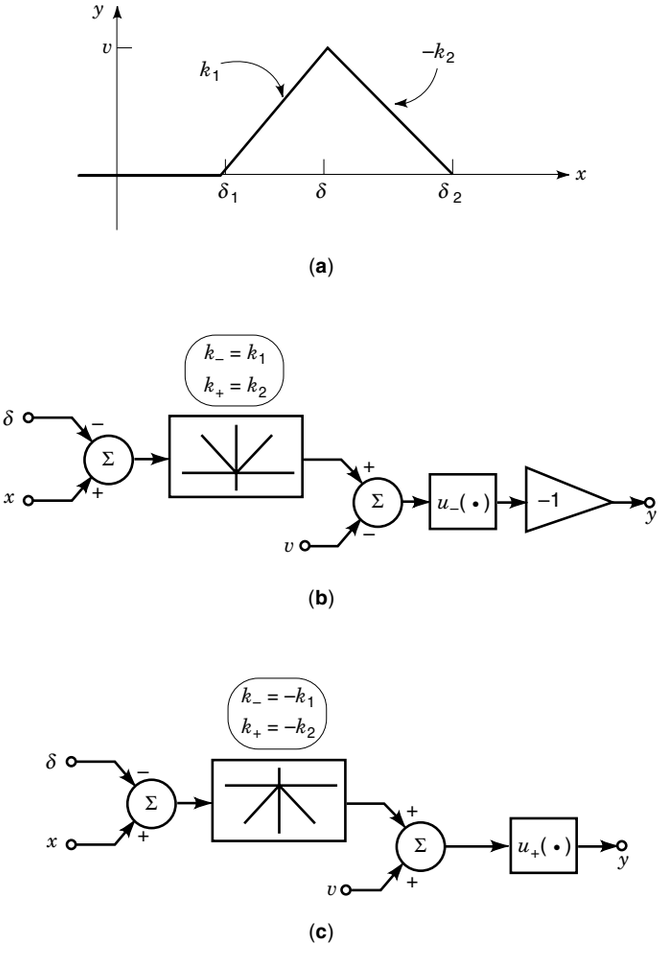


Figure 30. Linear basis functions.

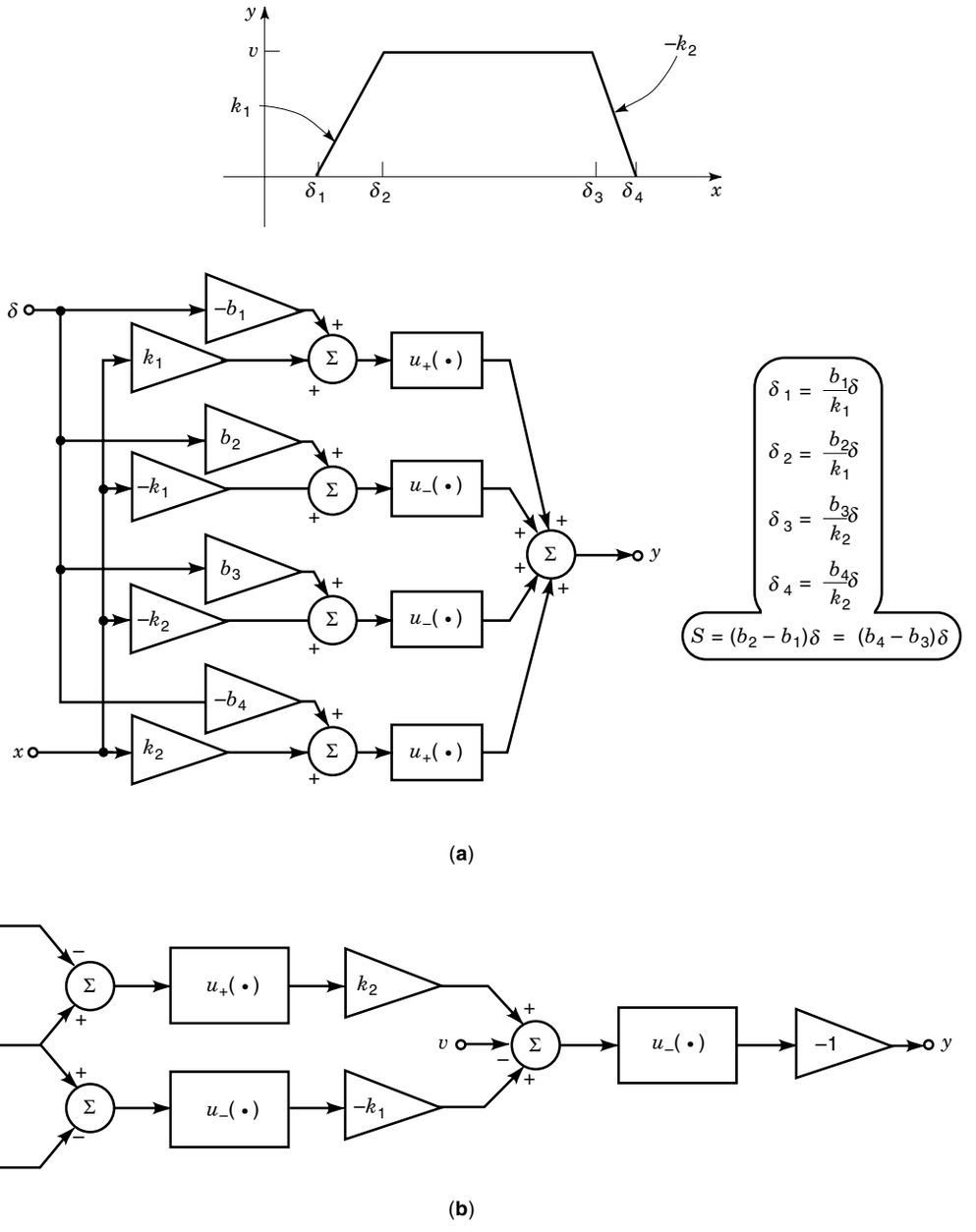


Figure 31. Trapezoidal membership functions.

height of the basis function and then rectifying in the proper direction to obtain the triangular input–output representation.

Finally, Fig. 31 shows some implementations of trapezoidal membership functions based on half-wave rectifiers. The circuit in Fig. 31(a) is a direct realization of the characteristic decomposition in extension operators. A more simple circuit can be obtained by nested rectifications. Figure 31(b) shows an example based on the expression

$$y = -u_-[k_2u_+(x - \delta_3) - k_1u_-(x - \delta_2) - v] \tag{55}$$

which allows saving functional blocks as compared to Fig. 31(a).

Alternative realizations of the trapezoidal membership functions are shown in Fig. 32. That in Fig. 32(a) is similar to the architectures used for linear basis functions but with an additional nested rectification. Of course, a dual implementation starting from a negative full-wave rectifier is also possible. The circuit in Fig. 32(b) obtains the trapezoidal function by adding the outputs of two PWL soft-sigmoid blocks with central slopes of opposite signs. Finally, the implementation in Fig. 32(c) is a combination of two shifted Hermite linear basis functions with identical height, in order to obtain a flat response between the breakpoints δ_2 and δ_3. Other realizations of trapezoidal functions consist of combinations of sigmoid characteristics or linear basis functions with maximum and/or minimum operators.

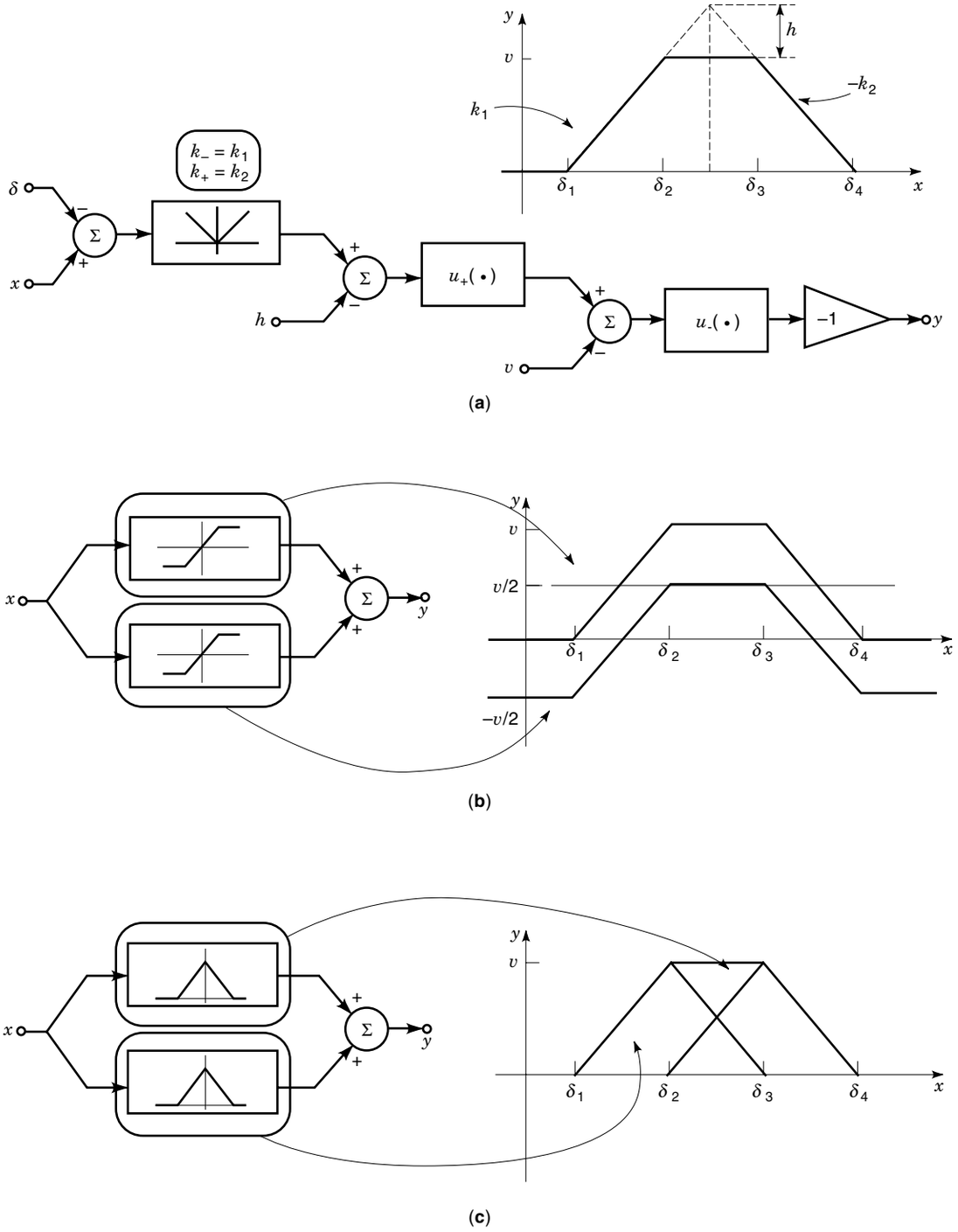
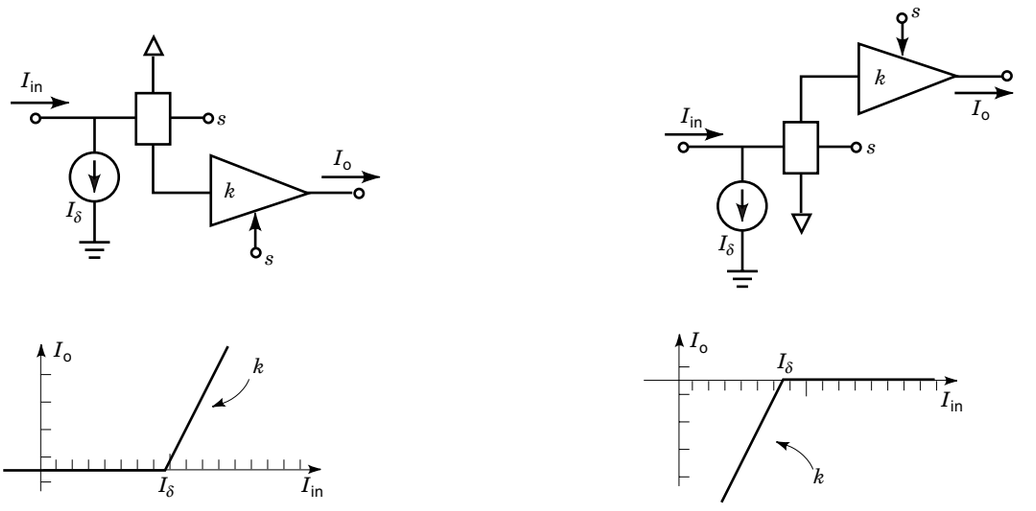


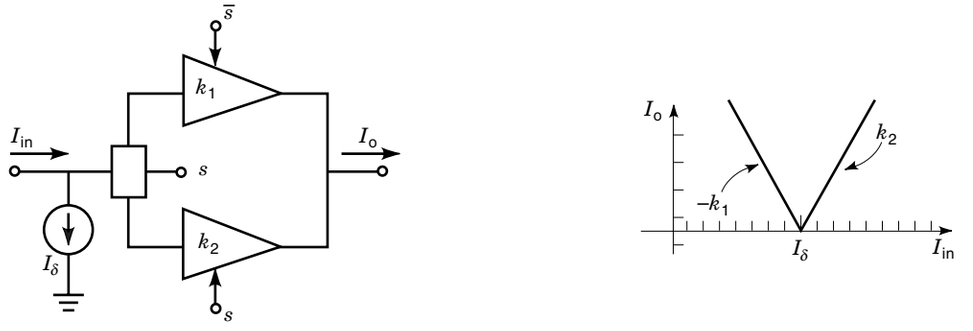
Figure 32. Alternative trapezoidal membership function implementations.

As an example of application of the preceding synthesis strategy for PWL functions, Fig. 33 shows an extensive catalog of circuit solutions (24) based on the current feedback comparators, which are represented as square boxes. They have three terminals corresponding to the input and drain nodes of the comparator and, in some cases, a fourth terminal for the binary signal V_s. On the other hand, triangular blocks represent tunable current amplifiers with gain $k > 0$, where the flow of the output current can be made positive or negative according if the binary control signal s is in the high or low state.

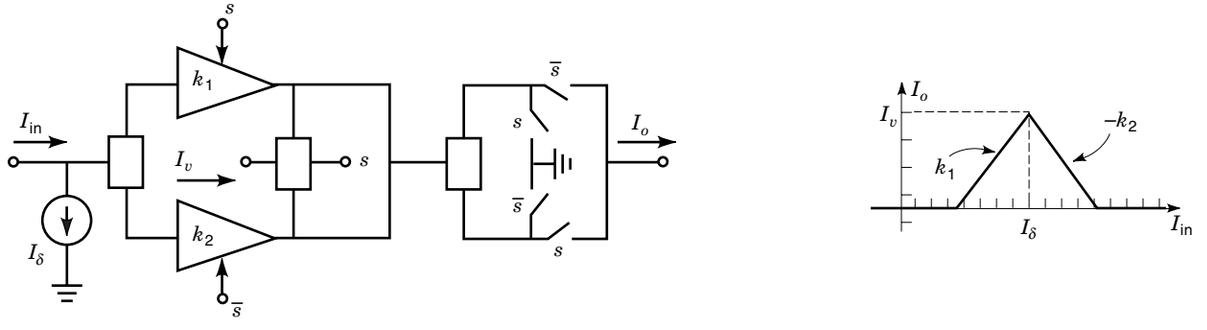
Figure 33(a) shows the construction of the positive concave and convex extension operators and Fig. 33(b), the realization of the positive full-wave rectification function. In both cases, negative functions can be easily obtained by driving the current amplifiers with complemented binary signals.



(**a**)



(**b**)



(**c**)

Figure 33. Block diagrams for (a) concave and convex extension operators; (b) full-wave rectification; (c) Hermite linear basis function. Block diagrams for (d) dead-zone nonlinearity; (e) soft limiter function; (f) discontinuous function; and (g) trapezoidal function. (Figure continues on next page.)

Figure 33(c) shows the block diagram for a linear basis function formed by three current comparators, two current amplifiers, and four analog switches in the output stage. Note that the central current comparator provides the binary signal that determines the sign of the current amplifiers and the output branch through which I_o flows.

Figure 33(d) shows a realization for the dead-zone nonlinearity. In this case, binary signals to the current amplifiers are externally supplied, resulting in a complete control on the slopes of the characteristic.

Figure 33(e) shows the implementation of a soft limiter characteristic, which comprises three current comparators

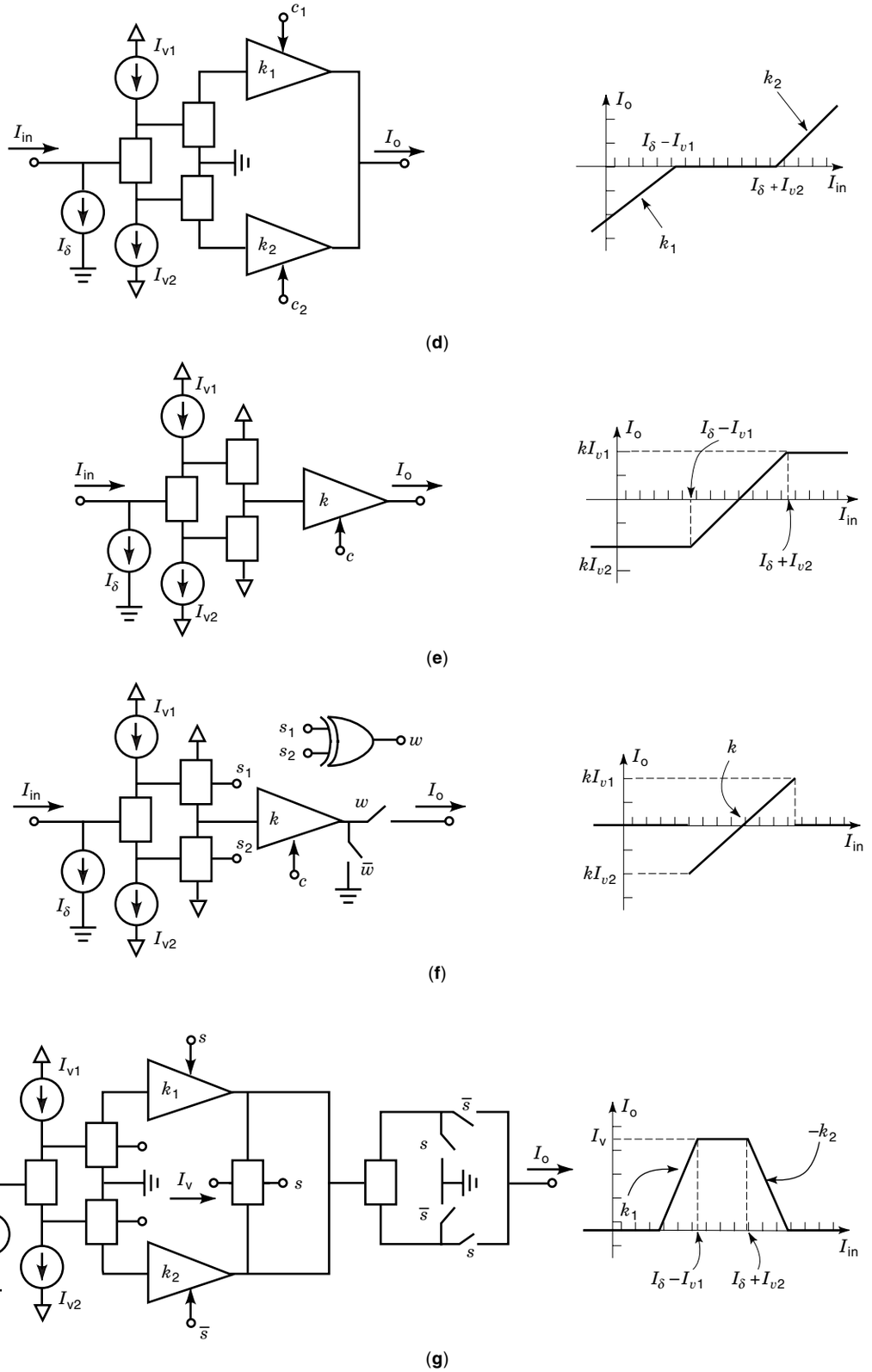


Figure 33. ***(Continued)***

and one current amplifier. This realization is inspired by the block diagram of Fig. 28(d), the only difference being that current amplification is performed at the backend of the circuit. Relevant features of the circuit are its low area consumption (bear in mind that current comparators may consists of just six transistors if the voltage amplifier is implemented with a CMOS inverter), high-speed operation (no nodal saturation takes place), and high precision (errors in the rectification knots are in the order of few picoamperes).

Figure 33(f) shows an example of construction of functions with finite jump discontinuity, taking advantage of the binary signal generated by the current comparators, together with the logic gates.

Finally, Fig. 33(g) shows the realization of a trapezoidal function. The architecture is similar to that in Fig. 31(b). Note that instead of using two linear basis function like those in Fig. 32(c), the function symmetry enables the number of circuit components to be reduced.

BIBLIOGRAPHY

1. J. Singh, *Semiconductor Devices: An Introduction,* New York: McGraw-Hill, 1994.
2. P. R. Gray and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits,* 3rd ed., New York: Wiley, 1993.
3. A. B. Grebene, *Bipolar and MOS Analog Integrated Circuit Design,* New York: Wiley, 1984.
4. A. Hausner, *Analog and Analog / Hybrid Computer Programming,* Englewood Cliffs, NJ: Prentice-Hall, 1971.
5. D. H. Sheingold, *Nonlinear Circuits Handbook,* Norwood, MA: Analog Devices, 1976.
6. R. Unbehauen and A. Cichocki, *MOS Switched-Capacitor and Continuous-Time Integrated Circuits and Systems,* Berlin: Springer-Verlag, 1989.
7. C. Mead, *Analog VLSI and Neural Systems,* Reading, MA: Addison-Wesley, 1989.
8. E. Vittoz, Analog VLSI signal processing: Why, where and how?, *Analog Integrated Circuits and Signal Processing,* **6**: 27–44, 1994.
9. A. Rodríguez-Vázquez et al., Synthesis and design of nonlinear circuits, in W. K. Chen (ed.), *The Circuits and Filters Handbook,* Boca Raton, FL: CRC Press 1995.
10. B. J. Sheu and J. Choi, *Neural Information Processing and VLSI,* Boston: Kluwer, 1995.
11. J. W. Fattaruso and R. G. Meyer, MOS analog function synthesis, *IEEE J. Solid-State Circ.,* **SC-22**: 1059–1063, 1987.
12. K. Kimura, A CMOS logarithmic IF amplifier with unbalanced source-coupled pairs, *IEEE J. Solid-State Circuits,* **SC-28**: 78–83, 1993.
13. C. Turchetti and M. Conti, A general approach to nonlinear synthesis with MOS analog circuits, *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.,* **CAS-40**: 608–612, 1993.
14. E. Seevinck, *Analysis and Synthesis of Translinear Integrated Circuits,* Amsterdam: Elsevier, 1988.
15. B. Gilbert, Current-mode circuits from a translinear viewpoint: A tutorial, in C. Toumazou, F. J. Lidgey, and D. G. Haigh (eds.), *Analogue IC design: The current-mode approach,* London: Peregrinus, 1990.
16. H.-J. Song and C.-K. Kim, An MOS four-quadrant analog multiplier using simple two-input squaring circuits with source followers, *IEEE J. Solid-State Circ.,* **SC-25**: 841–848, 1990.
17. Y. H. Kim and S. B. Park, Four-quadrant CMOS analogue multiplier, *Electron. Lett.,* **28**: 649–650, 1992.
18. Z. Wang, A four-transistor four-quadrant analog multiplier using MOS transistors operating in the saturation region, *IEEE Trans. Instrum. Meas.,* **IM-42**: 75–77, 1993.
19. E. Seevinck and R. F. Wassenar, A versatile CMOS linear transconductor/square-law function circuit, *IEEE J. Solid-State Circ.,* **SC-22**: 366–377, 1987.
20. J. S. Peña-Finol and J. A. Connelly, A MOS four-quadrant analog multiplier using the quarter-square technique, *IEEE J. Solid-State Circ.,* **SC-22**: 1064–1073, 1987.
21. I. M. Filanovsky and H. P. Baltes, Simple CMOS analog square-rooting and squaring circuits, *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.,* **CAS-39**: 312–315, 1992.
22. R. Wiegerink, *Analysis and Synthesis of MOS Translinear Circuits,* Boston: Kluwer, 1993.
23. B. Razavi, *Principles of Data Conversion System Design,* Piscataway, NJ: IEEE Press, 1995.
24. A. Rodríguez-Vázquez et al., High-resolution CMOS current comparators: Design and applications to current-mode function generation, *Analog Integrated Circuits and Signal Processing,* **7**: 149–166, 1995.
25. A. Rodríguez-Vázquez and M. Delgado-Restituo, Generation of chaotic signals using current-mode techniques, *J. Intelligent Fuzzy Syst.,* **2**: 15–37, 1994.
26. Z. Wang, Novel pseudo RMS current converter for sinusoidal signals using a CMOS precision current rectifier, *IEEE Trans. Instrum. Meas.,* **IM-39**: 670–671, 1990.
27. B. J. Hosticka et al., Design of nonlinear analog switched-capacitor circuits using building blocks, *IEEE Trans. Circuits Syst.,* **CAS-31**: 354–368, 1984.
28. F. Vidal and A. Rodríguez-Vázquez, Using building blocks to design analog neuro-fuzzy controllers, *IEEE Micro,* **15** (4): 49–57, 1995.
29. T. Yamakawa, A fuzzy inference engine in nonlinear analog mode and its application to fuzzy control, *IEEE Trans. Neural Netw.,* **4**: 496–522, 1993.
30. P. W. Hollis and J. J. Paulos, Artificial neural networks using MOS analog multipliers, *IEEE J. Solid-State Circ.,* **SC-25**: 849–855, 1990.
31. D. Broadarac et al., Novel sampled-data MOS multiplier, *Electron. Lett.,* **18**: 229–230, 1982.
32. C. Jansson, K. Chen, and C. Svensson, Linear, polynomial and exponential ramp generators with automatic slope adjustment, *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.,* **CAS-41**: 181–185, 1994.
33. L. W. Massengill, A dynamic CMOS multiplier for analog VLSI based on exponential pulse-decay modulation, *IEEE J. Solid-State Circ.,* **SC-26**: 268–276, 1991.
34. X. Arreguit, E. Vittoz, and M. Merz, Precision compressor gain controller in CMOS technology, *IEEE J. Solid-State Circ.,* **SC-22**: 442–445, 1987.
35. K. Bult and H. Wallinga, A class of analog CMOS circuits based on the square-law characteristics of an MOS transistor in saturation, *IEEE J. Solid-State Circ.,* **SC-22**: 357–365, 1987.
36. T. Pan and A. A. Abidi, A 50-dB variable gain amplifier using parasitic bipolar transistors in CMOS, *IEEE J. Solid-State Circ.,* **SC-24**: 951–961, 1989.
37. J. N. Babanezhad and G. C. Temes, A 20-V four quadrant CMOS analog multiplier, *IEEE J. Solid-State Circ.,* **SC-20**: 1158–1168, 1985.
38. F. J. Kub et al., Programmable analog vector-matrix multipliers, *IEEE J. Solid-State Circ.,* **SC-25**: 207–214, 1990.
39. S. Qin and R. L. Geiger, A 5-V CMOS analog multiplier, *IEEE J. Solid-State Circ.,* **SC-22**: 1143–1146, 1987.

40. D. C. Soo and R. G. Meyer, A four-quadrant NMOS analog multiplier, *IEEE J. Solid-State Circ.,* **SC-17**: 1174–1178, 1982.
41. S. L. Wong, N. Kalyanasundaram, and C. A. T. Salama, Wide dynamic range four-quadrant CMOS analog multiplier using linearized transconductance stages, *IEEE J. Solid-State Circ.,* **SC-21**: 1120–1122, 1986.
42. K. Kimura, An MOS four-quadrant analog multiplier based on the multitail technique using a quadritail cell as a multiplier core, *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.,* **CAS-42**: 448–454, 1995.
43. S.-I. Liu, Low voltage CMOS four-quadrant multiplier, *Electron. Lett.,* **30**: 2125–2126, 1994.
44. M. Ismail et al., Configurable CMOS multiplier/divider circuits for analog VLSI, *Analog Integrated Circuits and Signal Processing,* **5**: 219–234, 1994.
45. B. Song, CMOS RF circuits for data communication applications, *IEEE J. Solid-State Circ.,* **SC-21**: 310–317, 1986.
46. Z. Czarnul, Novel MOS resistive circuit for synthesis of fully integrated continuous-time filters, *IEEE Trans. Circuits Syst.,* **CAS-33**: 718–721, 1986.
47. M. Ismail, Four-transistor continuous-time MOS transconductor, *Electron. Lett.,* **23**: 1099–1100, 1987.
48. A. L. Coban and P. E. Allen, Low-voltage, four-quadrant, analogue CMOS multiplier, *Electronics Lett.,* **30**: 1044–1045, 1994.
49. T. Botha, CMOS analogue current-steering multiplier, *Electron. Lett.,* **28**: 525–526, 1992.
50. N. I. Khachab and M. Ismail, A nonlinear CMOS analog cell for VLSI signal and information processing, *IEEE J. Solid-State Circ.,* **SC-26**: 1689–1699, 1991.
51. E. Sánchez-Sinencio et al., Operational transconductance amplifier-based nonlinear function synthesis, *IEEE J. Solid-State Circ.,* **SC-24**: 1576–1586, 1989.
52. O. Landolt, E. Vittoz, and P. Heim, CMOS Self-biased Euclidean distance computing circuit with high dynamic range, *Electron. Lett.,* **28**: 352–354, 1992.
53. M. Sasaki, Current-mode analog fuzzy hardware with voltage input interface and normalization locked loop, *IEICE Trans. Fundamentals,* **E75-A**: 650–654, 1992.
54. J. Lazzaro et al., Winner-take-all networks of O(n) complexity, in D. S. Touretzky (ed.), *Advances in Neural Information Processing Systems,* Vol. 1, Los Altos, CA: Morgan Kaufmann, 1989.

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