OPERATIONAL AMPLIFIERS

The operational amplifier, or op amp, is a particularly useful building block for electronic circuits. Although composed of numerous other devices, an op amp is usually treated as a single circuit element, commonly called the ideal op amp. By considering the op amp as an ideal circuit element, it is possible to analyze and design many useful circuits quickly. Once an op-amp circuit has been designed, the practical limitations of real op amps should be considered. In most cases, the limitations of practical op amps can be compensated for. When designing an op amp, the particular application and the type of devices used to implement the op amp should be closely considered.

THE IDEAL OP AMP

The ideal op amp has a differential input to an ideal voltage amplifier that has infinite gain and a single-ended output. While an infinite gain is somewhat impractical, op amps are rarely used alone. Instead, op amps are used with external circuitry connected between their output and input to set the circuit's overall characteristics. Since it is an ideal voltage amplifier, the op amp's input impedance is infinite. Hence, the op amp does not draw any current from the circuitry connected to its input. Also, since it is an ideal voltage amplifier, the ideal op amp's output impedance is zero. Hence, the op amp's output voltage is unaffected by its output current. The ideal op amp's equivalent circuit and its symbol are shown in

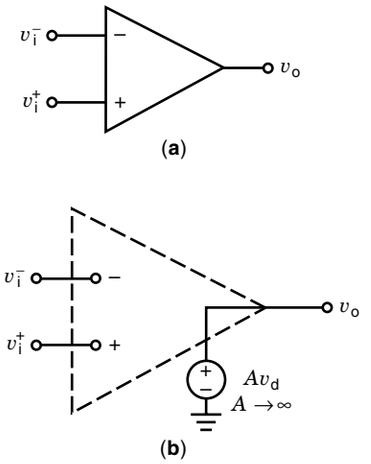

Figure 1. The ideal op amp: (a) symbol for an ideal op amp; (b) equivalent circuit.

Fig. 1. The terminals marked − and + are commonly referred to as the inverting terminal and the noninverting terminal, respectively. While practical op amps do not exhibit truly ideal behavior, their performance is such that the ideal op-amp model can be used to determine the behavior of most op-amp circuits with satisfactory results.

Common Op-Amp Configurations

Op-amp circuits combine an op amp with some external components. The characteristics of the resulting op-amp circuit are largely determined by the configuration of the external components. While numerous configurations exist, the most common of them are the inverting amplifier configuration and the noninverting amplifier configuration.

The Inverting Amplifier Configuration. The inverting configuration is shown in Fig. 2. The circuit's input-to-output relationship can be determined using straightforward circuit analysis. Since the op amp's input impedance is infinite it will have 0 input current. Therefore, the current through R_1 equals the current through R_2:

$$\frac{v_i - v_x}{R_1} = \frac{v_x - v_o}{R_2} \tag{1}$$

where v_i is the circuit's input voltage, v_o is the circuit's output voltage, and v_x is the voltage at the op amp's inverting terminal in Fig. 1. In addition, the op amp's gain A fixes the relationship between v_x and v_o:

$$v_x = \frac{-v_o}{A} \tag{2}$$

Combining Eqs. (1) and (2) yields the closed-loop gain

$$\frac{v_o}{v_i} = \frac{-R_2/R_1}{1 + (1 + R_2/R_1)/A} \tag{3}$$

where A is, by constrast, called the open-loop gain. For an ideal op amp, A is infinite so Eq. (3) reduces to

$$\frac{v_o}{v_i} = -\frac{R_2}{R_1} \tag{4}$$

The negative sign implies the output signal is inverted while the ratio $R_2 : R_1$ determines the amplification. Note that the gain is set by the ratio of the external components and is independent of the op amp's gain.

An important observation in the preceding analysis is that the voltage between the op amp's input terminals approaches 0 as the op amp's gain approaches infinity. This is due to the negative feedback provided by R_2. Provided the op amp has sufficiently high gain, when negative feedback is used, the voltage between the op amp's input terminals approaches 0 for finite output voltages. This leads to the concept of a *virtual short,* a situation in which two terminals have the same potential but no current flows between them. When one of the two terminals in a virtual short is connected to ground, the other is said to be a virtual ground. A *virtual ground* is a node that is at ground potential but does not have any current flowing directly to ground from it. An example of a virtual ground is the inverting terminal of the inverting amplifier configuration. The concept of a virtual short and a virtual ground is very useful for analyzing ideal op-amp circuits.

In Fig. 3, a virtual ground exists at the op amp's inverting terminal. Consequently, the currents through R_a, R_b, and R_c only depend on v_a, v_b, and v_c, respectively. These currents are all summed at the op amp's inverting terminal but cannot

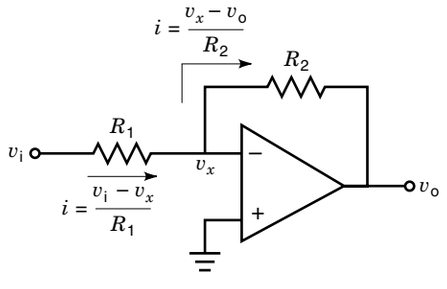

Figure 2. The inverting configuration.

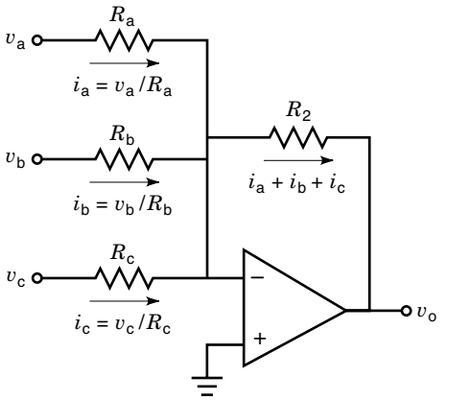

Figure 3. Generating a weighted sum.

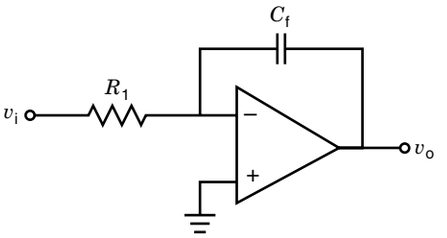

Figure 4. An inverting integrator.

flow into it. Therefore, the sum of the currents flows through R_2 to the output yielding an output voltage of

$$v_o = -R_2\left(\frac{1}{R_a}v_a + \frac{1}{R_b}v_b + \frac{1}{R_c}v_c\right) \tag{5}$$

The virtual ground prevents the input signals from interacting with each other. Consequently, the circuit's output is a weighted sum of the three inputs.

By replacing the resistors with other components, the inverting configuration can be used to perform other operations on the input signal (1,2). For example, if R_2 in Fig. 2 is replaced with a feedback capacitor C_f, as shown in Fig. 4, an integrator can be made. The input current due to the virtual ground at the op amp's inverting terminal is

$$i = \frac{v_i}{R_1} \tag{6}$$

This current then flows from the virtual ground through C_f. The voltage across the capacitor is the integral of the current through it and can be expressed as

$$\frac{v_o}{v_i} = -\frac{1}{R_1 C_f s} \tag{7}$$

where s is the Laplace variable. Such a circuit is known as an integrator and is commonly used in active filters.

For the inverting configuration, the presence of the virtual ground at the op amp's inverting input allows signals from different sources to be combined. The external circuit elements can be passive or active components. Provided the resulting circuits are stable and the op amp has sufficiently high gain, the overall transfer function is independent of the op amp.

The Noninverting Amplifier Configuration. The noninverting configuration is illustrated in Fig. 5. In this circuit the signal is applied directly to the op amp's noninverting terminal.

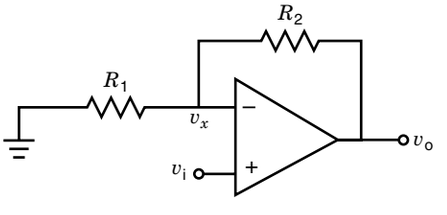

Figure 5. The noninverting configuration.

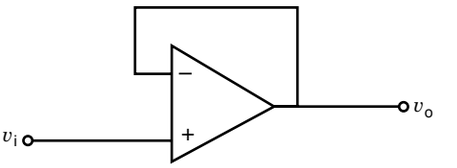

Figure 6. A voltage follower or unity-gain buffer.

Since R_2 and R_1 provide negative feedback, a virtual short exists between v_i and v_x. Therefore, the current through R_1 is v_i/R_1. Due to the op amp's high input impedance, this current also flows through R_2, resulting in an overall gain from v_i to v_o of

$$\frac{v_o}{v_i} = 1 + \frac{R_2}{R_1} \tag{8}$$

Once again the circuit's gain is set by the external components, independent of the ideal op amp.

Unlike the inverting configuration, the noninverting configuration does not draw current from the signal source. For the inverting configuration, the current drawn from v_i is determined by R_1. In the noninverting configuration, the signal is applied directly to the op amp's input terminal, which ideally has an infinite input impedance. Consequently the noninverting configuration does not load the signal source.

In cases where the signal voltage is large enough but the signal source has a high output impedance, the noninverting configuration can be used as a *unity-gain buffer*. By making R_2 0 and R_1 infinite as shown in Fig. 6, the output tracks the input due to the virtual short across the op amp's input terminals. The virtual short forces the output to track the input (i.e., $v_o = v_i$), but no current is drawn from the signal source. Instead, the op amp provides the load current. Due to its high input impedance, the op amp is particularly attractive for buffering applications.

APPLICATION ISSUES

Real op amps differ from the ideal op-amp model. These differences, commonly referred to as op-amp nonidealities, limit the range of signals for which an op-amp circuit can be used. In most applications the op amp's nonidealities do not cause significant problems. In cases where the op amp's nonidealities do cause problems, circuit design precautions often can be used to reduce the problems to acceptable levels. Alternatively, higher-performance op amps, which are typically more expensive, can be used. It is important to be aware of the op amp's dominant nonidealities, and their effect on op-amp circuits and techniques to compensate for their effects.

Finite Dc Gain

Unlike the infinite gain of an ideal op amp, the dc gain of a practical op amp is finite. Nevertheless, an op amp's dc gain, denoted by A_0, is typically quite high. A_0 ranges from 40 dB for high-speed op amps to 120 dB for precision op amps. A general-purpose op amp typically has a gain of 100 dB. The actual gain of an op amp is not a well-controlled parameter. Consequently, manufacturers typically specify both a minimum and a typical value for A_0.

The effect of an infinite A_O is to reduce the closed-loop gain of an op-amp circuit (1–3). If an op amp has a finite gain and the output voltage is v_o, there must be a nonzero voltage across the op amp's input terminals equal to v_o/A_O. Using this relationship, the op amp's finite gain reduces the closed-loop gain of the inverting configuration to

$$\frac{v_o}{v_i} = \frac{-R_2/R_1}{1 + (1 + R_2/R_1)/A_O} \tag{9}$$

while for the noninverting configuration, the closed-loop gain is reduced to

$$\frac{v_o}{v_i} = \frac{1 + R_2/R_1}{1 + (1 + R_2/R_1)/A_O} \tag{10}$$

When A_O is very large, Eqs. (9) and (10) reduce to Eq. (4) for the inverting configuration and to Eq. (8) for the noninverting configuration, respectively. When A_O becomes comparable to $1 + R_2/R_1$ a noticeable reduction in the closed-loop gain occurs. To ensure a well-controlled closed-loop gain, the minimum open-loop gain specified by the manufacturer must be significantly larger than the desired closed-loop gain. As a result, the op amp's finite dc gain limits the maximum gain that can be obtained accurately in an op-amp circuit.

Saturation

Although op amps can be used to provide large gains, in practical op amps the maximum output voltage is limited. When called upon to deliver output signals close to and beyond the op amp's supply voltage, the op amp's output signal is limited to a value determined by the op amp's supplies and becomes independent of the input signal. When the op amp's output has reached its maximum level, the op amp is said to be *saturated.*

Like any electronic amplifier, an op amp requires a power supply. Most stand-alone op amps require a positive, V^+, and a negative, V^-, power supply but no connection to ground. Typically, V^+ and V^- are of the same magnitude but of opposite polarity and range from ±5 V to ±18 V for general-purpose op amps. To meet the needs of specialized applications, special-purpose op amps such as single-supply op amps, for use with a single supply, low-voltage op amps, for supplies below ±5 V, and high-voltage op amps, for use with supplies beyond ±18 V, are commonly available.

Irrespective of the supply voltage, the op amp's maximum output voltage L^+ and minimum output voltage L^- cannot exceed the supply. For most op amps, the output saturates within 1 V to 3 V of the supply as illustrated in Fig. 7. In the case of low-voltage and single-supply op amps, the output swing often extends to the supply levels, yielding a *rail-to-rail* output swing. Output signals beyond this range are clipped, leading to distortion. To ensure that the output is not clipped at L^+ or L^-, the op-amp circuit's input signal must be kept suitably small.

Frequency Characteristic

The frequency characteristic of a compensated op amp is shown in Fig. 8 (1–3). Due to the op amp's internal capacitances, the op amp's gain decreases with frequency. For most general-purpose op amps, the manufacturer, through a technique known as compensation, controls the op amp's frequency response such that the gain rolls off at a constant −20 dB/decade from A_O to below 0 dB. The op amp's frequency response can be expressed as

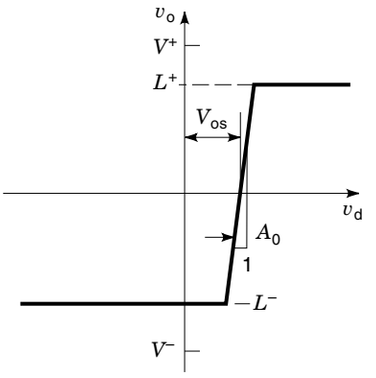

Figure 7. The op amp's dc input/output relationship.

$$A(\omega) = \frac{A_O}{1 + j\omega/\omega_b} \tag{11}$$

where $\omega_b = 2\pi f_b$ and f_b is the frequency of the op amp's dominant pole. Unfortunately, f_b is dependent on A_O. Hence, this formulation of the op amp's frequency response is rarely used.

Unity-Gain Bandwidth

A more predictable and useful point is the frequency at which the op amp's gain falls to unity. This point is called the op amp's *unity-gain bandwidth* and is denoted by f_t, as shown in Fig. 8. Typical values of f_t range from 1 MHz, for high-gain op amps, to over 100 MHz, for high-speed, low-gain op amps. Due to the op amp's one dominant pole, the op amp's bandwidth f_b can be expressed as

$$f_b = f_t/A_O \tag{12}$$

Since A_O can be fairly large, the op amp's bandwidth is typically fairly low. Based on the relationship in Eq. (12), the op amp's frequency response is commonly expressed as

$$A(\omega) = \frac{A_O}{1 + j\omega(A_O/\omega_t)} \tag{13}$$

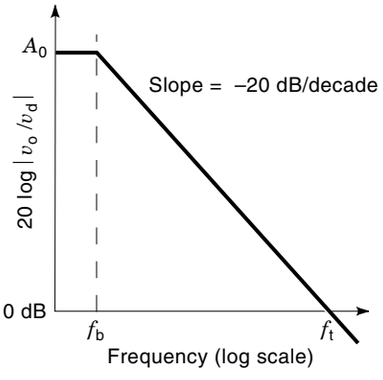

Figure 8. Frequency response of a compensated op amp.

where $\omega_t = 2\pi f_t$.

To determine the high-frequency response of an op-amp circuit such as the inverting configuration or the noninverting configuration, the op amp's high-frequency gain, as given by Eq. (13), can be approximated by

$$A(\omega) \approx \omega_t / j\omega \tag{14}$$

If Eq. (14) is used in place of A_0 in Eqs. (9) and (10),

$$\frac{v_o}{v_i}(\omega) = \frac{-R_2/R_1}{1 + \dfrac{j\omega}{\omega_t/(1+R_2/R_1)}} \tag{15}$$

is obtained for the inverting configuration and

$$\frac{v_o}{v_i}(\omega) = \frac{1+R_2/R_1}{1 + \dfrac{j\omega}{\omega_t/(1+R_2/R_1)}} \tag{16}$$

is obtained for the noninverting configuration. For both circuits, the closed-loop bandwidth is given by

$$\omega_{clb} = \frac{\omega_t}{1+R_2/R_1} \tag{17}$$

where $1 + R_2/R_1$ is commonly referred to as the *feedback factor* and is denoted by B. Based on Eqs. (15) and (16) it can be seen that the bandwidth of an op-amp circuit is the op amp's unity-gain bandwidth divided by the feedback factor. Greater feedback factors imply lower gains. Hence, the lower the desired gain, the wider the circuit's bandwidth.

Slew Rate

Due to internal circuitry limitations, the output voltage of an op amp cannot change instantaneously. The maximum rate at which the op amp's output voltage can change is called the *slew rate,* SR:

$$\text{SR} = \left.\frac{dv_o}{dt}\right|_{\max} \tag{18}$$

Slew rate is expressed using the units V/μs. The primary effect of a finite slew rate is that the output and input of an op-amp circuit are not linearly related while the op amp is slewing. Consequently, slewing causes distortion.

The maximum frequency at which an op amp can be used without slew-rate distortion depends on the size of the output signal. For a sine wave output with a peak amplitude of V_a, the output voltage will be $v_o = V_a \sin(2\pi ft)$ and its maximum rate of change is $2\pi f V_a$. To avoid slew-rate distortion, $2\pi f V_a$ must be less than SR. Slew-rate distortion can be avoided either by keeping the signal frequency small or by keeping the signal amplitude small. For a *full-power signal,* that is, a signal with a peak-to-peak amplitude of $L^+ - L^-$, the maximum frequency for which an undistorted output can be obtained is given by

$$f_{\max} = \frac{\text{SR}}{\pi(L^+ - L^-)} \tag{19}$$

This frequency is called the op amp's *full-power bandwidth.*

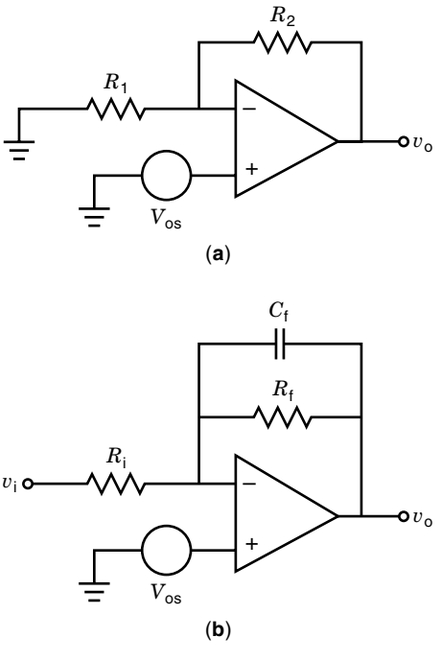

Figure 9. (a) The effects of the offset voltage on the inverting and noninverting configurations. (b) Reducing the effects of an offset voltage on the inverting integrator.

Offset Voltages. Ideally, a zero differential input voltage to an op amp will produce a zero output voltage. For a practical op amp, a 0 differential input voltage typically produces an output of either L^+ or L^-, as shown in Fig. 7. To restore the op amp's output voltage to 0, a voltage defined as the *input referred offset voltage* V_{os} must be applied between the input terminals.

V_{os} arises from mismatches in the devices used in the op amp's input stage and circuit asymmetries (4). Since V_{os} depends on physical devices, it is subject to drift due to temperature changes and as the circuit ages. Nevertheless, V_{os} is quite small. For a general-purpose op amp V_{os} is in the range of 0.1 mV to 10 mV. When a low V_{os} is required, precision op amps are available with V_{os} in the microvolt range.

To model the effects of V_{os}, a voltage source equal to V_{os} but of unknown polarity is connected to one input terminal of the ideal op amp. Then, provided the op-amp circuit is linear, superposition can be used to determine the resulting output voltage due to V_{os} and the circuit's input voltage. To analyze the effect of V_{os} on either the inverting or noninverting configurations, the circuit shown in Fig. 9(a) can be used. Note that the op amp has been replaced with an ideal op amp with V_{os} in series with its noninverting terminal and the input v_i has been set to 0. Note also that due to superposition, the effect of the op amp's V_{os} on both the inverting and noninverting configurations will be the same. The output due to V_{os} acting alone is called the *output offset* and is found to be

$$v_o = V_{os}(1 + R_2/R_1) \tag{20}$$

Clearly, if R_2/R_1 is large, a large output offset will result. If a high gain is required but dc gain is not, a capacitor can be added in series with R_1 to reduce the output offset to V_{os}.

One class of circuits that is particularly affected by the op amp's offset voltage is the inverting integrator shown in Fig. 4. Due to the presence of V_{os}, a dc current flows through R_1 and is integrated on C_f, which causes the output to saturate at either L^+ or L^-. To avoid the problem, a feedback resistor, R_f can be added as shown in Fig. 9(b). R_f limits the dc gain to a finite value and therefore limits the output offset voltage.

When very small offsets are required, a number of solutions exist: The simplest solution is to use a low-offset op amp. Alternatively, many op amps have connections for an offset nulling network. In either case, the offset will still be subject to drift due to temperature and aging. To reduce the offset problem further, techniques such as autozeroing, correlated double sampling, and chopper stabilization can be employed (5).

Input Bias Currents. To operate properly, all op amps require an input current. These input currents arise from the needs of the op amp's input devices. If bipolar junction transistors (BJTs) are used, the input bias currents are the required base currents of the input devices. If field-effect transistors (FETs) form the input stage, the FET's gate leakage currents give rise to the input bias currents. Since there is a bias current for each input, the average of the two currents, I_B, and the difference or offset between the two currents, I_{os}, are usually specified (2). As the op amp's bias currents flow through the external components, they cause input errors similar to V_{os} and hence can be combined with V_{os} using superposition.

Common-Mode Rejection. Practical op amps display both a differential gain and a common-mode gain. Since the op amp has two input terminals, two types of input signals can be defined: a differential signal v_d, which is the difference between the two signals, $v_d = v_i^+ - v_i^-$, and a common-mode signal, v_c, which is their average, $v_c = (v_i^+ + v_i^-)/2$. An ideal op amp does not respond to v_c. For practical op amps, changing v_c changes v_o, which implies a *common-mode gain* A_c,

$$A_c = v_o/v_c \tag{21}$$

Like the differential gain, the common-mode gain is a function of frequency. Typically, A_c is relatively small over a specified range, known as the op amp's *input common-mode range.* For input signals beyond the common mode range, A_c rises rapidly and the op amp no longer functions properly. In most cases an op amp's input common-mode range does not extend to either the positive or negative supply voltage. For single-supply op amps, the input common-mode range typically does extend to and often slightly beyond one supply. For very-low-voltage op amps, the input common-mode range may extend to both supply levels, yielding what is referred to as a *rail-to-rail* input range.

Within the common-mode range, A_c is usually specified in terms of the *common-mode rejection ratio,* CMRR:

$$\text{CMRR} = A/A_c \tag{22}$$

At dc the CMRR is usually very large but decreases with increasing frequency. The dc CMRR is usually expressed in decibels and ranges from 60 dB to 120 dB for most op amps.

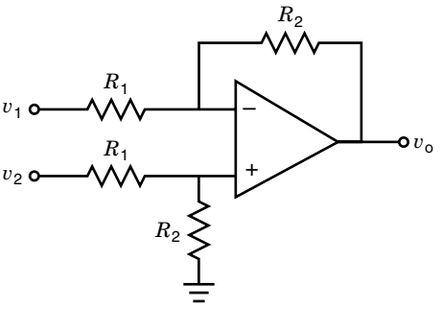

Figure 10. The differential configuration.

For the purpose of circuit analysis, an alternate interpretation of the CMRR is the ratio of the change in V_{os} due to a change in v_c.

$$\frac{1}{\text{CMRR}} = \frac{\Delta V_{os}}{v_c} \tag{23}$$

The two interpretations of CMRR are equivalent.

The common-mode gain is only a problem in op-amp circuits for which a sizable v_c is applied directly to the op amp. Consequently, with a virtual ground at the op amp's output, the inverting configuration is unaffected by the common-mode gain. For circuits such as the noninverting configuration and for the differential configuration, shown in Fig. 10, a sizable v_c is present at the op-amp inputs. Hence, these circuits are affected by the op amp's common-mode rejection properties. In particular, if the signal at the op amp's noninverting terminal exceeds the op amp's input common-mode range, the circuit ceases to amplify the input signal linearly.

Even within the specified input common-mode range, the differential configuration will not function properly if the op amp's CMRR is too low. Ideally, a differential amplifier amplifies the difference between two signals. For the differential configuration, the input and output are related by

$$v_o = \frac{R_2}{R_1}(v_2 - v_1) \tag{24}$$

The differential configuration amplifies the difference between the two input signals and rejects their common-mode component. The effect of the op amp's common-mode gain can be determined as follows: Since the CMRR and the presence of a common-mode signal v_c at the op amp's input effectively give rise to a signal dependent V_{os} [see Eq. (23)], the resulting V_{os} can be expressed as

$$V_{os} = v_c/\text{CMRR} \tag{25}$$

Then, by assuming the op amp is ideal except for the finite V_{os} given by Eq. (25), the effects of a nonzero v_c and finite CMRR can be calculated. For the differential configuration, a finite CMRR changes the output from that given by Eq. (24) to

$$v_o = \frac{R_2}{R_1}(v_2 - v_1) + \frac{R_2}{R_1}\left(\frac{v_2}{\text{CMRR}}\right) \tag{26}$$

It can be seen that the output now depends on both the difference in the applied signals and on the value of v_2. Since v_2 contains both a differential and common-mode component, the differential configuration's performance will be degraded if the op amp's CMRR is too low.

Summary. The applications of op amps are limited by their nonideal behavior. The op amp's offset voltage and CMRR limit the accuracy of op-amp circuits. The op amp's finite gain and saturation levels limit the maximum useful gain of an op-amp circuit. The op amp's frequency response and finite slew rate limit the maximum frequencies for which the op amp can be used. In most cases, special-purpose op amps or circuit techniques can be used to reduce the degradation caused by the op amp's nonidealities.

IMPLEMENTATION ISSUES

An op amp can be implemented in many ways. Typically, an op amp is a multistage design composed of a differential input stage, one or more high-gain middle stages, and, if required, a low-impedance output stage. While many different technologies can be used to implement op amps, currently they are most commonly implemented using either bipolar devices (3,6) or complementary metal oxide semiconductor (CMOS) devices (3,4,7). A simplified schematic of a typical bipolar implementation of a three-stage op amp is illustrated in Fig. 11.

The input stage is a differential pair formed by the matched devices Q_{1a} and Q_{1b}. This configuration inherently rejects common-mode signals while producing an output current proportional to the differential input voltage, $i = g_{m1}\, v_i$. The ratio of Q_{1a}'s and Q_{1b}'s output current to the input voltage is called the transconductance g_{m1}. At this point, the voltage gain is usually relatively small.

In the high-gain stages, the relatively small voltage swing at the input stage's output is amplified to yield a very high voltage gain. For example, the output current of the first stage in Fig. 11 is effectively multiplied by the current gain

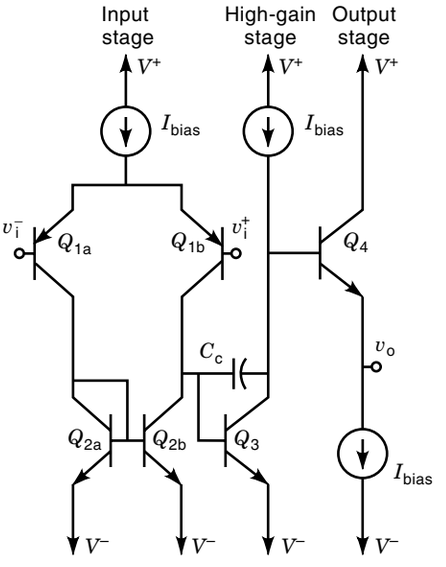

Figure 11. A simplified three-stage op amp.

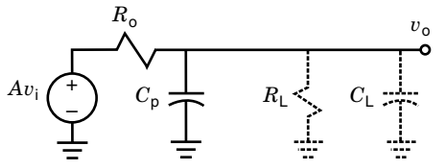

Figure 12. A Thévenin equivalent circuit for the output of an op amp's high-gain stage.

of Q_3, β_3, to yield a current of $i = \beta_3 g_{m1} v_i$. Provided the output stage adequately buffers the load, this current reacts with the output resistance of Q_3, r_{o3}, to yield a gain of

$$v_o/v_i = -\beta_3 g_{m1} r_{o3} \tag{27}$$

While this gain can be fairly high, the output impedance of the node is also very high.

To buffer this high-impedance node, a voltage follower, illustrated in Fig. 11 as an emitter follower (i.e., Q_4), is used. This last stage does not provide any voltage gain. Instead, it reduces the op amp's output resistance so that the op amp's gain is unaffected by the load.

The actual configuration and number of stages in an op amp depends on many factors: the type of load, resistive or capacitive, that is to be driven, the type of devices, bipolar or CMOS, that is to be used to implement the op amp, and the need for compensation, to ensure stability, should all be considered.

Resistive or Capacitive Loads

The type of load "seen" by the op amp, be it resistive or capacitive, determines the need for a buffering stage between the output of the op amp's high-gain stage and the load. The output of the high-gain stage can be modeled as a voltage source, AV_i, with a large output resistance R_o and a parasitic shunt capacitance C_p, as shown in Fig. 12. R_o is typically very high to yield a large voltage gain [see Eq. (27)]. Often R_o is in the megaohm range. When a resistive load R_L is connected directly to the output of the high-gain stages, the overall gain will be reduced by the voltage divider formed by R_o and R_L. For a purely capacitive load C_L, this load appears in parallel with C_p and does not affect the dc gain. Consequently, for resistive loads a buffering stage is required on the op amp's output while for capacitive loads, a buffering stage is typically not required.

Bipolar and CMOS Implementations

Currently the two most common devices for implementing op amps are bipolar devices (i.e., BJTs) and CMOS devices [i.e., metal oxide semiconductor FETs (MOSFETs)]. Both devices have advantages and disadvantages that determine how they are best used in the different stages of an op amp.

Input Differential Stage. The input stage converts the differential input voltage to a current. A number of factors are important in this stage:

- Random input offset voltages are largely determined by the matching of the input devices.

- The base or gate currents of the input devices determines the input bias currents.
- The input devices' transconductance determines the input stage's voltage-to-current gain and SR (6).
- The bias current of the differential pair typically limits the op amp's slew rate.

Generally, BJTs display better device-to-device matching then MOSFETs. Therefore, BJTs are preferred for op amps with low input referred offsets. Unfortunately, due to their base currents, BJT input devices will require much larger input bias currents than MOSFET input devices. For a large input transconductance, BJTs are preferred over MOSFETs. The BJT's high transconductance also provides a relatively high bandwidth for the input stage but, due to the BJT's high transconductance-to-bias-current ratio, the slew rate will be poor. To improve the slew rate compared to the input transconductance, either emitter degeneration with BJTs or MOSFETs with their lower transconductance-to-bias-current ratio can be used. Since any necessary gain can be achieved in the following stages, the primary difference between BJT and MOSFET inputs is the tradeoff between the input offset voltage and the input bias currents.

High-Gain Stages. In an op amp it is desirable to achieve a very high gain without introducing a large number of parasitic poles that make compensating the circuit difficult. In practical terms, the gain should be achieved with as few stages as possible and with as few high-impedance nodes as possible.

For the BJT, with its large transconductance, it is often possible to achieve the desired gain with two gain stages as illustrated in Fig. 11. This circuit can then be compensated with a single compensation capacitor C_C.

When trying to implement the same circuit using MOSFETs, two problems arise: First the gain for a common source stage is typically much lower than that of a common emitter stage. Consequently, two or more MOSFET gain stages may be required to achieve the same gain as a single BJT gain stage. Second, the compensation provided by C_C is often inadequate due to a zero introduced by the feedforward path through C_C and the low stage gain. Pole–zero cancellation can be used to compensate this circuit by placing a resistor in series with C_C (4,7). The resistor should have a value equal to $1/g_m$ of the common-source stage. While pole–zero cancellation will solve the latter problem, the former problem, that of a relatively low stage gain, remains. If multiple common-source stages are used to boost the gain, the ensuing compensation problem becomes very complex.

To achieve high-gain op amps using MOSFETs, without stability problems, cascode designs are used (3,7). To maximize the signal swing at the output, the folded cascode configuration shown in Fig. 13 is commonly used. Unlike the bipolar design, which used a differential pair followed by a common emitter stage to achieve a high gain, the folded cascode uses a differential pair followed by a common gate stage. Now the circuit only has one high-impedance node and it occurs at the output. If the gain provided by one level of cascoding is insufficient, additional levels of cascoding can be added, while still maintaining only one high-impedance node.

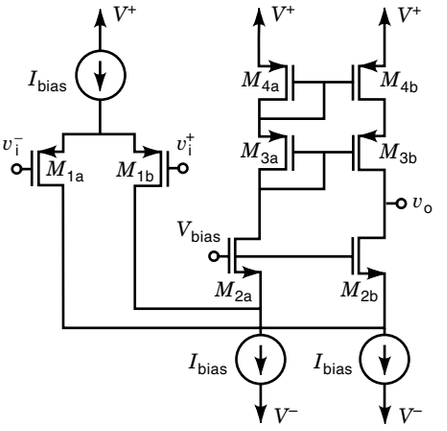

Figure 13. A folded cascode op amp.

Output Buffers. The primary concern for the output buffer is the buffer's output impedance. When the output buffer is implemented as an emitter or source follower, the output impedance is given by $1/g_m$ of the output device. Due to the BJT's relatively high transconductance-to-bias-current ratio, BJTs make a better choice for low output impedance buffers. When the op amp is only required to drive relatively small on-chip capacitances, there is no need for an output buffer stage.

In summary, BJTs are well suited for op amps with high gains, low output resistances, and low input referred offsets. Consequently bipolar op amps are typically used for circuits with resistive loads and for precision applications. MOSFETs are well suited for applications requiring very low input bias currents and for driving on-chip capacitive loads, this makes them well suited for switched-capacitor circuits.

Compensation

Op amps are typically used in circuits employing feedback. For a typical feedback circuit such as that shown in Fig. 14, the feedback signal is subtracted from the input signal before being applied to the amplifier. The subtraction operation reduces the signal seen by the amplifier. For a practical circuit, the amplifier gain A is a function of frequency and the feedback factor B may also be a function of frequency. Hence, the loop gain AB is also a function of frequency. Consequently, due to phase shifts around the loop, at certain frequencies, the feedback and input signals may be in phase. Then, the input and feedback signals add together increasing the signal "seen" by the amplifier. At this point the circuit becomes unstable. The amplifier's output grows and the circuit oscillates at the frequency at which the input and feedback signals are

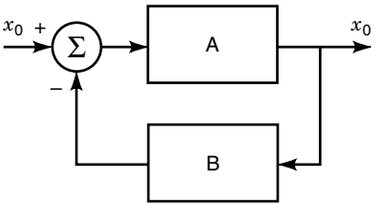

Figure 14. A generalized feedback system.

in phase. This frequency corresponds to a phase shift around the loop of ±180°. Consequently, in a feedback circuit, it is desirable to ensure that the magnitude of the phase shift around the loop is much less than 180° when the gain around the loop is greater than or equal to 1.

Phase margin is defined as the difference between the phase of the loop gain and −180° when the loop gain is equal to unity. To avoid peaking in the circuit's frequency response, it is necessary to have a phase margin of 60° or more (2). In applications where some peaking in the frequency response can be tolerated, lower phase margins may be used.

The phase margin of an op-amp circuit can be estimated from a Bode plot of the op amp's transfer function. By adding a line for $1/B$ to the plot, the difference between the A and B lines is equal to AB (i.e., $\log|AB| = \log|A| - \log|1/B|$). The point at which the two lines intersect is the loop's unity gain point. This is illustrated in the asymptotic Bode plot shown in Fig. 15. The $1/B$ line is frequency independent in this case and hence can be implemented with resistive feedback, such as was used for the inverting and noninverting configurations of Figs. 2 and 4. From this plot, the phase margin is almost 0 and hence would be inadequate for most applications.

To ensure an adequate phase margin, op amps must typically be compensated. *Compensation* involves either moving the existing poles of an op amp or adding new ones to ensure that the final circuit has the desired phase margin. Op amps come in two main types: compensated and uncompensated. A compensated op amp has been compensated by the manufacturer to be stable for all values of resistive feedback up to $B = 1$ (i.e., a unity-gain buffer). An uncompensated op amp will not be stable for all values of resistive feedback but typically has provisions for the user to perform the necessary compensation for the desired gain. While easier to use, compensated op amps will have an unnecessarily low bandwidth for gains greater than 1. To achieve a better bandwidth for higher-gain applications, uncompensated op amps can be used.

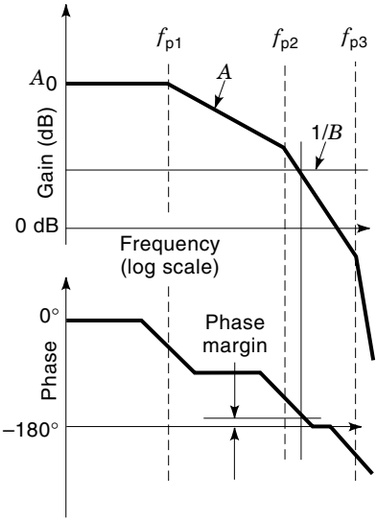

Figure 15. A Bode plot for analyzing the phase margin of an op-amp circuit.

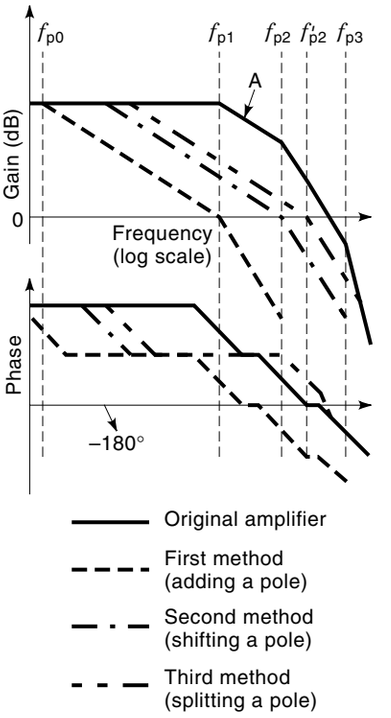

Figure 16. Compensating an op-amp circuit for a phase margin of 45° at unity gain.

Compensation can be performed in a number of ways (1–3,7,8). The simplest approach is to add a new pole at f_{p0} to ensure that the loop gain falls to unity at the desired phase margin, as illustrated in Fig. 16. For this example, the desired phase margin is 45°. This technique will reduce the circuit's closed-loop bandwidth to approximately the op amp's first, or dominant, pole f_{p1}, which can be as low as a few hertz. A better approach is to identify the op amp's dominant pole. Then increase the capacitance at that node until f_{p1} is reduced far enough to reduce the closed-loop gain to unity at the desired phase margin (2). As illustrated in Fig. 16 this approach yields a closed-loop bandwidth comparable to the op amp's second pole f_{p2}, resulting in a significant increase in bandwidth.

In the common three-stage bipolar op amp of Fig. 11, the dominant pole is typically at the base of Q_3. While a large capacitor can be connected between the base of Q_3 and V^-, a better approach is to connect the compensation capacitor (C_C) between the base and collector of Q_3 as shown. This exploits the Miller multiplier effect, which results in increasing the effective capacitance seen at Q_3's base. In addition to lowering f_{p1}, this technique, called *Miller compensation,* has the effect of moving the pole at Q_3's collector higher in frequency due to *pole splitting* (6). Since the pole at Q_3's collector is often f_{p2}, Miller compensation has the effect of splitting f_{p1} and f_{p2}. Pole splitting in this circuit results in a larger compensated bandwidth than would be achieved by moving f_{p1} alone, as illustrated in Fig. 16.

While there are many other techniques for compensating op-amp circuits (1,8), one that is particularly useful is that used for the folded cascode CMOS op amp in Fig. 13. This op

amp has been designed for driving capacitive loads. The circuit's dominant pole is that formed by the cascode's output resistance and the load capacitance. To compensate this circuit, the load capacitance should be increased and no additional circuitry is required. This last example illustrates one of the advantages that can be achieved by using an op amp specifically designed for the application at hand.

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