PHASE-LOCKED LOOPS

Although the first description of the *phase-locked loop* (PLL) was published by Appleton (1) in 1923, the PLL did not attract widespread attention till much later. Today PLLs of various types are used extensively in electrical engineering, from telecommunication systems to measurement equipment.

Depending on the loop components, especially on the operation of the phase detector, analog, digital, sampling, and hybrid PLLs are distinguished. The behavior of these circuits is described by differential, difference, and mixed integro-difference equations.

Even though applications of PLLs require a variety of circuit configurations, and the mathematical models mentioned above require different kinds of mathematical treatment, their behavior can be approximated and studied by means of a simple feedback structure. Unfortunately, the behavior of this structure is complicated to analyze, because it is nonlinear, may contain edge-triggered digital circuits, and is driven by random noise. In many cases, analytical results are not available in closed form; they are often buried in complicated mathematics that cannot be assimilated easily by the circuit designer. On the other hand, the design of PLLs for many applications can be performed successfully, based on a simple linearized model and by means of a few "rules of thumb." In this article one shall differentiate clearly between the essential elements and secondary effects of loop behavior, the key assumptions and approximations involved in the analysis will be highlighted, and the conditions under which the approximations are valid will be collected. The main goals are to provide a survey of PLL theory and applications and to summarize the most important design rules and equations.

This article is organized as follows. The next section is devoted to the theory of the *analog phase-locked loop* (APLL). First the baseband model for the APLL is developed, then the linear theory of the APLL (tracking, modulation, and noise) is discussed. Finally, the most important nonlinear effects (acquisition, cycle slips, hang-up) are considered. The subsequent section discusses the most common applications of PLLs.

The key element of the loop that determines the practical performance of a PLL is the phase detector. To obtain the best circuit performance, different phase detectors have been developed for various applications. The operation of the most widely used phase detectors is then discussed.

The *Digital Phase-Locked Loop* (DPLL) has become popular in many applications recently. A section is devoted to DPLL circuits.

In other applications, analog, discrete-time, and edge-triggered digital circuits have to be used, or their mixed application assures the best loop performance. These loops are called *hybrid phase-locked loops* (HPLL). The most commonly used HPLLs are the *sampling phase-locked loop* (SPLL) and the *charge-pump phase-locked loop.* The operation of SPLLs and charge-pump PLLs will be discussed.

ANALOG PHASE-LOCKED LOOP

In an APLL, all loop components are analog circuits, that is, their operation can be modeled by ordinary differential equations. For the sake of simplicity, an analog multiplier shall be used as a phase detector in this section. This circuit is referred to as a *sinusoidal* APLL.

The APLL was the first, and is the most widely studied version of the PLL. Many excellent books (2–11), two IEEE special issues (12,13) and a tutorial (14) have been devoted to the theory and applications of the APLL.

In many applications, the block diagram of the APLL has to be completed with extra loop components such as a frequency divider, mixer, and so on. That is why the results developed for the APLL cannot be used directly in many cases. However,

- the theory of the APLL is very well developed and is easy to understand;
- equations describing the loop behavior in different applications can be developed in closed form;
- having understood the operation of the APLL, it is easy to study more complex PLL configurations; and
- the APLL equations give a simple but useful approximation for many circuit design problems.

This article presents a *concise* treatment of the sinusoidal APLL. First, the baseband model for the APLL is developed. Then the so-called linear APLL theory is discussed. In the majority of applications, the APLL operates in its linear region. The linear theory can be applied only if the *phase-locked* condition has been achieved and is maintained. Under phase-locked condition the average input and voltage-controlled oscillator (VCO) frequencies are exactly equal and the VCO phase tracks the input phase. The phase-locked condition is achieved as a result of a highly nonlinear, so-called acquisition, process. In the last part of this section, the most important aspects of nonlinear APLL theory are discussed.

Basic Loop Configuration

A PLL is a feedback system that continuously tries to track the phase of an input signal. It contains a *phase detector* (PD), a time-invariant linear *loop filter,* and a *voltage-controlled oscillator* (VCO); the oscillator to be synchronized. As shown in Fig. 1, the phase detector compares the phase of the input signal against the phase of the VCO output and produces an error signal. This error signal is then filtered, in order to remove noise and other unwanted components of the input spectrum, and the filter output controls the instantaneous VCO frequency. By proper design of the PD, VCO, and loop filter, the same APLL configuration can be used for tracking and carrier recovery, modulation and demodulation, and so forth.

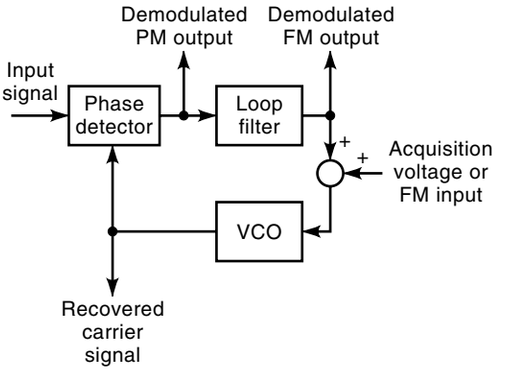

Figure 1. APLL block diagram showing inputs and outputs for various telecommunication applications.

A nonzero output voltage must be provided by the PD, in order to control the VCO frequency if the input frequency differs from the VCO center frequency. Consequently, the PLL tracks the phase of input signal with some phase error. However, this phase error can be kept very small in a well-designed PLL.

Acquisition and Tracking

In every application, the PLL tracks the phase of the incoming signal. However, before a PLL can track, it must first reach the phase-locked condition.

In general, the VCO center frequency ω_0 differs from the frequency ω_i of the incoming signal. Therefore, first the VCO frequency has to be tuned to the incoming frequency by the loop. This process is called *frequency pull-in.* Then the VCO phase has to be adjusted according to the input phase. This process is known as *phase lock-in.*

In the following, three important loop characteristics are defined.

Pull-in Range. $\Delta\omega_P = |\omega_i - \omega_0|$ is the maximum initial frequency difference between the input and VCO center frequency both in positive and negative directions, for which the PLL eventually achieves the phase-locked condition. The pull-in range is related to the dynamics of the APLL.

Lock-in Range. $\Delta\omega_L = |\omega_i - \omega_0|$ is the frequency range over which the PLL achieves the phase-locked condition without cycle slips. Cycle slips will be defined later.

Hold-in Range. Suppose the phase-locked condition has been achieved in the PLL. Now vary the input frequency ω_i slowly and the VCO frequency will follow it. The hold-in range $\Delta\omega_H = |\omega_i - \omega_0|$ is determined by the lower and upper values of ω_i, for which the phase-locked condition is lost. The hold-in range represents the maximum static tracking range and is determined by the saturation characteristics of the nonlinear loop elements in the PLL.

Loop Equation and Nonlinear Baseband Model

The block diagram of the APLL to be studied is shown in Fig. 2, where $F(p)$ denotes the transfer function of the loop filter. In the equations developed below, the time variable t is suppressed for conciseness where it does not cause misunderstanding. In order to write the differential equations in compact form, the operation of differentiation d/dt in the time-domain is denoted by multiplication by the *Heaviside operator* p. Recall that if the transfer function $F(s)$ of a linear network is given in the complex frequency domain s then $F(p) = F(s)|_{s=p}$. For more details on the Heaviside operator see page 73 in (6).

It shall be assumed during the PLL analysis that the loop components are linear; the only source of nonlinearity is the phase detector. The instantaneous VCO frequency can be varied about its center value ω_0 by the VCO control voltage.

Almost all signals and processes used in electrical engineering can be considered narrowband (15). Let the incoming signal

$$s(t, \Phi) = \sqrt{2}A \sin \Phi \tag{1}$$

be a narrowband signal, where $A(t)$ describes the *amplitude modulation* produced at the transmitter on purpose and/or caused by the time-varying channel through which the signal is transmitted. Let the phase of the incoming signal be expressed with respect to the VCO center frequency as

$$\Phi = \omega_0 t + \theta_i \tag{2}$$

where $\theta_i(t)$ is the input *phase modulation* produced at the transmitter and/or caused by the channel.

As shown in Fig. 2, the incoming signal $s(t, \Phi)$ is corrupted by additive input noise $n_i(t)$. In almost all applications, the additive input noise is a narrowband process centered about ω_0. By means of the analytic signal approach (15), narrowband processes or signals can be expressed as a product of a slowly varying complex envelope and a sinusoidal carrier. For example, an arbitrary narrowband signal $g(t)$ centered about ω_0 can be expressed in terms of a complex envelope $\tilde{g}(t)$ as

$$g(t) = Re\{\tilde{g}(t) \exp(j\omega_0 t)\} \tag{3}$$

Since the carrier frequency component has been removed, the complex envelope is a slowly varying function

$$\tilde{g}(t) = g_I(t) + jg_Q(t) \tag{4}$$

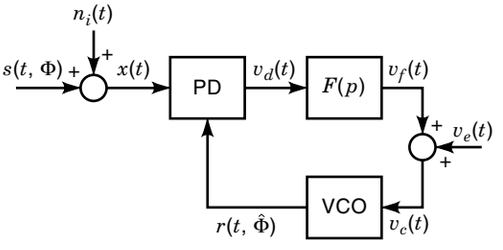

Figure 2. APLL block diagram indicating the additive input noise that corrupts the input signal.

where $g_I(t)$ and $g_Q(t)$ are the low-frequency *in-phase* and *quadrature components* of the narrowband signal $g(t)$.

Let $n_i(t)$ be modeled by a narrowband Gaussian random process of zero mean and symmetrical power spectral density. Then the sample function of the narrowband noise can be expressed from Eqs. (3) and (4) in *canonical form* (6,15) as

$$n_i = \sqrt{2}[n_I \cos(\omega_0 t) - n_Q \sin(\omega_0 t)] \tag{5}$$

The in-phase and quadrature components are

$$n_I = \frac{1}{\sqrt{2}}[n_i \cos(\omega_0 t) + \hat{n}_i \sin(\omega_0 t)] \tag{6}$$

and

$$n_Q = \frac{1}{\sqrt{2}}[\hat{n}_i \cos(\omega_0 t) - n_i \sin(\omega_0 t)] \tag{7}$$

where $\hat{n}_i(t)$ is the Hilbert transform of $n_i(t)$ (15).

The VCO output is also a narrowband signal

$$r(t, \hat{\Phi}) = \sqrt{2}V_o \cos \hat{\Phi} \tag{8}$$

where $\hat{\Phi}(t)$ is the loop estimate of $\Phi(t)$ that can be expressed, with respect to the VCO center frequency as

$$\hat{\Phi} = \omega_0 t + \theta_o \tag{9}$$

In Eq. (8) and Eq. (9) V_o and $\theta_o(t)$ denote the rms amplitude and phase of the VCO output.

The PD multiplies the input signal $x(t) = s(t, \Phi) + n_i(t)$ and VCO output $r(t, \hat{\Phi})$ and produces both difference- and sum-frequency terms. The PD always contains a low-pass filter that eliminates the sum-frequency component. By means of simple trigonometric identities is obtained for the PD output

$$\begin{aligned} v_d &= AV_o \sin\theta_e + V_o(n_I \cos\theta_o + n_Q \sin\theta_o) \\ &= K_d[A \sin\theta_e + N(t, \theta_o)] \end{aligned} \tag{10}$$

where the phase error is defined by

$$\theta_e(t) = \Phi(t) - \hat{\Phi}(t) = \theta_i(t) - \theta_o(t) \tag{11}$$

and $K_d = V_o$, a dimensionless quantity, is the gain of the PD. The *equivalent noise process* is defined by

$$N(t, \theta_o) = n_I \cos\theta_o + n_Q \sin\theta_o \tag{12}$$

The statistical properties of $N(t, \theta_o)$ are given in the following section.

It follows from Eq. (10) and Eq. (12) that

- even in the noise-free case, the PD output depends not only on the phase error $\theta_e(t)$ but also on the amplitude $A(t)$ of the incoming signal; and
- the equivalent noise process $N(t, \theta_o)$ is independent of $\theta_e(t)$; it appears as an additive term in the PD output.

The instantaneous VCO frequency $\dot{\theta}_o(t) = d\theta_o(t)/dt$ referenced to ω_0 is related to its input through

$$\dot{\theta}_o = K_v v_c + \dot{\Psi}_2 = K_v(v_f + v_e) + \dot{\Psi}_2 \tag{13}$$

where $v_c(t) = v_f(t) + v_e(t)$ denotes the VCO control voltage, $v_f(t) = F(p)v_d(t)$ is the output voltage of the loop filter, $v_e(t)$ denotes the external control voltage, K_v is the VCO gain in rad/V$_s$, and $\Psi_2(t)$ denotes the VCO jitter, that is, the phase noise.

Taking into account the transfer function of the loop filter, from Eq. (10) and Eq. (13),

$$\theta_o = \frac{KF(p)}{p}[A\sin\theta_e + N(t,\theta_o)] + \frac{K_v}{p}v_e + \Psi_2 \tag{14}$$

where $K = K_dK_v$ defines the *loop gain* in rad/V$_s$. Substituting Eq. (14) into Eq. (11), the following nonlinear stochastic integro-differential equation is obtained

$$\theta_e = \theta_i - \frac{KF(p)}{p}[A\sin\theta_e + N(t,\theta_o)] - \frac{K_v}{p}v_e - \Psi_2 \tag{15}$$

which describes the operation of APLL. In general, the input phase modulation $\theta_i(t)$ consists of three terms

$$\theta_i = d + M + \Psi_1 \tag{16}$$

where $d(t)$ describes the Doppler effect appearing in the channel, $M(t)$ is the digital or analog phase/frequency modulation, and $\Psi_1(t)$ denotes the jitter, that is, phase noise of the transmitter oscillator.

The loop equation given by Eq. (15) has two important advantages. Due to the introduction of a phase error, the high-frequency terms have been dropped and all signals involved in the loop equations have become low-frequency signals, that is, slowly varying functions. This means that, for example, in a computer simulation a low sampling frequency can be used, that is, a short simulation time is required. A further advantage of the phase error description is that it simplifies the problem to be studied. In many cases, such as the acquisition problem, Eq. (15) becomes an autonomous differential equation that is relatively easy to study.

Note that, in an implemented APLL, the phase error does not exist as an explicit variable; it has been introduced only to derive a simple mathematical model for the APLL. However, if $\theta_e(t)$ is known, then all signals appearing in an implemented APLL can be expressed easily by the equations developed above.

The baseband model of the APLL can be developed from Eq. (15) as shown in Fig. 3. The sinusoidal nonlinearity in Eq. (15) is due to the particular type of PD and the sinusoidal VCO and input waveforms. However, other kinds of PD and signals can be also applied. Fortunately, the unified baseband model shown in Fig. 3 remains valid for each loop configuration if the loop nonlinearity $g(\cdot)$ is selected according to the actual PD characteristics and $n_g(t)$ describes the equivalent noise process for the case to be studied. If an analog multiplier is used as the PD and the signals are sinusoidal, then $g(\cdot) = \sin(\cdot)$ and $n_g(t) = N(t, \theta_o)$. Lindsey and Chie (11) have collected $g(\cdot)$ and $n_g(t)$ for many other loop configurations.

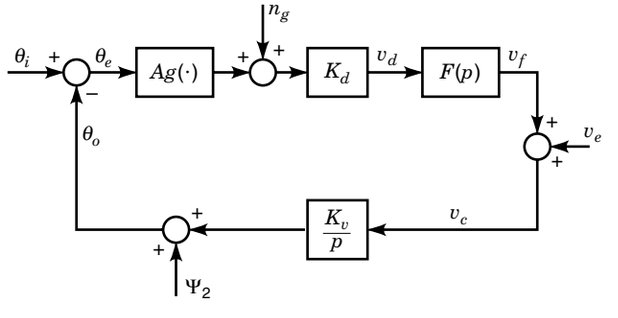

Figure 3. Unified baseband model of APLL.

Note that the input and output of the baseband model are not measurable signals but are the input and output phase modulations, respectively. If the real input and output signals have to be determined, then $s(t, \Phi)$ and $r(t, \hat{\Phi})$ can be expressed using Eqs. (1) and (8).

Statistical Properties of Equivalent Noise

In order to use the baseband model in calculations, one needs to know the statistical properties of the equivalent noise process $N(t, \theta_o)$ that depends on both the additive input noise $n_i(t)$ and the output phase $\theta_o(t)$. This section summarizes the properties of the in-phase and quadrature components of $n_i(t)$ and gives the statistical properties of $N(t, \theta_o)$.

Recall that the additive input noise is modeled by a narrowband Gaussian random process with zero mean. It can be expressed either in canonical form or as a sinusoidal signal

$$n_i = \sqrt{2}[n_I\cos(\omega_0 t) - n_Q\sin(\omega_0 t)] = \sqrt{2}N_n(t)\cos(\omega_0 t + \theta_n) \tag{17}$$

where the envelope $N_n(t)$ and phase $\theta_n(t)$ processes are defined by

$$N_n(t) = \sqrt{n_I^2(t) + n_Q^2(t)} \qquad \text{and} \qquad \theta_n(t) = \tan^{-1}\left[\frac{n_Q(t)}{n_I(t)}\right] \tag{18}$$

Note that the envelope $N_n(t)$ differs from the complex envelope defined by Eq. (3). If the power spectral density of $n_i(t)$ is symmetrical about ω_0, then a very simple relationship exists between the autocorrelation functions of $n_i(t)$ and $N_n(t)$

$$R_n(\tau) = 2r(\tau)\cos(\omega_0\tau) \tag{19}$$

where $R_n(\tau)$ and $r(\tau)$ denote the autocorrelation functions of $n_i(t)$ and $N_n(t)$, respectively.

If $n_i(t)$ has a symmetrical power spectral density about ω_0 then the most important properties of the in-phase $n_I(t)$ and quadrature $n_Q(t)$ components of $n_i(t)$ are as follows (10,15):

1. If $n_i(t)$ is a Gaussian process, then both $n_I(t)$ and $n_Q(t)$ are also Gaussian.
2. If $n_i(t)$ has zero mean, then both $n_I(t)$ and $n_Q(t)$ have zero mean values. Note that $n_i(t)$ is a bandpass signal, that is, it always has zero mean.
3. The in-phase and quadrature components have the same variance as the narrowband noise $n_i(t)$.
4. The correlation functions of $n_I(t)$ and $n_Q(t)$ can be expressed (6) as

$$\begin{aligned}\overline{n_I(t)n_I(t+\tau)} &= \overline{n_Q(t)n_Q(t+\tau)} = r(\tau)\\ \overline{n_I(t)n_Q(t+\tau)} &= -\overline{n_Q(t)n_I(t+\tau)} = 0\end{aligned} \tag{20}$$

where overbar symbolizes the time-averaging operation. The first equation shows that the autocorrelation func-

tions of $N_n(t)$, $n_I(t)$ and $n_Q(t)$ are equal to each other, while the second one means that $n_I(t)$ and $n_Q(t)$ are independent.

5. Both the in-phase and quadrature noise components have the same power spectral density that is related to the power spectral density $S_N(f)$ of $n_i(t)$ as

$$S_I(f) = S_Q(f) = \begin{cases} S_N(f - f_0) + S_N(f + f_0), & -B \le f \le B \\ 0, & \text{elsewhere} \end{cases} \tag{21}$$

where $S_N(f)$ occupies the frequency band $f_0 - B \le |f| \le f_0 + B$ and $f_0 > B$.

To complete the APLL baseband model, the statistical properties of $N(t, \theta_o)$ have to be determined. The problem is that the equivalent noise depends not only on $n_i(t)$, but also on $\theta_o(t)$. Due to the closed loop, the noise modulates the VCO and $\theta_o(t)$ also becomes a random process. Because the PD is nonlinear, the fluctuations in $\theta_o(t)$ intermodulate with the incoming signal and additive input noise $n_i(t)$.

The nonlinear operation of the PD makes exact analysis impossible, so some kind of approximation must be used. Viterbi (3) introduced two assumptions, in order to get a simple but useful result:

1. The additive bandpass noise $n_i(t)$ has a symmetrical power spectral density; and
2. The bandwidth of $n_i(t)$ is much wider than the bandwidth of $\theta_o(t)$.

The bandwidth of $\theta_o(t)$ is determined by the noise bandwidth of the loop, which will be defined later. In this case, the correlation time (6) of the additive input noise is much less than that of the output phase. Consequently, $\theta_o(t)$ can be thought of as a slowly varying function compared to $n_i(t)$ and the two processes are approximately independent (3).

Under these assumptions the equivalent noise process can be approximated by white noise. The process $N(t, \theta_o)$ shall be treated as though it were white so that $\theta_o(t)$ embedded in $N(t, \theta_o)$ does not enter into the APLL analysis, either linear or nonlinear. Thus, if the additive input noise $n_i(t)$ is white with spectral density $N_0/2$, then the power spectral density of the equivalent noise $n_g(t)$ indicated in Fig. 3 is uniform with value $N_0/2$.

Fortunately, the assumptions listed above are valid for almost all practical applications of the APLL and the design of different circuit configurations operating in either the linear or nonlinear region can be performed based on a simple baseband model.

Linear Operation of the APLL

Linear APLL theory is used extensively in designing APLLs for different applications from telecommunication to measurement engineering. Furthermore, many system parameters used in circuit development and characterization are introduced and defined in the linear theory.

The linear operation of APLL assumes that

- the phase-locked condition has been achieved and is maintained, and
- the phase error remains in the neighborhood of its quiescent value, that is, one may write $g(\theta_e) \approx g(\theta_{ss}) + dg(\theta_e)/d\theta_e|_{\theta_{ss}} \Delta\theta_e$, where θ_{ss} is the quiescent value of $\theta_e(t)$ and $\Delta\theta_e(t)$ denotes its perturbation.

In this section the linear baseband model for the APLL will be developed, and then the transfer functions for different APLL applications will be determined. After evaluating the stability properties, the tracking (transient and modulation) behavior and the noise performance of the APLL are studied, based on the linear baseband model.

Linear Baseband Model. Recall that the behavior of the APLL can be described by the following nonlinear stochastic differential equation:

$$\theta_e = \theta_i - \frac{KF(p)}{p}[Ag(\theta_e) + n_g] - \frac{K_v}{p}v_e - \Psi_2 \tag{22}$$

where, for simplicity of notation, the dependence on t in all variables has been omitted, the function $g(\cdot)$ describes the nonlinearities of the loop, and $n_g(t)$ denotes the equivalent noise process that depends on the additive input noise and the characteristic of phase detector. In this section, it shall be assumed that the APLL operates under phase-locked condition.

First the quiescent value of the phase error must be determined. Let $n_g(t) = \Psi_2(t) = 0$ and let the input phase modulation be

$$\theta_i = (\omega_i - \omega_0)t + \theta_{i0} = \Delta\omega_i t + \theta_{i0}$$

where $\Delta\omega_i$ is the initial frequency detuning and θ_{i0} denotes the phase of the incoming signal. Taking into account that under steady-state conditions all signals are constant and that the Heaviside operator p means d/dt in the time-domain, from Eq. (22) the quiescent value θ_{ss} of $\theta_e(t)$ can be obtained as

$$\theta_{ss} = g^{-1}\left(\frac{\Delta\omega_i - K_v v_{e0}}{KF(0)A}\right) \tag{23}$$

where v_{e0} denotes the external dc control voltage of $F(0)$ is the dc gain of the loop filter.

If the phase error remains in the neighborhood of θ_{ss} then $\Delta g \approx dg(\theta_e)/d\theta_e|_{\theta_{ss}} \Delta\theta_e$, where $\Delta\theta_e = \theta_e - \theta_{ss}$. Furthermore, let $K_g = dg(\theta_e)/d\theta_e|_{\theta_{ss}}$ be lumped with K_d. Then the linear loop equation for the phase error takes the form

$$\theta_e = \theta_i - \frac{KF(p)}{p}\left(A\theta_e + \frac{n_g}{K_g}\right) - \frac{K_v}{p}v_e - \Psi_2 \tag{24}$$

where, in order to have a compact notation, $\theta_e(t)$ is not distinguished from its perturbation $\Delta\theta_e(t)$, and the new value of loop gain is $K = K_g K_d K_v$. Note that K_g is measured in rad^{-1} and the new value of loop gain K is given in $(v_s)^{-1}$. The output phase can be expressed as

$$\theta_o = \frac{KF(p)}{p}\left(A\theta_e + \frac{n_g}{K_g}\right) + \frac{K_v}{p}v_e + \Psi_2 \tag{25}$$

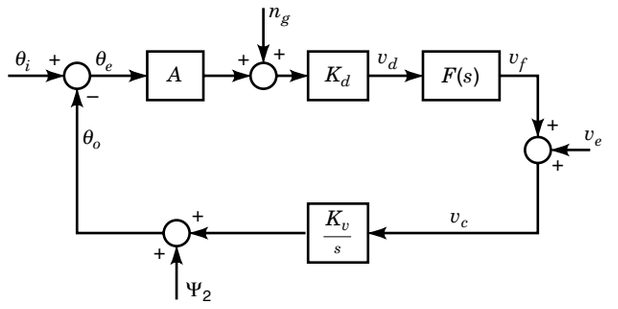

Figure 4. Linear baseband model of APLL.

The linear baseband model can be constructed from Eqs. (24) and (25). The linear model shown in Fig. 4 will be needed in the following section to develop the loop transfer functions and to determine the most important properties of the APLL. Although every real APLL is nonlinear, in many applications after the acquisition process the APLL must operate in its linear region in order to avoid distortion.

Transfer Functions. In order to describe the behavior of APLL by means of transfer functions, Eq. (24) has to be rearranged as

$$\tilde{\theta}_e(s) = [1 - H(s)]\left[\tilde{\theta}_i(s) - \frac{K_v}{s}\tilde{v}_e(s) - \tilde{\Psi}_2(s)\right] - H(s)\frac{\tilde{n}_g(s)}{AK_g} \quad (26)$$

and substituting Eq. (11) into Eq. (25) the output phase has to be expressed as

$$\tilde{\theta}_o(s) = H(s)\left[\tilde{\theta}_i(s) + \frac{\tilde{n}_g(s)}{AK_g}\right] - [1 - H(s)]\left[\frac{K_v}{s}\tilde{v}_e(s) - \tilde{\Psi}_2(s)\right] \quad (27)$$

where is introduced the Laplace transform variable s. Hereafter a tilde denotes the Laplace transform of the signal over which it appears.

Note that only two transfer functions are required to characterize the APLL completely, namely, the *closed-loop transfer function*

$$H(s) = \frac{AKF(s)}{s + AKF(s)} \quad (28)$$

and the *error function*

$$1 - H(s) = \frac{s}{s + AKF(s)} \quad (29)$$

have to be determined. The closed-loop transfer and error functions have low-pass and high-pass characteristics, respectively. The parameters of $H(s)$ and $[1 - H(s)]$ are determined by the loop-filter $F(s)$, the loop gain K, and the rms amplitude A of the incoming signal. If $A(t)$ varies due to either amplitude modulation or a time-varying channel, then all parameters of $H(s)$ and $[1 - H(s)]$, for example, the cut-off frequency, also vary with time. In the majority of applications, this time dependence is not allowed, that is, an AGC circuit preceding the APLL must be used in order to fix the amplitude of the input signal.

APLLs are classified according to the type and order of the loop. Let

$$G(s) = \frac{AKF(s)}{s} \quad (30)$$

denote the open-loop transfer function. The loop type is given by the number of poles at the origin, that is, the number of perfect integrators in $G(s)$, while the loop order is equal to the number of poles in $G(s)$.

In the following are considered, as examples, a few important loop filter configurations, and the closed-loop APLL characteristics are determined. The closed-loop parameters for other loop filter configuration are given in Table 1.

Case I: $F(s) = 1$; First-Order, Type-One Loop. Substituting $F(s) = 1$ into Eqs. (28) and (29), the closed-loop transfer function

$$H(s) = \frac{1}{1 + \dfrac{s}{AK}} \quad (31)$$

and error function

$$1 - H(s) = \frac{\dfrac{s}{AK}}{1 + \dfrac{s}{AK}} \quad (32)$$

can be expressed. The transfer function $H(s)$ has a well-defined 3-dB bandwidth, which we call the *closed-loop bandwidth* and label ω_{3dB}. Note that the closed-loop bandwidth

- is equal to AK; and
- varies with the amplitude A of the input signal.

The disadvantage of a first-order APLL is that only one free design parameter is available. The loop gain K determines all parameters of the APLL. For example, the quiescent phase error θ_{ss} given by Eq. (23) and the closed-loop bandwidth appearing in Eq. (31) cannot be selected independently of each other; a small θ_{ss} results in a large closed-loop bandwidth. It is not possible to implement simultaneously a small tracking error and a small closed-loop bandwidth. This problem can be overcome by introducing more free parameters, that is, a first-order loop filter.

Case II: Second-Order, Type-Two Loop. The circuit diagram of the most frequently used active loop filter is shown in Fig. 5. Due to the finite DC gain, the transfer function of the loop filter

$$F(s) = \frac{1 + s\tau_2}{s\tau_1} \quad (33)$$

cannot be implemented, but is approximated closely by an operational amplifier. The time constants in Eq. (33) are: $\tau_1 = R_1C$ and $\tau_2 = (R_1 + R_2)C$. A loop implemented with an active loop filter is often referred to as an *ideal second-order* APLL.

After substituting Eq. (33) into Eq. (28) and (29) the closed-loop transfer function

$$H(s) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad (34)$$

Table 1. Parameters of the Linearized APLL

Loop Order	Loop Type	Loop Filter $F(s)$	Key Parameters	$H(s)$
First	One	1	$B_L = AK/4$	$\dfrac{4B_L}{s+4B_L}$
Second	One	Passive lag filter	$\omega_n^2 = AK/\tau_1$	
		$\dfrac{1}{1+s\tau_1}$	$2\zeta\omega_n = 1/\tau_1$	$\dfrac{\omega_n^2}{s^2+2\zeta\omega_n s+\omega_n^2}$
			$B_L = AK/4$	
		Passive lead-lag filter	$\omega_n^2 = AK/\tau_1$	
		$\dfrac{1+s\tau_2}{1+s\tau_1}$	$2\zeta\omega_n = \dfrac{1+AK\tau_2}{\tau_1}$	$\dfrac{\left(2\zeta\omega_n - \dfrac{\omega_n^2}{AK}\right)s+\omega_n^2}{s^2+2\zeta\omega_n s+\omega_n^2}$
			$2B_L = \omega_n\left[\zeta\left(1-\dfrac{\omega_n}{2AK\zeta}\right)^2 + \dfrac{1}{4\zeta}\right]$	
	Two	Active filter	$\omega_n^2 = AK/\tau_1$	
		$\dfrac{1+s\tau_2}{s\tau_1}$	$2\zeta\omega_n = \dfrac{AK\tau_2}{\tau_1}$	$\dfrac{2\zeta\omega_n s+\omega_n^2}{s^2+2\zeta\omega_n s+\omega_n^2}$
			$2B_L = \omega_n\left(\zeta+\dfrac{1}{4\zeta}\right)$	

is obtained and then the error function,

$$1 - H(s) = \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{35}$$

where the *natural frequency* ω_n and the *damping factor* ζ of loop are given by

$$\omega_n = \sqrt{\frac{AK}{\tau_1}} \quad \text{and} \quad \zeta = \frac{\tau_2\omega_n}{2} \tag{36}$$

The closed-loop bandwidth can be expressed as

$$\omega_{3dB} = \omega_n\left[2\zeta^2 + 1 + \sqrt{(2\zeta^2+1)^2+1}\right]^{1/2} \tag{37}$$

The magnitudes of the APLL frequency response and error response are plotted in Figs. 6 and 7, respectively, for several values of damping factor. Note that $H(s)$ and $[1 - H(s)]$ really have low-pass and high-pass characteristics, respectively as claimed.

The quiescent value of the phase error, the loop's transient behavior, and the closed-loop bandwidth are the three basic APLL parameters that have to be selected in design of every APLL. The main advantage of the ideal second-order APLL is that these parameters can be selected independently of each other:

- The high dc gain of the operational amplifier ensures that $\theta_{ss} \approx 0$; furthermore θ_{ss} does not depend on A.
- Equation (37) shows that ω_n can be calculated from the required closed-loop bandwidth and damping factor. Then AK/τ_1 is given by Eq. (36).
- The transient behavior of the loop is controlled by the damping factor. From Eq. (36), τ_2 can be calculated.

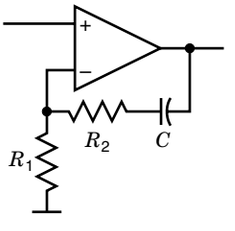

Figure 5. Circuit diagram of the most widely used active loop filter.

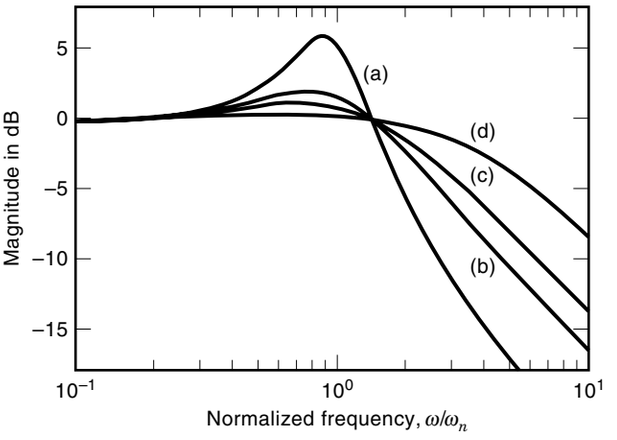

Figure 6. Frequency response of APLL implemented with an active loop filter for several values of damping factor: (a) $\zeta = 0.3$; (b) $\zeta = 0.707$; (c) $\zeta = 1$; and (d) $\zeta = 2$.

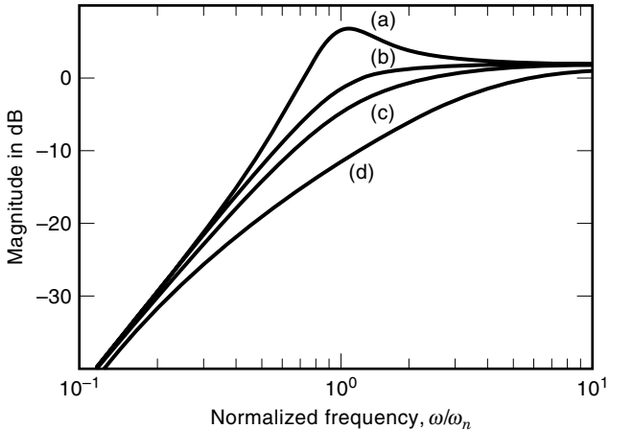

Figure 7. Error response of an ideal second-order APLL for various values of damping factor: (a) $\zeta = 0.3$; (b) $\zeta = 0.707$; (c) $\zeta = 1$; and (d) $\zeta = 2$.

A further advantage of second-order loops is that they are unconditionally stable for all values of loop gain. However, note that all closed-loop parameters depend on the rms amplitude of the incoming signal.

Case III: Second-Order, Type-One Loop. The passive lead-lag filter offers a very simple APLL configuration. The circuit diagram of the loop filter is shown in Fig. 8; its transfer function is

$$F(s) = \frac{1 + s\tau_2}{1 + s\tau_1} \tag{38}$$

where $\tau_1 = (R_1 + R_2)C$ and $\tau_2 = R_2C$.

The closed-loop transfer function can be expressed in the form

$$H(s) = \frac{s\left(2\zeta\omega_n - \dfrac{\omega_n^2}{AK}\right) + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{39}$$

with

$$\omega_n = \sqrt{\frac{AK}{\tau_1}} \qquad \text{and} \qquad \zeta = \frac{\omega_n}{2}\left(\tau_2 + \frac{1}{AK}\right) \tag{40}$$

Note that if AK is large enough, then these equations reduce to Eqs. (34) and (36).

The design procedures for APLLs using passive lead-lag or active filters are similar. The only difference is that the application of a passive lead-lag filter results in a nonzero θ_{ss} given by Eq. (23).

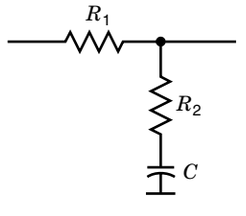

Figure 8. Circuit diagram of the passive lead–lag loop filter.

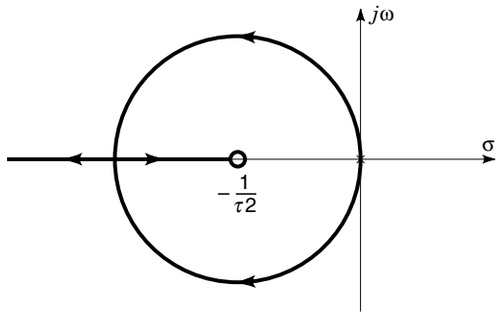

Figure 9. Root locus for second-order APLL implemented with active loop filter.

Other loop filters are also used in practical APLL circuits. A short summary of loop parameters and closed-loop transfer functions is given in Table 1 for different loop filter configurations.

Stability Considerations. So far, stability of the APLL has been assumed. A necessary and sufficient condition for stability is that all of the poles of the closed-loop transfer function lie in the left half-plane. As shown by Eqs. (31), (34) and (39), the positions of the poles vary as the loop gain is changed. The locus that the poles trace out in their migrations in the complex s-plane as the loop gain varies from zero to infinity is known as the *root locus plot.*

The root loci for the active and passive loop filters are shown in Figs. 9 and 10, respectively. Root loci for other loop filters are given in (3) and (10).

The root loci for the first- and second-order APLLs lie entirely in the left half-plane, that is, these circuits are unconditionally stable. However, the third-order APLL may become unstable for low values of AK (10). Because A is the rms amplitude of the input signal, a third-order APLL may become unstable for weak signals, even if it is stable under normal operating conditions. The unconditional stability of the second-order APLL makes it popular in situations where the amplitude of the input signal is not constant.

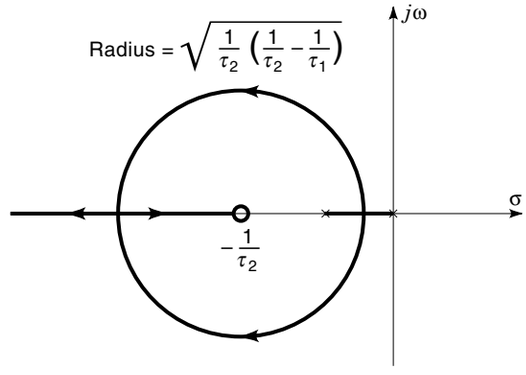

Figure 10. Root locus for second-order APLL including a passive lead-lag filter.

There is another technique that is very often used for the design of APLLs. Bode plots offer a simple but useful graphic tool for the analysis (10), since

- all the important closed-loop parameters appear as distinctive points on the Bode plot; and
- the loop stability can be also determined.

The Bode plot consists of a pair of graphs, where both the magnitude and phase of the open-loop transfer function are plotted. The open-loop transfer function of an APLL is given by Eq. (30) that is repeated here for convenience

$$G(s) = AK\frac{F(s)}{s} \tag{41}$$

The frequency ω_B, where the open-loop gain becomes 0 dB is a good approximation of the closed-loop bandwidth. The Bode criterion for stability is that the absolute value of the phase of $G(j\omega)$ at ω_B must be less than 180°.

Figure 11 shows the Bode plot for the most commonly used second-order APLLs implemented with (a) active and (b) passive lead-lag loop filters. The pole and zero frequencies and the most important closed-loop parameters are indicated on the Bode plot. Note that the absolute value of the phase shift never exceeds 180°, that is, these loops are unconditionally stable. The Bode plot shows that the damping factor is controlled by the zero frequency of the loop filter. Placing the zero at the unity-gain point ω_B yields a damping factor $\zeta = 0.5$. The natural frequency ω_n is assigned by the frequency at which the extension of the -40 dB/decade line segment crosses the unity-gain ordinate.

The open-loop transfer function is proportional to the amplitude of incoming signal, as shown by Eq. (41). If A varies, then the Bode plot has to be shifted up or down along the vertical axis. In these cases both ω_n and ζ vary, but at least the second-order APLL remain stable for any value of incoming amplitude.

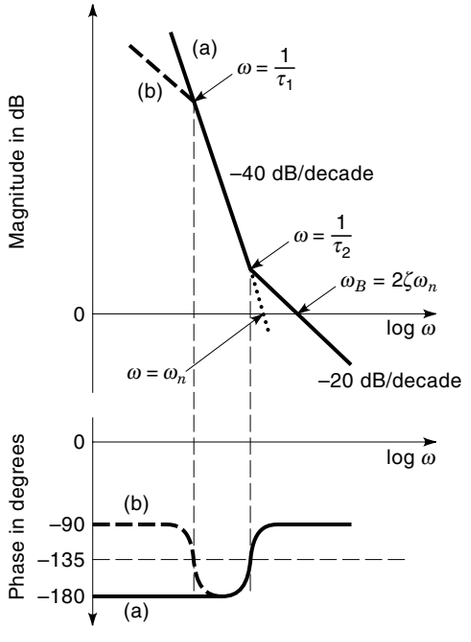

Figure 11. Bode plot of second-order APLLs implemented with (a) active and (b) passive lead–lag loop filters.

Linear Tracking. In many applications the phase of the incoming signal must be tracked with a small phase error. To evaluate the tracking properties of APLL, one determines the phase error response to different input phases $\theta_i(t)$. Three cases will be considered:

1. Transient response to phase step, frequency step and frequency ramp,
2. Sinusoidal modulation; and
3. Modulation with an arbitrary stationary process.

In this section the linearized loop equation will be used to determine the tracking properties of the loop. Recall that Eq. (26) is valid for perturbations of the variables about their quiescent values.

From Eq. (26) is obtained the phase error response to the input phase

$$\tilde{\theta}_e(s) = [1 - H(s)]\tilde{\theta}_i(s) = \frac{s}{s + AKF(s)}\tilde{\theta}_i(s) \tag{42}$$

This linear approximation is valid if $\theta_e(t)$ remains small enough both during the transient and under steady-state conditions. For the sinusoidal PD and if $\theta_{ss} = 0$, the phase error has to be less than 1 radian. In this case one may use the approximation $\sin\theta_e \approx \theta_e$.

By means of the final value theorem of the Laplace transform, the steady-state value of the phase error can be expressed directly from the error function

$$\lim_{t\to\infty}\theta_e(t) = \lim_{s\to 0} s[1 - H(s)]\tilde{\theta}_i(s) \tag{43}$$

The most commonly encountered excitations can be expressed as

$$\theta_i(t) = \left(\Delta\theta_i + \Delta\omega_i t + \Delta\dot{\omega}_i\frac{t^2}{2}\right)u(t) \tag{44}$$

where $u(t)$ is the unit step function and the first, second, and third terms denotes a phase step, frequency step and frequency ramp, respectively. The steady-state values of the phase error for different loop filter configurations are given in Table 2.

A heuristic derivation of the steady-state phase response to a frequency step helps one better to understand the operation of the loop. In steady-state, the input and VCO frequencies are equal. The control voltage needed to retune the VCO by $\Delta\omega_i$ is $\Delta\omega_i/K_v$. The dc gain of the loop filter is $F(0)$, that is, the steady-state value of the PD output is $\Delta\omega_i/K_vF(0)$. The phase error required to produce this output voltage is

$$\theta_e = \frac{\Delta\omega_i}{AK_dK_vF(0)} = \frac{\Delta\omega_i}{AKF(0)} \tag{45}$$

Table 2 shows the most important advantage of the ideal second-order APLL. In real applications, the frequency of the incoming signal always differs from the VCO center fre-

Table 2. Steady-State Values of the Phase Error Response to a Few Commonly Encountered Excitations

Loop		Loop Filter	Steady-State Phase Error Response (in rad) to		
Order	Type	$F(s)$	Phase Step	Frequency Step	Frequency Ramp
First	One	1	0	$\frac{\Delta\omega}{AK}$	∞
Second	One	$\frac{1+s\tau_2}{s\tau_1}$	0	0	$\frac{\Delta\dot{\omega}}{\omega_n^2}$
	Two	$\frac{1+s\tau_2}{1+s\tau_1}$	0	$\frac{\Delta\omega}{AK}$	∞

quency. Even if an ideal integrator cannot be implemented, the high dc gain of the operational amplifier used in the active loop filter keeps the steady-state phase error extremely small, independent of the frequency error. Due to the *constant* and *zero* phase error,

- the PD gain K_d lumped with $K_g = dg(\theta_e)/d\theta_e|_{\theta_{ss}}$ becomes constant, that is, the closed-loop parameters do not depend on the frequency error; and
- the widest linear region of the analog multiplier can be exploited, where $\sin\theta_e \approx \theta_e$.

The error responses of different APLLs to commonly used inputs can be found in the literature. [For a good survey of sources see (11), Table III p. 19.]

Next, we determine the loop response to angle-modulated input signals. For sinusoidal phase modulation one may write

$$\theta_i(t) = \Delta\theta \sin(\omega_m t) \tag{46}$$

where $\Delta\theta$ is the peak phase deviation and ω_m denotes the modulation frequency.

The steady-state phase error response can be calculated from Eq. (42) as

$$\theta_e(t) = |1 - H(\omega_m)|\Delta\theta \sin(\omega_m t + \Theta) \tag{47}$$

where the gain $|1 - H(\omega_m)|$ and phase shift Θ are given by

$$|1 - H(\omega_m)|e^{j\Theta} \equiv [1 - H(s)]|_{s=j\omega_m} \tag{48}$$

Let the input frequency modulation be expressed as

$$\theta_i(t) = \int_0^t \Delta\omega \sin(\omega_m\tau)\, d\tau = \frac{\Delta\omega}{\omega_m}\cos(\omega_m t) \tag{49}$$

where $\Delta\omega$ denotes the peak frequency deviation. The phase error is

$$\theta_e(t) = |1 - H(\omega_m)|\frac{\Delta\omega}{\omega_m}\cos(\omega_m t + \Theta) \tag{50}$$

where $|1 - H(\omega_m)|$ and Θ are given by Eq. (48). The error response is shown in Fig. 12 for the first-order and ideal second-order loops. The high-frequency asymptote is the same for both loops, but the responses are completely different below the closed-loop bandwidth. The second-order APLL ensures a much smaller tracking error than the first-order loop. One should not forget that if the APLL is used to process angle-modulated signals, then a smaller phase error results in less distortion.

Inspecting Figs. 7 and 12, it can be seen that the tracking error becomes very large at ω_n in the second-order loop for small damping factors. Recall that the linear approximation can be used only if the phase error remains small enough, even at ω_n.

It has been assumed above that the input angle-modulation is produced by a single sinusoidal signal. In general, the modulating signal is a random process and all that may be known are its mean and covariance function. In this case the aim is to determine the power spectral density and variance of the phase error process caused by the input PM and FM.

Let the input phase modulation process $\theta_{i,\mathrm{PM}}(t)$ be a wide-sense stationary process with zero mean and power spectral density $S_{i,PM}(\omega)$. As shown in (3), the power spectral density of the phase error process in steady-state can be expressed as

$$S_{e,PM}(\omega) = |1 - H(\omega)|^2 S_{i,PM}(\omega) \tag{51}$$

and its variance is

$$\sigma_{e,PM}^2 = \frac{1}{2\pi}\int_{-\infty}^{\infty} S_{e,PM}(\omega)\, d\omega \tag{52}$$

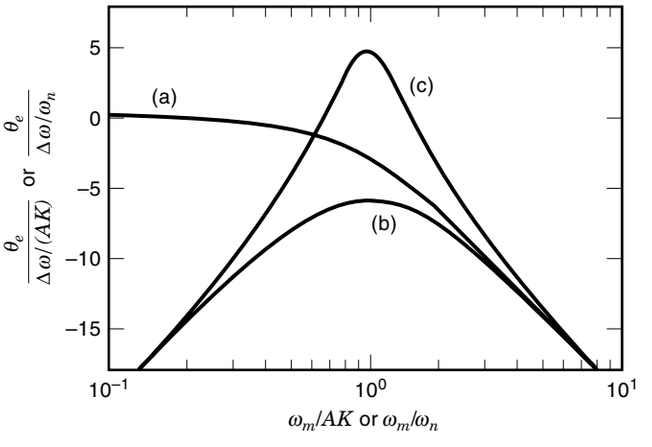

Figure 12. Phase error generated by sinusoidal FM in (a) first-order and ideal second-order APLL for (b) $\zeta = 1$ and (c) $\zeta = 0.3$. The modulation frequency ω_m and the peak frequency deviation $\Delta\omega$ are normalized to AK in the first-order loop and to ω_n in the second-order loop. To make the figures comparable, $AK = \omega_n$.

The variance of $\theta_e(t)$ represents the mean square value of the phase error process, which must be kept small for almost all t in order to make the linear model valid. If the input of the phase modulator generating $\theta_i(t)$ is a stationary random process of zero mean and power spectrum $S_m(\omega)$ then

$$S_{i,PM}(\omega) = K_{PM}^2 S_m(\omega) \tag{53}$$

where K_{PM} is the modulator gain. Substituting Eq. (53) into Eq. (51), the parameters of the phase error process can be expressed.

In the case of FM, the input phase modulation is

$$\theta_i(t) = K_{FM} \int_0^t m(t)\, d\tau \tag{54}$$

where K_{FM} denotes the modulator gain. Even if the modulating process $m(t)$ is stationary its integral will not necessarily be, so that the relationship between the power spectral densities of the input frequency modulation process and the phase error process cannot be given. However, Viterbi has shown in (3) that the power spectrum of the phase error process can be expressed as

$$S_{e,FM}(\omega) = K_{FM}^2 \frac{|1 - H(\omega)|^2}{\omega^2} S_m(\omega) \tag{55}$$

where $S_m(\omega)$ is the power spectrum of the input of FM modulator. The variance of the phase error process is

$$\sigma_{e,FM}^2 = \frac{1}{2\pi} \int_{-\infty}^{\infty} S_{e,FM}(\omega)\, d\omega \tag{56}$$

Noise Performance for High SNR. As demonstrated earlier, narrowband additive input noise $n_i(t)$ can be modeled by an equivalent noise process $n_g(t)$ entering the baseband model after the PD nonlinearity $g(\cdot)$, as shown in Fig. 3. If an analog multiplier is used as the PD, then $n_g(t) = N(t,\ \theta_o)$. The statistical properties of $N(t,\ \theta_o)$ have been summarized earlier. Recall here the most important characteristics of $N(t,\ \theta_o)$. Let $n_i(t)$ have a symmetrical power spectral density $N_0/2$ and let the bandwidth of $\theta_o(t)$ be much less than that of $n_i(t)$. In this case the equivalent noise $n_g(t)$ is a Gaussian process with uniform spectral density $N_0/2$. Furthermore, if the variance of the phase error caused by noise and input angle-modulation, if any, is sufficiently small, then the linear baseband model shown in Fig. 4 can be used to evaluate the noise performance of the APLL. Provided that the linear model is valid, the superposition theorem holds and the effect of noise and input angle-modulation can be determined independently of each other.

The equivalent noise process having a power spectral density $S_N(\omega) = N_0/2$ is wide-sense stationary with zero mean. Let the point where $n_g(t)$ is applied to the loop be considered as input, and let $\theta_e(t)$ and $\theta_o(t)$ be considered as outputs. The magnitude of the two frequency responses is obtained as

$$\left| \frac{K_d K_v F(\omega)}{j\omega + A K_d K_v F(\omega)} \right| = \frac{|H(\omega)|}{A} \tag{57}$$

The power spectral densities of the phase error $S_{e,N}(\omega)$ and the output phase $S_{o,N}(\omega)$ processes become

$$S_{e,N}(\omega) = S_{o,N}(\omega) = |H(\omega)|^2 \frac{N_0}{2A^2} \tag{58}$$

from which is obtained the variances of the phase error and the output phase

$$\sigma_{e,N}^2 = \sigma_{o,N}^2 = \frac{N_0}{2A^2} \frac{1}{2\pi} \int_{-\infty}^{\infty} |H(\omega)|^2\, d\omega \tag{59}$$

Let the noise bandwidth B_L of the loop be defined as the bandwidth of an ideal low-pass filter, whose output variance is $\sigma_{e,N}^2$ when it is driven with Gaussian white noise of power spectral density $N_0/2A^2$

$$B_L = \frac{1}{2\pi} \int_0^{\infty} |H(\omega)|^2\, d\omega \tag{60}$$

Then Eq. (59) becomes

$$\sigma_{e,N}^2 = \sigma_{o,N}^2 = \frac{N_0 B_L}{A^2} \tag{61}$$

The noise bandwidths for the most important loop filter configurations are given in Table 1.

Noise bandwidth for the ideal second-order loop is plotted against damping in (10) (see Fig. 3.3 on p. 32). The minimum B_L is achieved for $\zeta = 0.5$, but the noise bandwidth does not exceed the minimum by more than 25% for any damping between 0.25 and 1.0.

Since the input additive noise and angle-modulaton are independent processes, the total variance of the phase error is the sum of Eqs. (52) and (59). Taking into account Eqs. (51) and (60) we get for PM

$$\sigma_e^2 = \sigma_{e,PM}^2 + \sigma_{e,N}^2 = \frac{1}{2\pi} \int_{-\infty}^{\infty} |1 - H(\omega)|^2 S_{i,PM}(\omega)\, d\omega + \frac{N_0 B_L}{A^2} \tag{62}$$

The linear approximation can be used only if the total variance of $\theta_e(t)$ is small enough. For the ideal second-order loop, σ_e^2 has to be less than 0.2 (10). If, in addition to the input noise and angle-modulation, other random processes such as VCO noise or frequency modulation of the VCO output signal are present then the effects of these processes must also be accommodated in σ_e^2 by applying the technique described above.

Since there is no "signal" in the baseband model of the APLL, an unambiguous definition of the *signal-to-noise ratio* (SNR) in the loop cannot be given. The variance of the phase error is used by Viterbi (3) and Lindsey (6) to define the SNR in the APLL

$$\mathrm{SNR}_L = \frac{A^2}{N_0 B_L} \tag{63}$$

Nonlinear Operation of APLL

The linear theory of the APLL has been very well developed and is very easy to understand. In the majority of circuit de-

sign and development, the linear APLL model is applied and nonlinear effects are considered only as unwanted problems.

However, in many important situations the nonlinear model of the APLL has to be considered, for example, if the lock limits or acquisition properties have to be determined, if the APLL operates at low SNR, and so forth.

In contrast to the linear APLL theory, a unified theory describing the nonlinear operation of APLL in closed form does not exist. Many times individual methods and heuristic arguments are used to solve the problem. The details of the nonlinear mathematical analysis are beyond the scope of this exposition. In this section only the most important aspects of nonlinear APLL theory will be discussed; the interested reader should refer to the literature for further details, when the need arises. The latest results on nonlinear theory can be found in three IEEE publications (11–13), while the nonlinear APLL theory is given in many excellent books (3–10).

Nonlinear Tracking in the Absence of Noise. In this section we assume that the phase-locked condition has been achieved, but the frequency or phase of input signal is changed. First the hold-in range is determined, then the nonlinear transient response to a phase or/and frequency step is determined by means of the phase-plane portrait. In this chapter only the noise-free case is considered.

Let ω_i denote the frequency of the input signal. Then the input frequency error can be expressed from Eq. (2) as $\Delta\omega_i = \omega_i - \omega_0$. The *hold-in range* is equal to the input frequency error, which can be tracked by the APLL, that is, for which the phase-locked condition is maintained. Mathematically the hold-in range is equal to the maximum frequency error for which Eq. (15) has a steady-state solution

$$\sin\theta_e = \frac{\Delta\omega_i - K_v v_{e0}}{AKF(0)} = \frac{\Lambda_0}{AKF(0)} \tag{64}$$

where v_{e0} is a dc voltage, $\Lambda_0 = \Delta\omega_i - K_v v_{e0}$ denotes the initial equivalent frequency detuning, and $F(0)$ is the dc gain of loop filter. Because the sine function cannot exceed unit magnitude, the hold in range is

$$|\Delta\omega_H - K_v v_{e0}| = AKF(0) \tag{65}$$

The physical meaning of the hold-in range is that the PD output voltage is bounded and so the maximum VCO frequency detuning is also bounded.

Equation (65) states that the hold-in range can be made arbitrarily large by using very high loop gain K. Of course, this is not entirely correct because some other loop component will then saturate before the phase detector. In the ideal second-order loops, saturation of the loop amplifier generally limits the hold-in range. Note that the hold-in range is a *static parameter,* that is, its value does not depend on the order of APLL.

Consider next the nonlinear tracking properties, that is, the *dynamics* of a first-order APLL in the absence of noise. Assume that the APLL is operating in steady-state when the input frequency is suddenly changed so that

$$\theta_i(t) = \Delta\omega_i t + \theta_{i0} \tag{66}$$

where θ_{i0} is constant. Substituting $F(p) = 1$, $N(t, \theta_o) = \Psi_2 = 0$ and $d\theta_i/dt = \Delta\omega_i$ into Eq. (15) one gets a nonlinear differential equation

$$\frac{d\theta_e}{dt} = \Delta\omega_i - K_v v_{e0} - AK\sin\theta_e = \Lambda_0 - AK\sin\theta_e \tag{67}$$

Observe that Eq. (67) is an autonomous differential equation.

To get the nonlinear transient response of APLL to the input frequency step, Eq. (67) must be solved. The initial value θ_{e0} of the phase error depends on the phase error measured under the previous steady-state conditions and θ_{i0}.

A better insight into the APLL operation can be obtained if we plot $\dot\theta_e = d\theta_e/dt$, called the *frequency error,* as a function of θ_e, as shown in Fig. 13. A plot of a single solution in the phase plane is called a *trajectory.* The trajectory starts from the initial value θ_{e0} of the phase error and goes to its steady-state value for which $d\theta_e/dt = 0$. An ensemble of trajectories emerging from different initial conditions is known as *phase-plane portrait* or *flow.* A trajectory shows the dynamic behavior of a loop in function of time as it settles (or fails to settle) toward equilibrium.

As shown in Fig. 13, all trajectories of a first-order APLL coincide with each other. Let the trajectory be started from an initial phase error θ_{e0}. If $d\theta_e/dt$ is positive for that value of $\theta_{e\phi}$, then the phase error will increase as a function of time. In fact, the APLL follows the trajectory plotted in Fig. 13 and moves toward the right until it reaches the steady-state for which $d\theta_e/dt = 0$. Similarly, if $d\theta_e/dt$ is negative for θ_{e0}, then the phase error decreases until it reaches the steady-state conditions. In either case, the point belonging to steady-state is stable, since, after a small perturbation of θ_e in either direction, the system will tend to return to the steady-state.

Since almost all phase detectors have a periodic characteristic, they cannot distinguish a phase step of $\Delta\theta_i + 2\pi n$, $n = 1, 2, 3, \ldots$ from one of $\Delta\theta_i$. Therefore the APLL never loses lock when it is driven by a pure phase step, irrespective of the magnitude of the loop order.

In the first-order APLL, a frequency step breaks the lock if, and only if, the frequency error exceeds the hold-in limit. In this case, the phase-locked condition cannot be recovered and the APLL remains unlocked.

In a second-order loop, the frequency step may also break the lock if its magnitude is large enough. However, after a

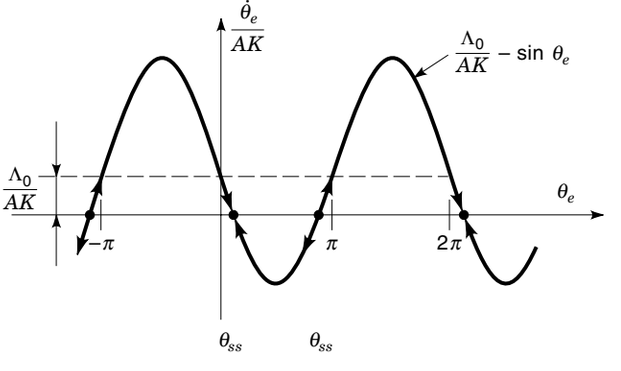

Figure 13. Phase-plane portrait for first order APLL.

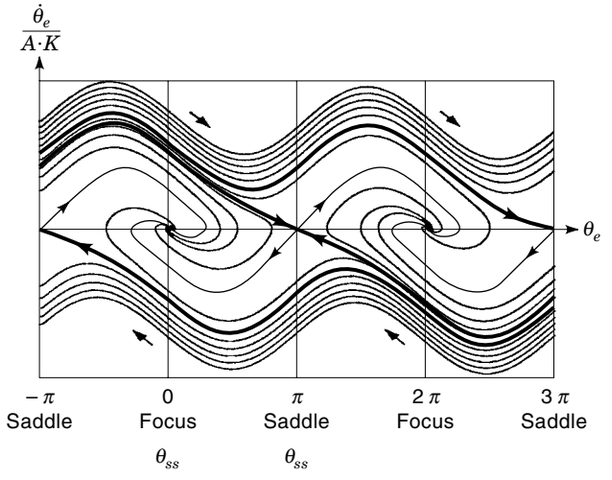

Figure 14. Phase-plane trajectories of the ideal second-order APLL for $\zeta = 0.707$.

transient the APLL may achieve the phase-locked condition again.

To obtain the phase-plane trajectories for the ideal second-order APLL, first the time variable has to be eliminated in Eq. (15). Substituting $F(p) = (1 + p\tau_2)/p\tau_1$ and Eq. (66) into Eq. (15) one obtains

$$\frac{d^2\theta_e}{dt^2} + \left(AK\frac{\tau_2}{\tau_1}\cos\theta_e\right)\frac{d\theta_e}{dt} + \frac{AK}{\tau_1}\sin\theta_e = 0 \tag{68}$$

Letting $t = \tau/(AK\ \tau_2/\tau_1)$, so that $d\theta_e/dt = AK\ \tau_2/\tau_1\ d\theta_e/d\tau$, one can eliminate one constant from Eq. (68). Taking into account that $AK\ \tau_2/\tau_1, \neq 0$, Eq. (68) can be written as

$$\frac{d^2\theta_e}{d\tau^2} + \cos\theta_e\frac{d\theta_e}{d\tau} + \frac{\tau_1}{AK\tau_2^2}\sin\theta_e = 0 \tag{69}$$

If one divides Eq. (69) by $\dot{\theta}_e = d\theta_e/d\tau$ and recognizes that $d^2\theta_e/d\tau^2 = d\dot{\theta}_e/d\tau$, then the first term of Eq. (69) becomes $\ddot{\theta}_e/\dot{\theta}_e = (d\dot{\theta}_e/d\tau)/(d\theta_e/d\tau) = d\dot{\theta}_e/d\theta_e$. Eliminating τ in Eq. (69), one may treat the phase error θ_e and the normalized frequency error $\dot{\theta}_e$ as independent variables (3)

$$\frac{d\dot{\theta}_e}{d\theta_e} = -\cos\theta_e - \frac{\tau_1}{AK\tau_2^2}\frac{\sin\theta_e}{\dot{\theta}_e} \tag{70}$$

To get the phase-plane portrait, the solution of Eq. (70) must be determined for different initial conditions. The phase-plane trajectories for an ideal second-order APLL are shown in Fig. 14.

The phase-plane portrait of an APLL with a periodic phase detector characteristic is also periodic with the same period in variable θ_e, but is aperiodic in $\dot{\theta}_e$. Trajectories proceed as a function of time clockwise only as marked by arrows in Fig. 14. Intersection of trajectories may occur only at *singular points,* that assign the possible steady-state solutions of loop equation. Both stable and unstable singular points appear; equilibrium occurs at stable singularities. In second-order APLLs, an equilibrium is called a *stable node* or *stable focus* if the loop is overdamped ($\zeta > 1$) or underdamped ($\zeta < 1$), respectively. The steady-state phase-locked conditions which are reached asymptotically are called *equilibria.*

The unstable singularity is called a *saddle point.* Even if the loop state gets just into a saddle point, where it is in equilibrium, it cannot remain there, because any disturbance, such as noise, will displace it slightly and then the saddle point repels the loop state.

A trajectory that terminates on a saddle point is called *separatrix.* The separatrices are marked by heavy curves in Fig. 14.

Consider a stable singular point and the two separatrices that terminate on the two adjacent saddle points. If the initial conditions lie between these separatrices and the initial phase error is in the 2π interval centered about the stable equilibria to be achieved, then the trajectories emerging from these initial conditions will terminate at that equilibrium point without cycle slip. If the initial conditions lie outside these separatrices, then the loop slips one or more complete cycles before achieving the phase-locked condition.

We are now ready to evaluate the nonlinear transient graphically for a second-order APLL. First, the initial conditions have to be determined from Eq. (66) and the previous steady-state conditions. Then the initial conditions have to be plotted on the phase-plane portrait, and the trajectory emerging from them gives the actual transient response of APLL.

The phase-plane portrait is a very useful tool for the determination of APLL dynamics. Phase-plane portraits for other loop configurations can be found in (3) and (6).

Acquisition Behavior in the Absence of Noise. Before a PLL can track, it must first acquire the phase-locked condition. In general, the PLL quiescent frequency differs from the frequency of the incoming signal. Therefore, first the VCO frequency has to be tuned to the incoming frequency by the loop. This process is called *frequency pull-in.* Then the VCO phase has to be adjusted according to the input phase. This process is known as *phase lock-in.*

The two parts of the acquisition process can be recognized easily by plotting the phase error as a function of time. Figure 15 shows that the phase error $\theta_e(t)$ generally goes through multiple periods of 2π before finally settling in to the phase-locked condition. When the phase exceeds 2π, a cycle slip occurs between the incoming and VCO phases. The position of

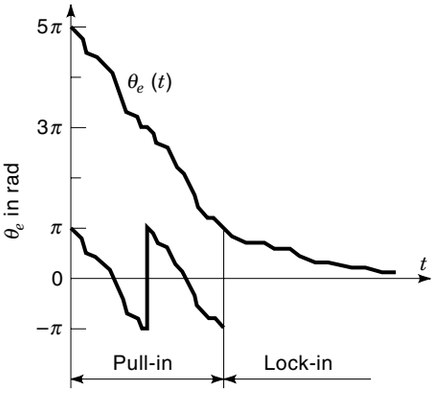

Figure 15. Distinction between pull-in and lock-in.

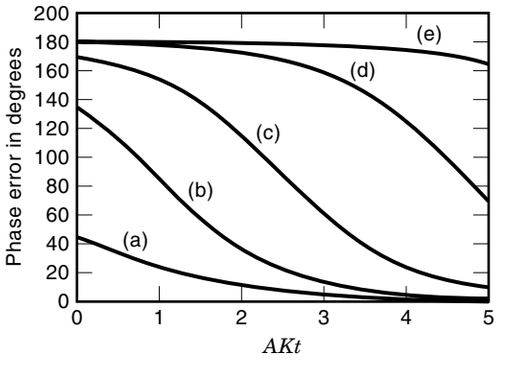

Figure 16. Acquisition behavior of first-order APLL. The initial values of phase error θ_{i0} are (a) 45°; (b) 135°; (c) 170°; (d) 178.86° and (e) 179.886°.

cycle slips can be seen easily if one plots the modulo-2π process for $\theta_e(t)$, shown in Fig. 15 by the lower curve. The jumps of 2π in $\theta_e(t)$ indicate the occurrence of a cycle slip. Note that there are no cycle slips during the lock-in process.

Acquisition is inherently a highly nonlinear phenomenon. It is started from given initial conditions and no external excitation is applied, apart from the initial phase and frequency error. This means that acquisition can be described by an autonomous nonlinear differential equation and it can be studied by the phase-plane portrait introduced in the previous section.

If the loop acquires lock by itself, the process is called *self-acquisition.* If it is assisted by extra circuits, it is called *aided acquisition.* Since self-acquisition is relatively slow and unreliable, acquisition-aids are often used. For a good survey of different aided acquisition techniques, see (10).

The acquisition behavior of a first-order APLL is described by Eq. (15) and can be studied by means of the phase-plane portrait shown in Fig. 13. Under steady-state conditions, $d\theta_e/dt = 0$. It is clear from Eq. (15) and Fig. 13 that $d\theta_e/dt$ becomes zero at any of the following values of phase error:

$$\begin{aligned} \theta_{ss} &= \sin^{-1}\left(\frac{\Lambda_0}{AK}\right) + 2n\pi, \qquad n = 0, 1, 2, \ldots \\ \hat{\theta}_{ss} &= -\sin^{-1}\left(\frac{\Lambda_0}{AK}\right) + (2n-1)\pi, \qquad n = 0, 1, 2, \ldots \end{aligned} \tag{71}$$

provided $|\Lambda_0| \leq AK$. Referring to Fig. 13 one sees that the equilibrium points denoted θ_{ss} are stable, $\hat{\theta}_{ss}$ are unstable. If the phase error is equal to $\hat{\theta}_{ss}$ then any perturbation in either direction, caused by noise, for example, will cause θ_e to move until it reaches the next stable equilibrium. If $|\Lambda_0| > AK$, no stable equilibrium exists and the loop never reaches the phase-locked condition, but $\theta_e(t)$ moves along the sinusoidal trajectory.

Figure 13 shows that an infinitely large number of equilibrium points exists. Since every cycle of the trajectory has a stable equilibrium, θ_e cannot change by more than one cycle before phase-locking. Thus the pull-in and lock-in ranges are equal, so cycle slipping never occurs during acquisition in the first-order loop.

The phase transients of the first-order APLL during acquisition are shown in Fig. 16 for different values of the initial phase error θ_{i0}. Note that for small θ_{i0}, the loop operation remains near the equilibrium and the phase transient is almost exponential, as expected from the linear theory of the APLL. However, if $\theta_{i0} > 135°$, the waveforms diverge considerably from exponential and the acquisition time becomes very long. The acquisition parameters of the first-order loop are given in Table 3.

Table 3. Acquisition Parameters of First- and Second-Order APLLs

Loop Order	Loop Filter $F(s)$	Acquisition Range (rad/s)	Acquisition Time (s)
First	1	$4B_L$	$\dfrac{2}{B_L}$
Second	$\dfrac{1+s\tau_2}{1+s\tau_1}$	$2\sqrt{AK\zeta\omega_n}$	$\dfrac{\Lambda_0^2}{2\zeta\omega_n^3}$
	$\dfrac{1+s\tau_2}{s\tau_1}$	∞	$\dfrac{\Lambda_0^2}{2\zeta\omega_n^3}$

As explained above, the first-order loop always achieves the phase-locked condition without cycle slips. The same is not valid for the second- and higher-order loops; for these, the lock-in range is smaller than the pull-in range. The phase-plane portrait for an ideal second-order APLL is shown in Fig. 14.

Gardner has proposed a simple method to estimate the lock-in range (10). Let $F(\infty)$ denote the high-frequency asymptotic response of the loop filter. For a second-order loop $F(\infty) = \tau_2/\tau_1$. If the deviation of the input frequency from the VCO center frequency is greater than $1/\tau_2$, then the second-order loop behaves like a first-order one, with open loop-gain $K = K_d K_v F(\infty)$. As a useful engineering approximation one may say that higher-order loops have the same lock-in range as first-order ones with equivalent gain. If $v_{e0} = 0$, one may write

$$\omega_L \approx \pm AKF(\infty) \tag{72}$$

The frequency pull-in, or simply pull-in, is much slower than the lock-in process. The acquisition problem cannot be solved in closed form; some approximation must be used. Richman has developed a model (16) for the analysis of pull-in process. Consider an ideal second-order APLL. The loop filter can be divided into two parallel paths

$$F(s) = \frac{1+s\tau_2}{s\tau_1} = \frac{1}{s\tau_1} + \frac{\tau_2}{\tau_1} \tag{73}$$

as shown in Fig. 17. Note that there is a high-frequency ac path from the PD output to the VCO input with flat gain of τ_2/τ_1 and a dc path which contains a perfect integrator.

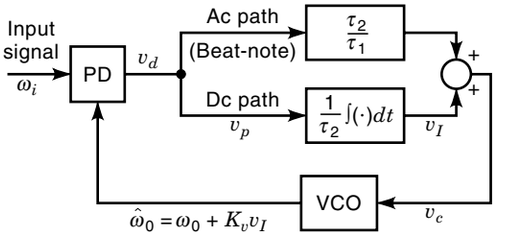

Figure 17. Pull-in model for the ideal second-order APLL.

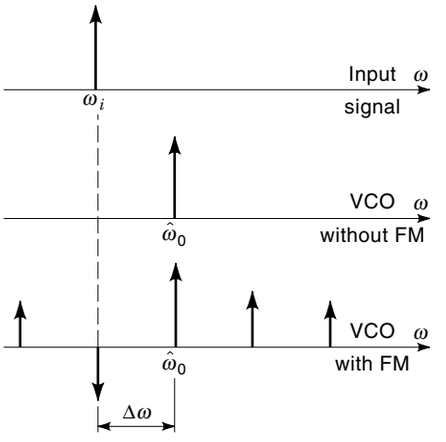

Figure 18. Pull-in spectra. The instantaneous center frequency of the VCO is denoted by $\hat{\omega}_0$.

One can understand the pull-in process easily by plotting the relevant spectra in the loop. Initially, the input and the VCO frequencies are ω_i and ω_0, respectively, as shown by the upper two traces of Fig. 18. Let $\hat{\omega}_0(t)$ denote the instantaneous VCO center frequency, which is a slowly varying function, and which is determined by the integrator output v_I. The frequency difference $\Delta\omega = \hat{\omega}_0 - \omega_i$ is called the *beat-note.*

The analog multiplier used as a phase detector generates the beat-note, which gets through the ac path and modulates the VCO, generating FM sidebands as shown in the lower trace of Fig. 18. Observe that the FM sideband $(\hat{\omega}_0 - \Delta\omega)$ coincides with ω_i and produces a negative dc voltage at the PD output denoted by v_p in Fig. 17. This dc voltage is integrated by the dc path and the slowly varying output $v_I(t)$ of integrator pushes $\hat{\omega}_0$ toward ω_i. The pull-in process is terminated when $\hat{\omega}_0 = \omega_i$.

Many approximate formulas for pull-in limits and pull-in time have been developed by different authors for various loop configuration. For a good survey, see Sec. 5.3 of (10). Formulas giving the acquisition parameters of first- and second-order loops are given in Table 3.

Hangup Phenomenon. APLLs occasionally have extremely long acquisition time that cannot be tolerated in many applications. In these cases, the loop seems to stick for a long time at a certain value of phase error before moving toward the phase-locked condition. This phenomena, studied by Gardner in (17), is known as the *hangup effect.*

Almost all phase detectors have a phase error characteristic which is periodic. Due to this periodicity, the loop equation has two steady-state solutions in every period. The locations of steady-state solutions have been called the *normal equilibrium null* and *reverse null* by Gardner (10).

The slope of the PD characteristic is positive at the normal equilibrium null providing negative feedback for the loop. At the reverse null, the slope becomes negative causing positive feedback in the APLL.

Consider an APLL implemented with an analog multiplier and assume that $\Lambda_0 = 0$, that is, that the steady-state phase error is zero. The phase trajectories originating near 180° remain in that vicinity for a long time before decaying toward equilibrium at 0°. Examples for hangup are shown in Fig. 16, where the phase transients are plotted for different initial values of phase error. It must be emphasized that the hangup effect appears in every APLL, independently of the loop order.

It is obvious from Fig. 17 that the rate of VCO control voltage is proportional to the dc output v_p of the phase detector that is, in reality, a slowly varying signal. Voltage v_p can be considered as a restoring force. If v_p is very small, as occurs near the reverse null, then restoring force is also small and the loop converges extremely slowly toward the phase-locked condition.

Techniques and design rules that help to avoid the hangup effect are given in (17).

False Lock to Data Sidebands. The recovery of suppressed carriers is also performed by PLLs. The most commonly used circuit configurations will be discussed later. Since the carrier is completely suppressed in these cases, the carrier recovery circuit must regenerate a harmonic of the carrier (squaring loop) or, equivalently, must generate a phantom carrier (Costas loop). In both solutions, the loop operation can be modeled by a proper nonlinear operation followed by a CW tracking loop.

In addition to the regenerated signal, discrete frequency components spaced by integer multiples of half the symbol rate also appear about the desired frequency due to the nonlinear operation (18,19). If the quiescent frequency of the VCO is close enough to one of these sidebands, then the loop will lock onto that spectral component instead of the desired frequency. This phenomena is called *false lock to data sidebands.* The probability of false lock is especially high when the SNR_L is high.

Note that this kind of false lock is completely different from that which appears in a superheterodyne PLL receiver. In that case, false lock is caused by the narrowband IF filter, which is included in the so-called *long loop.* For a comprehensive discussion of the false lock problem in long loops, and for further references, see (10).

APLL Behavior in the Presence of Noise. When one tests the behavior of a real APLL and reduces the SNR_L below about 7 dB, the fluctuation in phase error, called *phase jitter,* becomes more than predicted from Eq. (62). In this section, the behavior of the APLL for low SNR_L when the linear approximation is no longer applicable is briefly discussed.

We have seen that PLLs have an infinitely large number of stable equilibrium points. At low SNR_L, the phase error migrates among the different stable equilibrium points, that is, the *probability density function* (pdf) of θ_e appears as a multimodal function with each mode centered about a stable equilibrium point.

To understand the problem, let the SNR_L be very high at the beginning and then let it be reduced later.

For high SNR_L, a small fluctuation in phase error about θ_{ss} appears. This small fluctuation can be determined by means of linear APLL theory.

If the SNR_L is reduced then the linear approximation results in a large error [see Fig. 3.4 in (10)]; even more, cycle slips occur. Migration caused by the cycle slipping problem can be studied only in the context of nonlinear theory.

The detailed study of nonlinear APLL theory goes beyond the scope of this chapter. This section will only summarize the basic ideas and the most important results. Interested

readers may refer to the original sources of nonlinear APLL theory (3,7).

The migration of phase error among the different stable equilibrium points is illustrated in Fig. 19. The figures show how the steady-state pdf of phase error is developing from its initial position. Let the APLL initially be in phase lock so that $p(\theta_e, t|\theta_{ss}, t_0) = \delta(\theta_e, -\theta_{ss})$. With time, the initial phase begins to diffuse in the vicinity of θ_{ss}, due to noise, but cycle slip does not yet appear. However, after a sufficiently long period, more and more cycle slips appear in both directions. The average time for the occurence of cycle slips depends on SNR_L. After a long time, the probability density of phase error will appear as a multimodal function, with each mode centered about a stable equilibrium point. If one considers the equilibrium points as attractors, then one may say that the phase error migrates among the basins of all of these attractors in the long run. As a result, the pdf of the phase error possesses an unbounded variance.

Tikhonov (21,22) and Viterbi (23) have shown that the phase error process reduced by modulo-2π is stationary and possesses a bounded variance. If one treats the cycle slip effect as an independent problem and if one is interested in the steady-state behavior of the APLL, then one may attend to determining the pdf of the reduced modulo-2π phase error process, which is denoted by $\phi(t)$.

The loop operation can be described in the presence of noise by a nonlinear stochastic differential equation [see Eq. (15)]. An exact nonlinear theory for APLLs can be developed by means of Fokker–Planck theory (6). The solution of the

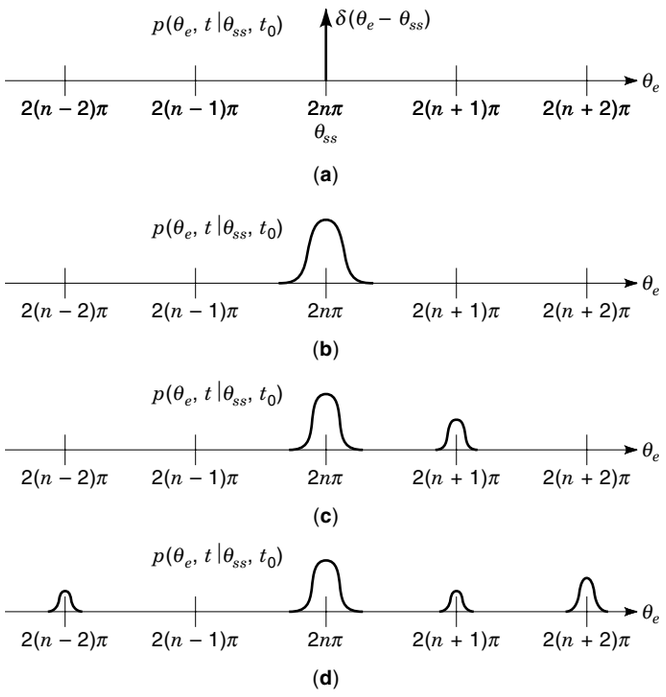

Figure 19. Qualitative behavior of the phase error pdf with time. Initially, the APLL is (a) in equilibrium position θ_{ss}; then (b) the pdf expands due to diffusion. Later a cycle slip appears and the phase error migrates (c) to the adjacent stable equilibrium on the right side. Then after a long period (d) the pdf appears as a multimodal function about the stable equilibrium positions.

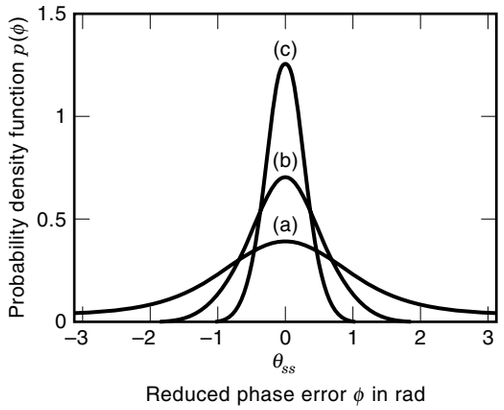

Figure 20. Probability density functions of reduced phase error for a first-order APLL with zero detuning. The curves are given for SNR_L values of (a) 0 dB (b) 5 dB and (c) 10 dB.

Fokker–Planck equation gives the pdf for the reduced phase error process in closed form. Consider the first-order APLL implemented with a sinusoidal phase detector. Viterbi (3) has shown that, for zero detuning, the pdf of the reduced phase error process is

$$p(\phi) = \frac{\exp(\alpha \cos \phi)}{2\pi I_0(\alpha)}, \qquad -\pi \le \phi < \pi \tag{74}$$

where $\alpha = 4A/N_0K = \text{SNR}_L$ is the loop signal-to-noise ratio and $I_0(\alpha)$ denotes the zeroth-order modified Bessel function. Typical probability densities of $\phi(t)$ for a first-order loop and zero detuning are shown in Fig. 20; probability density functions for other parameters are given in (3). The measured and calculated probability density functions are compared in (7).

The Tikhonov probability density function can also be used to describe the behavior of higher-order APLLs. Lindsey has shown in (6) that, if the parameter α is suitably modified, then the steady-state pdf of higher-order loops can be approximated by Eq. (74).

Cycle slips in the carrier recovery circuit destroy the performance of digital telecommunication systems. Cycle slips may occur either in isolated form or in bursts (24).

Consider again a first-order APLL with zero detuning. Using the Fokker–Plank technique, Lindsey has shown in (6) that the mean time between cycle slips is

$$\tau = \frac{\pi^2 \alpha I_0(\alpha)}{2B_L} \tag{75}$$

These values agree perfectly with the measured data (24). Observe that τ is inversely proportional to the noise bandwidth of the APLL, that is, for efficient carrier recovery a narrowband loop must be used.

Equation (75) can approximate the mean time between cycle slips in higher-order APLLs if the parameter α is modified appropriately (6). A better theory, giving more accurate results, has been published in (25); for measured data, see (24).

PLL APPLICATIONS

The baseband model of the analog phase-locked loop and the linear and nonlinear APLL theories were discussed in the

previous sections. The operation principle and versatility of PLLs cannot be understood without surveying the bases of different PLL applications. The aim of this section is to provide this survey and not to discuss the latest circuit configurations developed for various PLL applications.

Although various circuit configurations have been developed for different applications, the baseband model discussed above can be adopted, with minor modification, to these loop configurations.

In all PLL applications, the phase-locked condition must be achieved and maintained. In order to avoid distortion, many applications require operation in the linear region, that is, the total variance of the phase error process appearing due to noise, modulation, and so on, must be kept small enough.

Recall that only the PD output, VCO control voltage, input phase $\theta_i(t)$, and output phase $\theta_o(t)$ appear in the PLL baseband model. All these signals are low-frequency signals, $\theta_i(t)$ and $\theta_o(t)$ are the phase modulations of the input and output signals. Sometimes it is not easy to determine the spectrum of the original bandpass input and output signals. If an analog multiplier is used as the phase detector, then, by knowing the spectrum of the PD output and exploiting the frequency shifting property of the analog multiplier, the output spectrum can be determined easily.

Different phase detectors are used in different applications, in order to achieve the best circuit performance. The most commonly used PD circuit configurations will be discussed later; many of these are edge-triggered. The operation of PLLs implemented by an edge-triggered PD cannot be described exactly by the simple APLL model. However, Gardner has shown that, even in these cases, the APLL theory can be used as a good approximation of the real operation if the closed-loop bandwidth is less than one tenth of the input frequency (26).

The PLL is one of the most commonly used circuits in electrical engineering. A detailed discussion of different applications is beyond the scope of this article; for a comprehensive survey of applications, see (11) and (14).

In addition to the conventional applications, new applications for the various PLLs have been published recently. It has been shown that both the analog (27) and sampling PLLs (28) may exhibit chaotic behavior. Bernstein and Lieberman have proposed the application of an ideal sampling PLL for random number generation (29). The quality of generated random numbers has been evaluated by the run test in (30). By means of a chaotic APLLs, very simple chaotic telecommunication systems can be implemented (31).

Tracking Bandpass Filter

Bandpass filters that must select very narrowband angle-modulated signals cannot be implemented by conventional analog filters, due to their temperature dependence. In other applications, the carrier frequency of an angle-modulated signal varies. These problems can be overcome if a PLL tracking the carrier is used as a bandpass filter. The PLL separates the spectrum of the angle-modulated signal from other interfering signals, or limits the transmitted spectrum to within specified bounds. The output phase modulation is determined by the closed-loop transfer function as given by Eq. (27)

$$\tilde{\theta}_o = H(s)\tilde{\theta}_i(s) \tag{76}$$

The filter characteristic is determined by the closed-loop transfer function. A further advantage of PLL bandpass tracking filters is that they reject the amplitude modulation, that is, they can also be used as limiters.

The block diagram of a bandpass tracking filter is shown in Fig. 21. If the loop parameters depend on the amplitude of the input signal, an AGC circuit must precede the PD in order to keep the filter parameters constant. Note that the problems of and the difficulties associated with the design and implementation of a high-frequency bandpass filter are reduced to the design and implementation of a baseband loop filter. The design of PLL bandpass filters is discussed in detail in (32).

CW Carrier Recovery

In every coherent receiver the carrier has to be recovered from the noisy input signal (15). Here, it is assumed that the carrier is present all the time in the received spectrum; the recovery of a suppressed carrier will be considered later. The aim of CW carrier recovery is to retrieve the unmodulated carrier and to suppress as much noise, modulation, and interference as possible. Note that the CW carrier recovery circuit is a narrowband bandpass tracking filter implemented by a PLL, as shown in Fig. 21.

The noise-free recovery of a carrier in a noisy environment requires a very narrowband PLL [see Eq. (61)]. As shown by Table 3, the acquisition properties of narrowband PLLs are very poor. We may overcome this problem by using two different loop bandwidths: a wide one during the acquisition process and a narrow one in steady-state, after the phase-locked condition has been achieved (10).

The Doppler effect must also be considered in many carrier recovery circuits. The ideal second-order PLL can track a frequency ramp, but the reduction of tracking error requires a wide loop bandwidth (see Table 2). On the other hand, the noise-rejection performance of a PLL is inversely proportional to the loop bandwidth. For low SNR, this contradiction can be solved by using third- or higher-order loop configurations (33).

PLL Amplifier

The implementation of high-gain amplifiers in the extremely high-frequency region is very expensive. As shown in Fig. 22, the PLL can be also used for amplification of angle-modulated signals. In the simplest circuit configuration, the multipliers denoted by their multiplication factor N and the amplifier fol-

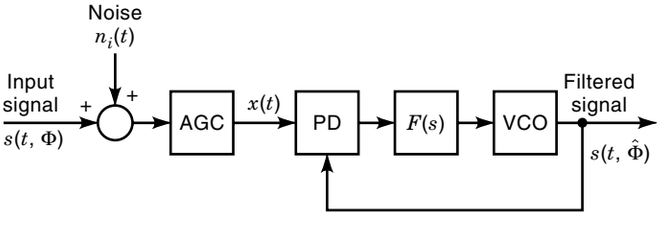

Figure 21. PLL configuration for bandpass tracking filter and CW carrier recovery. The AGC circuit is used to keep the input amplitude, that is, loop parameters, constant.

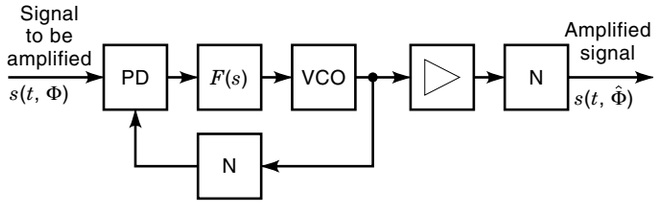

Figure 22. Amplification of angle-modulated high frequency signals by PLL.

lowing the PLL are missing. The gain is determined by the ratio of VCO output and input powers. Note that the amplification is performed in the baseband. In addition to amplification, the PLL also operates as a limiter and filter for the incoming angle-modulated signals.

Sometimes it is cheaper to implement the VCO and power amplifier below the input frequency band, as shown in Fig. 22. Due to the frequency multiplier placed in the feedback path of the APLL, the VCO output frequency is f_i/N, where f_i is the input frequency. The input phase/frequency deviation is also divided by N; however, the modulating frequency remains unchanged. Then the output frequency multiplier following the power amplifier restores the original carrier frequency and phase/frequency deviation.

Frequency Synthesis and Angle Modulation by PLL

Signals with high-frequency stability and high spectral purity are often required in electrical engineering. In many applications, the frequency of generated signal must be varied by a digital code.

The PLL is widely used in frequency synthesis to generate spectrally pure signals and, if necessary, to operate as an analog or digital frequency or analog phase modulator. Frequency multiplication and/or division, furthermore frequency addition and/or subtraction, may be performed, using a PLL in conjunction with programmable frequency dividers and mixers as shown in Fig. 23. As a result, the output frequency f_o can be expressed as a combination of reference and offset frequencies, division ratios of frequency dividers. In frequency synthesis, the PLL input is called *reference signal* and its frequency is denoted by f_R. To optimize the system performance, frequently a multiloop circuit configuration (36) is used.

In frequency synthesis applications, the dominant noise sources are the VCO, frequency dividers, mixers, and phase detectors. The main design goals are to minimize the output phase noise, to avoid the generation of spurious output signals, and to minimize the unwanted output FM caused by the periodic output of the phase detector. These requirements can be satisfied with special PD configurations, such as phase-frequency detector with a charge pump circuit or sample-and-hold phase detector. The operation of these PDs will be discussed later. Many system aspects must be considered during the development of frequency synthesizers. A detailed discussion of these questions can be found in (36–39).

In addition to frequency synthesis, PLLs can be also used as FM or PM modulators. The corresponding transfer functions for FM and PM are

$$\begin{aligned} s\tilde{\theta}_o(s) &= [1 - H(s)]K_v\tilde{V}_{FM}(s) \\ \tilde{\theta}_o(s) &= H(s)\frac{N}{AK}\tilde{V}_{PM}(s) \end{aligned} \tag{77}$$

where K_v and N/AK are the gains of the FM and PM modulators, respectively. The closed-loop error $[1 - H(s)]$ and transfer $H(s)$ functions are given by Eqs. (29) and (28), respectively. The only difference is that the frequency synthesizer has a frequency divider in the feedback path. Therefore, the loop gain becomes

$$K = \frac{K_d K_v}{N} \tag{78}$$

The equations given above and the APLL theory discussed earlier are valid only if an ordinary differential equation can describe the operation of the PLL. The phase detectors used in frequency synthesis are edge-triggered circuits. This is why the exact modeling of these circuits can be performed only by an integro-difference equation (26), (40). However, if the closed-loop bandwidth is less than one-tenth of the reference frequency f_R, then the continuous-time approximation can be used and the APLL theory is a good approximation of the circuit operation (26).

Coherent Demodulation by APLL

The noise performance of coherent demodulators is much better than that of their noncoherent counterpart (15). A circuit configuration, which is suitable for coherent PM, FM, and AM demodulation, is shown in Fig. 24.

PM Demodulator. Assume first that the input signal $s(t, \Phi)$ is phase modulated and $A(t) = A$ = constant. The demodulated PM signal can be measured at the output of the phase

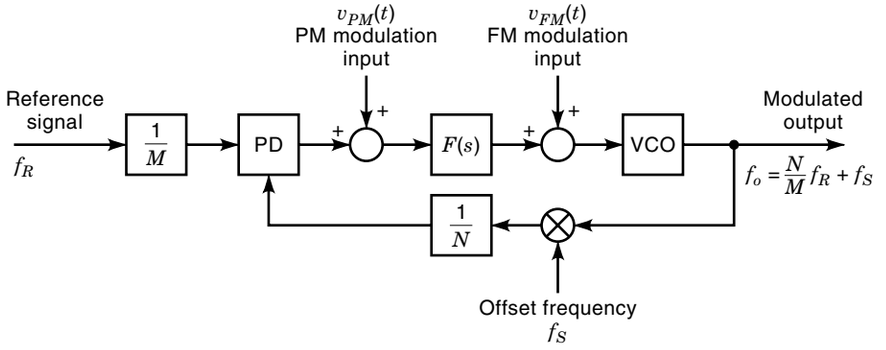

Figure 23. Frequency synthesis by PLL.

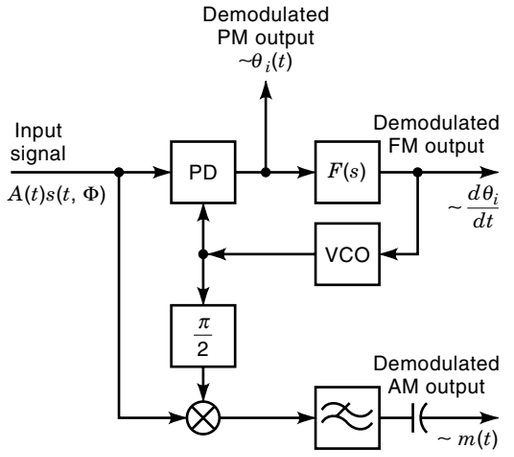

Figure 24. Coherent PM, FM and AM demodulation by APLL.

detector. In this case, the PD output signal is given by

$$\tilde{V}_d(s) = [1 - H(s)]AK_d\tilde{\theta}_i(s) \tag{79}$$

where $\tilde{\theta}_i(s)$ denotes the input PM and AK_d is the gain of the PM demodulator. The demodulated PM signal is multiplied by the closed-loop error function which has a high-pass characteristic. Distortion can be avoided if the closed-loop bandwidth is less than the lowest modulation frequency. The other source of distortion is the PD nonlinearity. This type of distortion does not appear if the total variance of the phase error given by Eq. (62) remains small enough.

FM Demodulator. Assume that a frequency modulated input signal is applied to a PLL. If the phase-locked condition is maintained, then the VCO frequency follows the incoming frequency. Since the VCO frequency is proportional to the VCO control voltage, the FM modulation may be recovered from the VCO control voltage. By means of the transfer function concept, one may write

$$\tilde{V}_c(s) = H(s)\frac{1}{K_v}s\tilde{\theta}_i(s) \tag{80}$$

where $1/K_v$ is the gain of FM demodulator. This equation shows that the FM demodulator output, that is, the VCO control voltage, is proportional to the input FM if the closed-loop bandwidth exceeds the highest modulation frequency.

The distortion caused by the PD nonlinearity is reduced by feedback so the PD distortion is not critical. However, the VCO transfer characteristic must be linear, in order to get an FM demodulator with low distortion.

AM Demodulator. Let the input signal be amplitude modulated

$$x(t) = [1 + m(t)]\sqrt{2}A_0 \sin(\omega_i t + \theta_{i0}) \tag{81}$$

where $m(t)$ carries the information to be transmitted, and A_0, ω_i and θ_{i0} are constants. The PLL demodulator contains a carrier recovery circuit (see the PLL in Fig. 24) and an AM demodulator (see the analog multiplier and low-pass filter in Fig. 24). Since the PLL needs an input signal to be tracked continuously, the spectrum of the AM signal must contain a carrier component.

If the carrier is recovered by an ideal second-order PLL, then the VCO output is

$$r(t, \hat{\Phi}) = \sqrt{2}V_o \cos(\omega_i t + \theta_{i0}) \tag{82}$$

and the difference-frequency output of multiplier

$$A_0V_o[1 + m(t)] \tag{83}$$

contains the demodulated signal $m(t)$; A_0V_o is the gain of the AM demodulator.

Suppressed Carrier Recovery Circuits

In digital telecommunications, the optimum detection of transmitted data requires that both the carrier and clock signals be available at the receiver (15). The carrier and clock recovery circuits are used to retrieve these signals from the noisy incoming waveform.

In order to maximize the power efficiency, modern digital modulation techniques suppress the carrier completely, that is, all transmitted energy resides in the data sidebands. Narrowband PLLs cannot be used for carrier recovery, because the carrier frequency is missing from the input spectrum.

The missing carrier frequency component can be regenerated by nonlinear circuits called *regenerators.* The regenerator can be placed before the narrowband PLL as an entirely separate circuit, or it may be included in the loop. Examples for the first and second solutions are the squaring and Costas loops, respectively.

Many factors have to be considered during the selection and development of a suppressed carrier recovery circuit (20). Here, only the basic operating principles of these circuits is surveyed. Interested readers may find a discussion of the carrier recovery problem in the literature (7,10,20,41–43).

For the sake of simplicity, only *binary phase shift keying* (BPSK) modulation shall be considered here. In BPSK, the binary information to be transmitted is mapped to the phase of a sinusoidal carrier. If the data bit is a "1", the phase of the carrier is zero; while if the data bit is a "0", the carrier phase becomes $-180°$. If the probabilities of 1s and 0s are equal, then the carrier is completely suppressed. In the noise-free case, the received signal can be expressed in the form

$$v_i(t) = m(t)\sin(\omega_i t + \theta_i) \tag{84}$$

where ω_i is the carrier frequency and the carrier phase θ_i is arbitrary but constant. The binary data stream is given by $m(t)$. From the carrier recovery problem of view, the *intersymbol interference* (ISI) problem (20) can be disregarded, that is, we may assume $m(t) = \pm 1$. Three basic types of carrier recovery circuits will be discussed in the following: the *squaring loop,* the *Costas loop* and the *inverse modulator.*

Squaring Loop. In this case, the nonlinear operation is performed by a square-law device, that is, a frequency doubler circuit. As shown in Fig. 25, the nonlinear operation precedes

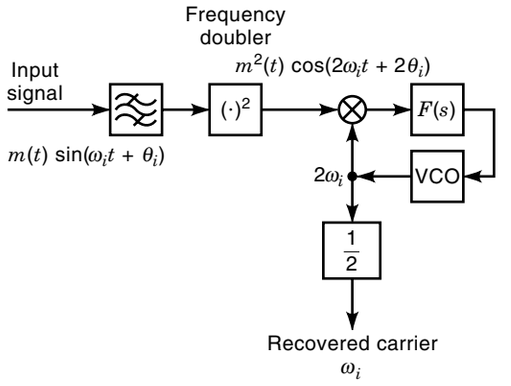

Figure 25. Suppressed carrier recovery by squaring loop.

the narrowband PLL. From Eq. (84) the output of frequency doubler circuit is obtained:

$$v_x(t) = v_i^2(t) = \frac{1}{2}m^2(t)[1 - \cos(2\omega_i t + 2\theta_i)] \tag{85}$$

Taking into account that $m(t) = \pm 1$, that is, $m^2(t) = 1$ one may write

$$v_x(t) \sim \cos(2\omega_i t + 2\theta_i) \tag{86}$$

Equation (86) shows that, after the frequency doubler, a conventional narrowband PLL can be used to recover the second harmonic of the carrier. Finally, the double-frequency output of the PLL is frequency divided by two, in order to recover the original carrier signal.

Costas Loop. In the squaring loop the nonlinear operation is performed in the RF band. The Costas loop offers an alternative solution, where the BPSK modulation is removed in the baseband.

The block diagram of Costas loop is shown in Fig. 26. The circuit contains *in-phase* (*I*-arm) and *quadrature* (*Q*-arm) channels and an analog multiplier, that is, a phase detector that precedes the loop filter. The *I*- and *Q*-arms consist of an analog multiplier and a low-pass filter.

To understand the operation of Costas loop, assume that the phase-locked condition has been achieved and that the VCO output is

$$2\cos(\omega_i t + \theta_o) \tag{87}$$

The output of the low-pass filters in the *Q*- and *I*-arms are $m(t)\sin(\theta_i - \theta_o)$, and $m(t)\cos(\theta_i - \theta_o)$, respectively. Taking into account that $m^2(t) = 1$, one may express the output of the baseband multiplier as

$$\frac{1}{2}m^2(t)\sin[2(\theta_i - \theta_o)] \sim \sin(2\theta_e) \tag{88}$$

By comparing Eqs. (10) and (88) we conclude that, in the noise-free case, the output of the baseband multiplier in a Costas loop is equal to the PD output of a conventional APLL. The only difference is that the phase error is multiplied by a constant of two that results in a higher PD gain.

In addition to carrier tracking, the Costas loop demodulates the incoming BPSK signal. If the phase error is small, then the output of the low-pass filter in the *I*-arm becomes

$$m(t)\cos(\theta_i - \theta_o) \approx m(t) \tag{89}$$

Inverse Modulator. Two slightly different versions of an inverse modulator or remodulator can be found in the literature (10). The terms "inverse modulator" and "remodulator" are used interchangeably and indiscriminantly. As an example, the operation of an inverse modulator is discussed here.

The block diagram of an inverse modulator contains demodulator and modulator circuits, as shown in Fig. 27. Assume that the PLL involved has achieved the phase-locked condition and that the VCO output is

$$2\cos(\omega_i t + \theta_o) \tag{90}$$

Then the output of the demodulator can be expressed as

$$m(t - t_d)\cos(\theta_i - \theta_o) \tag{91}$$

where $(\theta_i - \theta_o)$ is the phase error of the PLL and t_d denotes the time delay of the low-pass filter involved in the demodulator. This demodulated signal modulates the recovered carrier in the modulator and produces an output

$$2m(t - t_d)\cos(\theta_i - \theta_o)\cos(\omega_i t + \theta_o) \tag{92}$$

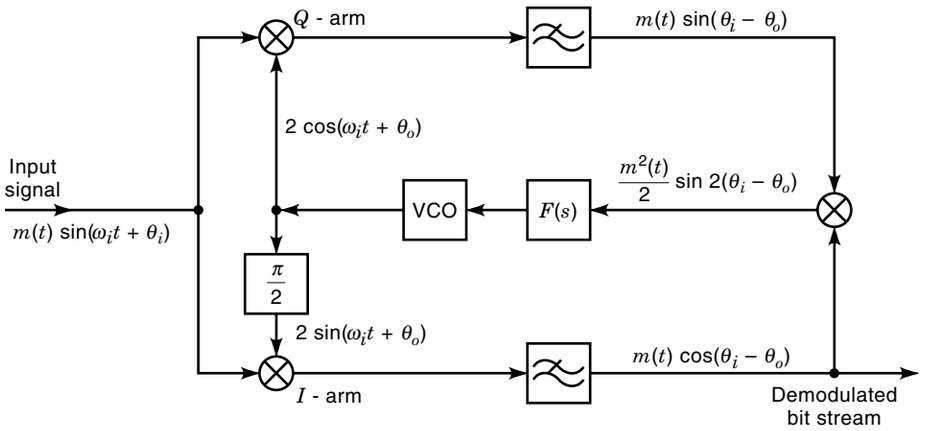

Figure 26. Demodulation of BPSK signal by Costas loop.

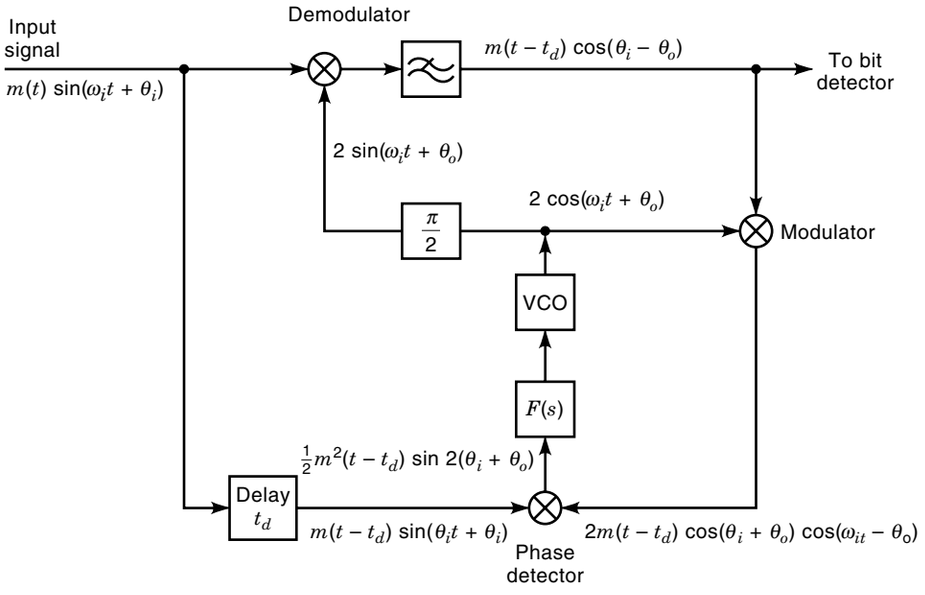

Figure 27. Block diagram of the inverse modulator.

which is multiplied in the phase detector by the delayed input signal $m(t - t_d)\sin(\omega_i t + \theta_i)$. The input signal has to be delayed, in order to cancel the effect of the delay in the demodulator.

Neglecting the sum frequency component the PD output is obtained:

$$m^2(t - t_d)\cos(\theta_i - \theta_o)\sin(\theta_i - \theta_o) \sim \sin(2\theta_e) \tag{93}$$

As in Eq. (88), this signal can be considered as the PD output of an equivalent PLL. Observe that if the phase error is small enough, then the demodulator output is equal to $m(t)$.

Clock Recovery Circuit

In addition to the carrier, the timing information, that is, the clock signal, also has to be recovered in the digital telecommunication systems (7,20). There are two basic classes of clock recovery circuits, but a PLL can be recognized behind both solutions.

The clock frequency component is regenerated from the incoming signal via some nonlinear operation in the first class of clock recovery circuits. These approaches offer the simplest solution, but their performance is only suboptimal. Note that these solutions are analogous to the squaring loop used in suppressed carrier recovery. Examples for these circuits are the cross-symbol synchronizer (44) and the squaring loop symbol synchronizer (45).

The other class of clock recovery circuits is based on *maximum a posteriori estimation* (MAP) techniques (7,46). Many variants of this technique are currently used; they differ mainly in the phase, that is, clock error, detector characteristics. The operation of the early-late gate clock recovery circuit (47), as an example, will be discussed here.

The block diagram of the early-late gate clock recovery circuit is shown in Fig. 28. The circuit contains a pair of gated integrators called *early* and *late* gates, each performing its integration over a time interval of $T/2$ s. The input bit stream is

$$\sum_n a_n p(t - nT) \tag{94}$$

where T is the symbol duration and $p(t)$ denotes a rectangular pulse width duration T. Integration by the early and late

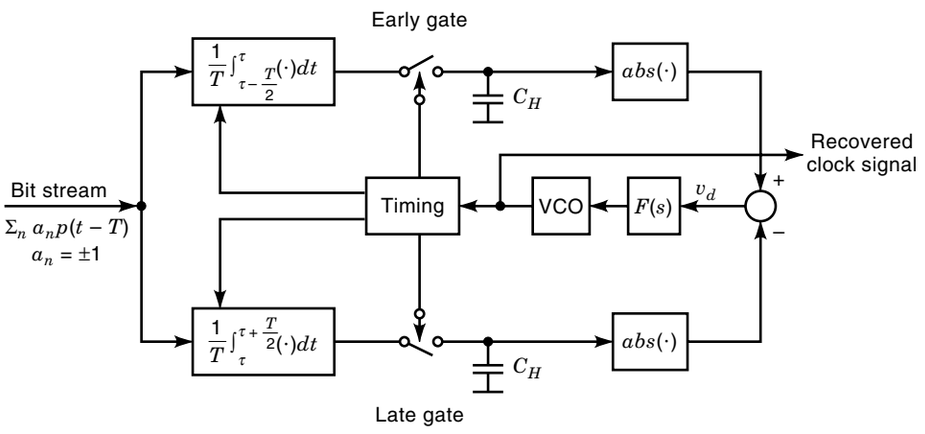

Figure 28. Block diagram of the early-late gate clock recovery circuit.

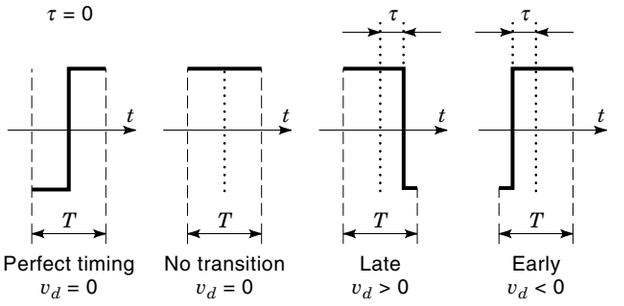

Figure 29. Typical waveforms in the early-late gate clock recovery circuit.

gates are performed during the $T/2$ s, just before and after, respectively, the estimated location of data transition. Gate intervals adjoin each other, but do not overlap.

Waveforms helping to understand the operation of clock recovery circuit are shown in Fig. 29. If the timing error is zero, then the data transition falls just on the boundary between the operation of the early and late gates. In this case, the estimated and incoming data transitions coincide with each other, and the output of the two integrators, stored in the hold capacitors C_H, are equal. As a result, the error voltage $v_d(t)$ becomes zero.

Because the error voltage is produced from the absolute values of the integrator outputs, it is also zero if the data transition is missing.

If a transition of input data does not coincide with the estimated time instant of a transition, then a timing error denoted by τ in Fig. 29 appears. In this case, the data transition falls not on the boundary of operation of the early and late gates, but occurs within the operation interval of one or other gates as shown in Fig. 29. Since the input signal changes its polarity during the gate operation, the associated integration reaches a smaller magnitude than for the other gate, where a transition does not occur. Comparing the magnitudes of the two integrators gives the error voltage $v_d(t)$, which can be used after low-pass filtering to control the VCO frequency.

PHASE DETECTORS

The loop component that has the greatest influence on the performance of a PLL is the phase detector. There are many types of phase detectors, each having its own special benefits. Some can be used at very high frequencies; others may operate in a noisy environment. Different types of phase detectors are used in various applications in order to obtain the best performance. In this section, we consider the most important characteristics of a PD and discuss commonly used PD configurations.

It has been shown that the gain of the phase detector K_d [or AK_d, in the sinusoidal APLL, see Eq. (10)] has a direct influence on every PLL parameter from the quiescent value of the phase error to the noise bandwidth. In the majority of applications, these parameters have to be kept constant, even if the amplitude of the incoming signal varies. However, the product AK_d appears in the loop equations for certain phase detectors, in which case all of the loop parameters depend on the input amplitude. In these cases, an AGC or limiting circuit may be needed before the phase detector, in order to keep the input amplitude constant.

If one plots the PD output voltage against the phase error, two important PD characteristics can be observed. The phase range over which the feedback is negative in the loop is limited. Furthermore, the region over which the linear approximation is valid for the PD limits the maximum of allowable excursion of the phase error in many applications. The sizes of these regions are different for different phase detectors.

Many phase detectors implemented by digital circuitry are edge-triggered circuits. In certain applications, the phase detector must operate in very noisy environment. However, edge-triggered PDs are intolerant of missing or extra signal transitions. This transition-sensitive property makes the use of edge-triggered PDs impossible if the input SNR is low.

In addition to the desired dc voltage, a periodic signal appears at the output of the PD under phase-locked condition. This periodic signal is attenuated, but cannot be completely suppressed by the low-pass filter included in the phase detector and the loop filter. The periodic signal getting through to the VCO input causes unwanted frequency modulation of the output signal, that is, sidebands appear. These sidebands are especially unwelcome in frequency synthesizer applications.

Earlier it was mentioned that the PLL acquisition consists of frequency and phase pull-in processes. In higher-order PLLs, the pull-in time can be extremely long; worse still, for many loop configurations there is no guarantee that the phase-locked condition will be reached. This problem can be overcome by means of a *phase-frequency detector,* which operates as a phase detector under phase-locked condition, but provides a frequency-sensitive signal to aid frequency pull-in when the loop is out of lock.

Certain types of phase detectors, like a high-speed sampler, can be used in the extremely high-frequency region, while others, such as the sample-and-hold phase detector, may operate up to about 1 MHz. The *operating frequency region* is another important PD characteristic.

From an operation point of view, one must distinguish between analog and edge-triggered phase detectors. In edge-triggered circuits, the information is transmitted only at discrete-time instants. Examples of edge-triggered phase detectors are the RS flip-flop, sample-and-hold phase detector, and phase-frequency detector. Digital frequency dividers used in the feedback path are also edge-triggered circuits. If a PLL contains edge-triggered circuit(s) then an integro-difference equation is required to model its operation correctly. However, if the closed loop bandwidth of the PLL is less than one-tenth of the input frequency, then the continuous-time approximation can be used, that is, the APLL theory may be applied (26).

In addition to phase detectors, many other loop components are used in various PLL applications, from frequency dividers to VCO circuits. Discussion of these loop components goes beyond the scope of this article; the interested readers should consult the literature. The components of the APLL are surveyed in (10); for the components of frequency synthesizers, see (36–39); the building blocks of digital PLLs are discussed in (48).

Gardner has distinguished in (10) two basic categories of phase detectors: the *multiplier-type* and *sequential* circuits.

The multiplier-type phase detector determines the product of the input and VCO waveforms. The PD output, which is

used as an error signal in the PLL, is the average value of this product. These circuits have no memory and they can operate in very noisy environments.

The output of a sequential phase detector is proportional to the time interval between the zero crossings of the input and VCO waveforms. The information is carried by the position of signal transitions; other details of waveforms have no influence on the PD output. These detectors contain a memory of past crossing events. Since these phase detectors are controlled by the signal transitions, missing or extra edges disturb their operation. In general, they are more sensitive to noise then multiplier-type phase detectors.

Multiplier-Type Phase Detectors

Four-Quadrant Analog Multiplier. Four-quadrant analog multipliers can be used as multiplier-type phase detectors (10). Assume that the PD inputs are sine and cosine waveforms. Then the output of the four-quadrant analog multiplier can be expressed as

$$v_d = AK_d[\sin\theta_e + \sin(2\omega_0 t + \theta_e)] \tag{95}$$

where ω_0 is the frequency of two inputs, $V_o = K_d$, A and V_o denote the RMS amplitude of the input signals.

Equation (95) shows the disadvantages of the circuit. In addition to the phase error, the PD output also depends on the amplitudes of the input signals. This means that the steady-state phase error θ_{ss}, the stability, and every closed-loop parameter vary with A. Furthermore, an unwanted sinusoidal signal at the second harmonic of the input frequency also appears at the output of the PD, with an amplitude equal to the maximum available dc output. This sinusoidal signal results in unwanted FM at the VCO output.

On the other hand, analog multipliers can be used at very low values of input SNR. This is why they are almost exclusively used in coherent demodulators and suppressed carrier recovery circuits.

Balanced Mixers. Balanced mixers offer another possible implementation of multiplier-type phase detector, which can operate at extremely high frequencies. Monolithic integrated circuits and extremely wideband diode rings can be used even in the microwave frequency region (10). These circuits are also multipliers, where the VCO signal (also called the *local signal*) drives the transistors or diodes into saturation, that is, they operate in switching mode. For the other input, also called the *received signal,* the balanced mixer is linear.

The advantages and disadvantages of balanced mixers and analog multipliers are the same. The only difference is caused by the high level of local signal. Balanced mixers have a so-called local leakage, that is, in addition to the sum-frequency component, the input frequency component also appears at the output of the PD.

Exclusive-OR Gate. The exclusive-OR gate can be considered as a digital implementation of a balanced mixer. The balanced mixer operates as an exclusive-OR gate when it is driven by rectangular waveforms of appropriate amplitude.

The output of an exclusive-OR gate is a square wave, whose duty cycle depends on the phase error. The average value of this square wave is taken to be the PD output.

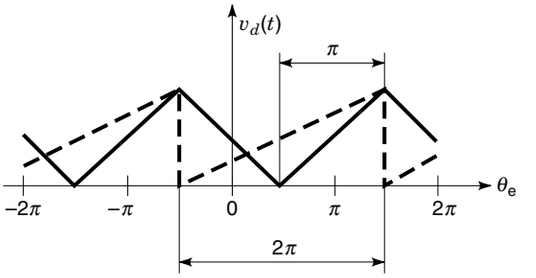

Figure 30. The average output voltage of the exclusive-OR (solid line) and edge-triggered RS flip-flop (dashed line) if they are used as phase detectors. The linear phase regions are marked.

If both inputs have a 50% duty cycle, then the phase detector has a triangular characteristic, as shown in Fig. 30, where the average value of the gate output is plotted against the phase error. The harmonic content of output and the PD characteristic for other duty cycles are given in (39).

The exclusive-OR gate must be driven by standard digital signals, which are not usually available in communications receivers. The high level of periodic output prohibits their use in high-quality frequency synthesis. They are used in digital environments and narrowband loops, particularly when the unwanted output sidebands can be tolerated. They are often used in frequency synthesis, not as the phase detector but as a lock indicator.

High-Speed Sampler. The high-speed sampler is commonly used in frequency synthesis to lock a VCO to an integer multiple of a reference frequency. The high-speed sampler is basically a single-balanced mixer, driven by a narrow pulse on the local input (39). The sampling signal, that is, the stream of narrow pulses, is generated by a step-recovery diode from the reference frequency. For the sampling signal the mixer is balanced. During a pulse, the two diodes of the sampling gate conduct and charge the output capacitors.

The phase detection capability of the high-speed sampler can be understood easily in the frequency domain. Harmonics of the reference frequency are generated by the step-recovery diode and the appropriate harmonic of the reference signal is multiplied by the VCO signal. The difference-frequency component is used as the PD output. The only difference between the high-speed sampler and a harmonic mixer is that there are two hold capacitors in the sampler that enhance the level of the low-frequency PD output.

The main disadvantage of every phase detector, based on sampling, is that any periodic disturbances or noise about any harmonics of the reference, that is, the sampling frequency, are translated to the low-frequency region. All of these signals appear at the PD output as unwanted signals. It must be emphasized that the sampling process also folds a broadband noise floor over many times, aliasing the noise from the vicinity of many harmonics of the sampling frequency to the low-frequency region. This is why sampling-type PDs can be used for reference signals with very high spectral purity; otherwise, a bandpass filter must preceed the PD, in order to reject the unwanted signals.

Sequential Phase Detectors

Edge-Triggered Flip-Flop. The edge-triggered RS flip-flop can be used as a sequential phase detector (39). The input

and VCO signals are connected to the S and R inputs of a flip-flop, respectively. The PD output signal appears at the Q output, which is a square wave; its average value is proportional to the phase difference between the S and R inputs. This phase detector has a sawtooth characteristic, as shown in Fig. 30.

The benefits of the edge-triggered RS flip-flop are: it offers a simple and digital-compatible phase detector; furthermore it has a 2π-wide and linear phase range. The first disadvantage results from its edge-triggered operation; it cannot be used in a noisy environment. The second drawback is that the reference frequency is present in the spectrum of PD output.

Sample-and-Hold Phase Detector. Sample-and-hold phase detectors are often used for frequency synthesis and in *zero-crossing digital phase-locked loops* (ZC-DPLL).

Frequency synthesizers have to produce signals with extremely high spectral purity. The phase detectors discussed so far have a periodic output in their steady-state, which causes unwanted sidebands at the PLL output. The unique feature of the sample-and-hold phase detector is that its output is a pure dc signal under phase-locked condition.

The sample-and-hold PD shown in Fig. 31 is an edge-triggered circuit, that is, a sequential phase detector. Let f_R denote the frequency of the reference signal. The first block generates the sampled signal $v_R(t)$, which is synchronized with the reference signal. The sampled signal may have any shape; assume that it has a sawtooth waveform in our case. Since the PD is edge-triggered, this sawtooth waveform converts the time interval between transitions of the reference and sampling signals into a voltage. The sampling switch is closed at the sampling time instants denoted by t_k, $k = 0, 1, 2, \ldots$ and the voltage of the hold capacitor C_H becomes equal to the instantaneous value of the sampled signal. Note that the voltage $v_d(t)$ of the hold capacitor, which is the PD output, is linearly proportional to the time between transitions of the reference and sampling signals, that is, to the phase error. The capacitor C_H holds this voltage until the next sampling time instant.

The sampling switch can be implemented by an integrated CMOS or discrete FET switch. In both cases, the switch has a series resistance which is modeled by R_S in Fig. 31. Due to R_S, a finite sampling time is required to charge or discharge the hold capacitor. The sampling switch is closed at the sampling time instant t_k and remains closed during the sampling time t_S.

The sampled signal $v_R(t)$ and PD output $v_d(t)$ are plotted by solid and dashed lines, respectively, in Fig. 32. When the sampling switch is closed, the PD output voltage $v_d(t)$ varies exponentially from its previous value to the new one. The time constant $R_S C_H$ of the sampling switch has to be much

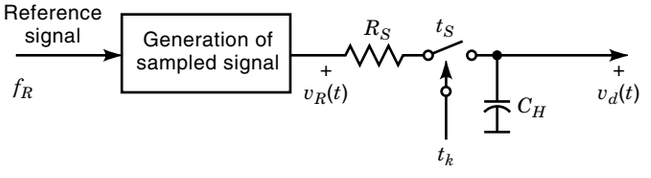

Figure 31. Simplified circuit diagram of sample-and-hold phase detector.

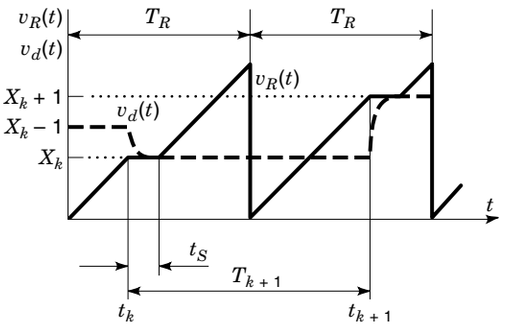

Figure 32. Waveforms in the sample-and-hold phase detector.

less than the sampling time t_S. Note that the sampled signal is kept constant during the finite sampling time t_S. This must be done in order to avoid the appearance of a periodic signal at the PD output in steady-state.

Figure 33 shows the waveforms of sample-and-hold phase detector in steady-state. Since the sampled signal (solid line) is kept constant during the finite sampling time, the PD output (dashed line) becomes a pure dc voltage.

More details on the sample-and-hold phase detector and its design are given in (38) and (39).

Phase-Frequency Detector with Charge Pump. Most of the phase detectors discussed so far have two disadvantages:

1. Since they are not sensitive to the frequency error, their pull-in time can be extremely long.
2. Apart from the sample-and-hold phase detector, they have a periodic steady-state output.

The phase-frequency detector provides a signal that is sensitive to the frequency error during acquisition and operates as a phase detector under phase-locked condition. As shown in Fig. 34, it contains a logic circuit (the phase-frequency detector) and a charge pump circuit, implemented by controlled current sources I_U and I_D. The output of the phase detector is a current $i_d(t)$.

The edge-triggered phase-frequency detector is driven by the reference and frequency-divided VCO signals $s(t)$ and $v_o(t)$, respectively. The logic circuit has two outputs; if one of these is active, then the other output is disabled. If the di-

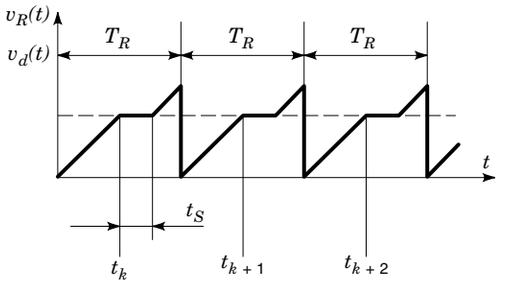

Figure 33. Steady-state waveforms in the sample-and-hold phase detector. Note if the sampled signal $v_R(t)$ (solid line) is kept constant during t_S, then the PD output $v_d(t)$ (dashed line) becomes a pure dc voltage.

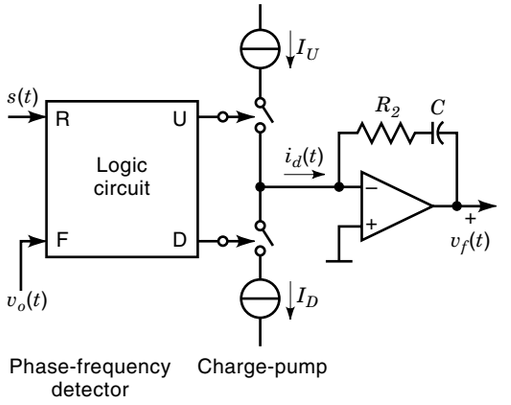

Figure 34. Simplified circuit diagram of phase-frequency detector with charge pump circuit.

vided VCO frequency is greater than the reference frequency, then the U output is active and the D output is zero. In the opposite case, the U output becomes zero and the output signal appears at the D output. The current sources I_U and I_D are controlled by the U and D outputs. Depending on the sign of the frequency error, the PD output contains only positive or negative current pulses. This behavior of the logic circuit provides frequency detection capability for the phase detector.

The output of the logic circuit is a rectangular pulse, the duration of which depends on the phase error. The input signals of the phase-frequency detector and the output current of the charge pump circuit are shown in Fig. 35. The PD output current $i_d(t)$ has the following properties:

- The sign of current pulses is determined by the sign of frequency error; and
- The duration of current pulses is proportional to the phase error.

The VCO control voltage is equal to the output voltage $v_f(t)$ of the charge pump circuit. In steady-state, the VCO output frequency, and hence $v_f(t)$, becomes constant. It can be achieved only if $i_d(t) = 0$, that is, if both the U and D outputs of the logic circuit become zero. It follows from the operation of the phase-frequency detector that in this case the edges of

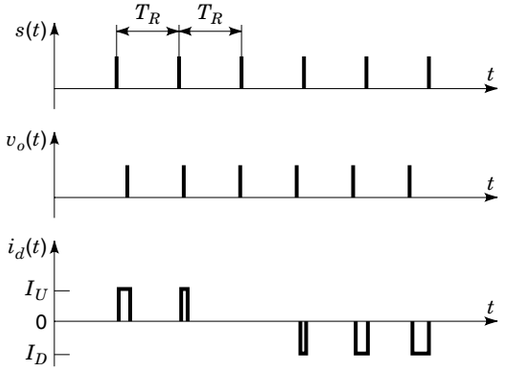

Figure 35. Input signals of the phase-frequency detector and output current of the charge pump circuit.

the reference and divided VCO signals coincide with each other. This means that the steady-state phase error is zero in the charge pump PLL.

The final advantage of the phase-frequency detector is that its linear phase region is 4π.

OTHER PLL CONFIGURATIONS

The operation, baseband model, and analysis of analog PLLs have been discussed earlier. The APLL contains only analog loop components and its operation can be described by a pure differential equation.

Continued progress in the production of digital integrated circuits and the widespread use of digital signal processing have resulted in strong interest in the implementation of PLLs directly in the digital domain. Various implementations of DPLLs contain only digital loop components, that is, their operation can be modeled by a pure difference equation.

In other applications, the circuit configuration requires the use of edge-triggered or digital loop components (e.g., frequency synthesis), or they are used to achieve the best PLL performance (e.g., sample-and-hold phase detector). These PLLs are called hybrid phase-locked loops and their operation can be described by an integro-difference equation.

PLLs are categorized into three basic classes in the literature (14):

1. analog;
2. digital; and
3. hybrid

phase-locked loops. The most important characteristics of PLLs are summarized in Table 4. Sampling and charge pump PLLs belong to the class of hybrid phase-locked loops.

In contrast with the APLL, a general theory does not exist for these circuits. As typical examples, we will discuss the operation of the ZC-DPLL, SPLL and charge pump PLL is this section.

Digital Phase-Locked Loops

Various circuit configurations have been proposed by different authors for the implementation of the DPLL concept. Lindsey and Chie (48) have grouped the implementations into four classes, according to the operation of their phase detectors:

1. *Flip-Flop (FF)-DPLL,* in which a positive zero-crossing of the input signal sets a flip-flop circuit and the local clock resets it. The phase error is derived from the elapsed time between the set and reset time instants.
2. *Nyquist Rate (NR)-DPLL,* in which the input signal is sampled at the Nyquist rate.
3. *Lead / Lag (LL)-DPLL,* in which the PD determines at each cycle, whether the input leads or lags the local clock signal.
4. *Zero crossing (ZC)-DPLL,* in which the loop tracks the zero crossings of the incoming sinusoidal signal.

In this section, as an example, only the theory of ZC-DPLL is surveyed. This DPLL configuration is the easiest to model

Table 4. Most Important Characteristics of Phase-Locked Loops

Type of PLL	PD	Loop Filter	VCO	Loop Equation
APLL	Analog multiplier	Analog	Analog	Pure differential
ZC-DPLL	Ideal sampler	Digital	Digital	Pure difference
SPLL	Sample-and-hold	Analog	Analog	Integro-difference
Charge-pump PLL	Phase-frequency detector with charge pump	Analog	Analog	Integro-difference

The hybrid PLL comprises the SPLL and charge pump PLL.

and analyze; however, its operation is indicative of the general behavior of any DPLL.

The block diagram of ZC-DPLL proposed by Natali (49) is shown in Fig. 36. In the following equations, the time variable t is again suppressed for conciseness, where it does not cause misunderstanding.

Let the incoming signal be

$$s(t) = \sqrt{2}A\sin(\omega_R t + \theta_i) \tag{96}$$

where ω_R is the center frequency, that is, the carrier frequency of $s(t)$, and $\theta_i(t)$ denotes the input phase modulation. The incoming signal is corrupted by bandpass filtered Gaussian white noise $n_i(t)$. The signal $s(t) + n_i(t)$ is sampled by an ideal sampler (i.e., $R_S = t_S = 0$) at the sampling time instants t_k, $k = 0, 1, 2, \ldots$, the samples are held by C_H and converted to a digital signal x_k by an *analog-to-digital converter* (ADC). The incoming signal, sampling time instants and output of the ADC are plotted in Fig. 37 for the noise-free case.

In order to express the phase error, the sampling time instants determined by the digital clock have to be mapped to the phase of an equivalent sinusoidal signal. Let t_k be assigned by the positive zero-crossings of the equivalent sinusoidal signal characterized by its phase $\omega_R t + \theta_o(t)$. Then the positive zero-crossings

$$\omega_R t_k + \theta_o(t_k) = \omega_R t_k + \theta_{ok} = 2\pi k \tag{97}$$

that is, the sampling time instants, can be expressed as

$$t_k = \frac{2\pi k - \theta_{ok}}{\omega_R} \tag{98}$$

where $\theta_{o0} = 0$ and $k = 0, 1, 2, \ldots$. Knowing the sampling time instants, one may express the output of the ADC as

$$x_k = \sqrt{2}A\sin(\omega_R t_k + \theta_{ik}) + n_{ik} = \sqrt{2}A\sin\theta_{ek} + n_{ik} \tag{99}$$

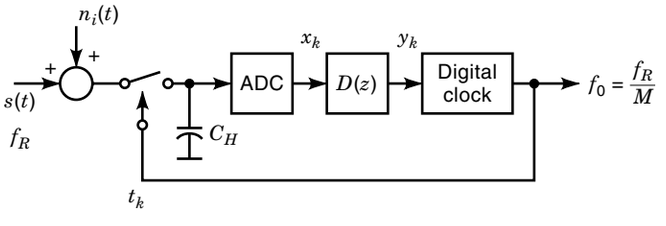

Figure 36. Block diagram of the ZC-DPLL.

where $\theta_{ek} = \theta_{ik} - \theta_{ok}$ is the phase error. The output of the digital loop filter is

$$y_k = D(z)x_k = D(z)(\sqrt{2}A\sin\theta_{ek} + n_{ik}) \tag{100}$$

The time elapsed between the $(k-1)th$ and kth samples is denoted by

$$T_k = t_k - t_{k-1}, \qquad k = 1, 2, 3, \ldots \tag{101}$$

and the output of the digital filter is used to control the next period of a digital clock, according to the algorithm

$$T_k = T - y_{k-1} = T - z^{-1}D(z)(\sqrt{2}A\sin\theta_{ek} + n_{ik}) \tag{102}$$

In Eq. (102), T is the nominal clock period that can be M/f_R, $M = 1, 2, 3, \ldots$. For $M = 1$, the ZC-DPLL takes samples at every positive zero crossing of the incoming signal, while $M > 1$ indicates subharmonic locking.

Let f_o denote the PLL output frequency. Subharmonic locking, that is, $f_o = f_R/M$, $M = 2, 3, 4, \ldots$ may occur in every PLL where a sampling phase detector is used. Subharmonic locking means that the PD takes one sample at every Mth period of $s(t)$. For the sake of simplicity, it will be assumed that $M = 1$ in this section.

The difference between the kth and $(k-1)th$ phase error samples is

$$\theta_{ek} - \theta_{ek-1} = \theta_{ik} - \theta_{ik-1} - (\theta_{ok} - \theta_{ok-1}) \tag{103}$$

similarly, from Eq. (97) one may get

$$\theta_{ok} - \theta_{ok-1} = 2\pi - \omega_R(t_k - t_{k-1}) = 2\pi - \omega_R T_k \tag{104}$$

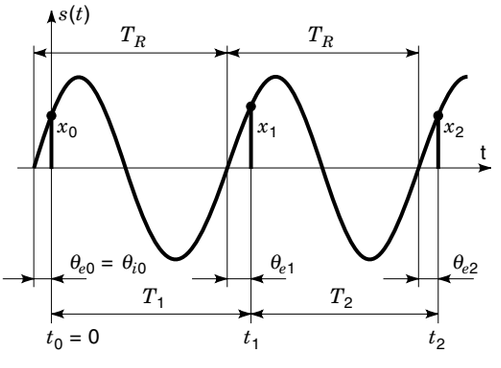

Figure 37. Waveforms of a ZC-DPLL in absence of noise.

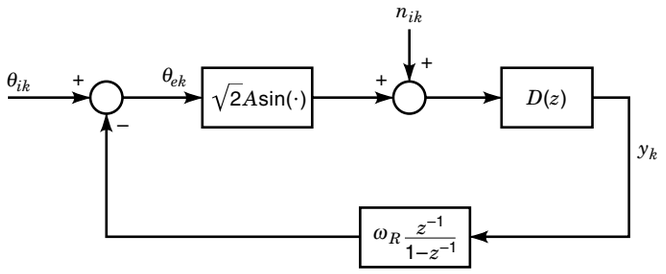

Figure 38. Nonlinear baseband model of ZC-DPLL.

If $M = 1$, then $T = 2\pi/\omega_R$. Using the unit delay operator z^{-1} and substituting Eq. (102) into Eq. (104) and the result into Eq. (103), one gets the loop equation

$$\theta_{ek} = \theta_{ik} + \omega_R \frac{z^{-1}}{1 - z^{-1}} D(z)(\sqrt{2}A \sin\theta_{ek} + n_{ik}) \tag{105}$$

which is a nonlinear stochastic difference equation.

In Eq. (105), the unit delay operator appears. Sometimes it is claimed that the z-transform can be used only in case of uniform sampling. Here is used the definition of z^{-1} given in (50), which is valid for arbitrary time sequences. In the ZC-DPLL and SPLL (see next section), the sampling time instants are varied; this is how the feedback is used to control the operation of the loop.

From Eq. (105), a nonlinear baseband model of the ZC-DPLL can be constructed. The model is shown in Fig. 38, where $\omega_R z^{-1}/(1 - z^{-1})$ denotes the transfer function of digital clock. Note that the baseband models of the analog (see Fig. 3) and digital PLLs are structurally equivalent.

Linear and nonlinear theories of DPLLs are surveyed in (48); the stability of the ZC-DPLL is analyzed in (51) and (52). Interested readers are referred to these papers.

Sampling Phase-Locked Loop

A block diagram of the SPLL is shown in Fig. 39. The sinusoidal reference signal $s(t)$ corrupted by noise $n_i(t)$ synchronizes a sawtooth waveform in the phase detector. The sampled signal $v_R(t)$ is kept constant during the finite sampling time t_S, as shown in Fig. 32. The PD output $v_d(t)$ is an *analog signal* that is processed by an analog loop filter $F(s)$. The instantaneous VCO frequency is controlled by $v_c(t)$ and is divided by a frequency divider; the division ratio is N. The sampling time instants t_k are determined by the frequency divider output.

The waveforms of the sample-and-hold phase detector are shown in Fig. 32. Let x_k denote the value of the sampled signal at t_k and assume that $R_S C_H \ll t_S$. While the sampling switch is closed, the PD output voltage $v_d(t)$ varies from x_{k-1} to x_k. In the time interval $(t_k + t_S, t_{k+1})$ the sampling switch is open, that is, $v_d(t) = x_k$.

Here only the course and milestones of SPLL analysis are discussed. The equations will be given only for the simplest case, when $F(s) = A_0$. The details of SPLL theory and many design equations can be found in (53).

The development of a baseband model for the SPLL can be divided into three main steps:

1. First, the synchronization of $v_R(t)$ with the noisy reference signal has to be modeled.
2. Then, the next sampling time instant t_{k+1} has to be determined.
3. Finally, all signals have to be generated in the continuous-time domain.

Let ω_R, φ_{R0} and $\hat{\theta}_R(t)$ denote the frequency, phase, and phase modulation of the reference signal

$$s(t) = \sqrt{2}V_R \sin[\omega_R t + \varphi_{R0} + \hat{\theta}_R(t)] \tag{106}$$

The synchronization of $v_R(t)$ is edge-triggered, that is, a new voltage ramp is started when the noisy reference signal becomes zero. Thus,

$$s(t_n) + n_i(t_n) = 0 \tag{107}$$

where t_n, $n = 0, 1, 2, \ldots$ denotes the starting time instants of voltage ramps. In the general case, the synchronization and sampling are independent of each other. Note that the value of the sampled signal at t_k depends on two variables n and k, where n describes the synchronization, while k appears due to sampling. A baseband model for the general case cannot be developed.

Because of sampling, subharmonic locking is also possible. Assume that one sample is taken in every Mth reference period, that is, the output frequency is

$$f_o = \frac{N}{M} f_R \tag{108}$$

It has been shown in (53) that if cycle slip does not occur, then one may write

$$n = Mk \tag{109}$$

and the independent variable n can be canceled from the equations. Then the sampled signal at t_k can be expressed as

$$x_k = v_R(t_k) = g(\theta_{ek}) \tag{110}$$

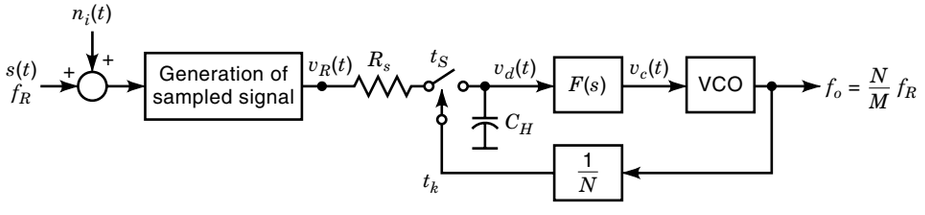

Figure 39. Block diagram of SPLL. A frequency divider with a division ratio of N has been placed in the feedback path.

where the nonlinear periodic function $g(\cdot)$ describes the shape of sampled signal and θ_{ek} is the phase error

$$\theta_{ek} = \theta_{Rk} - \frac{M}{N}\theta_{ok} \tag{111}$$

In Eq. (111), θ_{ok} is the output phase modulation and the equivalent input phase modulation θ_{Rk} involves the effects of both noise and phase modulation of the reference signal

$$\theta_{Rk} = \varphi_{R0} + \hat{\theta}_R\left(kMT_R - \frac{\varphi_{R0}}{\omega_R}\right) + \frac{1}{\sqrt{2}V_R}n_i\left(kMT_R - \frac{\varphi_{R0}}{\omega_R}\right) \tag{112}$$

Let $T_{k+1} = t_{k+1} - t_k$ denote the time between two adjacent sampling time instants. Then following the method shown earlier for the ZC-DPLL, one may express the phase error as

$$\theta_{ek} = \theta_{Rk} - \omega_R\frac{z^{-1}}{1-z^{-1}}(MT_R - T_{k+1}) \tag{113}$$

The main difference between the ZC-DPLL and SPLL circuits is in the signal processing technique by which the next sampling time instant t_{k+1} is determined. In the SPLL, the PD output is an analog voltage and is processed by the analog loop filter and VCO circuits.

Note that the time interval T_{k+1} can be divided into two distinct periods; from t_k to $t_k + t_S$ the sampling switch is closed, while from $t_k + t_S$ to t_{k+1} the sampling switch is open. This means that the topology of the SPLL is changed at t_k and $t_k + t_S$. Since the VCO output is a sinusoidal signal and the frequency divider is edge-triggered, the variation in the VCO phase is $2\pi N$ between t_k and t_{k+1}. Let ω_0 denote the VCO center frequency. Then the variation in the VCO phase can be expressed as

$$\int_{t_k}^{t_{k+1}}[\omega_0 + K_v v_c(t)]\,dt = \omega_0 T_{k+1} + K_v\left[\int_{t_k}^{t_k+t_s} v_c(t)\,dt + \int_{t_k+t_s}^{t_{k+1}} v_c(t)\,dt\right] \equiv 2\pi N \tag{114}$$

The determination of t_{k+1} requires the solution of the integro-difference equation given by Eq. (114).

Equation (114) cannot be solved in closed form, it must be separated into a pure difference and a pure differential equation. Kolumbán has shown that this separation can be performed in three cases (53):

1. If the dominant time constant of the open loop transfer function is much less than t_S;
2. If the dominant time constant of the open loop transfer function is much greater than T_k; and
3. If the SPLL remains in the neighborhood of equilibrium during the operation.

Fortunately, at least one of these conditions is almost always valid in practice.

For example, consider the case when the loop filter is omitted, that is, $F(s) = A_0$. In this case, the dominant time constant is $R_S C_H$, which is much less than t_S. The elapsed time between two adjacent sampling time instants can be expressed as

$$T_{k+1} = \frac{2\pi N + A_0 K_v (x_k - x_{k-1}) R_S C_H}{\omega_0 + A_0 K_v x_k} \tag{115}$$

The outputs of the SPLL are analog signals. Equations (113) and (110) give the sampled signal at the sampling time instants only; the analog signals have to be expressed in terms of x_k. It has been shown in (53) that the PD output voltage $v_d(t)$ can be generated from x_k by means of a zero-order hold circuit and an RC low-pass filter as shown in Fig. 40. It must be emphasized that the sampling is not uniform in the SPLL, that is, the hold time of the zero-order hold circuit varies during its operation.

The nonlinear baseband model of the SPLL can be constructed from Eqs. (113) and (110). Then the discrete-time signal x_k is converted to the continuous-time domain by a zero-order hold circuit as shown in Fig. 40. The time interval T_{k+1} can be calculated from Eq. (115) if the loop filter is omitted. Expressions for T_{k+1} for other loop configurations can be found in (53).

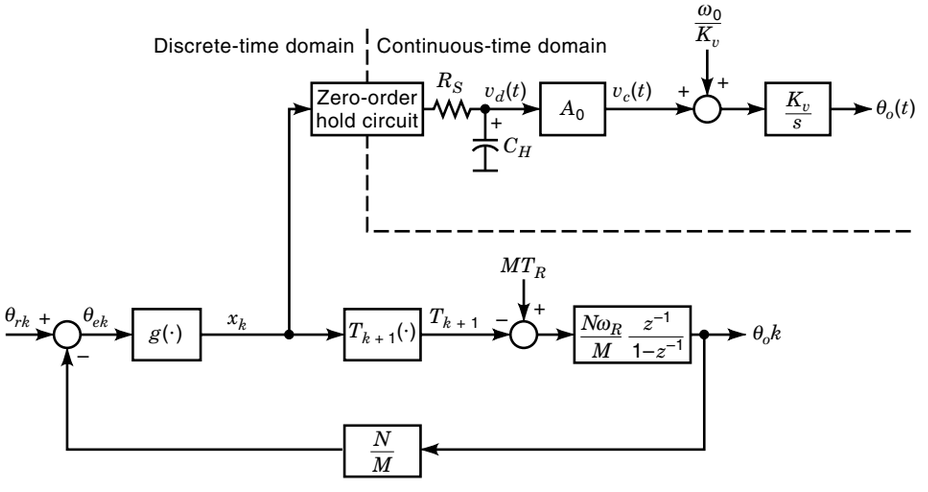

Figure 40. Nonlinear baseband model of SPLL. The dashed line separates the discrete- and continuous-time domains.

SPLLs are used primarily in frequency synthesis, because they offer excellent spectral purity. Due to their discrete-time operation, the frequency switching time can be minimized if all poles of closed-loop transfer function are placed as close to the origin in the z-plane as possible (54). The SPLL can be also used as an FM or PM modulator (55). This section has shown only the main steps of SPLL analysis; a complete analysis in the frequency domain is given in (40). The SPLL is especially suited to applications where a very simple high-performance synthesizer is required (56).

Charge-Pump Phase-Locked Loop

Charge pump PLLs are widely used for frequency synthesis, since

- their phase-frequency detector is sensitive to both phase and frequency errors; and
- they are available as cheap integrated circuits.

The block diagram of a charge pump PLL is shown in Fig. 41. The operation of the phase-frequency detector has been discussed earlier. The PD output $i_d(t)$ charges or discharges the capacitor C. The resistor R_2 introduces a zero into the open-loop transfer function, that is, it ensures the stability of the loop. Charge pump PLLs are widely used in frequency synthesis, normally with a frequency divider with division ratio N in the feedback path.

Depending on the phase and/or frequency error, $i_d(t)$ charges or discharges C. The VCO control voltage $v_c(t)$ is determined by the capacitor voltage. If the reference signal is unmodulated, then, in steady-state, $v_c(t)$ is a dc voltage, that is, the charge stored on C should be constant. This will happen only if $i_d(t) = 0$, that is, current pulses do not appear at the PD output in steady-state. Fortunately, if there are no current pulses at the PD output in steady-state, then unwanted FM does not appear at the PLL output.

The charge pump PLL contains both edge-triggered and analog circuits, just like the SPLL. By contrast, a baseband model for the charge pump PLL has not yet been published. Gardner has developed a system of nonlinear difference equations in (26), which can be solved numerically to determine the transient response of the loop. The equations have been linearized, in order to perform the stability analysis of the loop. However, the signals can be calculated only in the discrete-time domain; their functions are not expressed in the continuous-time domain.

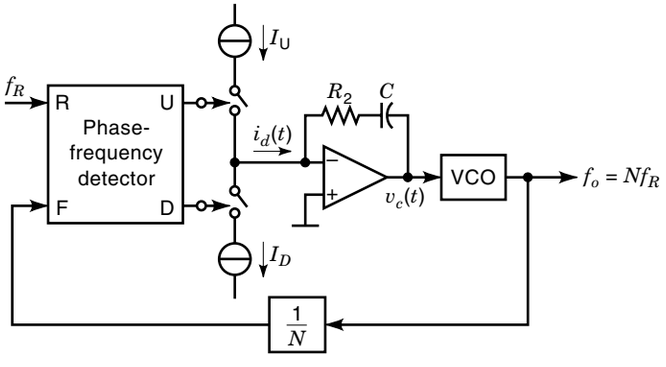

Figure 41. Block diagram of a charge pump phase-locked loop.

Gardner has determined the transient response, using both the continuous-time approximations, that is, the APLL model, and the exact nonlinear difference equations. By comparing the results, he has shown that if the reference frequency f_R exceeds ten times the closed loop bandwidth, then the continuous-time approximation can be used in circuit design (26).

The primary disadvantage of the charge pump PLL, and the reason why it is not suitable for high-quality frequency synthesis, is the so-called *crossover distortion* (39). This means that, compared with its nominal value, the PD gain varies from -20 dB to $+10$ dB if the phase error is reduced below a certain value. This effect appears, due to an internal logic race condition in the digital part of the phase-frequency detector. To avoid instability problems, the phase error has to be pushed out of this region, generally a 1 MΩ resistor is connected in parallel with the series R_2–C circuit. However, this means that the phase error is greater than zero in steady-state, and an unwanted FM appears at the output of every built charge pump PLL.

To exploit the excellent frequency acquisition property of the phase-frequency detector and the high spectral purity offered by the sample-and-hold PD, both phase detectors are implemented on the same integrated circuit. The phase-frequency detector operates during the frequency pull-in and, if the phase error goes below a certain threshold, then the phase-frequency detector is switched off and the sample-and-hold PD is used. In this way, the performance of a frequency synthesizer can be optimized during both the pull-in transient and in steady-state.

CLOSING REMARKS

The goal of this article was to survey the theory and most important applications of phase-locked loops. The main emphasis was put on the APLL theory, because it is the simplest to understand and it is the basis of every other PLL analysis. While the APLL theory has been very well established, the theory of the digital and hybrid PLLs is subject to continuous development. For example, the effect of quantization that appears in DPLLs was neglected in this article. Gardner has shown that the quantizing nonlinearity leads to a limit cycle under the phase-locked condition (57).

A new model which can describe the transient behavior of the charge pump PLL even if it is not locked has been developed in (58).

Clock generation and distribution is a very important problem in high performance microelectronics. This question is discussed in (59,60).

The clock recovery circuit is one of the key elements of digital data communication equipment. It is hard to find the optimum trade-off between acquisition, tracking, and noise properties. A systematic design and optimization procedure has been proposed in (61).

Last but not least it must be emphasized that another article in this encyclopedia has been devoted to the latest results on applications of PLLs.

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See also FREQUENCY SYNTHESIZERS.