CIRCUIT STABILITY OF DC OPERATING POINTS

To some readers it might seem incongruous that we refer to the notion of stability in the context of dc circuits, but that is exactly what this article is about. Numerous observations have been made, dating back at least to the turn of the century (1,2), that stability related properties seem to be embodied in dc circuits. In 1965 Stern (3) wrote:

> Mathematically speaking, there is no basis for discussing stability in resistive networks, since they are not described by differential equations. Physically, however, it is well known that in a resistive network with multiple states of equilibrium some of these states are usually unstable. Thus some dynamic mechanism of instability must exist in the network.

Only during the past few years has the issue been formulated in a manner that permits adequate insight into its character such that a rigorous theory has begun to emerge. A major stride forward was announced in (4), and subsequent work has yielded further results. The problem of assessing the stability of each operating point of a nonlinear dc circuit is still not completely solved. Much basic understanding has been attained, however, and this article is intended as a survey of that knowledge. We begin with several important definitions.

FUNDAMENTAL DEFINITIONS

Equilibrium Points vs. Operating Points

We will first make a clear distinction between a circuit's *equilibrium point* and its *operating point.* In any dynamic system described by a set of differential equations

$$\frac{dx}{dt} = f(x) \tag{1}$$

where $x \in R^n$ and $f : R^n \to R^n$, the set of equilibrium (or singular) points is defined to be $\{x : f(x) = 0\}$. When we refer to an equilibrium point it is within this context of a given dynamic system. When the dynamic system is an electric circuit the derivative terms in Eq. (1) will necessarily arise from the presence of capacitors and inductors.

A natural starting point when analyzing a dc circuit is to solve for its operating point. This entails ignoring all capacitors and inductors while solving for the voltages and currents across all branches of the static elements (e.g., transistors and resistors). In such an analysis there are no state variables defined, hence the concept of an equilibrium point has no meaning. This set of dc branch voltages and currents constitutes the operating point, defined independently of any dynamic system; in others words, an operating point is independent of the vaue or location of any capacitor or inductor in the circuit.

As a simple example, the circuit in Fig. 1(a) has its equilibrium point given by $v_c = 10$ V, while the circuit in Fig. 1(b) has its equilibrium point given by $i_L = 5$ A. Although these equilibrium points are different, since they correspond to different dynamic systems [indeed, the equilibrium point of Fig. 1(a) is unstable, while the Fig. 1(b) circuit is stable], they both correspond to the same dc operating point, defined by the branch voltages and currents of the static elements shown in Fig. 1(c).

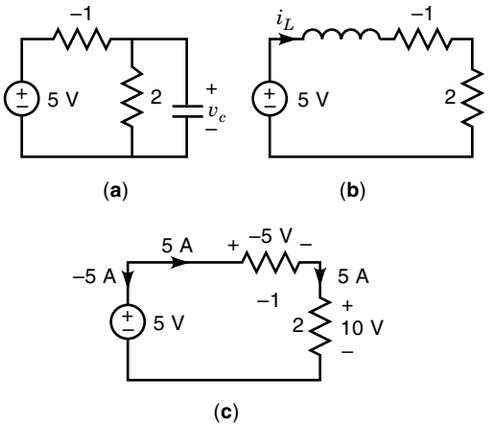


Figure 1. Illustration of equilibrium point versus operating point.

For circuits having isolated (but perhaps multiple) equilibrium points there is a unique correspondence from any equilibrium point to an operating point. In fact, the two terms are often used interchangeably in the literature and many textbooks, since there is usually no need for the distinction. Throughout this article, however, we will maintain the distinction between an equilibrium point and an operating point, since this is crucial to the discussion of the concepts presented.

Stability of Equilibrium Points and Operating Points

It is well known what is meant by the stability of an equilibrium point possessed by an autonomous circuit. (An autonomous circuit has no time-varying independent sources, only dc sources.) A general definition can be formulated as follows (5):

Definition 1. An equilibrium point x^* is said to be *stable* if, for each $\epsilon > 0$, there exists a $\delta > 0$ such that $\|x(t) - x^*\| < \epsilon$, for all $t \geq t_0$, whenever $\|x(t_0) - x^*\| < \delta$. Otherwise, the equilibrium point is said to be *unstable.*

There are many methods to ascertain whether a given equilibrium point is stable or unstable; two well-known methods are Lyapunov's first and second methods (6). We will use Lyapunov's first method, which entails linearizing the circuit around the equilibrium point in question and then examining the natural frequencies there. If all natural frequencies are located in the open left half-plane then the equilibrium point is stable. If at least one natural frequency is in the open right half-plane then the equilibrium point is unstable.

We now turn our attention from equilibrium points to operating points, and we make the following operating point stability definitions; notice that these definitions do *not* depend on the location or value of any capacitors or inductors (except that we, of course, assume they are positive since this is how they occur in nature).

Definition 2. A dc circuit's operating point is said to be *potentially stable* if, by inserting some set of positive-valued

shunt capacitors and series inductors into the circuit, the corresponding equilibrium point of the resulting dynamic circuit is stable, even in the presence of parasitic capacitors and inductors.

In the above definition we use the term "parasitic" to mean arbitrarily small values of capacitors and inductors that are, as in real circuits, placed anywhere throughout the circuit. In the next section we will give an example illustrating why such elements must be mentioned in this definition.

Definition 3. An operating point that is not potentially stable is said to be *unstable.*

We emphasize that if an equilibrium point is unstable this means with respect to a particular set of capacitor and inductor values. If an operating point is unstable, this means it is unstable for any set of positive-valued capacitors or inductors. Since there is an infinite number of possible dynamic circuits (and, therefore, an infinite number of resulting equilibrium points) that could be constructed from a given operating point, the above definitions are unsuitable for directly testing for an operating point's instability. A more practical method is required. Such a method is given in the next section.

HOW TO IDENTIFY UNSTABLE DC OPERATING POINTS

Consider the linear dynamic circuit shown in Fig. 2(a). We presume that this has come from the linearization, around a particular operating point, of some nonlinear circuit. The linear n-port N contains only positive-valued resistors. Ports 1 through k, called *dependent-source ports,* are each terminated by either a dependent current source in parallel with a positive-valued capacitor or a dependent voltage source in series with a positive-valued inductor. A controlling signal, shown in Fig. 2(a) as x_i or x_j, is the voltage across a dependent current source or the current through a dependent voltage source. The value of a dependent source gain a_i may be zero. (This is useful when a port i corresponds to an open-circuit voltage or a short-circuit current that is used as a controlling signal, but is not connected to an actual, nonzero dependent source.) Ports $k+1$ through n, called *outside ports,* are terminated with positive-valued capacitors and inductors, called *outside capacitors* and *outside inductors,* as shown. These model other capacitors and inductors that may be present in the linearized circuit.

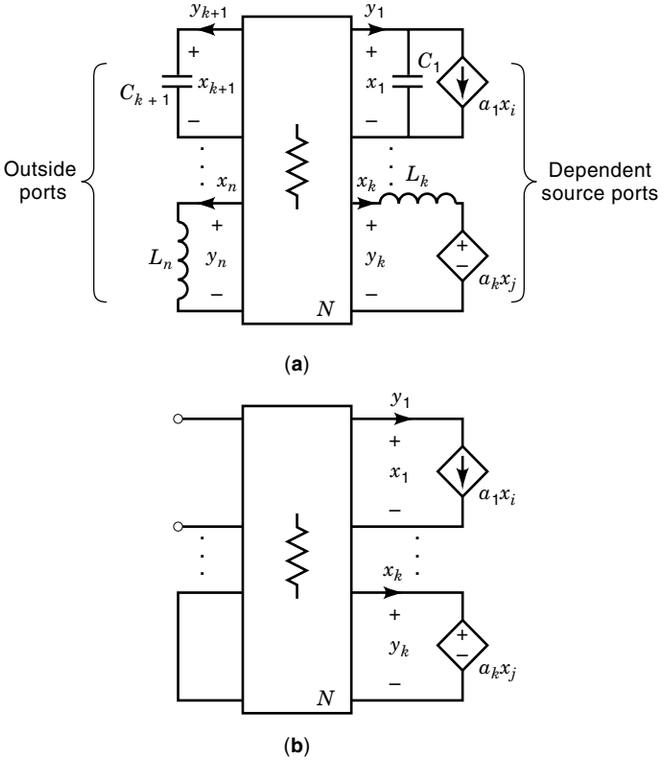


Figure 2. Generalized linear circuits.

The class of nonlinear circuits from which this linear circuit can be derived is quite general. We assume that all capacitors and inductors in the original circuit are uncoupled and have strictly monotone-increasing charge-voltage or flux-current characterizations. We assume that the resistive elements (e.g., resistors and transistors) can be expressed in a very general representation (7). In general, any circuit consisting of positive-valued resistors, diodes, transistors of any kind, and capacitors and inductors with strictly monotone-increasing charge-voltage or flux-current characteristics, respectively, linearized at a given operating point, can be modeled by the circuit in Fig. 2(a).

We also assume that no set of dependent current (voltage) source ports forms a cut set (loop) by itself or with any set of outside capacitors (inductors). Otherwise the circuit in Fig. 2(b), derived from Fig. 2(a), when analyzed at dc, could be ill-posed, in that it could contain cut sets of dependent current sources and/or loops of dependent voltage sources.

In addition, let us assume (these assumptions can be relaxed; see the appendix of Ref. 4) that there exist no cut sets (loops) made up exclusively of outside capacitors (inductors). Then the resistive n-port N in Fig. 2(a) can be characterized (8) at its ports by

$$\begin{bmatrix} Q_A & Q_B \\ Q_C & Q_D \end{bmatrix} \begin{pmatrix} \boldsymbol{y}_d \\ \boldsymbol{y}_o \end{pmatrix} + \begin{pmatrix} \boldsymbol{x}_d \\ \boldsymbol{x}_o \end{pmatrix} = 0 \tag{2}$$

where the vector $\boldsymbol{x}$ consists of the usual state variables (capacitor voltages and inductor currents), and is partitioned into $\boldsymbol{x}_d$, a vector whose components are the state variables appearing at the dependent source ports, and $\boldsymbol{x}_o$, a vector of state variables appearing at the outside ports. Vectors $\boldsymbol{y}_d$ and $\boldsymbol{y}_o$ are the respective port-variable complements of $\boldsymbol{x}_d$ and $\boldsymbol{x}_o$. The $n \times n$ matrix Q, shown partitioned in Eq. (2), has a nonnegative determinant, since N contains only passive reciprocal elements.

The port constraints of the circuit in Fig. 2(a) are given by

$$\begin{pmatrix} \boldsymbol{y}_d \\ \boldsymbol{y}_o \end{pmatrix} = K \frac{d}{dt} \begin{pmatrix} \boldsymbol{x}_d \\ \boldsymbol{x}_o \end{pmatrix} + \begin{bmatrix} A_A & 0 \\ 0 & 0 \end{bmatrix} \begin{pmatrix} \boldsymbol{x}_d \\ \boldsymbol{x}_o \end{pmatrix} \tag{3}$$

where K is a diagonal $n \times n$ matrix whose diagonal elements specify the positive linearized capacitor and inductor values. Matrix A, shown partitioned in Eq. (3), is the $n \times n$ matrix whose elements specify the appropriate dependent source coefficients. Notice that its entries are nonzero only in the upper

left-hand $k \times k$ submatrix, since all controlling variables and dependent sources are, by assumption, confined to ports 1, . . ., k. Combining Eq. (2) and Eq. (3) we have the dynamic equations of the circuit:

$$QK\frac{d}{dt}\begin{pmatrix}\boldsymbol{x}_d\\ \boldsymbol{x}_o\end{pmatrix} + (QA + I_n)\begin{pmatrix}\boldsymbol{x}_d\\ \boldsymbol{x}_o\end{pmatrix} = 0 \tag{4}$$

where I_n denotes the $n \times n$ identity matrix. From this, the natural frequencies of the circuit can be found; they are the values of s that satisfy

$$\det[sQK + (QA + I_n)] = 0 \tag{5}$$

We define the constant Γ as follows:

$$\Gamma \equiv \det(Q_A A_A + I_k)$$

We can now state the following theorem:

Theorem 1. Given an operating point of a circuit which can be linearized as in Fig. 2(a) with its dynamic equations written as in Eq. (4), if $\Gamma < 0$ then the operating point is *unstable.*

Remark. Notice that Q_A and A_A, from Eqs. (2) and (3), are associated with the dc equations of the circuit that results when $\boldsymbol{y}_o$ is set to zero—that is, when all outside capacitors are replaced with open circuits and all outside inductors are replaced with short circuits. Thus, Γ can be derived from the linearized operating point of the *dc* circuit; in order to use Theorem 1 for any given circuit, we need only define a port for each dependent source and ignore the presence of any outside capacitors and inductors. This, of course, is consistent with the definition of an unstable *operating point.*

The proof of Theorem 1 can be found in Ref. 4.

We will now give an example of the use of Theorem 1. Consider the circuits in Fig. 3(a) and Fig. 3(b). These circuits are used to generate a current that is independent of the supply voltage.

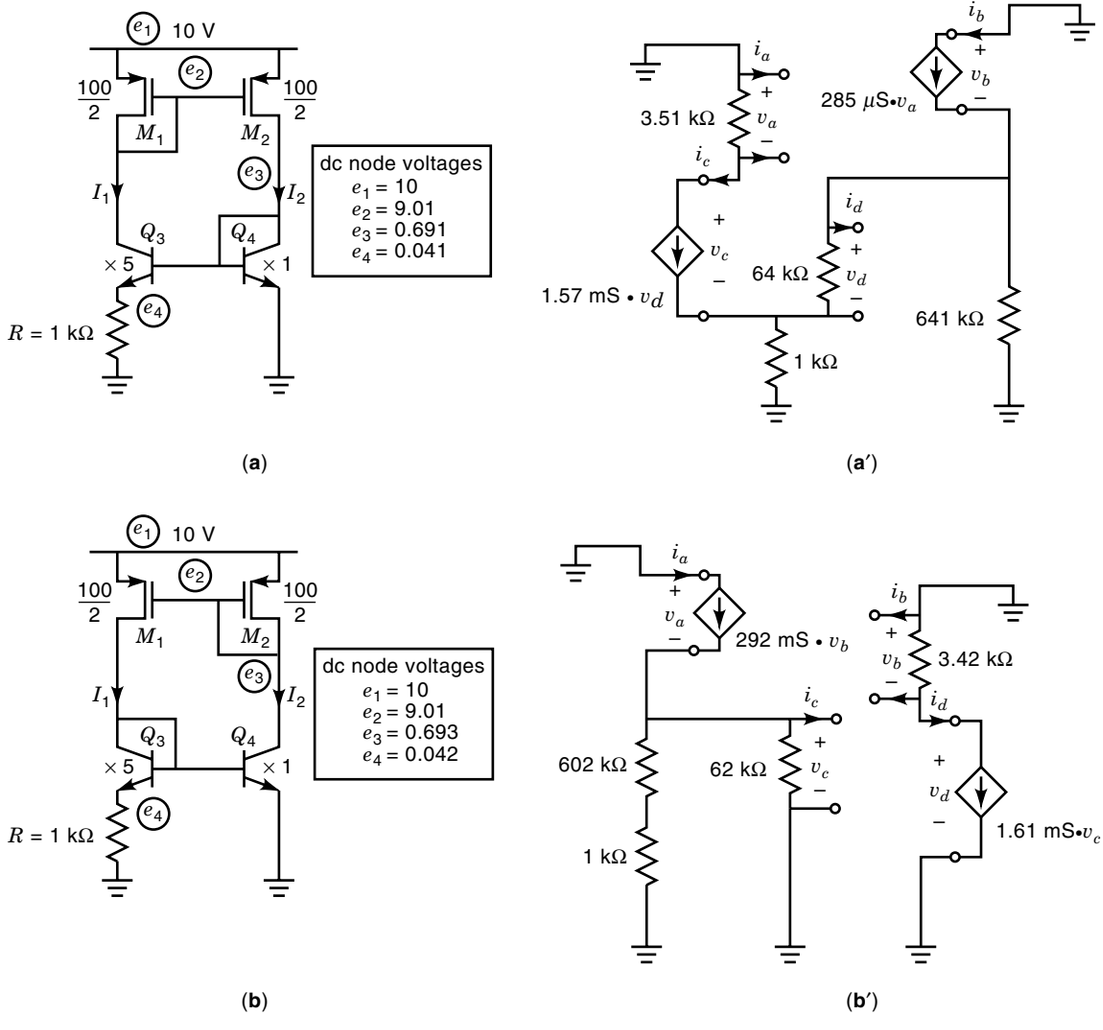


Figure 3. Two versions of a current reference circuit.

The operation of these circuits is explained as follows: A pair of currents I_1 and I_2 are set up subject to two sets of constraints. The first constraint, imposed by the current mirror made up of M_1 and M_2, sets $I_1 = I_2$. The second constraint is a consequence of the combination of Q_3, Q_4, and R and is given by

$$I_1 = I_2 = \frac{V_t}{1000} \ln 5$$

where V_t is a parameter proportional to absolute temperature, approximately 26 mV at room temperature. Details of this circuit's operation can be found in Ref. 9. Both Fig. 3 circuits realize the desired operating point at which $I_1 = I_2 = 42\ \mu A$, as is verified by the results of the SPICE dc operating point analysis shown along with the circuits. However, this operating point is unobservable in one of these circuits. We will use Theorem 1 to identify which one. The Fig. 3(a) and Fig. 3(b) circuits are shown, linearized at the operating point in question, in Fig. 3(a′) and Fig. 3(b′), respectively. These linear circuits are presented in the form of four-ports.

For the Fig. 3(a′) circuit we can write the following equation in the form of Eq. (2):

$$\begin{bmatrix} 3510 & 0 & -3510 & 0 \\ 0 & 635 & 10 & -625 \\ -3510 & 10 & 4495 & 975 \\ 0 & -625 & 975 & 1600 \end{bmatrix} \begin{pmatrix} i_a \\ i_b \\ i_c \\ i_d \end{pmatrix} + \begin{pmatrix} v_a \\ v_b \\ v_c \\ v_d \end{pmatrix} = 0 \tag{6}$$

For the Fig. 3(b′) circuit we can write:

$$\begin{bmatrix} 1562 & 0 & -1562 & 0 \\ 0 & 3420 & 0 & -3420 \\ -1562 & 0 & 1562 & 0 \\ 0 & -3420 & 0 & 3420 \end{bmatrix} \begin{pmatrix} i_a \\ i_b \\ i_c \\ i_d \end{pmatrix} + \begin{pmatrix} v_a \\ v_b \\ v_c \\ v_d \end{pmatrix} = 0 \tag{7}$$

The A_A matrix, as defined in Eq. (3), is given, for the Fig. 3(a′) circuit, by

$$A_A = \begin{bmatrix} 0 & 0 & 0 & 0 \\ .000285 & 0 & 0 & 0 \\ 0 & 0 & 0 & .00157 \\ 0 & 0 & 0 & 0 \end{bmatrix} \tag{8}$$

and, for the Fig. 3(b′) circuit, is given by

$$A_A = \begin{bmatrix} 0 & .000292 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & .00161 & 0 \end{bmatrix} \tag{9}$$

We now evaluate Γ for each circuit. For the Fig. 3(a′) circuit,

$$\Gamma = 1.55 \tag{10}$$

and for the Fig. 3(b′) circuit,

$$\Gamma = -1.51 \tag{11}$$

Since $\Gamma < 0$ for the Fig. 3(b′) circuit, the operating point indicated in the Fig. 3(b) circuit must be unstable.

Recall that Theorem 1 specifies a sufficient condition for operating point instability, but not a necessary one. The above analysis does not prove that the operating point shown in Fig. 3(a) is potentially stable, but it can be verified that this is the case simply by building this circuit and observing the dc node voltages shown in Fig. 3(a).

The instability criterion $\Gamma < 0$ given in Theorem 1 has been incorporated into the dc operating point analysis of SPICE (10). A discussion of that topic will be given in the section titled Identifying Unstable Operating Points Using SPICE.

MODELING REQUIREMENTS FOR REACTIVE ELEMENTS

How capacitors and inductors are appropriately modeled was addressed in another result, which was derived as a by-product of the development of the stability criterion. In particular, Theorem 2 in (4) states that any dependent current (voltage) source must have a capacitor (inductor) placed in parallel (series) with it. This requirement holds even if the value of a dependent source gain is zero. (Such zero-valued dependent sources are needed when a port corresponds to an open-circuit voltage or a short-circuit current that is used as a controlling signal but is not directly connected to an actual, nonzero dependent source.) This result is important because there are locations in certain circuits where capacitors and inductors *must* be modeled in order to observe unstable natural frequencies. The dangers of leaving out such critical capacitors and inductors are illustrated in the following example. Consider the circuit shown in Fig. 4. This circuit has been designed to be a second-order low-pass g_m–C filter using the "pseudodifferential" technique (11). The capacitors C_1 and C_2 determine the filter's desired transfer function. The capacitor

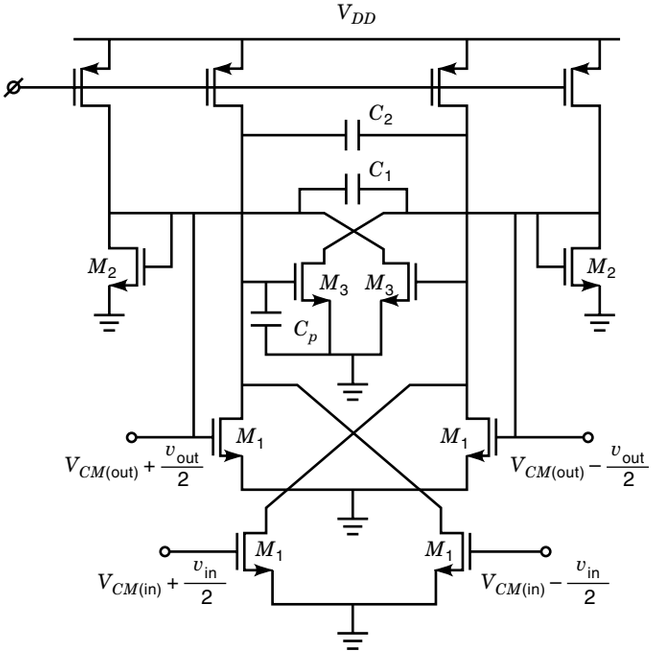


Figure 4. Second-order low-pass g_m–C filter.

C_p is considered to be parasitic and we will initially assume it to be small enough so that its effect is insignificant at the filter's frequencies of interest.

Setting $C_p = 0$, this circuit's natural frequencies (i.e., the filter's poles) are given by the values of s that satisfy the following characteristic equation:

$$C_1C_2s^2 + \frac{g_{m2}}{2}C_2s + \frac{g_{m1}g_{m3}}{4} = 0$$

Since both solutions to the above equation lie in the left half-plane, we could then conclude that the filter is stable. Unfortunately, this conclusion is incorrect, as we will now show.

Let us now assume $C_p > 0$. The resulting (now third-order) characteristic equation is:

$$C_1C_2C_ps^3 + \left(-2C_1C_2\frac{g_{m1}g_{m3}}{g_{m2}} - C_1C_p\frac{g_{m1}g_{m3}}{2g_{m2}} + C_2C_p\frac{g_{m2}}{2}\right)s^2 - C_2g_{m1}g_{m3}s - \frac{(g_{m1}g_{m3})^2}{2g_{m2}} = 0$$

Note that, for any value of $C_p > 0$, no matter how small, the s^3 term in the above equation is positive and the s^0 term is negative. Thus we can conclude that there is at least one real-valued natural frequency that lies in the right half-plane, thereby making the circuit unstable. Since any real MOS transistor will always have some nonzero capacitance between its gate and source (indeed, the correct operation of any transistor hinges upon the presence of such a capacitance), then any analysis that does not take this capacitance into account would be prone to error, as illustrated above. From the viewpoint of a circuit designer, this circuit is said to have positive feedback for common-mode signals, thereby resulting in instability. As explained in (11), this problem is typically overcome by adding circuitry to cancel out the common-mode signals between stages. The resulting circuit would then possess a potentially stable operating point.

The above example illustrates that there are certain locations in a circuit where capacitances (and inductances), no matter how small, must be modeled. A sharper result concerning such locations was later given in (12):

Theorem 2. Given the linear dynamic circuit shown in Fig. 2(a), let a capacitor be modeled in parallel with each pair of terminals whose voltage is the controlling signal for some dependent source, and let an inductor be modeled in series with each branch whose current is the controlling signal for some dependent source. If $\Gamma < 0$ then, regardless of whether or not any additional capacitors and inductors are modeled, the resulting characteristic polynomial will have its highest- and lowest-order nonzero coefficients of opposite signs, making it apparent that the corresponding operating point is unstable.

GENERAL PROPERTIES OF OPERATING POINT STABILITY IN EVENTUALLY PASSIVE CIRCUITS

Thus far we have addressed only the stability of each of a circuit's specific operating points, one at a time. Once the stability of an operating point is determined there is nothing that can be inferred, on the basis of Theorems 1 and 2, regarding the stability of any other operating points that the circuit may possess; the stability of each operating point is assessed separately.

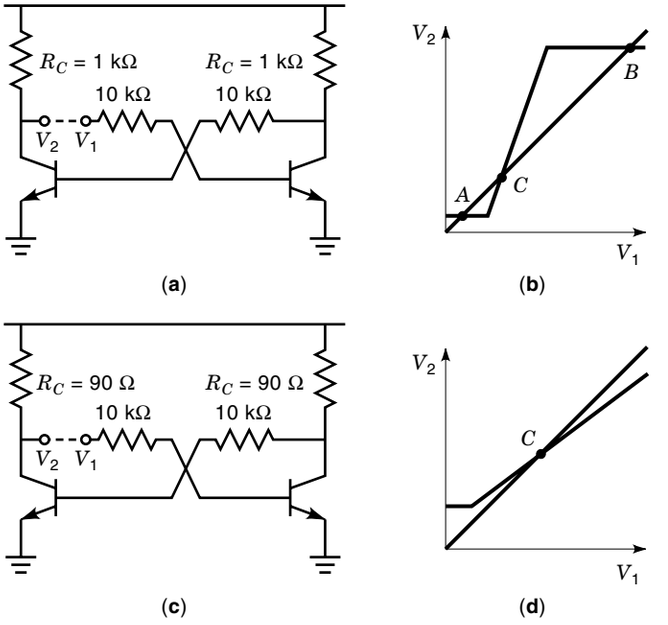


Figure 5. Latch circuits with different loop gains.

One may question whether the existence of multiple operating points and the stability of the various operating points are really separate issues. Might there be some connection between the presence of multiple operating points for a circuit and the stability of the operating points? This question is motivated by the following examples.

Figure 5(a) shows a simple latch circuit. It is shown in (4) that operating points A and B in Fig. 5(b) are potentially stable, and that operating point C is unstable. Let us now change the circuit slightly to the circuit shown in Fig. 5(c), where R_C has been reduced from 1 kΩ to 90 Ω. This circuit's unique operating point C in Fig. 5(d) can be shown to be potentially stable. It happens, in fact, that as the value of R_C is reduced from 1 kΩ to 90 Ω, operating points A and B disappear exactly when operating point C changes from unstable to potentially stable.

Now consider the nonlinear one-port shown in Fig. 6(a) (13). If this one-port is driven by a 24 V voltage source, then it

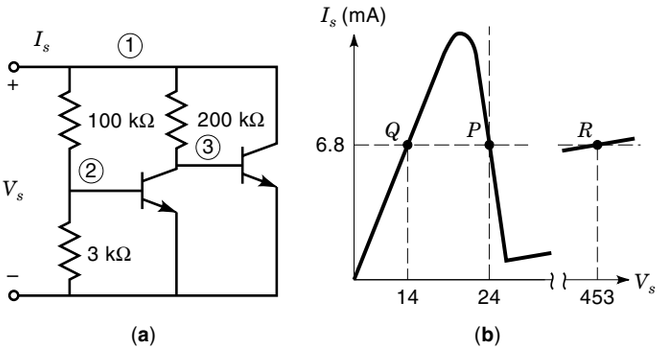


Figure 6. Nonlinear one-port with driving-point characteristic.

can be shown that operating point P in Fig. 6(b) is the unique, potentially stable operating point of the circuit. If the one-port is driven instead by a 6.8 mA current source, it then happens that this circuit possesses, in addition to P, which is now *unstable,* two more operating points, Q and R, both of which are potentially stable.

Notice that in both of these examples, an unstable operating point occurred only in the presence of two other, potentially stable operating points. Furthermore, in analyzing the latch we saw that the stability of operating point C changed at the bifurcation point (brought about by changing some of the resistor values) at which the circuit changed from possessing three operating points to possessing only one. In this section we will show how all of these issues are connected in a natural way.

Two Classes of Unstable Operating Points

Although Theorem 1 gives a sufficient condition for an operating point to be unstable, it is not a necessary condition; there may exist unstable operating points where $\Gamma > 0$ holds. To show why this is true, consider the following characteristic equation, assumed to have been derived from an augmentation with capacitors and inductors of the circuit in Fig. 2:

$$a_n s^n + a_{n-1} s^{n-1} + \cdots + a_1 s + \Gamma = a_n \prod_{k=1}^{n} (s - \lambda_k) = 0 \qquad (12)$$

where $a_n > 0$ and each λ_k is a natural frequency. Clearly, $\Gamma/a_n = \prod_{k=1}^{n}(-\lambda_k)$ and, in general, this product can be factored into three parts, corresponding to positive real roots, negative real roots, and complex roots:

$$\begin{aligned} \frac{\Gamma}{a_n} &= \left[\prod_{r=1}^{R} \alpha_r\right] \cdot \left[\prod_{l=1}^{L} \alpha_l\right] \cdot \left[\prod_{c=1}^{C} (\alpha_c + j\beta_c)(\alpha_c - j\beta_c)\right] \\ &= \left[\prod_{r=1}^{R} \alpha_r\right] \cdot \left[\prod_{l=1}^{L} \alpha_l\right] \cdot \left[\prod_{c=1}^{C} (\alpha_c^2 + \beta_c^2)\right] \end{aligned} \qquad (13)$$

Here we assume that there are R positive real roots, implying that each α_r is negative; L negative real roots, implying that each α_l is positive; and C pairs of complex conjugate roots. Since all but the α_r terms must be positive and $a_n > 0$, Eq. (13) implies

$$\operatorname{sgn} \Gamma = (-1)^R \qquad (14)$$

which shows that $\Gamma < 0$ if and only if there is an odd number of positive real roots for the capacitor/inductor augmentation at issue. This leads to the following definition:

Definition 4. If an operating point $\mathcal{O}$ of a dc circuit satisfies Theorem 1 and, equivalently, if every robust dynamic circuit (i.e., all capacitor/inductor-augmented circuits with a sufficient number of arbitrarily small, but positive, capacitors and/or inductors included) that can be constructed around $\mathcal{O}$ has an *odd* number of natural frequencies in the open right half-plane, then we say that $\mathcal{O} \in \mathcal{U}^o$.

(Notice that a circuit possesses an odd number of open right half-plane roots if and only if it possesses an odd number of positive real roots.)

At this point perhaps it is natural to question whether circuits exist which, when the dc biasing is appropriate, possess operating points having an even number of positive real natural frequencies. Such circuits do exist (14) and such operating points would also be unstable, but they would not be identified as such by Theorem 1, since the constant term Γ in any corresponding characteristic polynomial would be positive. The following definition identifies such operating points.

Definition 5. Given an operating point $\mathcal{O}$ of a dc circuit, if every robust dynamic circuit that can be constructed around $\mathcal{O}$ has an *even* nonzero number of natural frequencies in the open right half-plane, then we say that $\mathcal{O} \in \mathcal{U}^e$.

Although a special class of $\mathcal{U}^e$ operating points has been identified in Ref. 14, finding definitive criteria that identify such operating points is still an open problem.

(Almost) Half of All Dc Operating Points Are Unstable

We will now prove some general results for the number of unstable operating points that a circuit must possess. We begin by stating the following result from Ref. 15:

Theorem 3. Let a dc circuit contain positive-valued resistors, independent sources, and passive, voltage-controlled nonlinear elements whose ports form neither loops nor cut sets. If the circuit has a finite number of operating points, all of which are isolated, then it possesses an *odd* number of structurally stable operating points.

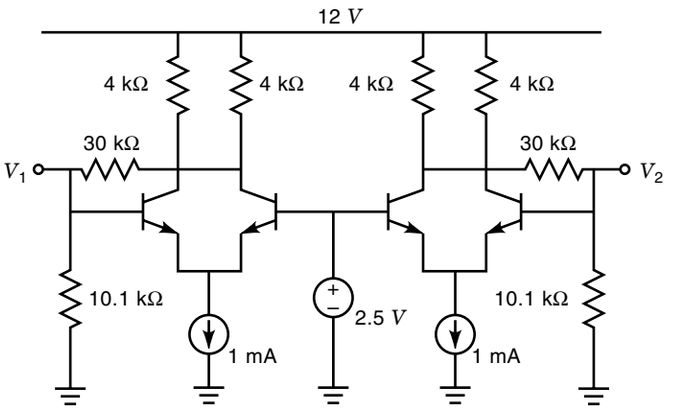
The circuit description in the above theorem covers any circuit that can be built or fabricated out of real electrical components. A structurally stable operating point is one that does not disappear or split into a pair of operating points when any of the circuit's parameters are varied slightly.

Theorem 3 is proved in (15) using the degree of a mapping. In particular, it is shown there that any structurally stable operating point can be assigned an index of $+1$ or -1, and that the sum of the indices of all of a circuit's operating points must add up to $+1$. Hence, the total number of operating points of any circuit must be odd.

From this we can also conclude that if a circuit possesses n operating points, then $(n - 1)/2$ of these operating points must have index of -1. In (14) it is proved that the index of any operating point is identical with the sign of the corresponding value of Γ. Since $\Gamma < 0$ implies that the operating point is $\mathcal{U}^o$, we have the following result:

Theorem 4. If a dc circuit as specified in Theorem 3 has n structurally stable operating points, then $(n - 1)/2$ of them must be $\mathcal{U}^o$ and therefore must be unstable.

It is not necessarily true that the remaining $(n + 1)/2$ operating points, all of which have an index $+1$, will be potentially stable; a $\mathcal{U}^e$ unstable operating point also has an index of $+1$. As an illustration of Theorems 3 and 4, consider the



V_1	V_2	Index	Stability type
1.8	1.8	+1	Potentially stable
1.8	2.7	+1	Potentially stable
2.7	1.8	+1	Potentially stable
2.7	2.7	+1	Potentially stable
2.5	2.5	+1	u^e
1.8	2.5	−1	u^o
2.7	2.5	−1	u^o
2.5	1.8	−1	u^o
2.5	2.7	−1	u^o

Figure 7. An illustration of Theorems 3 and 4.

circuit in Fig. 7. The entire circuit possesses nine operating points which are listed in the figure. As Theorem 4 predicts, four of these operating points are $\mathscr{U}^o$. Of the remaining five operating points that are not $\mathscr{U}^o$, four are potentially stable; the fifth can be shown to be $\mathscr{U}^e$ using results given in (14).

Results similar to those given in this section have been applied in other scientific fields as well. For example, degree theory has been used to obtain results regarding the number and stability of equilibrium states in chemically reacting systems (16,17).

IDENTIFYING UNSTABLE OPERATING POINTS USING SPICE

Background

Designers of integrated circuits have commonly looked to the SPICE dc operating point analysis to give an accurate solution to the dc circuit being simulated. Although SPICE does generally give an accurate solution to the static *equations* that describe the dc circuit, the solution may not be an observable operating point of the *physical circuit* itself. Since it has been shown that there exist circuits with operating points that are inherently unstable (no insertion of capacitors or inductors can make the resulting dynamic circuit's corresponding equilibrium point stable), these unstable operating points are physically unobservable. As a result, one might conjecture that an unstable operating point is also unobservable from the standpoint of dc circuit simulation. In other words, one might infer that, when using an iterative algorithm to solve the nonlinear equations describing a dc circuit, the iterates would tend to be "driven away" from an unstable solution in the same way that the actual circuit, during operation, would drive itself away from the unstable operating point. This conjecture is false. As a counterexample, consider the circuit shown in Fig. 8, which is well known to possess an unstable operating point.

For this circuit the SPICE dc operating point analysis was found to converge to the unstable operating point, as indicated in Fig. 8, when no `.nodeset` commands were specified in the SPICE input file. (SPICE will use a zero voltage value at each node as an initial guess, unless a `.nodeset` command specifies otherwise. The `.nodeset` command is normally used when there are convergence problems or when more than one dc operating point is desired.) It is evident that the numerical stability of the Newton–Raphson (or some similar) algorithm used in SPICE is not necessarily related to the physical stability of the operating point that is being simulated. In fact, provided that the starting point is close enough, the Newton–Raphson algorithm is guaranteed to converge to any operating point of a circuit, stable or unstable (18). In the example of Fig. 8, setting all node voltages to zero in the initial guess (the default) led to convergence to the unstable operating point shown.

We now show how a certain class of unstable operating points can be identified as a by-product of the SPICE dc operating point analysis. The following section then discusses two practical examples showing how this addition to the SPICE dc operating point analysis can be useful to a circuit designer. Recall that, from Definition 4, any operating point of a circuit that satisfies Theorem 1 is said to be a $\mathscr{U}^o$ operating point. $\mathscr{U}^e$ operating points (which are not identified by Theorem 1) are rare in most practical circuits.

In most versions of SPICE the dc circuit equations are expressed in modified nodal analysis (MNA) form (19):

$$\begin{pmatrix} \hat{\boldsymbol{i}} \\ \hat{\boldsymbol{v}} \end{pmatrix} = F\left[\begin{pmatrix} \tilde{\boldsymbol{v}} \\ \tilde{\boldsymbol{i}} \end{pmatrix}\right] \tag{15}$$

Let the circuit contain p nodes and m independent and dependent voltage sources. Then in Eq. (15), $\tilde{\boldsymbol{v}} \in R^p$ is a vector each of whose components is a node voltage; $\hat{\boldsymbol{i}} \in R^p$ is a vector whose components are the sums of independent current source values entering each node; $\hat{\boldsymbol{v}} \in R^m$ is a vector each of whose components is either an independent voltage source value, or zero if the component corresponds to a dependent voltage source; $\tilde{\boldsymbol{i}} \in R^m$ is a vector whose components are the currents flowing through each independent or dependent voltage source; $\boldsymbol{F}: R^{p+m} \rightarrow R^{p+m}$ is a smooth mapping. The jth equation, $j = 1, \ldots, p$, of Eq. (15) is the KCL constraint that equates the sum of all independent current sources entering node j with the sum of the rest of the currents leaving node

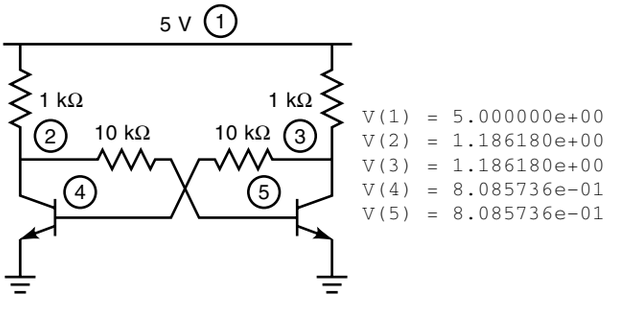


Figure 8. An example of an unstable operating point.

j. The $(k + p)$th equation, $k = 1, \ldots, m$, sets the value of the kth voltage source equal to the voltage difference between the two nodes (one of them may be ground) across which the source is connected.

Once SPICE has converged to a solution

$$\begin{pmatrix} \tilde{v} \\ \tilde{i} \end{pmatrix}^*$$

of Eq. (15), the elements of the Jacobian matrix

$$F'\left[\begin{pmatrix} \tilde{v} \\ \tilde{i} \end{pmatrix}^*\right]$$

evaluated at the solution are available, since these will have been computed and used by SPICE in the course of its normal iterative solution process. The following simple relationship between this Jacobian and operating point stability was given in (10):

Theorem 5. For any operating point, $\operatorname{sgn} \Gamma = (-1)^m \operatorname{sgn}[\det F']$, where m is the total number of dependent and independent voltage sources contained in the circuit.

In SPICE it happens that F' is stored in its L–U decomposed form after the dc solution has been obtained. Thus $\det F'$ is given simply by the product of the diagonal terms in the L–U matrix. Since we are interested only in the sign of this determinant, we need only count the number r of negative terms along the diagonal. If $(m + r)$ is odd (where, as mentioned in Theorem 5, m is the number of dependent and independent voltage sources contained in the circuit), then $(-1)^m \det F' < 0$, so $\Gamma < 0$, indicating that the operating point is unstable.

Using this algorithm, a very simple modification of SPICE has been made that delivers a warning to the user, along with the operating point information, whenever a $\mathscr{U}^o$ operating point is encountered. Since the algorithm only requires counting the voltage sources and counting the negative entries along the diagonal of the final L–U Jacobian matrix, this extra analysis requires a negligible increase of memory and CPU time.

Two Examples

Op-Amps Connected with Positive and Negative Feedback. To illustrate the use of the above algorithm in SPICE, consider the SPICE dc analysis of the two op-amp circuits shown in Fig. 9. The model of the 741 op-amp used in our simulations is the one shown in Ref. 9, p. 424. In both circuits, the SPICE simulations converged to the operating point shown in Fig. 9. Our modified SPICE algorithm automatically shows the Fig. 9(b) operating point to be unstable. It may be argued that such instability can be determined by performing an ac or pole-zero analysis, both of which are available in most circuit simulators. However, the Fig. 9(a) circuit that we simulated was not properly internally compensated; a pole-zero analysis on this circuit would show that, in fact, both circuits are unstable for the particular capacitor values used.

While the Fig. 9(a) circuit can be stabilized by adjusting the value of an internal capacitor; the Fig. 9(b) circuit cannot. This is the essence of the difference between instability of a circuit's equilibrium point—that is, the instability of an equilibrium point of a dynamic circuit with a specific set of capacitors and inductors specified—and the instability of a dc circuit's operating point, as discussed in the section titled How to Identify Unstable Dc Operating Points, and in Ref. 4. The pole-zero and ac analyses cannot be used to determine a circuit's dc operating point stability because such analyses must be performed on a circuit with specific capacitors and inductors prescribed.

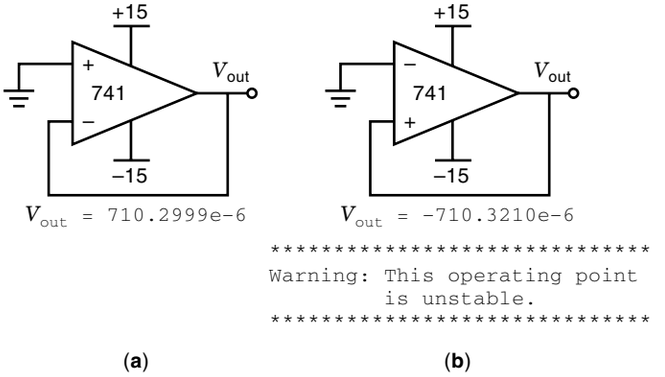


Figure 9. Op-amp circuits connected with (a) positive and (b) negative feedback. Warning message is automatically printed out by modified SPICE algorithm.

Bandgap Voltage Regulator. The fact that SPICE can converge to an unstable operating point is undesirable for two reasons. First, SPICE can find an operating point that "looks" correct, but is worthless in that it is actually unstable and hence physically unobservable. As mentioned previously, the instability of the operating points indicated in Fig. 8 and Fig. 9(b) is well known to most circuit designers. There are other circuits, however, where it is not as obvious that an unstable operating point has been encountered. Consider, for example, the design of a circuit commonly used as a bandgap reference voltage. The design concept, as illustrated in Fig. 10, is based on the placing of two sets of constraints on a pair of branch currents I_1 and I_2. The first, imposed by the connection shown of Q_1, Q_2, and R_1, gives

$$V_T \ln \frac{nI_2}{I_1} = I_1 R_1 \tag{16}$$

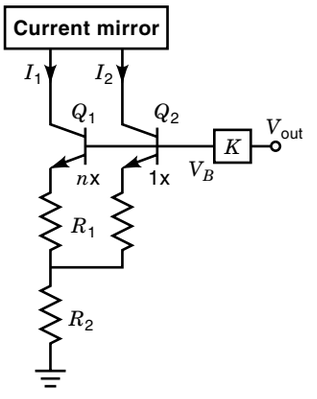


Figure 10. Design concept of bandgap voltage reference.

The second, from the current mirror, simply gives

$$I_1 = I_2 \tag{17}$$

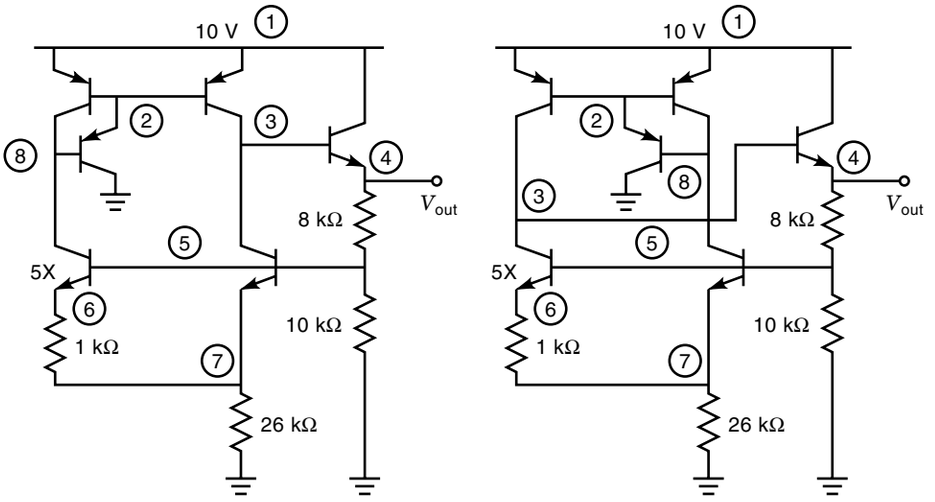
Combining Eq. (16) and Eq. (17), we have

$$I_1 = I_2 = \frac{V_T}{R_1} \ln n \tag{18}$$

The output V_{out} is then given by

$$KV_B = K[V_{be}(Q_2) + 2I_2R_2] \tag{19}$$

This gives a voltage with very low dependence on temperature. Further details on the operation of this circuit can be found in (9). The Fig. 10 block diagram can be implemented in the two different ways shown in Fig. 11(a) and Fig. 11(b). Both circuits correctly realize the Fig. 10 design, where the output voltage at node 4 is approximately 5 V. The SPICE dc operating point analysis, whose results are shown in Fig. 11(c) and Fig. 11(d), confirms this. (The difference between the output voltages of the two circuits is due to second-order effects, such as nonzero base currents.) It happens that the dc operating point in the Fig. 11(a) circuit is potentially stable, whereas in Fig. 11(b) it is unstable. This fundamental prop-



(a) (b)

```
V(1) = 1.000000e+01
V(2) = 9.309432e+00
V(3) = 5.585356e+00
V(4) = 4.845284e+00
V(5) = 2.688440e+00
V(6) = 2.039494e+00
V(7) = 1.999687e+00
V(8) = 8.720304e+00
i(vs) = -3.46535e-04
```

(c)

```
V(1) = 1.000000e+01
V(2) = 9.305452e+00
V(3) = 6.203722e+00
V(4) = 5.460580e+00
V(5) = 3.029703e+00
V(6) = 2.378533e+00
V(7) = 2.335150e+00
V(8) = 8.712343e+00
i(vs) = -3.92694e-04
*****************************
Warning: This operating point
         is unstable.
*****************************
```

(d)

```
V(1) = 1.000000e+01
V(2) = 9.413378e+00
V(3) = 1.722498e+00
V(4) = 1.022720e+00
V(5) = 5.681401e-01
V(6) = 2.314104e-02
V(7) = 2.242561e-02
V(8) = 8.928227e+00
i(vs) = -5.76906e-05
*****************************
Warning: This operating point
         is unstable.
*****************************
```

(e)

Figure 11. Two realizations of a bandgap voltage regulator circuit. Warning message is automatically printed out by modified SPICE algorithm.

erty distinguishing the two circuits in Fig. 11 is well known; however, it is not always obvious using a simple hand calculation to determine the dc behavior. Since the SPICE dc operating point analysis converges to the desired operating point in both cases, it is impossible to tell solely from its results which circuit functions correctly. Moreover, it is proved in (14) that if a circuit's operating point is found to be unstable, then the circuit must possess at least two additional operating points. Hence another important by-product of identifying an unstable operating point is knowledge of the existence of other, possibly potentially stable operating points. This information could alert the designer to possible latch-up conditions that would otherwise have gone undetected.

In the example of Fig. 11(b), we have a circuit that, on the basis of its dc operating point analysis, *looks* correct, but in fact is incorrect for the desired application. We will now consider an example of a circuit that looks *incorrect* on the basis of its dc operating point analysis, but which actually operates correctly. Consider again the circuit shown in Fig. 11(a). If no `.nodeset` command is given for its dc operating point analysis, SPICE will converge to the different operating point shown in Fig. 11(e), where the output voltage at node 4 is approximately 1 V. This result might well cause the circuit designer to consider taking steps to prevent possible latch-up into the unwanted Fig. 11(e) state. If, however, the designer could be warned that that operating point is unstable, no such concern would be necessary since the circuit could not possibly latch-up into the unstable operating point. (The designer would, however, be well advised to find the circuit's third dc operating point and examine its stability and latch-up potential.)

Designers familiar with bandgap circuits can easily identify instability in the Fig. 11(b) circuit by recognizing the presence of positive feedback. We urge the reader to review the discussion given in Section I of (4), however, to better appreciate the heuristic, nonrigorous character of the arguments that usually form the basis for such positive feedback criteria for assessing dc operating point instability. See also Section 8-3.2 of (3). Nonetheless, the SPICE algorithm discussed in the Background of this section does not rely on such experience-based insights; it is perfectly general, applies to all circuits, and does not require the use of heuristic analytical methods.

APPLICATION OF OPERATING POINT STABILITY TO NONLINEAR ONE-PORTS

A number of results concerning the presence of negative differential resistance (NDR) have been reported in the literature, including (20–22). These papers deal rigorously with finding sufficient conditions for the presence of NDR. Very little has been said, however, regarding the relationship between NDR and stability, except that it is usually assumed that the presence of NDR automatically implies instability.

This assumption is not always true. A counterexample is shown in Fig. 12. This one-port, constructed by terminating a current conveyor (23) with a 2 kΩ resistor, exhibits a resistance of -2 kΩ for $I \in [-500\ \mu\text{A}, 2\ \text{mA}]$, where all transistors are biased in the forward-active region. However, it can be shown that if this one-port is driven by a current source, then

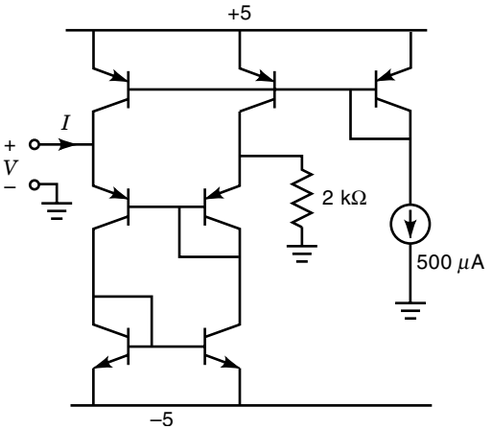


Figure 12. Transistor one-port with NDR.

the resulting equilibrium point can be made stable, even in the presence of a capacitor connected across the port. This somewhat surprising behavior is due to the inevitable presence of other parasitic capacitors across each transistor junction. However, if we were instead to drive this one-port with a voltage source, then, as we will subsequently prove, the resulting circuit would be unstable independent of the location or values of any capacitors that may be present at the input or at any other location in the circuit.

The qualitative difference between the current source-driven and voltage source-driven one-port in Fig. 12 is discussed in (4). The operating point of the circuit created by driving the Fig. 12 one-port with a current source is potentially stable, even though the one-port exhibits negative differential resistance, while the operating point of the circuit created by driving the Fig. 12 one-port with a voltage source is unstable.

We will now extend the circuit-related stability results to the stability of dc one-ports. An operating point of a one-port is defined by its port voltage, port current, and internal branch voltages and currents, but the port termination is not specified. Given an operating point $\mathcal{O}$ of a one-port, let $\mathcal{O}_s$ denote the operating point of the circuit formed by the voltage source termination of the port that realizes $\mathcal{O}$, and let $\mathcal{O}_o$ denote the operating point of the circuit formed by the current source termination of the port that realizes $\mathcal{O}$.

Definition 6. An operating point $\mathcal{O}$ of a nonlinear one-port is said to be open-circuit (short-circuit) unstable if $\mathcal{O}_o$ ($\mathcal{O}_s$) is unstable. Otherwise it is said to be open-circuit (short-circuit) potentially stable.

We now develop results that give a fundamental relationship between a nonlinear one-port's open-circuit operating point stability, its short-circuit operating point stability, and its driving-point characteristic. We will also show how we can use the results presented in this article to identify, by inspection, unstable regions of a nonlinear one-port's driving-point characteristic.

Assume that at dc a one-port, linearized at any operating point, does not contain any cut set consisting exclusively of dependent current sources, or of dependent current sources and the port; we also disallow any loop consisting of depen-

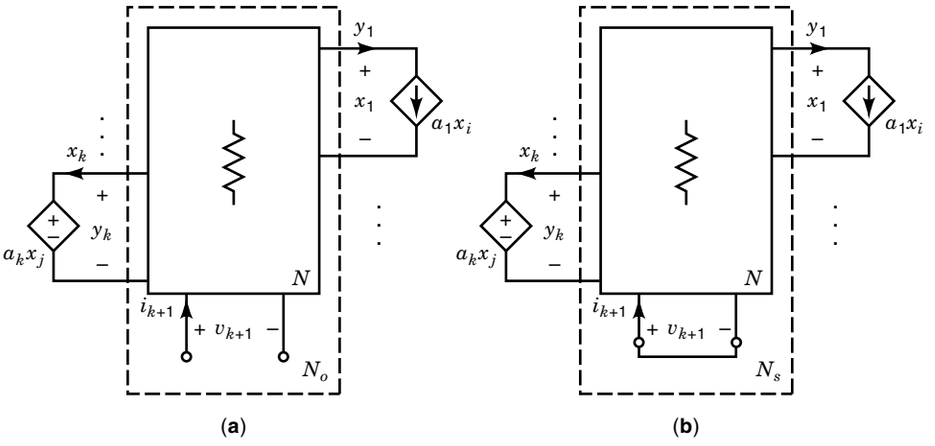


Figure 13. General linear active one-ports.

dent voltage sources, or of dependent voltage sources and the port. We will model this linearized circuit as the passive $(k + 1)$-port N, terminated by dependent sources, shown in Fig. 13(a) and Fig. 13(b), where the first k ports are defined by the location of the dependent sources and the $(k + 1)$th port is the location of the original one-port. Define N_o as the k-port that results when the $(k + 1)$th port is open-circuited, as shown in Fig. 13(a), and define N_s as the k-port that results when the $(k + 1)$th port is short-circuited, as shown in Fig. 13(b). Define Q_o as the hybrid matrix of k-port N_o such that $\boldsymbol{x} + Q_o\boldsymbol{y} = 0$, where vectors $\boldsymbol{x}$ and $\boldsymbol{y}$ are defined in Fig. 13. Likewise, define Q_s as the corresponding hybrid matrix of k-port N_s. Notice that Q_o and Q_s will, in general, be different because N_o and N_s differ topologically. While, in general, $Q_o \neq Q_s$, the above loop and cut set assumptions do guarantee that the same *kind* of hybrid matrix exists in both cases (8). Define the $k \times k$ matrix A to give the port constraints of N_o and N_s; that is, $y = Ax$. The entries of A will be the appropriate dependent source coefficients. I_k is defined as the $k \times k$ identity matrix. We now define the following stability-indicating constants for each of the two Fig. 13 circuits:

$$\Gamma_o \equiv \det(Q_oA + I_k) \tag{20}$$

$$\Gamma_s \equiv \det(Q_sA + I_k) \tag{21}$$

Let $g_p(A)$ denote the linearized port conductance of the one-port biased at a given operating point, and let $g_p(0)$ denote the port conductance of the same linearized one-port under the condition that all of the dependent sources have been set to zero. This notation is illustrated in Fig. 14. The following theorem is presented in (24):

Theorem 6.

$$g_p(A) = g_p(0) \cdot \frac{\Gamma_o}{\Gamma_s} \tag{22}$$

The following example shows how one can infer operating point stability information from a one-port's driving-point characteristic. Consider again the nonlinear one-port shown in Fig. 12. We have established that $\mathscr{O}_o$ is potentially stable. Hence $\mathscr{O}_o \notin \mathscr{U}^o$ and therefore $\Gamma_o > 0$. Since the slope of the driving-point characteristic at the operating point of interest is negative, $g_p(A) < 0$ at $\mathscr{O}$. Furthermore, we know that $g_p(0) \geq 0$ since the linearized one-port is passive in the absence of controlled sources. Therefore, it follows from Theorem 1 that $\Gamma_s < 0$. Hence $\mathscr{O}_s \in \mathscr{U}^o$, and we can conclude that the one-port is *short-circuit unstable* at $\mathscr{O}$. This result is generalized in the following theorem:

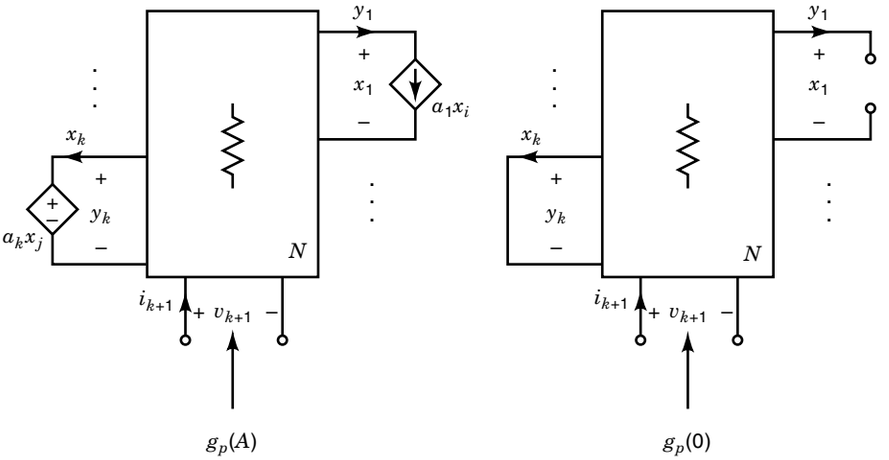


Figure 14. Illustration of $g_p(A)$ and $g_p(0)$.

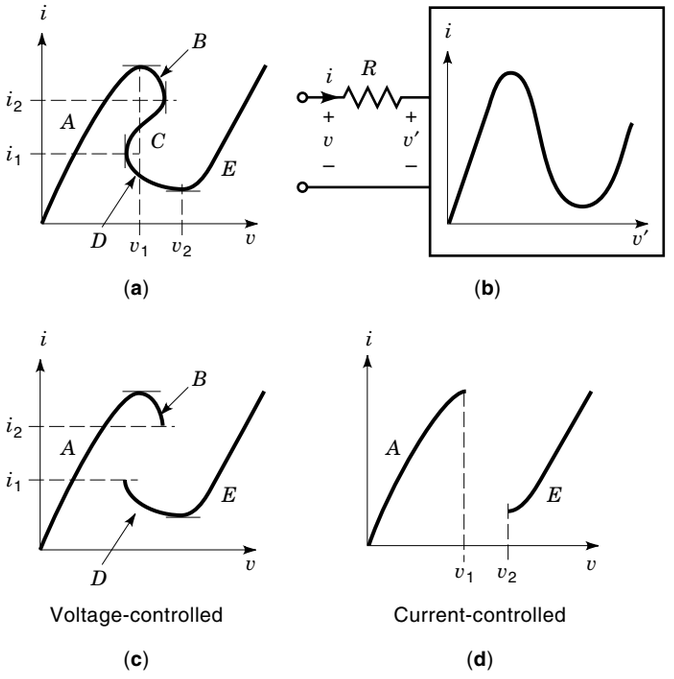


Figure 15. "C-Type" NDR circuit with driving-point characteristic.

Theorem 7. Let $\mathscr{O}$ be an operating point of a nonlinear one-port whose topology satisfies the loop and cut set assumptions stated above, and let $g_p(A)$ be the linearized port conductance at $\mathscr{O}$. The following statements are true:

(i) If $g_p(A) < 0$ then $\mathscr{O}_s \notin \mathscr{U}^o$ if and only if $\mathscr{O}_o \in \mathscr{U}^o$.
(ii) If $g_p(A) > 0$ then $\mathscr{O}_s \in \mathscr{U}^o$ if and only if $\mathscr{O}_o \in \mathscr{U}^o$.

Proof. By the assumptions on the topology of the one-port, $g_p(0) = 0$ only if $g_p(A) = 0$, and $g_p(0) = \infty$ only if $g_p(A) = \infty$. The proof is now immediate from inspection of the sign of each term of Eq. (22).

We can use Theorem 7 to identify regions of stability on a one-port's driving-point characteristic for both open-circuit and short-circuit terminations of the one-port as follows.

In Fig. 15(a) we show a one-port with a "C-type" driving-point characteristic, constructed by placing a positive resistor in series with an "N-type" circuit, as shown in Fig. 15(b) (23). The charactristic has been divided into five curve segments in Fig. 15(a), each of which is bounded on at least one end by a point at which the characteristic has either zero or infinite slope. We assume that all components in this one-port are described by $\mathscr{C}^2$ functions that are, along with their derivatives, bounded on any compact set. Also, let us assume for this example that the origin of the characteristic in Fig. 15(a) is known to be potentially stable when the one-port is terminated with either a short circuit or an open circuit. These assumptions imply that Γ_s and Γ_o are continuous and finite everywhere on the characteristic and that they are both positive at the origin.

As we proceed from the origin along segment A to the boundary between segments A and B, the slope changes from positive to negative through zero, which implies by Theorem 6 that either Γ_o changes from positive to negative through zero, or Γ_s changes from positive to negative discontinuously and without bound. But because Γ_s and Γ_o must vary continuously with all circuit parameters, it can only be true that Γ_o passes through zero. Thus we can conclude that all operating points on segment B are open-circuit unstable. As we move from segment B to segment C, the slope becomes infinite and then positive, implying that Γ_o remains negative and Γ_s changes from positive to negative. This means that all operating points on segment C are both open-circuit and short-circuit unstable. Similarly, all operating points on segment D are open-circuit unstable. In Fig. 15(c) and Fig. 15(d), we show the possibly observable operating points on the driving-point characteristic for a voltage source input and a current source input, respectively. We say "possibly" here because an operating point that is not $\mathscr{U}^o$ may still be unstable (i.e., if it is $\mathscr{U}^e$). The methods given in this section can only identify $\mathscr{U}^o$ operating points as being unstable. Notice that both curves show hysteresis from the point of view of the controlling signal. Furthermore, at any value of the controlling signal for which hysteresis is present, it can be seen by comparing Fig. 15(a) with Fig. 15(c) and Fig. 15(d) that there is another operating point present (between the two possibly observable operating points) that is unstable for the given termination. This is in agreement with the relationship between the number of $\mathscr{U}^o$ operating points and the number of other operating points that any eventually passive circuit must possess.

CONCLUSION

This article has surveyed a variety of results on the stability of dc operating points. In contrast to techniques often found in the literature, which are based on heuristic methods or overly simplified assumptions and consequently can be misleading, these results provide an analysis of operating point stability in a more rigorous context. We first made clear the difference between an operating point and an equilibrium point and then defined rigorously, based on the actual circuit dynamics, what it means for an operating point to be either potentially stable or unstable. We found a simple criterion, based only on the dc circuit's linearized equations, that can identify an operating point as being unstable. As a by-product of the derivation of this criterion we showed that, in order to correctly determine operating point stability, it suffices to model stray capacitance and inductance in a few specific locations, even though parasitic reactances might exist virtually everywhere in a physical circuit. Practical examples were given which used this criterion to identify unstable operating points.

Our attention then turned to the classes of $\mathscr{U}_0$ and $\mathscr{U}_e$ operating points, and we established that $\mathscr{U}_0$ operating points are quite prevalent—comprising approximately half of all operating points in circuits having multiple operating points. The modification of SPICE to permit it to identify $\mathscr{U}_0$ operating points was treated next. The stability results were extended to operating ports of nonlinear one-ports, where the relationship between negative differential resistance at an operating point and open- and short-circuit stability was described.

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