NONLINEAR NETWORK ELEMENTS

NETWORK, NONLINEAR

Most of the natural laws of physics can be stated in terms of partial differential equations (PDE) since they describe physical phenomena by relating space and time derivatives and these operations represent natural things such as velocity, acceleration, force, magnetic flux, currents.

From a theoretical point of view, the electrical behavior of semiconductor devices can be described solving a set of nonlinear partial differential equations given by the combination of Maxwell's equations and continuity equations for electrons and holes.

However, as for practically all modern microelectronic devices the wavelength associated with the maximum operating frequency is significantly longer than device dimensions, the set of equations can be restricted to Poisson's equation and to continuity equations for the free carriers.

Nonetheless, even the terminal behavior of a quite simple device like a *pn* junction can be achieved only through a cumbersome and very time-consuming numerical analysis.

For purposes of analysis and design, most modern nonlinear semiconductor devices and electronic systems can be replaced by models made of basic *nonlinear circuit elements* such as two terminal, multi-terminal and multi-port resistors, inductors, capacitors and independent voltage and current sources.

The interconnection of these elements is called *electric circuit*, whereas *physical circuit* is a collection of interconnected electrical devices.

In a physical circuit the current $I(t)$ through any device terminal and the voltage $V(t)$ across any pair of terminals at any time are well defined.

Additionally, if the electrical charges into the device can be considered function of the instantaneously values of the voltages applied to device terminal only, (quasistatic hypothesis (1, 2)), the device may be approximated by the connection of several *lumped circuit elements*, i.e. can be modeled by a finite number of equation involving only algebraic, ordinary differentiation and integration operations on the terminal variable at any time.

For example, in a one-port this means that the current entering one terminal appears *instantaneously* at the other.

The assumption of no spatial variables implies that all voltages $V(t)$ and currents $I(t)$ are functions of only one independent variable, namely, the time t.

In addition, all circuit elements are assumed to be ideal with perfectly conducting terminals, and without any parasitic effects.

There is no less of generality in this assumption, since any important parasitic effect may be modeled by introducing additional circuit elements.

Finally, we assume that each circuit element is defined for all voltage and current waveform for all frequencies. In other words, there are no time-rate dependent circuit parameters because such elements would produce a lack of predictability under arbitrary external interconnections.

A *model* is a representation of a device by using a set of basic components under a series of constraints and assumptions.

Models to be used in circuit simulators for the analysis and design of integrated circuits must be *analytical* and *simple* enough to enable simulations lasting not more than some tens of minutes even in the extreme case of transient analysis.

Thus, several hypothesis and limitations must be introduced.

Analytical models are often derived for a "*prototype device*" with a very simplified physical description (one-dimensional structure, regional approach, abrupt doping variations from one region to another).

The physical effects associated to the two- or three-dimensional nature of real geometries and profiles are subsequently introduced by simply performing "semi-empirical" manipulations to basic models and to some parameters definition.

By doing so, for a given device one can find in circuit simulators a set of models (called *compact models*) with several degrees of complexity.

This result, which could appear strange at the first glance, is very useful from a practical point of view, as the designer can validate new ideas on circuit topologies by making simulations with simple (and thus low time-consuming) models, turning to the adoption of higher-order modelling when the basic circuit really works.

Additionally, in model derivation for computer-aided-design (CAD) purposes it is supposed that device current-voltage and charge-voltage relationships can be written in such a way that device networks associated with mathematical models can be implemented by a suitable connection of one-port or multi-terminal devices.

The estimation of values of the several parameters in the models are left to detailed comparisons with experimental data; in such a way, several of the parameters do not maintain a real physical meaning but acquire just the meaning of "fitting" or "semi-empirical parameters".

Moreover, models for transient analysis are obtained by simply adding to dc models nonlinear reactive one-port elements which are automatically skipped from circuit simulators during dc analysis.

Hence, on the basis of the above observations, in this work we will firstly briefly review the models of basic nonlinear one-port and multi-terminal devices and then we will present models used in circuit simulators for some of the more important semiconductor devices.

BASIC IDEAL ELEMENTS

Network Theory is a series of definitions, methods and assumptions used to analyse the properties of any electrical circuit, in both its quantitative (i.e. values of the electrical variables) and qualitative (i.e. properties of the circuit) behaviours.

All the electrical variables are unambiguously defined and the basic laws of the Theory are Kirchhoff's current and voltage laws.

In Linear Circuit Theory (3, 4), elementary one-port (resistors, capacitors, inductors, independent current and voltage sources), basic two-ports (ideal transformer, gyrator, controlled sources, ideal operational amplifier) and complex N-ports, obtained by connecting the basic elements, are constructed.

For nonlinear circuits one can proceed in a similar way, both introducing nonlinear versions of the above elements, and considering a wider range of basic elements (12, 14).

To characterize a nonlinear device, one can refer to the terminal voltage V and current I that may be readily measured externally, together with the charge Q and the magnetic flux Φ that can be either measured by appropriate instruments or indirectly obtained by integrating $I(t)$ and $V(t)$ functions:

$$Q(t) = Q_o + \int_{t_o}^{t} I(\tau)d\tau \qquad \Phi(t) = \Phi_o + \int_{t_o}^{t} V(\tau)d\tau \qquad (1)$$

Considering all possible pairwise combinations of the four variable (V, I, Q, Φ), the four unrelated combinations (V, I), (Φ, I), (Q, V) and (Φ, Q) define the four basic two-terminal network elements named *resistor*, *inductor*, *capacitor* and *memristor*, respectively.

Moreover, a two-terminal element is said to be time-invariant iff its constitutive relation does not depend explicitly on time, otherwise it is time-varying.

Figure 1 shows typical symbols used to denote these nonlinear elements and the links between the different variables involved in the definitions.

It is worthwhile to note that the dark band in each symbol necessarily distinguishes the two terminals when the element characteristic is not symmetric.

Obviously, if the element is linear, its characteristic remains unchanged after swapping the terminal and standard symbols can be used.

The nonlinear element shown in Figure 1 are truly basic not only because they include the three classical circuit elements as special cases but also because the value of their associated small-signal resistance, inductance, capacitance and memristance are frequency independent, i.e they do not change with the frequency ω of an infinitesimally small sinusoidal testing signal about any fixed operating point.

It is possible to generalize the above definitions to introduce an infinity variety of higher order basic circuit elements by means of the complementary signal pair $(V^{(\alpha)}, I^{(\beta)})$ (5).

In this general case, the constitutive relation consists of a system of nonlinear, algebraic, ordinary differential and/or integral equations involving both the terminal variables V and I and their higher order derivatives:

$$V^{(\alpha)}(t) \triangleq \frac{d^{\alpha}V(t)}{dt^{\alpha}} \quad \alpha \in \mathcal{Z}.$$
$$I^{(\beta)}(t) \triangleq \frac{d^{\beta}I(t)}{dt^{\beta}} \quad \beta \in \mathcal{Z}.$$

Assuming negative values to indicate integration, using this notation, one can classify resistor (0,0) and memristor $(-1,-1)$ as zeroth-order elements while inductor $(-1,0)$ and capacitor $(0,-1)$ as first-order element.

It is worth to notice that given $V(t)$ and $I(t)$, we can generate the corresponding kth-order voltage signal $V^{(k)}(t)$ or the hth-order current signal $I^{(h)}(t)$.

By doing so, the complementary signal pair $(V^{(k)}(t), I^{(h)}(t))$ represents physical signals and can therefore be measured by appropriate instrumentations.

Nonlinear Resistor and Sources

A nonlinear resistor is a one-port device defined by a constitutive relation denoted by the algebraic relationship

$$f_R(V, I) = 0 \qquad (2)$$

Obviously, a resistor is said to be linear iff its constitutive relation is a straight line through the origin in the $V - I$ plane with a constant slope equal to R.

Relation (2) defines the so-called autonomous resistor, whereas if time is explicitly involved the resistor is said to be time dependent.

If, as often happens for real devices, an explicit single-valued relationship for the current versus voltage can be derived, previous equation can be rewritten as:

$$I = g(V) \qquad (3)$$

where function g is defined for the set of the admissible voltages for the resistor.

In this case, the resistor is said to be *voltage-controlled*. In the particular case in which current is independent of voltage, Eq. (4) becomes $I = I_o$ and describes a constant current source, and if the constant I_o is equal to zero one models an open circuit.

Alternatively, if the voltage can be written as a single-valued function of the current:

$$V = h(I) \qquad (4)$$

where function h is defined for the set of the admissible currents for the resistor, the resistor is said *current-controlled*.

In the particular case in which voltage is independent of current, i.e. $V = E_o$, one gets a constant voltage source, and if the constant E_o is equal to zero one describes a short circuit.

When relation (2) depends on some independent variable x one has a controlled resistor characterized by a family of $V - I$ curves, each of which corresponds to a specific value of the controlling variable.

A special class of controlled resistors includes the x-controlled voltage source and the x-controlled current source represented by $V - I$ curves that are independent of the terminal current I_x or voltage V_x, respectively.

If the controlling variable x is non electrical, the controlled source is usually called transducer, while when the controlling variable x is electrical, four type of nonlinear dependent sources extending the linear definitions are possible: voltage controlled voltage source (VCVS) $V = f(V_x)$, current controlled voltage source (CCVS) $V = f(I_x)$, current controlled current source $I = f(I_x)$ (CCCS) and voltage controlled current source $I = f(V_x)$ (VCCS).

These elements can be modelled using only nonlinear resistor and linear controlled sources. As an example, Fig. 2 shows two possible equivalent circuit models for a VCVS and CCCS nonlinear controlled source described by f_1 and

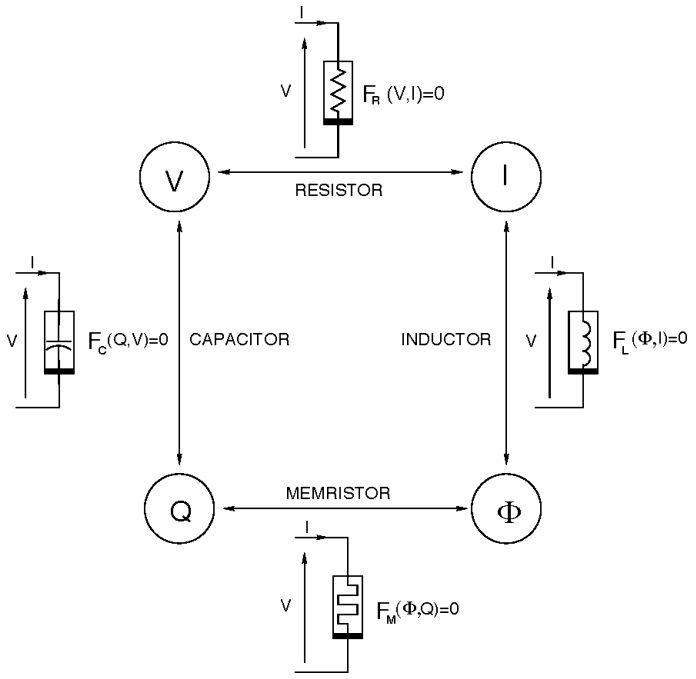

Figure 1. The four basic nonlinear elements and their symbols. Out of the possible pairings of the four basic variables V, I, Q and Φ, two are related by $I = \overset{2}{Q}$ and $V = \overset{2}{\Phi}$.

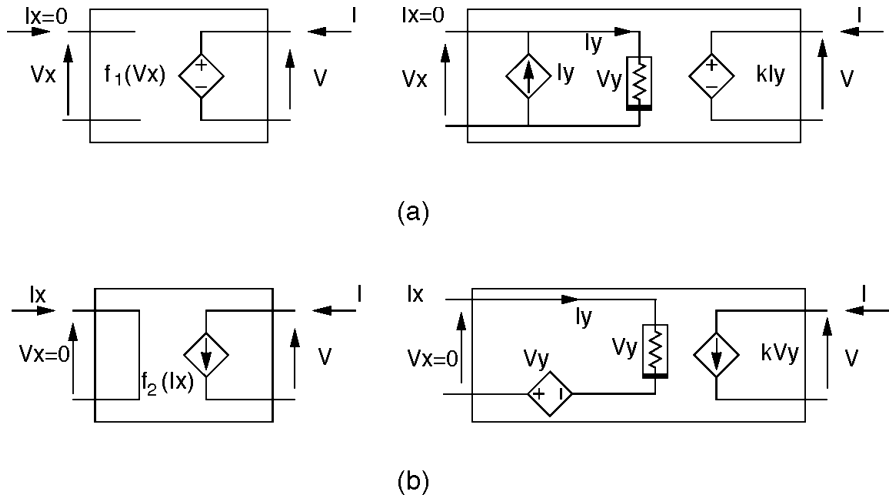

Figure 2. (a) A nonlinear Voltage Controlled Voltage Source (VCVS) (a) and (b) a nonlinear Current Controlled Current Source (CCCS) (b) together with two possible equivalent realization using linear controlled sources and nonlinear resistors.

f_2 functions and using nonlinear resistors with $I_y = k^{-1} f_1 (V_y)$ and $V_y = k^{-1} f_2 (I_y)$. Dually for the other two sources.

As well known (3), only a strictly monotonically increasing resistor is both voltage-controlled and current-controlled and can therefore be described by Eqs. (4)–(5).

Another interesting nonlinear resistor is the ideal diode shown in Fig. 3(a), having a constitutive relation expressed by:

$$f(V, I) = \begin{cases} I = 0 & \text{for } V < 0 \\ V = 0 & \text{for } I > 0 \\ VI = 0 & \forall I, V \end{cases} \qquad (5)$$

If the diode is reverse biased ($V < 0$) the current is zero, i.e. the diode acts as an open circuit, while if it is conducting ($I > 0$) the voltage is zero, i.e. the diode acts as a short circuit.

In this case, as the resistor is controlled by neither current nor voltage, the general relation (2) must be used. The model for a physical junction diode Fig. 3(b) will be presented in the Subsection "Semiconductor Diode".

Nonlinear Capacitors

A nonlinear autonomous capacitor is a one port device defined by a constitutive relation denoted by the algebraic

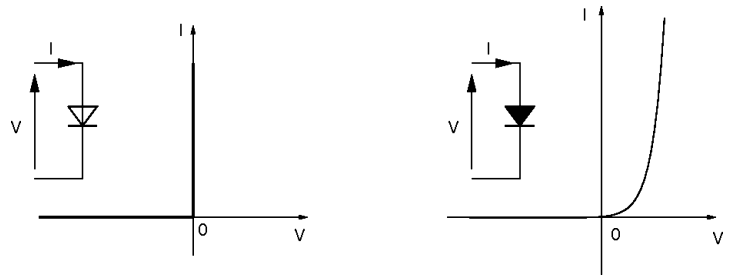

Figure 3. Symbols adopted for an ideal (a) and for a *pn* semiconductor junction diode (b) and their corresponding $I - V$ characteristics.

relationship

$$f_C(Q, V) = 0 \tag{6}$$

A capacitor is said to be linear iff its constitutive relation is a straight line through the origin in the plane $Q - V$ with a constant slope equal to C.

As for the resistor, it is possible to define a time-dependent capacitor and a controlled-capacitor, characterized by a family of $Q - V$ curves, each of which corresponds to a specific value of the controlling variable.

As, it often happens, one can give an explicit analytic form for the constitutive relation of the type

$$Q = q(V) \tag{7}$$

a nonlinear voltage-controlled capacitor results, while if one has

$$V = v(Q) \tag{8}$$

the capacitor is charge controlled. In particular, starting from Eq. (8), the current can be expressed in term of an incremental capacitance $C(V(t))$

$$I(t) = \frac{dq(V(t))}{dV}\frac{dV(t)}{dt} = C(V(t))\frac{dV(t)}{dt} \tag{9}$$

It is worth notice that the incremental capacitance is a function of the capacitor voltage and become a constant only in the case of a linear capacitor.

As an example of nonlinear capacitor (see Fig. 8) one can consider the following simplified formulation between the depletion region charge Q and junction voltage V for a reverse-biased *pn* junction diode (varactor):

$$Q = Q_o\left(1 - \frac{V}{V_J}\right)^{1-m} \qquad V < V_J \tag{10}$$

where V is the operating voltage, while Q_o, V_J and m are suitable constant parameters. Because the relation (10) is defined for $V < V_J$, this capacitor is not voltage-controlled for all values of voltage.

In a similar way, for a two-terminal MOS structure, one achieves the following relation between charge and applied gate bias (1):

$$Q = -C_{ox}(V - V_{FB} - \varphi_s - \gamma\sqrt{\varphi_s})$$

where the surface potential ϕ_s is a strongly nonlinear function of V, while C_{ox}, V_{FB} and γ are constant parameters.

Nonlinear Inductors

A nonlinear inductor can be defined as a one-port device establishing a nonlinear relationship:

$$f_L(\Phi, I) = 0 \tag{11}$$

Eq. (13) defines the so-called autonomous inductor, but it is possible to define a time-dependent inductor and a controlled inductor, characterized by a family of $\Phi - I$ curves, each of which corresponds to a specific value of the controlling variable. An inductor is said to be linear iff its constitutive relation is a straight line through the origin in the $\Phi - I$ plane with a constant slope equal to L.

Often, magnetic flux can be explicitly expressed as a function of the current:

$$\Phi = \varphi(I) \tag{12}$$

so the nonlinear inductor is said current-controlled, whereas it is flux controlled if

$$I = i(\Phi) \tag{13}$$

In the first case Eq. (14) can be expressed in term of an incremental inductance $L(I(t))$

$$V(t) = \frac{d\varphi(I(t))}{dI}\frac{dI(t)}{dt} = L(I(t))\frac{dI(t)}{dt} \tag{14}$$

For a linear inductor, the incremental inductance coincides with the inductance.

Two superconductors separated by a thin insulating layer such as oxide form a Josephson junction (6). A physical study proves that when contacts are built with the same metal, the current I varies sinusoidally with Φ, namely

$$I = I_0 \sin k\Phi \tag{15}$$

where I_0 is a device parameter and $k = 2e/\hbar$ a fundamental constant. This device is an example of a not current-controlled element, so its small-signal inductance is not uniquely defined. However, the Josephson junction is a flux-controlled device and can be classically modeled with a parallel connection of a linear capacitor C, a linear resistor R, and a nonlinear inductor L with the constitutive relation shown in Eq. (17).

A device made of a conducting wire wound around a ferromagnetic material shows a nonlinear measured $\Phi - I$ characteristic. In this case (see Fig. 5), the nonlinear behavior is due to the variation of the permeability of ferromagnetic materials with the applied magnetic field intensity.

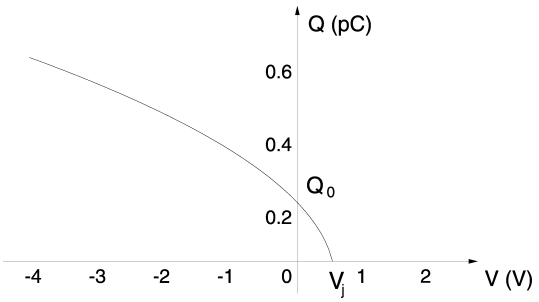

Figure 4. Nonlinear $Q - V$ characteristic referring to a depletion region charge Q as a function of junction voltage V.

The multi-valued function obtained applying a sinusoidal current excitation is commonly referred to as an hysteresis loop. A simple model describing this device operating under periodic excitation is mathematically defined by (7)

$$\dot{\Phi} = g[I - f(\Phi)] \tag{16}$$

and can be synthesized by connecting a nonlinear inductor described by $I_L = f(\Phi_L)$ in parallel with a nonlinear resistor characterized by $V_R = g(I_R)$ as shown in Fig. 6. In this case, g and f are continuous monotone increasing functions determined directly from the hysteresis loop.

Hysteretic phenomena are also deliberately introduced in circuits and systems. Generally speaking, one refers to hysteresis every time the value of the output depends on both the present and past value of the input. Usually one exploits this feature to build oscillators and noise rejection circuits such as comparators, Schmitt triggers and multivibrator circuits (8, 9) which find applications both in pulse and digital systems and have been recently used also in neural-type microsistems and to generate chaos (10). For this reason, only if parasitic energy storage elements such as lead inductance and capacitance of the interconnecting wires are included in the circuit model one can readily explain the jumps which occur measuring the physical circuit. In particular, a non monotone voltage-controlled resistor needs a small parasitic capacitor in parallel with it, while a model of a non monotone current-controlled resistor needs a series parasitic inductance to be complete (11).

Memristor

Finally, the memristor is a one port defined by a constitutive relation denoted by

$$f_M(\Phi, Q) = 0 \tag{17}$$

It is a component similar to a resistor but with memory capabilities (12).

In the Linear Circuit Theory, there is no need to introduce this element since it is equivalent to a linear resistor. In fact, derivating with respect to the time of the constitutive relation for a linear memristor $\Phi = RQ$ simply gives $V = RI$. A memristor is said to be linear iff its constitutive relation is a straight line through the origin in the $\Phi - Q$ plane with a slope equal to M. Differently, deriving with respect to time the nonlinear relation

$$\Phi = \varphi(Q)$$

leads to

$$V = \frac{d\varphi}{dQ} I = M(Q)I$$

that can be understood as a linear resistor described by Ohm's law, except that its small-signal resistance $M(Q)$ is not constant, but varies with the instantaneous value of the charge $Q(t) = \int_{-\infty}^{t} I(\tau)d\tau$.

Examples of physical devices showing a qualitative memristor-like behavior are thermistors, amorphous devices, some biological systems and, in general, switching and time-delay phenomena. Considering a negative temperature coefficient thermistor that can be described by

$$\frac{dT}{dt} = -\frac{\delta}{C}(T - T_0) + \frac{R(T_0)}{C}\exp\left[\beta\left(\frac{1}{T} - \frac{1}{T_0}\right)\right] I^2$$

one can model this device as current-controlled memristive one-port

$$V = R(T)I$$
$$R(T) = \left[R(T_0)\exp\left(-\frac{\beta}{T_0}\right)\right]\exp\left(\frac{\beta}{T}\right)$$

where $R(T_0)$ is the resistance measured at some reference temperature $T = T_0$, δ is the dissipation constant, C is the heat capacitance and β is a material constant (13).

Finally, this important element can be favorably use to model many quantum mechanical phenomena (tunneling, Coulomb blockade, ion-membrane dynamics) which are essential to the nonlinear dynamics of many modern (molecular and nano) devices.

MULTI-TERMINAL ELEMENTS

By means of the same approach used in the previous section, the concept of two-terminal element can be extended to characterize multi-terminal devices. In particular, one can select a set of measurable independent variables and take a series of external measurements to derive consistent relationships among the variables. Kirchhoff's current and voltage laws show that one terminal can be arbitrarily chosen to be the common, so that voltages of the remaining ones are measured with respect to it.

In this way, among the N currents entering the terminals and the N voltages between terminals, only $(N - 1)$ currents and $(N - 1)$ voltages are independent. In general, $N - 1$ distinct laboratory setups are required to completely

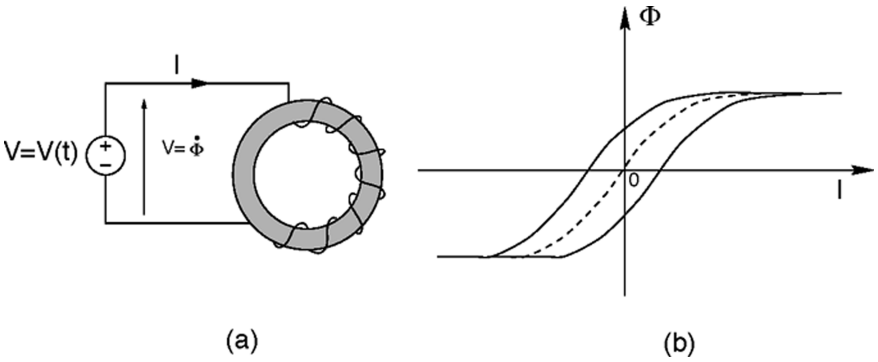

Figure 5. A nonlinear inductor driven by a periodic voltage signal (a) and the hysteresis loop associated with the steady-state waveform $\Phi(t)$ and $I(t)$.

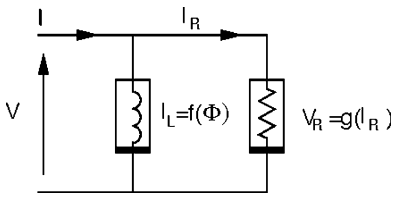

Figure 6. A simple lumped circuit model of hysteretic inductor operating under periodic excitation.

characterize an N–terminal element: each setup could involve as many sets of interesting variables (V_j, I_j, Q_j or Φ_j) curves as are necessary to include all desired combinations of parameter values of the controlling variables. Any independent combinations of these variables constitutes a valid set of measurements.

Similarly to the classification of two terminal elements, one can consider: N–terminal resistors, N–terminal capacitors, N–terminal inductors if the relationship involves only (V_j, I_j), (V_j, Q_j) (I_j, Φ_j), $j = 1 \cdots (N-1)$, respectively.

For example, ideal multi-terminal elements such as gyrators, ideal transformers, controlled sources and opamps are four-terminal resistors (3). Finally, there is another important class of networks called two-port resistors that transforms a given $V - I$ curve into a new $V' - I'$ one.

According to the type of transformation performed, they are called scalors, rotators and reflectors, together with mutators, i.e. linear algebric two-ports that are able to transform a basic network element (R, C, L, M) into an element of different type. These can be usefully adopted to generate many new nonlinear components (14).

Example 1

Under some simplifying assumption a three-terminal resistor is representative of many practical devices, such as bipolar, field-effect transistors and silicon-controlled rectifiers (SCR) (15).

A three-terminal resistor can be characterized by two separate sets of measurements: for example, the input and output characteristic curves. The first set is obtained by applying an independent source S_2 (which may be a voltage source or a current source) across terminals bc as show in Fig. 7(a) and measuring the $V_1 - I_1$ curve across terminals ac of the resulting two-terminal controlled element. For each value of the independent source S_2, a corresponding $V - I$ curve is obtained forming a whole family of $V_1 - I_1$ curves.

In a similar way, the second set is obtained by applying another independent source S_1 (which can be either a voltage source or a current source) across terminals ac as shown in Fig. 7(b) and measuring the $V_2 - I_2$ curve across terminals bc of the resulting two-terminal resistor. An analogous set of $V_2 - I_2$ curves can be plotted with the value of S_1 as a parameter. Additionally, any two sets of measurements which are independent of one another would be suitable forms of representation. As an example, Fig. 8 shows typical common-emitter input and output characterization for a *npn* bipolar transistor.

Of course, different choices of the independent variables and of the common terminal lead to different circuit descriptions. With four scalar variable V_1, V_2, I_1, I_2 and two equations, there are six different representations to characterize a resistive two-port that are summarized in Table 1 according to independent and dependent variables. These are current-controlled, voltage-controlled, hybrid and transition type representations that generalize the corresponding linear cases (3, 4). From a measurement accuracy point of view, it is desirable to choose a representation which involves only smoothly varying curve.

Table 1. Equations for the six possible representations of a nonlinear resistive two-port.

$V_1 = Z_1(I_1, I_2)$	$I_1 = Y_1(V_1, V_2)$
$V_2 = Z_2(I_1, I_2)$	$I_2 = Y_2(V_1, V_2)$
$V_1 = H_1(I_1, V_2)$	$I_1 = H_1'(V_1, I_2)$
$I_2 = H_2(I_1, V_2)$	$V_2 = H_2'(V_1, I_2)$
$V_1 = T_1(V_2, -I_2)$	$V_2 = T_1'(V_1, I_1)$
$I_1 = T_2(V_2, -I_2)$	$-I_2 = T_1'(V_1, I_1)$

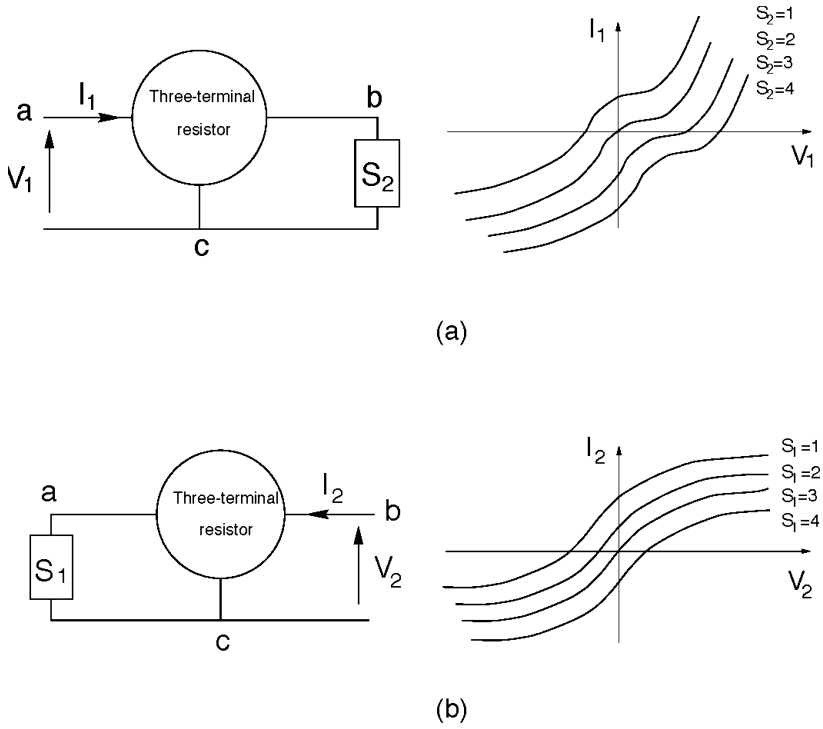

Figure 7. Typical setup for measuring the characteristic curves of a three-terminal resistor. Each set of curves can be interpreted as the $I - V$ curves of a two-terminal controlled resistor. In figure, terminal c is arbitrarily chosen to the common (ground) terminal

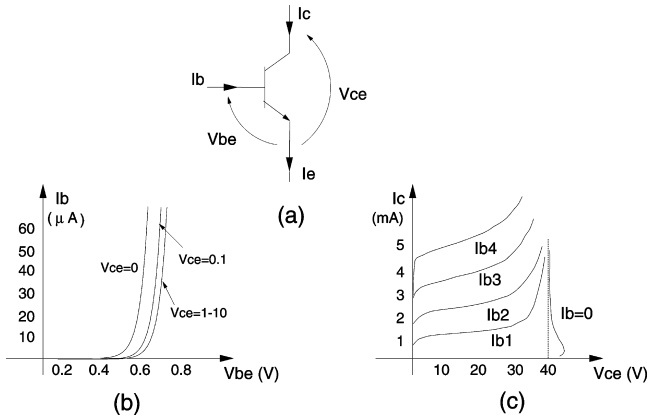

Figure 8. (a) The common-emitter configuration of a *npn* bipolar transistor. (b) Input $I_b - V_{be}$ characteristic with V_{ce} as a parameter and (c) output $I_c - V_{ce}$ characteristic with I_b as a parameter.

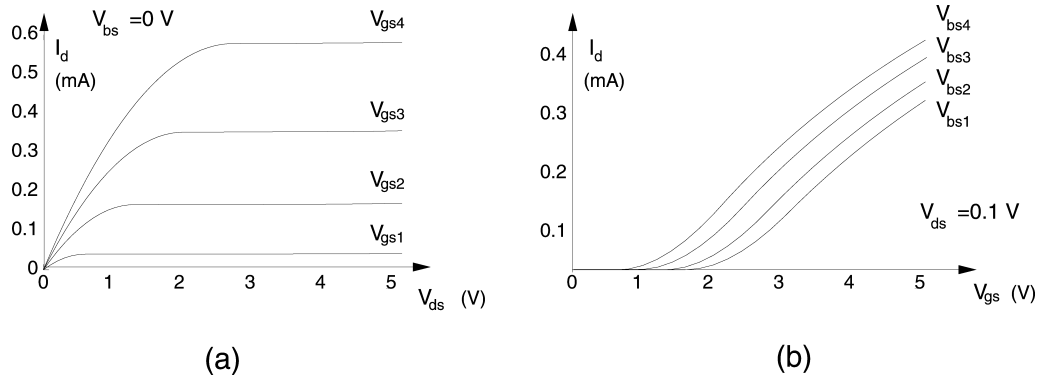

Figure 9. Typical characterization of a n-channel MOS transistor: (a) output characteristic $I_d - V_{ds}$ and (b) transcaracteristic $I_d - V_{gs}$.

It is worth notice that any N-terminal ($N > 3$) resistor can be considered as a three-terminal controlled resistor by connecting a voltage (or current) source between the remaining $N - 3$ terminal and the common reference. With these terminal voltages (or currents) fixed the resulting device can be characterized by the above described procedure. For example, the most important four-terminal resistor commercially available is the MOS transistor which when operates as a three-terminal device, is usually characterized by the two sets of $I - V$ characteristic curves shown in Fig. 9. With the *source* terminal fixed as common, the drain current I_d has been plotted against the *drain* and the *gate* voltages V_{ds} and V_{gs} respectively, considered *bulk* and *drain* biased with a constant voltage.

Example 2

A widely used example of four-terminal resistor is the operational amplifier (opamp) (see Fig. 10). This nonlinear resistor can be characterized by a finite gain model described by the three following relationships:

$$\begin{aligned} I_1 &= 0 \\ I_2 &= 0 \\ V_o &= \begin{cases} A(V_2 - V_1) & \text{if} |V_2 - V_1| < E \\ AE & \text{if} (V_2 - V_1) \geq E \\ -AE & \text{if} (V_2 - V_1) \leq -E \end{cases} \end{aligned} \tag{18}$$

where parameters A and E are called voltage gain and saturation voltage, respectively.

Thus, an operational amplifier acts as a nonlinear element if the magnitude of the input differential voltage exceeds the saturation voltage E (voltage comparator, threshold detector), while it operates as a linear device in the opposite case. In practice, operational amplifiers are built by a suitable connection of several devices such as bipolar, MOS or FET transistors, resistors and capacitors (16).

However, as in several applications there is no need of a detailed knowledge of the current and voltage behavior in all branches the amplifier, analog ICs manufacturers usually provide extremely simplified models for the entire circuits, called circuit macromodels (see the Subsection titled Circuit "Macromodelling").

DEVICE MODELS AND EQUIVALENT CIRCUIT MODELS

By definition, a circuit is equivalent to a given element iff they are indistinguishable when measured from their external terminals. This is a very strong requirement that, in most practical cases, forces to consider *circuit model* as approximately equivalent circuits. For this reason a model of an electronic device should ideally reproduce the same electrical behavior of the real device when connected with an appropriate excitation network and the results predicted from the model should represent a good approximation of the validating data constituted by the set of measured admissible voltage-current pairs. Depending on the applications, the acceptable error may be rather small (less than 5%) as in many analog signal processing applications or it may be quite large if one is interested only in the device model's qualitative performance. Additionally, a device model must avoid non-physical situations when it is used together with other models and should be able to predict previously unknown operating modes.

Two main different approaches are usually adopted in the derivation of device models: (1) the *black-box approach* and (2) the *physical approach*. Black-box modelling is useful when device physics or device operating mechanisms are not well understood, or when the device is very complex and a physical approach would be impractical, as for VLSI circuits with billion of components. Experimental observations, mathematical modeling, model validation and implementation by suitably connection of nonlinear elements (nonlinear network synthesis) are the basic four steps involved in this approach. Thus, the black-box method uses analytical expressions that have a curve fitting nature, poor forecasting abilities and correlation between parameters but requires a shorter development time than physical modelling.

Conversely, the analytical modelling approach starts from a study of the physics and operating mechanisms of the device, so its accuracy depends on the validity of the hypothesis and of the approximations made in its derivation. For this approach, physical study, introduction of suitably simplified equations and solutions, and nonlinear network synthesis are the typical steps. Frequently, the correspondence with internal operating mechanism is used to build a rough circuit model that subsequently is completed with the inclusion of essential parasitic elements. The advantages of physical-based models are the ability to foresee new phenomena, the adoption of physical parameters and the possibility of use the correlation between model parameter to define realistic statistical or mismatch models (17). On the contrary, the long developing time, the poor re-usability and the limited accuracy associated to the approximations used in the analytical expressions are their main drawbacks.

Once a device model is derived, the associated parameters must be identified before a meaningful computer simulation of any real circuit can be carried out. This important task, known as *model parameter identification problem*, generally involves both *ad hoc* measurements and computer optimization techniques which may be rather expensive in terms of computer time. In fact, most model parameters are not independent from each other so the value given to one may influence the value of others. Moreover, the set of values may not be unique with respect to the same fitting to measured data because the phenomena described by certain parameters cannot be distinguished clearly from each other in the measured characteristics (f.i. Early effect and avalanche multiplications in bipolar and MOS transistors).

One of the most widespread parameter extraction method consists of simplifying model equations considering a particular device bias to eliminate neglectable equation factors. This *direct method* finds parameters by using either graphical procedures or simple numerical techniques such as linear regression.

Global methods adopt a different approach since they try to find most parameters at the same time starting from some typical values and then to use computer optimization techniques to optimize these parameters by minimizing the error between the measured and predicted results.

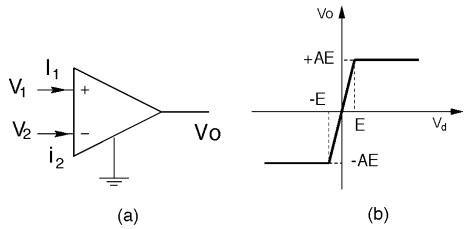

Figure 10. (a) Standard symbol of an operational amplifier and (b) the simple three-segment piecewise-linear relationship between the output voltage V_o and the differential input voltage $V_d = V_1 - V_2$ (transfer characteristic). The terminal voltages are measured with respect to the ground terminal.

The problem of model parameter extraction can be seen as an *optimization task*: a nonlinear function $\mathcal{F}(\mathcal{D}, \mathcal{S}; \mathcal{P})$ is minimized with respect to a set of parameters $\mathcal{P}$ constrained by a set of bonds $\mathcal{C}$. Function $\mathcal{F}$ describes the fitness between simulated (or computed) results $\mathcal{S}$ and a set of experimental data $\mathcal{D}$. This procedure leads to a set of parameter values that minimizes differences between simulation and validation data. In general, it is very difficult to find generally efficient methods for identifying model parameters, even for simpler models (37).

In the following Subsections, some analytical models for real devices often used in circuit simulators are presented and briefly discussed.

Semiconductor Diode

The electrical topology of a two-terminal semiconductor diode is shown in Fig. 11(a). The device can be modelled through the connection of three one-port components: a nonlinear resistor representing the voltage drops in the quasi-neutral regions and on ohmic contacts, a nonlinear capacitors representing both charge transit-time effects and depletion charge variations with voltage, and a nonlinear resistor (diode) representing the physical effects associated with charge transport from one region to another of the device. Thus, the constitutive equations for the diode model can be written as

$$I = I_d + I_c \tag{19}$$

$$V = V_1 + V_d = f_1(I) + V_d \tag{20}$$

$$I_d = I_s[\exp(V_d/nV_t) - 1] + I_b(V_d) \tag{21}$$

$$I_c = \tau \frac{dI_d}{dt} + \frac{dQ_j(V_d)}{dt} = \tau \frac{dI_d}{dt} + C_j(V_d)\frac{V_d}{dt} = C(V_d)\frac{dV_d}{dt} \tag{22}$$

where V_1 represents the voltage drop in the nonlinear series resistor, V_d is the voltage applied to the intrinsic diode, V_t the thermal voltage, τ the effective transit time, I_s the so-called diode saturation current, n the diode grading factor, while Q_j and C_j are the charge and depletion capacitance, respectively. Besides, $I_b(V_d)$ is a term that takes into account generation current in the space-charge region and breakdown phenomena for reverse-bias operation and is negligible for forward bias. The presence of a grading factor n always greater than 1 in real devices enables to model in a simple manner for non ideal effects. Additionally, to account for the finite physical dimensions of the junction, the depletion capacitance C_j can be expressed in the following way as a function of both area (bottom) and perimeter (sidewall):

$$C_j = C_{jb}\frac{A_s}{(1 - \frac{V}{\Psi_o})^{m_b}} + C_{jsw}\frac{P_{sw}}{(1 - \frac{V}{\Psi_s})^{m_{sw}}} \tag{23}$$

where A_s and P_{sw} are area and perimeter of the junction respectively. The two grading factors m_b and m_{sw}, due to the significant differences between the doping shapes in the direction of the main current flux and along the borders of the junction, differ from each other and are strongly process-dependent. Finally, the experimental current-voltage characteristic shows that the V_1 drop is significant only at high current levels; in this region, for the sake of easy modelling Eq. (25) can be substituted by $V_1 = RI$, where the series resistance R_s represents an average or "effective" value for the ohmic effects at high voltages.

Bipolar Transistor

The basic dc model for a three-terminal bipolar semiconductor transistor (BJT) can simply be represented through the so-called Ebers-Moll (EM) injection model (18, 19) reported in Fig. 12(a). Here the two diodes account for the direct injection of the carriers from the emitter (e) to the base (b) and from the collector (c) to the base, respectively. Only npn transistors will be considered here, since the same models would apply to pnp transistor with minor modifications. The two voltage-dependent current sources represent the fraction of the free carriers injected from the emitter reaching the quasi-neutral region of the collector, and the fraction of the free carriers injected from the collector reaching the quasi-neutral region of the emitter, respectively. With reference to a npn structure, the equations relating currents and voltages are simply given by:

$$I_e = I_{be}(V_{be}) + I_r(V_{bc}) \tag{24}$$

$$I_c = I_{bc}(V_{bc}) + I_f(V_{be}) \tag{25}$$

By exploiting the voltage-dependence associated with device physics one gets:

$$I_e = I_{es}(\exp(V_{be}/n_e V_t) - 1) - \alpha_R I_{bc} \tag{26}$$

$$I_c = I_{cs}(\exp(V_{bc}/n_c V_t) - 1) - \alpha_F I_{be} \tag{27}$$

where I_{es} and I_{cs} are the direct and reverse saturation currents (which depend on doping and junction areas), while n_e and n_c are called forward and reverse grading coefficients, and account for non ideal effects. Parameters α_F and α_R are the forward and reverse current-gains in the common-base configuration. Of course, in the normal forward operation mode, where the be-junction is forward bi-

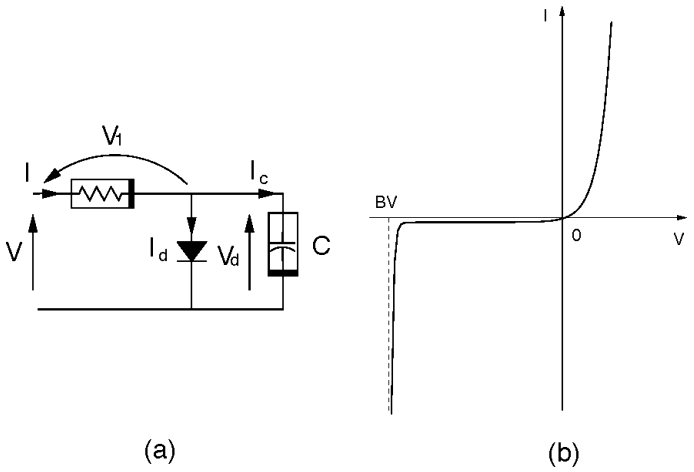

Figure 11. (a) Diode lumped model and (b) experimental $V - I$ characteristic.

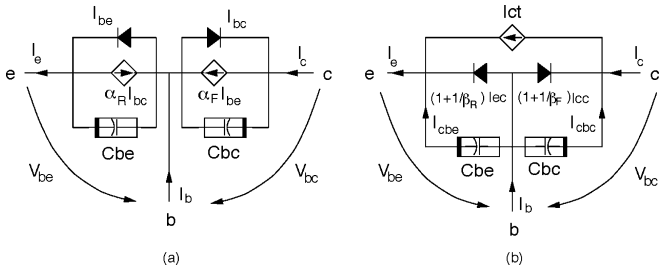

Figure 12. (a) Bipolar injection model and (b) transport model.

ased and the *bc*-junction is reversed biased, the current flowing through diode $I_{\rm bc}$ and current-generator $I_{\rm r}$ are negligible low so that device behavior can be represented only with diode current $I_{\rm be}$ and current source $I_{\rm f}$. Similar, but opposite, considerations can be developed for the normal reverse mode of operation. By considering that the sum of the emitter, base and collector currents must equal zero, a suitable rearrangement of Eqs. (31)–(32) leads to the following relationships

$$\begin{aligned} I_{\rm b} &= \frac{I_{\rm s}[\exp(V_{\rm be}/n_{\rm e}V_{\rm t})-1]}{\beta_F} + \frac{I_{\rm s}[\exp(V_{\rm bc}/n_{\rm c}V_{\rm t})-1]}{\beta_{\rm R}} \triangleq \frac{I_{\rm cc}}{\beta_{\rm F}} + \frac{I_{\rm ec}}{\beta_{\rm R}} \\ I_{\rm c} &= I_{\rm cc} - (1+\frac{1}{\beta_{\rm R}})I_{\rm ec} \triangleq I_{\rm ct} - \frac{I_{\rm ec}}{\beta_{\rm R}} \\ I_{\rm e} &= I_{\rm cc} - (1+\frac{1}{\beta_{\rm F}})I_{\rm ec} \triangleq I_{\rm ct} - \frac{I_{\rm cc}}{\beta_{\rm F}} \end{aligned} \tag{28}$$

where the transport saturation current $I_{\rm s}$ has been defined through the so-called reciprocity condition ($I_{\rm s} = \alpha_{\rm F}\ I_{\rm es} = \alpha_{\rm R}\ I_{\rm cs}$) and the forward and reverse current gains in the common emitter configuration

$$\beta_{\rm F} = \alpha_{\rm F}/(1-\alpha_{\rm F}) \quad \beta_{\rm R} = \alpha_{\rm R}/(1-\alpha_{\rm R}) \tag{29}$$

have been introduced. The equivalent circuit model corresponding to Eqs. (33), known as transport version of the Ebers-Moll model, is shown in Fig. 12(b) and has been implemented in most circuit simulators. The main differences between the two approaches lies in the reference currents used: (1) the injection model is based on the diode currents injected at the junction while (2) the transport model is based on the currents traversing the base region. Considering the approximations inherent in the model derivation, it turns on that the functional dependencies of model parameter in the case (2) are both more realistic from a physical point of view and simplify measurements procedures required for parameter determination.

It clearly appears that the device is completely modelled once the five (constant) parameters $I_{\rm s}$, $\beta_{\rm F}$, $\beta_{\rm R}$, $n_{\rm e}$ and $n_{\rm c}$ are known. Both the injection and transport model of Fig. 12 do not consider base-width modulation with bias and predict a constant collector (emitter) current $I_{\rm c}$ ($I_{\rm e}$) against *bc* (*be*) voltage for a device biased in the normal forward (reverse) mode. On the contrary, base-with modulation has a complex dependence on $V_{\rm be}$ and $V_{\rm bc}$. However, it has been experimentally found that for forward (reverse) operation the reduction in base-width strongly depends on $V_{\rm bc}$ ($V_{\rm be}$) and is practically independent of $V_{\rm be}$ ($V_{\rm bc}$) and induces an almost linearly increase in collector (emitter) current with respect to $V_{\rm bc}$ (or $V_{\rm be}$); in particular, Eqs. (33) can still be assumed valid by considering $\beta_{\rm F}$ and $\beta_{\rm R}$ simple function of $V_{\rm bc}$ and $V_{\rm be}$, respectively. Additionally, experimental results show that, as a first approximation, $\beta_{\rm F}$ and $\beta_{\rm R}$ can be substituted with the following simple expressions:

$$\beta_{\rm F} = \beta_{\rm FO}(1 - \frac{V_{\rm bc}}{V_{\rm AF}}); \quad \beta_{\rm R} = \beta_{\rm RO}(1 - \frac{V_{\rm be}}{V_{\rm AR}}) \tag{30}$$

where $\beta_{\rm FO}$ an $\beta_{\rm RO}$ can be interpreted as zero-bias forward and reverse common-emitter current gains, while parameters $V_{\rm AF}$ and $V_{\rm AR}$ represent the forward and reverse "effective" Early voltages.

Turning now to capacitive effects, one can notice that in a transistor, charge storage can be divided into two types: (1) voltage-dependent fixed charge in depletion regions and (2) current-dependent mobile charge. With reference to Fig.

12 the currents flowing through the two nonlinear capacitors C_{be} and C_{bc} represent both the effect of the effective transit time of injected carriers and of the depletion charges in the *be*-junction and in the *bc*-junction, respectively. Thus, similarly to capacitive currents in semiconductor diodes (see Eq. (27)), currents associated to charge variations can be expressed as:

$$I_{cbe} = \tau_F \frac{dI_{ec}}{dt} + \frac{dQ_{jbe}(V_{be})}{dt} = \tau_F \frac{dI_{ec}}{dt} + C_{jbe}(V_{be})\frac{dV_{be}}{dt} \quad (31)$$

$$I_{cbc} = \tau_R \frac{dI_{cc}}{dt} + \frac{dQ_{jbc}(V_{bc})}{dt} = \tau_R \frac{dI_{cc}}{dt} + C_{jbc}(V_{bc})\frac{dV_{bc}}{dt} \quad (32)$$

where τ_F and τ_R are the forward and reverse "effective transit-time", respectively, while C_{jbe} and C_{jbc}, each of which has an area and a perimeter contribution (associated with the area and perimeter of *be*- and *bc*-junctions, respectively), are called base-emitter and base-collector depletion capacitance. It seems useful to notice that in practice for integrated circuits in which electrically isolation from one device to another is mandatory, most of the bipolar transistors have an additional (substrate) terminal. For standard operating conditions, the presence of the substrate does not alter circuit behavior; however, the substrate can influence circuit performance or can induce circuit failures during transients.

MOS Transistor

Unlike bipolar transistors, metal-oxide-semiconductor (MOS) transistors (often called MOSFETs) are intrinsically four-terminal components (1, 29). The simplest dc model for these devices can be represented as in Fig. 13 and is described by the following set of equations:

$$I_g = 0 \quad (33)$$

$$I_d = f_m(V_{gs}, V_{ds}, V_{bs}) - f_d(V_{db}) \quad (34)$$

$$I_b = f_d(V_{db}) + f_d(V_{sb}) \quad (35)$$

in which, as usual, the gate current I_g flowing through the dielectric gate oxide has been assumed equal to zero. Current $f_m(V_{gs}, V_{ds}, V_{bs})$ represents the main carrier (minority) flow from source to drain, while the two terms f_d (V_{db}) and f_d (V_{sb}) are associated with currents flowing through the drain-bulk (D_{db}) and source-bulk (D_{bs}) junctions, respectively, which must be reversed biased for the correct operation of the MOSFET.

Several relationships for f_m (V_{gs}, V_{ds}, V_{bs}) have been presented in the literature, depending on the degree of approximation requested to the model and to the maximum acceptable computer time. However, in principle, even for prototype transistors with dimensions significally larger than those encountered in standard CMOS VLSI technologies, analytical expressions for f_m (V_{gs}, V_{ds}, V_{bs}) can be derived only if strong hypothesis are assumed for the behavior of some physical variables, such as electric field, quasi-Fermi potentials and carrier distribution in the depletion layer. In particular, by assuming the so-called charge-sheet hypothesis (1), considering only the drift component of the channel current, and a constant surface potential as far as bulk charge distribution is concerned, for a *n*-channel device (i.e. a device in which electrons are the carriers flowing from source to drain), I_d can simply be expressed as:

$$I_d = \begin{cases} \frac{\beta}{2}[2(V_{gs} - V_T)V_{ds} - V_{ds}^2] & \text{for } V_{ds} > V_{gs} - V_T, \quad V_{gs} \geq V_T \\ \frac{\beta}{2}(V_{gs} - V_T)^2 & \text{for } V_{ds} > V_{gs} - V_T, \quad V_{gs} \geq V_T \\ 0 & \text{for } V_{gs} \leq V_T \end{cases} \quad (36)$$

where V_T is the threshold voltage, $\beta = \beta' (W/L)$ is the extrinsic conduction factor, W and L represent channel with and length respectively and $\beta' = \mu\, C_{ox} = \mu\, \epsilon_{ox}/t_{ox}$ is a physical parameter depending on effective carrier mobility μ, oxide permittivity ϵ_{ox} and gate oxide thickness t_{ox}.

The first two Eqs. (42) express the drain current in the above-threshold regime; in particular, the first one refers to the linear or triode regime, while the second one corresponds to the saturation region, being $V_{ds}^{sat} = V_{gs} - V_T$ (saturation voltage) the V_{ds} value corresponding to the transition point from triode to saturation. Besides, the third relationship means a zero drain current for a device in the sub-threshold regime. The threshold voltage V_T depends on source-substrate voltage V_{sb} and on device technology. For example, for a *n*-channel MOSFET one can write:

$$V_T = V_{T0} + \gamma(\sqrt{V_{sb} - 2\Phi_F} - \sqrt{2\Phi_F}) \quad (37)$$

where V_{T0} is the zero-bias threshold voltage and γ and $2\Phi_F$ are physical-technological parameters called body coefficient and inversion potential. In particular, $2\Phi_F$ depends only on substrate doping and temperature, while $\gamma = \sqrt{2\epsilon_{si} q N_A t_{ox}/\epsilon_{ox}}$ depends on both gate oxide thickness and substrate doping concentration N_A (ϵ_{si} is the silicon permettivity). Thus, the device behavior is completely defined once the four model parameters β', V_{T0}, γ and $2\Phi_F$ and device dimensions W and L are known. In particular, for given values of gate-source and bulk-source voltages, Eq. (41) predicts a constant drain current for high values of V_{ds}.

However, measured output characteristics show that I_d is not exactly constant, but almost linearly increasing with V_{ds} in the saturation region. This effects is physically due to a reduction in the electrical channel length with V_{ds} (channel length modulation) when the device operates in saturation and, similarly to what happens in bipolar devices through the β_F dependence on Early voltage, it could be modelled by introducing a dependence of the extrinsic conduction factor on drain voltage. However, to maintain continuity in both drain current and in its derivates in the transition point from triode to saturation, in compact MOSFET models for circuit simulation it is assumed that channel modulation holds also in the triode region, even though this in incorrect from a physical point of view. By so doing one can get for I_d the following simplified model (often called Level 1 MOSFET model in circuit simulators):

$$I_d = \begin{cases} \frac{\beta}{2}[2(V_{gs} - V_T)V_{ds} - V_{ds}^2](1 + \lambda V_{ds}) & \text{if } V_{ds} > V_{gs} - V_T,\, V_{gs} \geq V_T \\ \frac{\beta}{0}(V_{gs} - V_T)^2(1 + \lambda V_{ds}) & \text{if } V_{ds} < V_{gs} - V_T,\, V_{gs} \geq V_T \\ 0 & \text{if } V_{gs} \leq V_T \end{cases} \quad (38)$$

where λ is another "fitting" model parameter, called-channel length modulation parameter, which can be considered (apart a minus sign) as the reciprocal of the Early voltage for MOS transistors. Often, to take into account

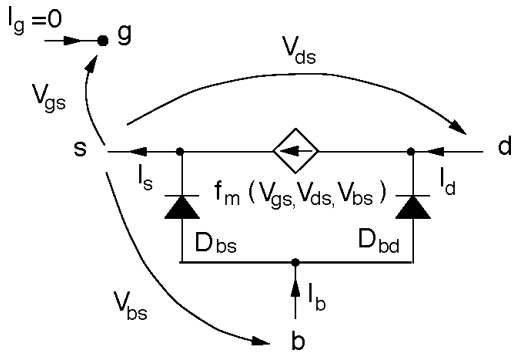

Figure 13. Large-signal circuit representation of the MOS transistor model.

also mobility reduction with electric field and, thus, to better fit experimental data, it is usual to render the intrinsic conduction factor β' a suitable function of both V_{gs} and V_{ds} (1).

Depending on the magnitude of the time-varying voltages, the dynamic operation can be classified as large signal operation or small signal operation. If the variation in voltages is sufficiently small, the device can be modeled with linear resistors, capacitors, current sources. Such a model is call a *small-signal model*. Otherwise, the device must represented by an analytical, nonlinear large-signal model. Both types of dynamic operation are influenced by device's capacitive effects. Thus, a capacitive model describing the intrinsic and extrinsic components of the device capacitance is an essential part of a compact MOSFET model for circuit simulation.

Turning now to capacitive effects, in a MOS transistors one has to consider both capacitive couplings associated with channel, substrate and gate charges in the intrinsic device, and capacitive effects associated with the non ideal fabrication processes. In the simple Meyer model (20), one assumes that: (1) capacitances in a MOSFET are reciprocal, that is $C_{gb} = C_{bg}$, $C_{gd} = C_{dg}$, $C_{gs} = C_{sg}$; (2) the change rate of gate charge Q_g is equal to change rate of channel charge when gate, source and drain bias changes. By so doing, one can introduce in the model (see Fig. 14) three interelectrodic capacitances C_{gs}, C_{gd} and C_{gb} (each of which is constituted by an intrinsic (nonlinear) and an extrinsic (linear) or "overlap" contribution) and two junction capacitances C_{js} (V_{sb}) and C_{jd} (V_{db}) whose voltage dependence is the same as the second term in Eq. (27). For the intrinsic components C'_{gj}($j = s, d, b$) of the interelectrodic capacitances, one can refer for example to the following usual definitions (1,19):

$$C'_{gs} = \frac{\partial Q_g}{\partial V_{gs}}|_{V_{gd}, V_{gb}} \quad C'_{gd} = \frac{\partial Q_g}{\partial V_{gd}}|_{V_{gs}, V_{gb}} \quad C'_{gb} = \frac{\partial Q_g}{\partial V_{gb}}|_{V_{gs}, V_{gd}}$$

where Q_g is the total gate charge. Within the same degree of approximation used to derive Eqs. (61), once defined the bulk charge as $Q_b = \gamma C_{ox} WL\sqrt{2\Phi_F + V_{bs}}$, for a device in the linear regime one has the following expression for Q_G:

$$Q_G = \frac{2}{3} WLC_{ox} \left[\frac{(V_{gd} - V_T)^3 - (V_{gs} - V_T)^3}{(V_{gd} - V_T)^2 - (V_{gs} - V_T)^2} \right] - Q_b$$

so we have:

$$\begin{aligned} C_{gs} &= \frac{2}{3} WLC_{ox}[1 - \frac{(V_{gd} - V_T)^2}{(V_{gs} - V_T + V_{gd} - V_T)^2}] \\ C_{gd} &= \frac{2}{3} WLC_{ox}[1 - \frac{(V_{gs} - V_T)^2}{(V_{gs} - V_T + V_{gd} - V_T)^2}] \\ C_{gb} &= 0 \end{aligned}$$

It is to be expected that C_{gb} is zero in strong inversion since the inversion layer in the channel from the drain to the source shields the gate from the bulk and prevents any response of the gate charge to a change in the substrate bias.

For a device in saturation ($V_{ds} > V_{dssat}$) the gate charge results:

$$Q_g = \frac{2}{3} WLC_{ox}(V_{gs} - V_T) - Q_b$$

and it is easy to obtain

$$C_{gs} = \frac{2}{3} WLC_{ox} \quad C_{gd} = C_{gb} = 0$$

Circuit Macromodelling: Operational Amplifiers

In principle, detailed electrical performances of complex integrated circuit or systems can be correctly predicted only if each device (whatever desired or parasitic) is represented by a proper device model. However, different degrees of approximation are required for the analysis and design of analog and digital ICs. The electrical performances to be simulated for the latter are usually logic levels, noise margins and delay time, while for the former one must correctly predict frequency response, phase margin, distortion, noise ..., and to do this it is extremely important to simulate several device details. In particular, designers of analog integrated circuits (whatever bipolar, CMOS and mixed bipolar-CMOS or BiCMOS (21)) must be very confident with device and circuit behavior and able to model with great accuracy the nuances in device and circuit performance and variations of these nuances with parameter variations. Conversely, quite different is the approach to circuit simulation of analog designers of circuits and systems which implement projects by simply interconnecting existing ICs and/or components or by interconnecting predesigned integrated building blocks (called macro-cells). The goal to reach with circuit simulation in these applications is a cheap and very fast prediction of circuit perfor-

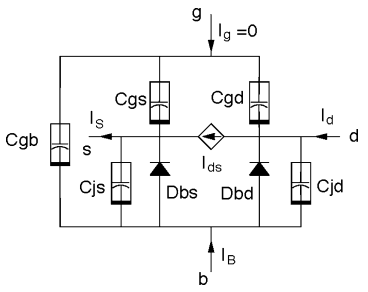

Figure 14. MOS transistor model complete with interelectrodic (C_{gs}, C_{gd}, C_{gb}) and junction (C_{js} (V_{sb}), C_{jd} (V_{db})) capacitances.

mance (f.i. the cut-off frequency of a filter), without the need of a detailed knowledge of the current and voltage behavior in all branches and nodes. Therefore, most of analog ICs factories render available to the users extremely simplified models for the entire circuits, called circuit macromodels, which neither model exactly device performance under all conditions nor fully replace bread-boarding for final verification. In fact, the aim of macromodelling is to obtain a circuit model of an IC, or a portion of an IC, which has a significantly reduced complexity to provide for smaller, less costly simulation time, or to allow the simulation of larger IC's or IC systems for the same time and cost. Thus, by using these macromodels one can obtain, within a given degree of approximation, the main pin-to-pin or pad-to-pad circuit performance.

Macromodels pose particularly difficult problems during circuit simulations. In particular: (1) if not all macromodel's equations are continuous, one can generate extremely large internal currents or voltages so that convergence problems arise, and (2) if some negative component values are used the solution can grow causing the simulator to fail if the time constant of the unstable mode is small compared to the transient analysis interval. Of course, as *a priori* not all circuit performance are considered, most of the elements in the macromodel are linear while the very few key nonlinear devices still present are usually modelled with basic device models discussed in Section Device and equivalent circuit models.

Operation amplifiers are common circuits that are suitably described by macromodels in order to simulate their non ideal characteristics. Advantages of this approach is evident considering that a typical IC opamp consists of about twenty transistors which, once simulated even by the simple Ebers-Moll model, would lead to over 160 components and 40 *pn* junctions.

Unlike the ideal opamp previously described, a real opamp is characterized by some particular features such as (1) finite input and output resistance ($R_i \neq \infty$, $R_o \neq 0$), (2) frequency-dependent open-loop voltage gain and phase shift, (3) output voltage limiting behavior and (4) finite limited slew-rate S_r defining the maximum time rate of change of the output voltage that can be attained under the worst case feedback configuration (usually unity-gain voltage follower).

Two most widely basic macromodeling techniques used are (1) simplification and (2) build-up (22). The former technique simplifies representative portions of the system circuitry by using simple ideal elements to replace numerous real elements. By so doing, the final model bears a strong resemblance to the real circuit. The latter technique implements circuit specifications by using composition of ideal elements, with no regard to resemble a portion of the actual circuit.

As an example, Figs. 15 and 16 show a full-transistor schematic and the macromodel circuit for a general-purpose typical FET-bipolar opamp (23). As can be seen, the macromodel (developed using both the aforementioned methodologies) represents the real opamp as a suitable connection of three stages: the input stage, the intermediate stage and the output buffer.

The input stage is an example of the simplification technique and in this case models the nonlinear input transfer characteristic and the input offset voltage. It includes a JFET input differential stage loaded with non ideal current sources which model the two active loads of the real circuit, while the current bias source of the stage is represented by the pair $2I_0$, RS. The voltage-dependent current source G_k draws a suitable current from the common source of the differential couple J1-J2 to give rise to an effect similar to that due to collector current of transistor Q_{12} that depends on the common mode voltage of the intermediate stage. The intermediate stage provides for open-loop gain, gain-bandwidth product, poles and zero frequency response and, together with the first stage, slew-rate. In particular, its single-ended part has been represented with a voltage dependent current source.

Finally, the output stage is modelled using the build-up technique and is devoted to the modelling of power dissipation, output impedance and maximum output voltage swing. The gain and the output resistance of such a stage have been modelled through GFOLL, R_{out} while diodes and the voltage sources V_{DCC} and V_{DEE} enable to achieve saturation values of the output voltage very close to those measured in the real opamp. Performance examples for this macromodel are summarized in Figs. 17 and 18.

Figure 17 refers to the common mode gain behavior showing comparison between full-circuit simulation and the simplification/build-up technique macromodel. Following Fig. 18 shows comparison between experimental and simulated slew performance of the opamp connected in the voltage-follower configuration. Of course, the macromodel proves itself useful to reduce computing time and essential to describe and control the main opamp behaviours.

Finally, let us notice that when non-frequently asked features of the opamp must be macromodelled, one has to refer to specifically devoted topologies (22–27).

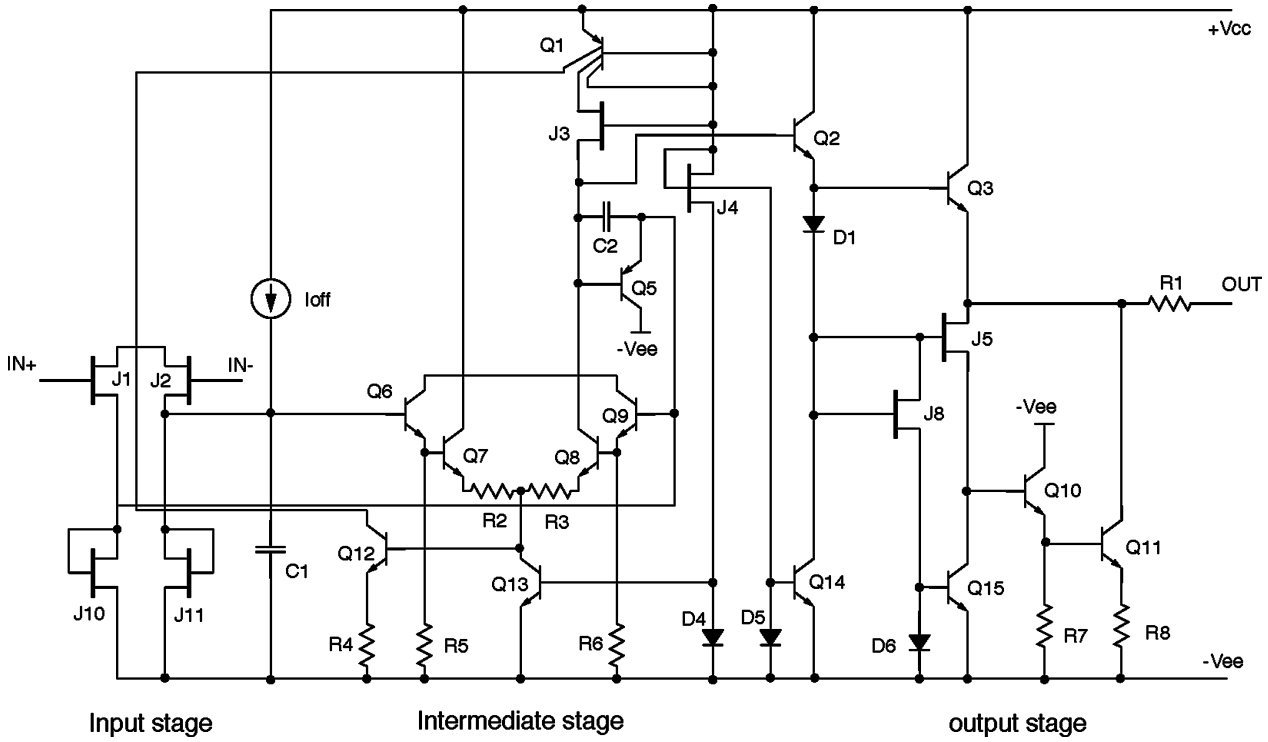

Figure 15. Schematic diagram of the LF355 operational amplifier.

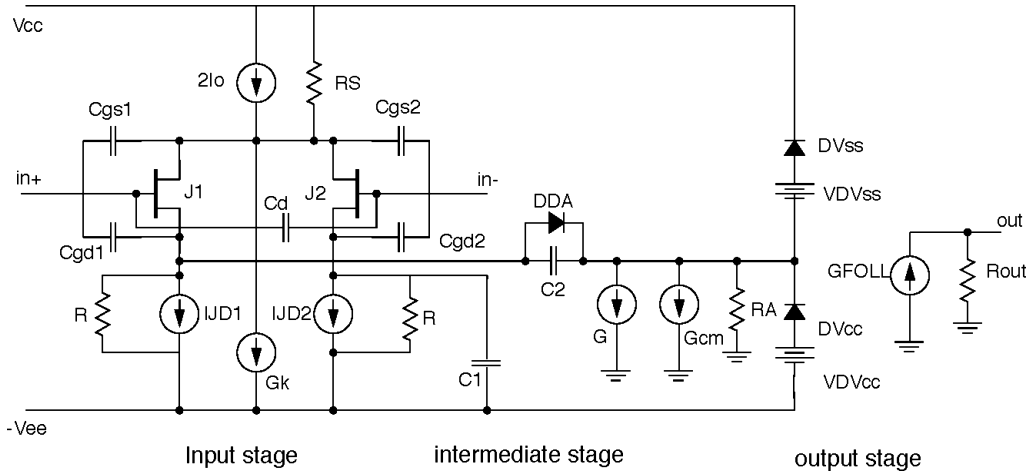

Figure 16. Macromodel circuit diagram for the LF355 operational amplifier in Fig. 15.

ADVANCED MODELS

Modern IC design is based on circuit simulation, the effectiveness of which depends on the accuracy and completeness of the compact models and characterization of the circuit elements and parasitics that comprise the IC.

In modern microelectronics VLSI technologies the channel length of MOSFETs and the base width of BJTs have very reduced physical dimensions; thus analytical models for these devices must be able to describe, at least in an approximate manner, several second-order physical phenomena associated with two- or three-dimensional effects. Compact model should be formulated physically, as functions of both the fundamental process parameters that control device electrical behaviour and the geometric layout parameter associated with a device.

The nonlinear equation solved in SPICE-like simulators generally require compact models to be formulated as equivalent networks. As already stated, this can be done by making voltage-controlled current and charge expressions more complex and by introducing in the models several additional pseudo-physical parameters and additional components. Although these empirical parameters, as much as possible a model and its parameters should be linked to the small number of physical parameters (junction depths, sheet resistance,doping levels) that control device electrical behaviour.

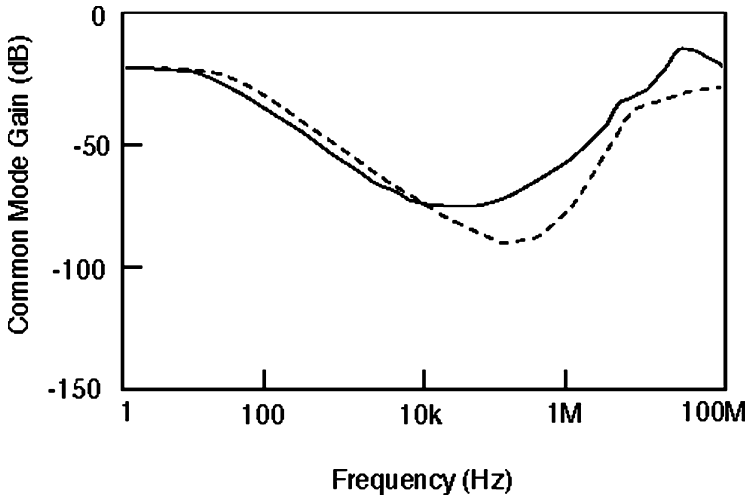

Figure 17. Common mode gain behaviour for the LF355 operational amplifier; comparison between full-circuit simulation (continuous line) and macromodel (dashed line).

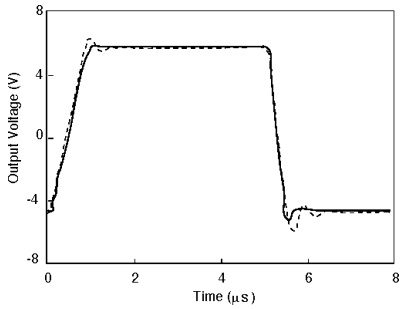

Figure 18. Experimental (line) and simulated (dots) slew performance of the LF355 operational amplifier connected in the voltage follower configuration for a −5V/5V input voltage step.

Advanced Bipolar Models

The first advanced model presented for the bipolar transistor was the very popular Gummel-Poon model (GP), which is implemented in practically all circuit simulators (19, 28). Starting from an original interpretation of the current flux in the transistor, based on the concept of an effective base-charge, the GP model was naturally able to describe several important physical effects. The model has the same topology of the transport Ebers-Moll shown in Fig. 12(b), so model equations are formally equal to Eqs. (33) with a suitable new definition of the saturation current. By so doing, current expressions are given by

$$\begin{aligned} I_{ct} &= \frac{I_{ss}}{q_b}\left[\exp\left(\frac{V_{be}}{V_t}\right) - \exp\left(\frac{V_{bc}}{V_t}\right)\right] \\ I_b &= \frac{I_{cc}}{\beta_F} + \frac{I_{ec}}{\beta_R} + C_2 I_{ss}\left[\exp\left(\frac{V_{be}}{n_e V_t}\right) - 1\right] \\ &\quad + C_4 I_{ss}\left[\exp\left(\frac{V_{bc}}{n_c V_t}\right) - 1\right] \end{aligned} \tag{39}$$

where the normalized base charge q_b can be expressed as:

$$q_b = \frac{q}{2} + \sqrt{\left(\frac{q_1}{2}\right)^2 + q_2} \tag{40}$$

and where

$$q_1 = 1 + \frac{V_{be}}{V_{AR}} + \frac{V_{bc}}{V_{AF}} \tag{41}$$

accounts for the Early effects associated with bias of both junctions, while

$$q_2 = B\,\frac{I_{ss}[\exp(V_{be}/V_t) - 1]}{I_{kf}} + \frac{I_{ss}[\exp(V_{bc}/V_t) - 1]}{I_{kr}} \tag{42}$$

models, through parameters I_{kf} and I_{kr}, high-level charge injection in both collector and emitter. The parameter B accounts for a larger transit time at high current density due to the increase of neutral base region (kirk effect) (29, 30). Base current expression is completed with two non ideal additional components which model, through parameters C_1, C_2, n_e and n_c, recombination in the space-charge regions (see Fig. 20), and series resistances between the internal nodes and the terminals account for the differences between internal and applied voltages, obtaining a significant improvement with respect to the previous EM model.

Recently, further improvements and modifications to the basic GP model have been introduced in some very advanced compact models for the BJT (31–35) implemented in public or proprietary circuit simulators. These new approaches model also the presence of the substrate terminal, series resistances associated to the finite conductance of the semiconductor layers, voltage-dependence of the buried layer conductance, avalanche breakdown, advanced modelling of base push-out and temperature dependence. Additionally, by adopting a different physical approach, new expressions for the base charge q_b have been developed.

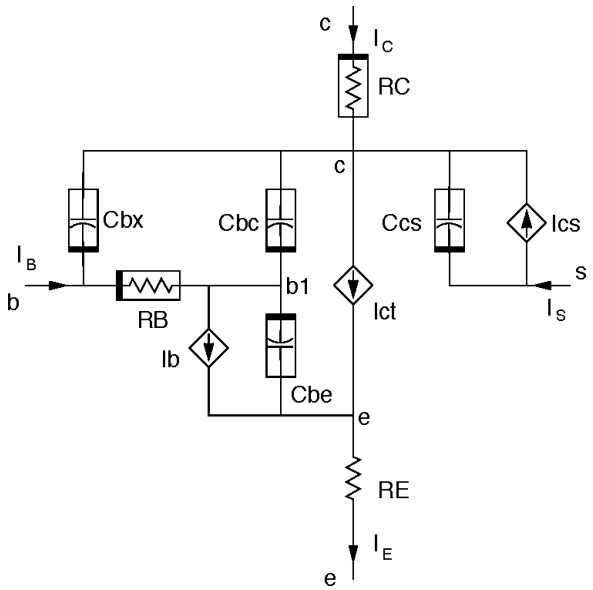

Figure 19. Circuit representation of the Gummel Poon model for a vertical *npn* bipolar transistor.

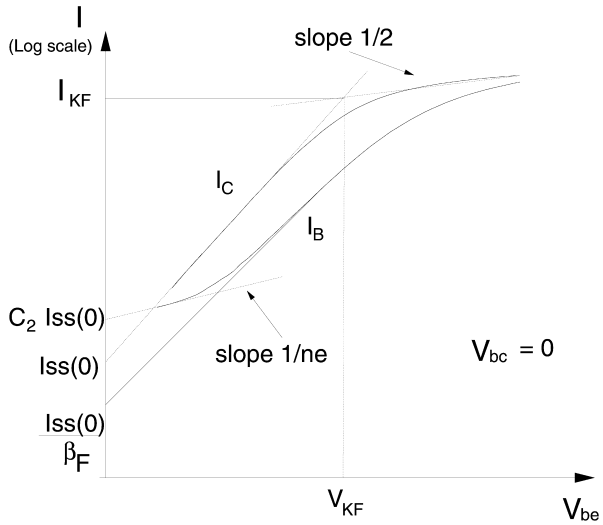

Figure 20. Plot of I_c and I_b versus V_{be} for $V_{bc} = 0$ showing the definitions of main parameters introduced with the Gummel Poon model.

For example, in Mextram model (34) one has

$$q_b = q_1(1+q_2) \quad q_1 = 1 + \frac{Q_{TE} + Q_{TC}}{Q_{B0}} \quad q_2 = 1 + \frac{Q_{BE} + Q_{BC}}{Q_{B0}}$$

where Q_{TE}, Q_{TC}, represent the depletion charges, Q_{BE}, Q_{BC} represent the diffusion charges directly obtained solving the differential equation for the majority carriers in the neutral base and Q_{B0} in the integral of the base charge. Unlike the Gummel Poon relation (40) that models the Early effect by using constant V_{AF} and V_{AR} parameters, this approach involves bias-dependent depletion charges which increase description of the Early voltage. Moreover, the model makes use of both constant (R_E, R_{CC}, R_{BC}) and variable (R_{b2}, R_{epi}) series resistance. The variable part of the base resistance is modulated by the base charges taking into account the base current crowding, while the epilayer resistance describes both current spreading in the epilayer and the decrease in resistance due to carrier injected from the base when internal base-collector junction is forward biased. Additionally, as at high frequencies and for steep transients the quasi-static hypothesis does not still apply, an excess phase shift, obtained by a suitable partitioning of the stored base charge and by introducing additional delay times, was implemented. This leads to both complex equivalent circuit models and current-voltage relationships: f.i. MEXTRAM equivalent circuit model shown in Fig. 21 have about 40 effective model parameters.

Another recent advanced model for high-speed/high-frequency bipolar applications is the HIgh CUrrent Model (HiCUM (35)). This model addressed some major disadvantages of the GP such as the poor descriptions of base resistance and junction capacitances in the regions of interest and inadequate description of both Si- and III-V material-based HBTs.

Among the major features of HiCUM we can mention the accurate description of the high-current operating re-

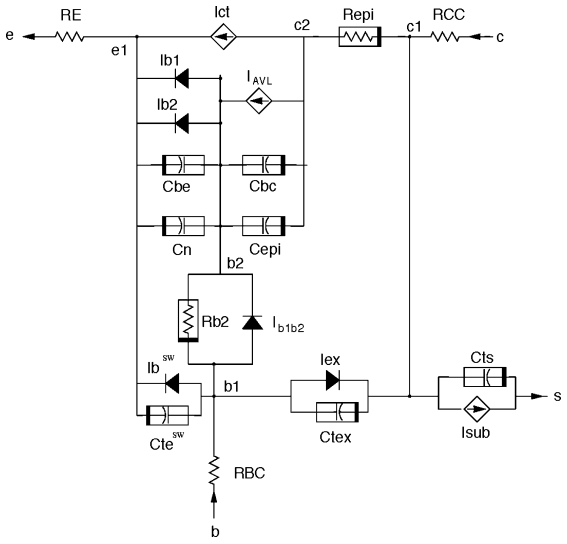

Figure 21. Mextram equivalent circuit for a vertical *npn* transistor. Current generator I_{avl} models avalanche multiplication current due to the high field in the space-charge region.

gion (including quasi-saturation and saturation), the distributed modelling of external base-collector region, self heating effects and sufficiently physical model equations allowing predictions of temperature and process variations, as well as scalability, even at high current densities.

Advanced MOSFET Models

The first attempt to ameliorate current-voltage behavior in MOSFET model was given by the so-called Level 2 model. This model copes with several short-channel effects such as the velocity saturation or the variation of the depletion charge along the length of the channel. This results in a more accurate but complex expression for the drain current I_{d}, leading to many convergence problems. For example, for a device in the triode region one has (20, 29)

$$I_{\mathrm{d}} = \frac{\mu W_{\mathrm{eff}} C_{\mathrm{ox}}}{L_{\mathrm{eff}}}\{(V_{\mathrm{gs}} - (V_{\mathrm{FB}} + 2\psi_{\mathrm{F}}))V_{\mathrm{ds}} - \frac{V_{\mathrm{ds}}^2}{2} - \frac{2}{3}\ f_{\mathrm{s}}\gamma[(V_{\mathrm{ds}} + 2\psi_{\mathrm{F}} - V_{\mathrm{bs}})^{3/2} - (2\psi_{\mathrm{F}} - V_{\mathrm{bs}})^{3/2}] - f_{\mathrm{n}}[\frac{V_{\mathrm{ds}}^2}{2} + (2\psi_{\mathrm{F}} - V_{\mathrm{bs}})V_{\mathrm{ds}}]\} \tag{43}$$

where f_{s} and f_{n} are two suitable parameters associated with two different phenomena: the decrease in the total depletion charge due to depletion region around source and drain (important in short-channel devices) and the increase in the depletion charge due to the spreading of the gate-induced depletion outside the channel edges and under the isolation (important in narrow-channel transistors). Additionally, to take into account carrier velocity against electrical field behavior and to have continuity in the drain current expression in the transition point from triode to saturation regime, a complex expression for the saturation voltage $V_{\mathrm{ds}}^{\mathrm{sat}}$ is adopted as well. A simplified version of Level 2 model based on semi-empirical considerations led to Level 3, a robust and popular model particularly suited for digital circuit design, but not very scalable and with discontinuities in the first derivative of the drain current (20).

The basic model formulation introduced in Subsection "MOS Transistor" revealed useful for devices with dimensions not lower than 5 μm. However, low-voltage high-speed VLSI CMOS circuits and systems require the availability of devices with very small geometry, so that advanced MOSFET models including several two- and three-dimensional effects are demanded from circuit designers.

From a topological point of view, compact models implemented in circuit simulators for these applications have the same topology of the basic circuit in Fig. 13, but with a quite different expression for the f_{m} ($V_{\mathrm{gs}}, V_{\mathrm{ds}}, V_{\mathrm{bs}}$) current-voltage relationship.

It is easy to understand that advanced models have become heavily empirical, with extensive mathematical conditioning. The number of model parameters has become very large, and most of these are basically empirical in character. Today, a general-purpose state of-the-art compact model consists of more than 300 equations and about 200 parameters containing both physical information such as oxide thickness or doping level and simplified descriptions of the physical effects such as mobility models. Often, the focus is mainly on the circuit simulation use of the device model, rather than on a physical description of the MOSFET and, therefore, mathematical fitness overrides physical understanding in the description of the device.

Compact models should be C^{∞}-continuous to enhance modeling accuracy and numerical performance, by avoiding problem, such as square roots or logarithms of negative numbers, exponential overflows. As a matter of fact, non-smooth models cause problems for dc convergence and parameter extraction and limit the order of integration that can be used for transient analysis.

In order to have continuity in the first derivatives of current equations with respect to voltages for the whole range of gate and drain biases, an extensive use of polynomial equations and other mathematical functions has been sometimes made, while in the more robust circuit

simulators and models smoothing functions have been implemented. The use of smoothing functions is particularly useful as it serves two interrelated purposes: (1) it eliminates the need to change equations at particular points (e.g. the V_{ds} voltage crosses the saturation voltage V_{ds}^{sat}), which allows for the use of a *single equation* for all regions of device operation (e.g. one unique expression for I_d rather than separate equations for weak-inversion, triode and saturation regions), and (2) it allows smooth and continuous derivatives to also be guaranteed, a very useful property in the development of the expressions for the device conductances and transconductances.

With the growth of both the number and empirical character of model parameters, increasing emphasis must be placed on parameter extraction; for examples, in the BSIM model (20) each parameter is made dependent on both effective channel length L_{eff} and width W_{eff} as

$$X = X_0 + \frac{X_L}{L_{eff}} + \frac{X_W}{W_{eff}} \tag{44}$$

through suitable fitting parameters X_0, X_L and X_W.

To model sub-threshold operation, in weak-inversion and moderate inversion Eq. (42) is substituted by a suitable exponential relation (similar to the one found in bipolar transistor) of the type:

$$I_d = I_0 \exp[\frac{(V_{gs} - V_T)}{nV_t}](1 - \exp[-\frac{V_{ds}}{V_T}])$$

where I_0 and n are fitting parameters. In particular, the slope factor n can be made a suitable linear function of both V_{bs} and V_{ds}, and *ad hoc* fitting expressions can be introduced to link the weak inversion current expression to the strong inversion expression. Of course, as most of the dependence are constructed on a semi-empirical basis, parameters provide little physical information, for example regarding the process technology.

Additionally, advanced models adopt a more robust and accurate charge approach to satisfy charge conservation and for a better efficiency in circuit simulations. The Meyer model described in Section "MOS Transistor" is simple and sufficiently accurate for many circuit applications but it has been found to yield non-physical results when used to simulate circuits that have charge storage nodes (such as MOS charge pumps, static RAM, switched-capacitor circuits, silicon-on-sapphire circuits) since charge built-up on these nodes is incorrectly predicted by the simulation (*charge non-conservation problem*). With the quasi-static assumption, all charges at each time t only depend on the values of terminal voltages at the same time, so we have

$$Q_j = Q_j(V_{gs}, V_{gd}, V_{gb}), \quad j = g, s, d, b$$

Moreover, the capacitances in a MOSFET cannot be arbitrary functions and the charge neutrality relationship

$$Q_g + Q_s + Q_d + Q_b = 0 \tag{45}$$

must be assured. Different capacitance models have been developed to solve the charge non-conservation problem. In order to ensure charge conservation, it can be shown that the reciprocity of the Meyer model requires Q_s to be independent of V_{ds} and V_{bs} and Q_d to be independent of V_{gs} and V_{bs}.

Another approach is the charge-based model in which the emphasis is put on the charge rather than the capacitance, from derivation through model implementation. The approach is to determine the charges in the drain, gate, source and bulk of a MOSFET and use them as state variables in the circuit simulation. Both the transient currents and the capacitances are obtained through mathematical differentiation of the charge with respect to time or voltage, respectively.

The charge-based capacitance model automatically ensures the charge conservation, as long as Eq. (59) is satisfied. The capacitive currents can be rewritten as

$$I_j = \frac{dQ_j}{dt} = \sum_{\substack{i \in \{g, s, d, b\} \\ i \neq j}} \frac{dQ_j}{dV_{ji}} \frac{dV_{ji}}{dt} \quad j = g, s, d, b; \tag{46}$$

By defining the following capacitances

$$\begin{cases} C_{ij} = \dfrac{dQ_i}{dV_j}, & i \neq j, i, j = g, s, d, b; \\ C_{ij} = -\dfrac{dQ_i}{dV_j}, & i = j. \end{cases} \tag{47}$$

and substituting Eq. (61) into Eq. (60) we can derive

$$\sum_{i \neq j} C_{ij} = \sum_{i \neq j} C_{ji} \tag{48}$$

so only 9 of the 16 capacitances are independent according to Eq. (62). The charge-based capacitance model needs the charge equations for all four terminals: Q_g and Q_b can be obtained directly by integrating the corresponding charge density over the channel. However it is difficult to model the charges on the source and drain terminals because only the total mobile channel charge $Q_i = Q_s + Q_d$ is known and a partition is needed. At $V_{ds} = 0$ the partition should be $Q_s = Q_d = Q_i/2$ due to symmetry, but several charge partition approaches have been suggested for the saturation region (50/50, 40/60, 0/100) that can be selected with a model parameter called. As an example, when >0.5, the 0/100 charge partition is chosen so $Q_s = Q_i$ and $Q_d = 0$ is assumed in the saturation region. Differently, $= 0.5$ and <0.5 assumes the 50/50 and 40/60 charge partition respectively. The latter choice is physically correct under the quasi-static condition as proven by 2D device simulation and experiments.

Among the tens of models proposed in the literature those which have reached a more assessed formulations and which are usually implemented in circuit simulators to analyze modern CMOS VLSI circuits are the BSIM3/4, MM9/11 and EKV models (20, 36). Their basic structure is similar to that of the previously described models but they make extensive use of smoothing functions to guarantee continuous and smooth expressions also for the charges. Moreover, in these last generation models one can also find dependencies that have been ignored in the past. Among these are threshold-voltage dependence on substrate and drain voltages, modelling of the breakdown for source-bulk and drain bulk-junctions, a sophisticated formulation for carrier mobility dependence on electric field components, advanced modelling for channel length modulation, gate-oxide leakage current due to traps in oxide, and tunneling current through oxide due to quantum-mechanical effect,

and non-quasistatic effects.

With the help of smoothing functions BSIM3 adopts a single-equation to describe device characteristics in various operating region (38). This eliminates the discontinuity in the *IV* and *CV* characteristics.

$$I_{\rm d} = \frac{W}{L}\,\mu_{\rm n} C'_{\rm ox} V_{\rm GST,eff}\left[1 - \frac{(1+\delta)V_{\rm DS,eff}}{2V_{\rm GST,eff} + 4kT/q}\right]V_{\rm DS,eff} \quad (49)$$

where $V_{\rm GST,eff}$ is a suitable smoothing function given by

$$\frac{V_{\rm GST,eff} = \frac{2nkT/q\, ln[1+exp(V_{\rm gs}-V_T}{2nkT/q})]}{\frac{1+2n\, exp(-V_{\rm gs}-V_T-2V_{\rm off}}{2nkT/q)}}, \quad (50)$$

that gradually changes the overdrive voltage $V_{\rm gs} - V_{\rm T}$ between two extreme values: when $V_{\rm gs} > V_{\rm T}$ then $V_{\rm GST,eff} \rightarrow V_{\rm gs} - V_{\rm T}$ and when $V_{\rm gs} < V_{\rm T}$ then $V_{\rm GST,eff} \rightarrow kT/q\ \exp[q(V_{\rm gs} - V_{\rm T} - V_{\rm off})/nkT]$. Similarly,

$$V_{\rm DS,eff} = V_{\rm DS,sat} - \frac{1}{2}(V_{\rm DS,sat} - V_{\rm ds} - \Delta + \sqrt{(V_{\rm DS,sat} - V_{\rm ds} - \Delta)^2 + 4V_{\rm DS,sat}\Delta}) \quad (51)$$

where the exact value of the parameter Δ determines the degree of smoothness in the transition between triode and saturation region. BSIM4 offers several improvements over BSIM3 in the transistor's noise modeling and in the incorporation of extrinsic parasitics (38).

MOS Model 9 employs simple smoothing functions similar to (65) to achieve continuity in device characteristics. It is accurate for sub-quarter micron technologies and exhibits good behaviours in circuit simulation. Recently, MOS Model 11 has been developed as the successor of Model 9. This new physics based model is particular suitable for digital, analog and RF CMOS technologies, and allows for a simple parameter extraction procedure, and it represent one of the first surface-potential based models (32).

While all other cited models employs source-referencing, the EKV (36) is the first one that uses the bulk-referencing method, so source and drain can be treated symmetrically, a particularly useful feature in analog circuits where the MOSFET is used bidirectionally. By developing a pich-off voltage $\frac{V_p = V_g - V_T}{n}$ which applies independently to the source and drain terminals, the weak-to-strong inversion transition and the linear-to-saturation transition (which are treated separately in other models) are both describes by the same weak-to-strong inversion model.

This fundamental philosophical change allows the EKV model a greater hope of fundamentally eliminating the asymmetry problems unavoidable in the source-referencing models. The normalized current in weak and in strong inversion can be expressed as

$$i_d \equiv \frac{I_D}{I_S} = i_f - i_r = F(v_p - v_s) - F(v_p - v_d)$$

where $i_f \equiv I_F/I_S$ is the forward normalized current which is also defined as the inversion coefficient and $i_r \equiv I_R/I_S$ is the reverse normalized current. The function $F(v) = [\ln(1 + e^{v/2})]^2$ is an interpolation function, which guarantees that the current equations and their derivatives are continuous and smooth.

The rapidly decreasing minimum channel-lengths in CMOS process leads to a drastic improvement of the high frequency performance that, combined with low-noise figures and low power consumption, make CMOS more suited for RF and high frequency applications, for which a good accuracy modelling of impedance, transconductance, circuit and voltage gain must be included in the model. As the device dimensions approach their fundamental limits, new physical phenomena become essential for the accurate reproduction of the device characteristics. Today, the threshold voltage-based MOSFET compact models ($V_{\rm T}$-based model) are considered standard but they proved to be inadequate for modeling future RF, mixed signal and low-voltage circuits. Some of the fundamental structural flaws of $V_{\rm T}$-based models include the use of source-referenced threshold voltage producing a singularity in the *IV* characteristic, nonphysical description of the moderate inversion region leading to erroneous results for the $G_{\rm m}/I_{\rm d}$ ratio, (an important figure of merit for analog designers) and inconsistent modeling of charges and currents producing negative transcapacitances. For these reasons, there is the need to replace $V_{\rm T}$-based models with either inversion charge ($Q_{\rm i}$) based or surface potential-based models ($\phi_{\rm s}$-based model).

Recent advances in this direction have brought both qualitative and quantitative improvement in the ability to simulate modern CMOS circuits. Moreover, surface-potential-based model includes both threshold-based and $Q_{\rm i}$-based methods as special cases that follow from the general approach under additional assumption. For all these regions, $\phi_{\rm s}$-based formulation seems to be the only viable foundation for the next generation of MOSFET compact models.

BIBLIOGRAPHY

1. Y. P. Tsividis, *The MOS Transistor*, New York: McGraw-Hill, 1988.
2. R. Beaufoy, J. J. Sparkes *The Junction Transistor as a Charge Controlled Device ATE Journal*, **13**: 310–327,October 1957.
3. L. O. Chua, C. A. Desoer and E. S. Kuh, *Linear and Nonlinear Circuits*, New York: McGraw-Hill, 1987.
4. C. A. Desoer and E. S. Kuh, *Basic Circuit Theory*, New York: McGraw-Hill, 1969.
5. L. O. Chua, Nonlinear Circuits IEEE Trans. *Circuits Syst.* **CAS-31**, 1984.
6. L. D. Landau, E. M. Lifshitz *Statistical Physics* Oxford: Pergamon, 1969.
7. L. O. Chua, K. A. Stromsmoe *Lumped circuit models for nonlinear inductors exhibiting hysteresis loops IEEE Trans. on Circuit Theory* **17**: 564–574,Nov 1970.
8. J. Millman, A. Grabel, *Microelectronics*, New York: McGraw-Hill, 1987.
9. D. A. Hodges, H. G. Jackson, R. A. Saleh *Analysis and Design of Digital Integrated Circuits in Deep Submicron Technology*, New York: McGraw-Hill, 2004.
10. K. Mitsubori and T. Saito,“ *A four-dimensional plus hysteresis chaotic generator*”, *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.* **41**: 782–789, 1994.

11. M. P. Kennedy, L. O. Chua Hysteresis in Electronic Circuits: a circuit theorist's perspective, *Int. Journal of Circuit Theory and Application*, **19**: 471–515, 1991.
12. M. Hasler and J. Neirynck, *Nonlinear Circuits*, Norwood: Arthech House, 1986.
13. L. O. Chua S. M. Kang *Memristive Devices and Systems Proc. IEEE*vol**64**pp. 209–223Feb. 1976.
14. L. O. Chua *Introduction to Nonlinear Network Theory* New York: McGraw-Hill, 1969.
15. S. Sze, K. K. Ng *Physics of Semiconductor Devices* 3rd ed., New York: John Wiley & Sons, 2006.
16. K. R. Laker and W. M. C. Sansen, *Design of Analog Integrated Circuits and Systems*, New York: McGraw-Hill, 1996.
17. S. W. Director, P. Feldmann, and K. Krishna, *Statistical integrated circuit design IEEE J. Solid-State Circuits* **28**: 193–202, 1993.
18. J. J. Ebers, J. L. Moll *Large-Signal Behavior of Junction Transistors, Proc. IRE*, **42**: 1761, 1954.
19. I. E. Getreu, *Modeling the Bipolar Transistor*, Amsterdam: Elsevier, 1976.
20. D. Foty *MOSFET Modeling with SPICE* New York: Prentice Hall, 1997.
21. P. R. Gray, P. J. Hurst, S. H. Lewis, R. G. Mayer *Analysis and design of Analog Integrated Circuits*, New York: John Wiley & Sons, 2001.
22. R. G. Meyer (ed.) *Integrated-Circuit Operational Amplifiers* IEEE Press, 1978.
23. G. R. Boyle, B. M. Cohn, D. O. Peterson, Macromodeling of Integrated Circuit Operational Amplifier, *IEEE J. Solid-State Circuits*, **SC-9**: 353–363, 1974.
24. D. Golzio, S. Graffi, Zs. M. V. Kovács, G. Masetti, Circuit Macromodels and Large-Signal Behaviour of FET-Input Operational Amplifiers *Int. Journal of Circuit Theory and applications*, **20**: 75–85 1992.
25. C. Hu, D. P. Leach, S.-P. Chan, An Improved Macromodel for Operational Amplifiers *Int. Journal of Circuit Theory and applications*, **18**: 189–203, 1990.
26. D. Golzio, S. Graffi, G. Masetti, New Macromodel and Measurements for the Analysis of EMI effects in 741 opamp Circuits *IEEE Trans. Electromagn. Compat.*, **33**: 25–34 1991.
27. G. Masetti *et al.*, Failures induced on analog integrated circuits from conveyed electromagnetic interferences: A review, *Microelectron. Rel.*, vol.**38**,p. 995, 1996.
28. H. K. Gummel, H. C. Poon, An Integral Charge Control Model of Bipolar Transistors *Bell Syst. Techn. J*, **49**: 827–851, 1970.
29. P. Antognetti, G. Massobrio *Semiconductor device Modeling with SPICE*, New York: McGraw-Hill, 1988.
30. R. S. Muller and T. I. Kamins, *Device Electronics for Integrated Circuits*, New York: John Wiley & Sons, 1986.
31. H. C. de Graaff and F. M. Klaassen, *Compact Transistor Modelling for Circuit Design*, Wien: Springer-Verlag, 1990.
32. R. van Langevelde, A. J. Scholten, D. B. Klaassen, *MOS11 Compact MOSFET Model Summary*.
33. C. McAndrew, J. A. Seitchik, D. F. Bowers, M. Dunn, M. Foisy, I. Getreu, M. McSwain, S. Moinian, J. Parker, D. J. Roulston, M. Schröter, P. van Wijnen, L. F. Wagner, VBIC'95, The Vertical Bipolar Inter-Company Model *IEEE J. Solid State Circuit* **31**: 1476–1483, 1996.
34. H. Stübing, H-M. Rein A Compact Physical Large-Signal Model for High-Speed Bipolar Transistors at High Current Densities *Part I and II IEEE Trans Elect Dev* **ED 34**, 1987.
35. A. Koldehoff, M. Schröter, and H.-M. Rein, A compact bipolar transistor model for very high-frequency applications with special regard to narrow stripes and high current densities, *Solid-State Electron.*, Vol.**36**,pp. 1035–1048, 1993.
36. C. Enz, F. Krummenacher, E. Vittoz An Analytical MOS Transistor Model Valid in All Regions of Operation and Dedicated to Low Voltage and Low Current Applications, *Analog Int. Circ. and Signal Proc.* **8**: 83–114, 1995.
37. F. Franzè, N. Speciale A Tabu Search Based Algorithm for Continuous Multiminima Problems, *International Journal for Numerical Methods in Engineering* **50**: 665–680, 2001.
38. W. Liu *MOSFET models for SPICE Simulation including BSIM3v3 and BSIM4*, John Wiley & Sons, Inc. 2001.
39. C. Galup-Montoro, M. C. Schneider *MOSFET Modeling for Circuit Analysis and Design*, World Scientific Publishing Co., 2007.

GUIDO MASETTI
NICOLÒ SPECIALE
D.E.I.S.-Università di
Bologna-Viale, Risorgimento
2, 40136, Bologna, Italy