TRANSLINEAR CIRCUITS

The concept of a *translinear circuit,* an approach to the realization of linear and nonlinear functions uniquely suited to implementation in monolithic bipolar integrated circuit (IC) form, was first realized by Gilbert in the mid-1960s. The principles were later articulated in two seminal papers, which described the application of translinear concepts to wideband amplifiers (1) and analog multipliers (2). Their design was based on the special properties of the bipolar junction transistor (BJT) and the use of a monolithic process was essential for accurate implementation. This was one of several novel ways in which translinear circuits differed radically from the discrete-transistor circuit design principles in use at that time. Another difference was the use of current-mode signal-processing, thereby making better use of the inherently large

dynamic range of the BJT, and achieving very high bandwidths; the dc to 500 MHz response of these circuits was remarkable at the time. Finally, unlike previous analog circuits, they were transistor-intensive and used few standard components such as resistors and capacitors.

The term *translinear* was coined only later (3). It now has a broader meaning and can be found in numerous articles and textbooks (4–8). The original translinear circuits consist of one or more *closed loops* of junctions operating with both fixed (bias) currents and variable (signal) currents. These are now called *translinear-loop* (TL) circuits. The *translinear-loop principle* (TLP) is a powerful rule that permits rapid assessment and analysis of the function of any given TL cell, as well as providing a route for synthesis.

The fundamental basis for translinear circuits is the accurate and dependable exponential relationship between the collector current, I_C, and the base-emitter voltage, V_{BE}, in the normal active region of operation, resulting in the well-known linear dependence of transconductance on the collector current, which is the basis of the word translinear. A remarkable aspect of the BJT is that this behavior is fundamentally independent of the device geometry (also referred to as device scaling), the impurity doping levels and profiles, or even of the technology; thus, a heterojunction transistor (using, for example, SiGe, GaAs, or InP) exhibits the same translinear qualities as a silicon homojunction BJT.

The broader contemporary meaning of the term embraces any cell in which the characteristic exponential behavior of a BJT is essential to the circuit function. Such circuits need not employ closed loops of junctions. A simple example is the *bipolar differential pair,* the basis of numerous monolithic circuits, which may profitably be viewed in translinear terms. This perspective is particularly valuable in developing complex nonlinear functions using very efficient cell structures. These are called *translinear network* (TN) cells. Examples of advanced TN design include circuits capable of exactly generating all the trigonometric functions using fully analog means (9), ultralow distortion transconductance cells (10), all bipolar non-TL analog multipliers, logarithmic and variable-gain amplifiers (11–15), log-domain filters (16,17) and much else.

Metal-oxide-semiconductor (MOS) transistors, in both their single-polarity and complementary (CMOS) form, using devices having a relatively long channel and operating in the weak inversion (also called subthreshold) region, are capable of exhibiting approximately exponential behavior, and can be used to realize the entire families of both TL and TN cells, but at lower speeds and with lower accuracy than their BJT counterparts. A considerable body of literature is devoted to MOS design methods invoking exponential device behavior.

An even broader interpretation of the term has been proposed based on the quite different assumption that the transconductance of MOS transistors in strong inversion is a linear function of (though not directly proportional to) the gate-source voltage. Several analogous loop topologies, named MOS translinear (MTL), have been proposed by Seevinck (18) and others (19,20). Unfortunately, the mathematical relationships and resulting equations are much less tractable, and few *compelling* examples of cells based on this idea have been offered to date. Furthermore, the underlying quadratic I_{DS} assumption, the starting point for the analysis and synthesis of MTL cells, is only approximate, departing significantly from the ideal due to channel-length modulation and substrate effects, which are rarely addressed in the literature with the necessary realism.

Accordingly, the word *translinear* will here be reserved exclusively for cells invoking high-accuracy exponential device behavior, to avoid going beyond the spirit of the original proposal and risking uncertainty about the intended meaning of the term. The strong-inversion idealization using MOS technologies should be called *voltage-translinear,* or VTL, since the term MTL is ambiguous, and might imply either this square-law VTL mode or classical translinear operation using the devices in the subthreshold regime, where they are said to exhibit exponential behavior.

TRANSLINEAR CELLS

By the time the word *translinear* was coined in 1975 nearly 10 years had elapsed since the possibility of translinear operation was first realized. The first practical applications, in 1966, were in the context of high-bandwidth (500 MHz) variable-gain cells developed for use in oscilloscope vertical amplifiers. One of many outgrowths of this idea was a *linearized* wideband four-quadrant analog multiplier and the concurrent invention of a monolithic doubly balanced modulator (or mixer, a nonlinear multiplier), first reported in 1968 (21). This structure is now widely known as the *Gilbert Mixer* (sometimes, Gilbert Cell). However, during the patent search phase, prior art of a similar kind by Jones, but using discrete transistors and standard design techniques, was discovered (22) in the form of a synchronous detector which used an identical core topology, although it did not anticipate the important method for *linearizing* the multiplier.

An early example of translinear design is illustrated in Fig. 1; this is a wideband variable-gain amplifier (1), which in a modern realization can provide a bandwidth of several gigahertz. These unusual circuits shared certain common features:

1. They required the use of *monolithically integrated* bipolar junction transistors, because isothermal operation, tight matching of device geometry, and accurately controlled doping levels are essential. Although their possibility was conceivable from the invention of the BJT in 1947, the full realization of their potential had to await the availability of analog-quality process technologies, now refined to a high art.
2. The cells were simple and elegant, being largely comprised of *dc-coupled bipolar transistors and current sources,* with practically no dependence on passive elements (such as resistors and capacitors). Their transistor-intensive schematics seemed more suggestive of current-mode logic, compared with the familiar analog circuits of the time, supported by their extensive retinue of passive components.
3. The transistors were arranged in *closed loops,* each containing at least two base-emitter junctions (as in a current mirror) but usually four; occasionally, six, eight, or more junctions were used. *Overlapping loops* were frequently employed.

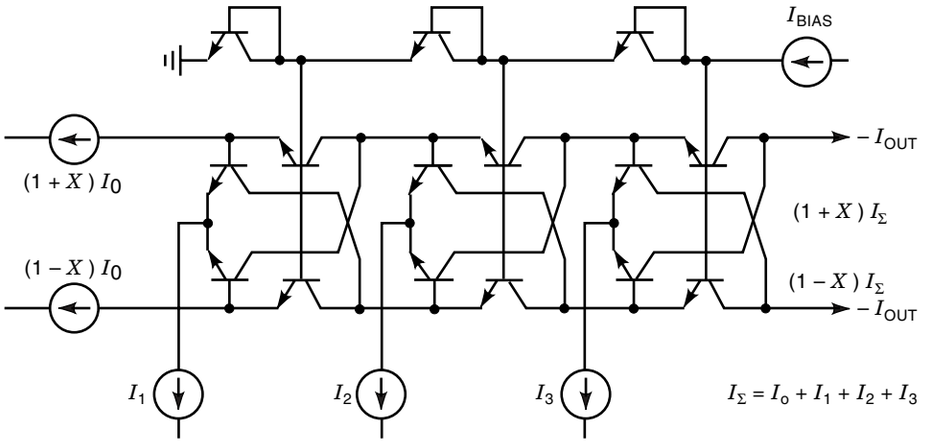


Figure 1. An illustrative translinear amplifier.

4. The signal variables—the cell inputs, outputs, and control biases—were all in *current-mode* form. Whatever voltages arose across the junctions were of only incidental importance, and were not used in analysis.
5. The *full-scale* voltage swings were very small—typically only a few tens of millivolts. (A change in I_C by a factor of ten changes V_{BE} by only 59.2 mV at 27°C, for an ideal BJT.)
6. The minimal branch impedances resulted in the *highest bandwidth.* The low impedances and low (incidental) voltage gains meant that collector-base and collector-substrate junction capacitances did not impact the circuit speed as seriously as in extant analog signal-processing circuits based on resistive loading and voltage-mode concepts.
7. Accurate operation of circuits of significant complexity was possible at *very low, single supply voltages*—down to 1 V in some cases; this was unusual at a time when standard supply voltages were ±15 V.
8. Unlike prevalent high-frequency analog signal-processing cells, these circuits exhibited highly-predictable, *fundamentally exact* and *temperature insensitive,* linear and nonlinear relationships between the signal variables—possibly their most valuable property.
9. Functional accuracy persisted right up to the extreme limits of the available operating range, not just a portion of this range.
10. Translinear-loop cells could implement a wide variety of *continuous-time algebraic functions,* including squaring, square-rooting, multiplication and division, multidimensional vector addition and subtraction, the direct computation of amplitude ratios in an array, polynomial, trigonometric, and implicit-form function generation, often within a few nanoseconds.

In a pre-microprocessor world, capabilities of this sort were potent assets of outstanding practical value, but their utility is undiminished today.

Current Mode Operation

During this period, the growing family of such cells were called *current-mode* circuits, since everything of importance about their behavior could be captured by a consideration of the junction currents alone. However, all cells in this class shared certain common topological features, for which a unique identifier was needed. Referring to them as current-mode was imprecise and lacked rigor, even though at that time there were few other circuits that operated in this mode.

In recent years, that term has been somewhat abused. Close inspection of the numerous papers on the topic of current-mode circuits shows that *both current and voltage* play an equal role in processing and transforming the signal. For example, the class of logic cells known as current-mode logic (CML) is not in any essential way current-mode. Current-mode logic gates merely make use of current-mode biasing, and steer currents under the control of the resulting gate output voltages. Current-feedback operational amplifiers are erroneously called current-mode circuits. Research papers have even reported on current-mode filters, which is clearly inappropriate, because an active filter fundamentally involves the continual interplay of current and voltage in the capacitors defining the frequency scaling. Thus, although one can readily conceive of a circuit that performs the nonlinear algebraic operation

$$U = \sqrt{(X^2 + Y^2 + Z^2)} \tag{1}$$

using only currents to represent the inputs X, Y, and Z and the output U, this is not possible in implementing the function $V_{out}(s) = V_{in}(s)/sT$, because analog-signal integration (in an inductorless embodiment) requires the accumulation of charge (through current flow) in a capacitor, thereby generating a voltage, which is then converted back to another current for subsequent integration. This inextricable codependence between voltage and current is found in the inverse operation of differentiation.

Translinear circuits are based on the remarkable fact that the transconductance of a BJT is linearly proportional to its collector current. Thus, the invented word *translinear* nicely

captured their nature, as well as identifying a certain class of topologies. The related exponential dependence of collector current on the base-emitter voltage is extraordinarily exact over six to eight decades for a modern bipolar transistor, and of great practical and commercial value. It remains applicable in the most aggressively scaled modern high-speed devices using fabrication methods radically different from those employed in the 1960s.

This key idea was envisaged as endowing the bipolar transistor with all the potential of a super-high-speed microelectronic slide-rule, the preeminent calculating aid of the time, whose ability to instantly determine products, quotients, and reciprocals was well-known to practicing engineers. A visual icon (Fig. 2) showing a BJT having a slide-rule where the emitter ought to be was used for many years in presentations of translinear concepts, to dramatically focus attention on this potential. Using two junctions in series was like adding lengths on the slide-rule scales to effect multiplication (Fig. 3).

Furthermore, the syllable *trans-* usefully conveyed the notion of a bridge between the familiar territory of linear circuits and their well-developed mathematics, and the uncharted terrain of nonlinear circuits and their often-transcendental equations, at a time when few nonlinear analog components were available in low-cost monolithic form. Nowadays, translinear principles are utilized in multipliers, mixers (23), modulators and demodulators, intermediate-frequency (IF) strips with automatic-gain-control (AGC) and many other variable-gain amplifiers (24,25), programmable filters (26,27), root-mean-square (RMS) circuits (28) for power measurement from line frequencies to several GHz (29) and other nonlinear circuits, such as those perfoming vector manipulation (30), and are hidden in numerous linear integrated circuits. For example, the classical four-transistor class AB output stage of many operational amplifiers (op-amps), the current conveyor, and current mirrors can be understood, analyzed, and optimized in translinear terms.

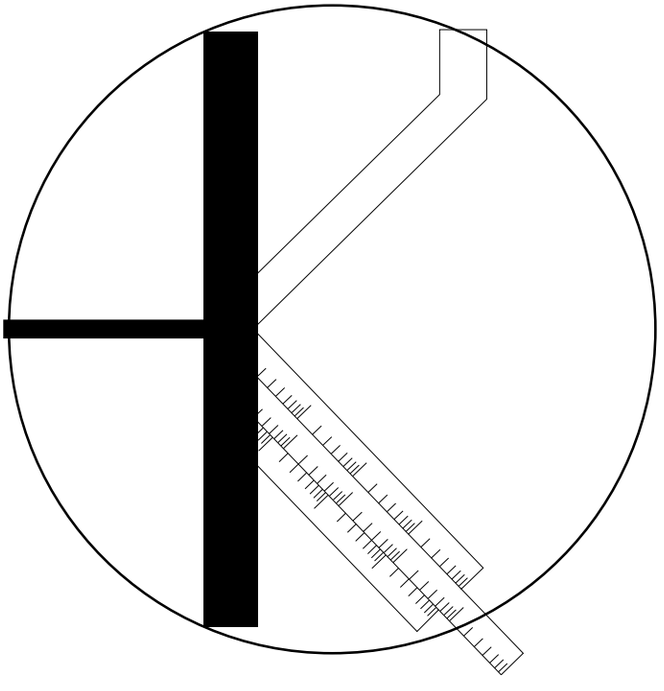


Figure 2. The microelectronic slide rule.

These circuits, which often involve loops of junctions within which the essential current relationships are generated, are called strictly translinear, or just TL. The cell function is essentially independent of the absolute magnitude of the operating currents, that is, the bias level. Instead it is a consequence of current ratios. Extensive use is made of the idea of a modulation factor to describe signals: this is a dimensionless variable, say x, in the range $0 < x < 1$, which represents the actual current-mode signals, $x\mathrm{I}_X$, $(1 - x)\mathrm{I}X$, or the alternative bipolar form, X, in the range $-1 < X < 1$, for example $(1 + X)I_X/2$, and so on. These forms are used in the simple four-quadrant multiplier cell shown in Fig. 4.

The cell function is invariant over bias levels I_O ranging from nanoamps (when operation is slow) up to milliamps (where the circuit remains useful at frequencies close to f_T, because voltage swings and internal impedances are at an absolute minimum). All TL functions remain exact right up to the limits of the available bias range and, most significantly, they are fundamentally insensitive to variations in temperature over the full range of operation possible with silicon. These were novel and still unique aspects of TL circuits not shared by any other basic analog cells. Note that the direction of current-flow in the transistors (CW or CCW) is an importance aspect of TL cells.

Modern Usage

Interest has recently focused on the possibility of exploiting translinearity in MOS transistors operated in the subthreshold regime, implying a linear dependence of the transconductance $\partial I_{DS}/\partial V_{GS}$ on the channel current. An early contributor to this field was Carver Mead (31), who used MOS translinear techniques to realize a wide variety of nonlinear functions in the development of artificial cochleas and retinas. Recently, higher-level learning and cognitive functions have been studied. Nanopower operation of CMOS translinear cells has broad utility in analog neural networks (32), which is an important and promising next step in the realization of artificial intelligence, leap-frogging an appeal to ever-faster Turing machines by replacing serially executed algorithms with highly interconnected parallel adaptive structures. It is of significance that such structures can benefit from all the nonlinear functions afforded by translinear techniques and implemented in an all-CMOS IC process to adequate accuracy by operating devices in the subthreshhold region.

Formal algebraic decomposition techniques, as precursors to cell synthesis, were developed by Seevinck (4), who later with Wiegerink (18) stretched the notion of translinearity further, asserting that junction field-effect transistors (JFETs) and MOS transistors in strong inversion exhibit transconductance, which is a linear function of the gate-source bias V_{GS}, starting with the popularly-assumed quadratic relationship $I_{GS} \propto (V_{GS} - V_{TH})^2$. Unfortunately, loops constructed of FETs generate awkward equations involving the sums of square-roots, quite unlike the powerful product/quotient form of classical TL.

More importantly, the underlying assumption is far from exact, even for long gate-lengths, and it becomes very unrelia-

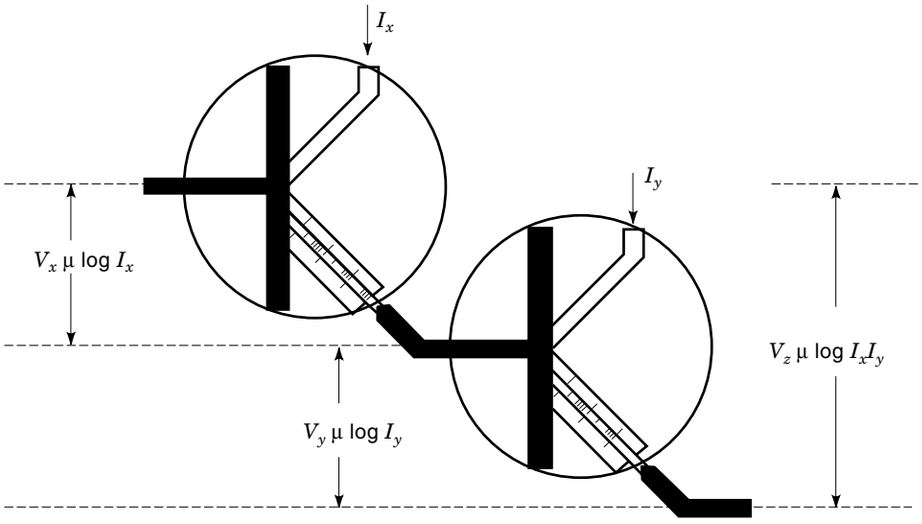


Figure 3. Multiplication using the microelectronic slide rule.

ble in a submicron realization, where the g_m more nearly approximates a linear function of I_{DS}. In the interest of preserving the important distinctions that first led to proposing the term translinear, and to minimize the confusion that results from using it in connection with the style of nonlinear design using closed loops involving the V_{GS} of MOS transistors in strong inversion, the latter are called VTL circuits. In this taxonomy, the unqualified adjective *translinear* implies classical current-mode translinearity where exponential behavior applies, which is accurate for all BJTs and other junction devices and approximately correct for MOS transistors in subthreshold operation.

Even beyond the domain of strictly translinear loops, the uniquely accurate, multidecade translinearity of the BJT has wide utility. Numerous circuits exist in which this valuable property, identified either in terms of transconductance linearly proportional to collector current, or equivalently, as collector current exponentially proportional to base-emitter voltage, is invoked. Thus, a translinear circuit is one in which the essential behavior arises directly from the exploitation of the exponential equations of the BJT, and of functions based on the intimately related hyperbolic trigonometric relationships.

Translinear Network Cells

A cell that invokes translinearity but does not utilize closed loops of junctions is called a *translinear network* (TN). The differential pair of Fig. 5 provides a simple example. It too can be analyzed using basic principles that hold for bias conditions from nanoamps to milliamps and are substantially independent of device scaling. This is a very different situation from that which prevails for MOS in strong inver-

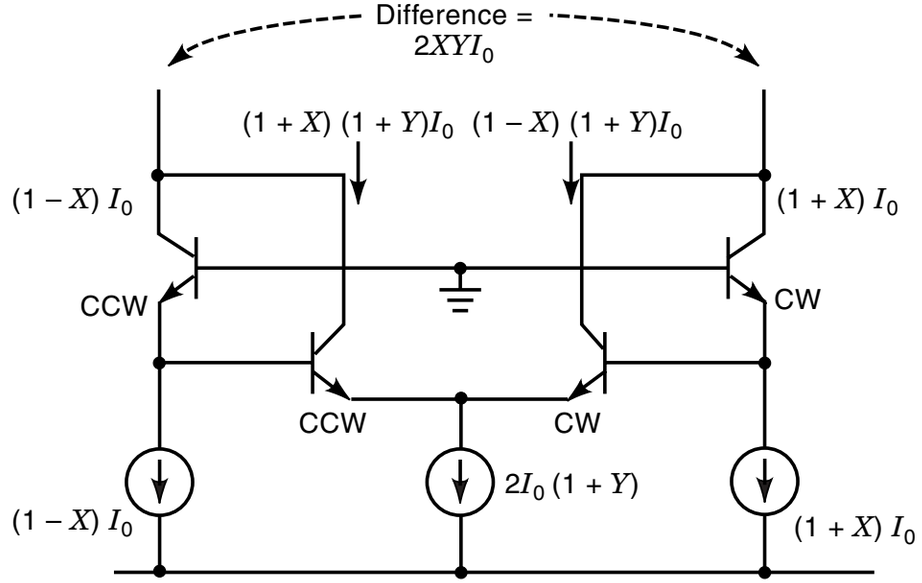


Figure 4. A basic TL (current-mode) multiplier.

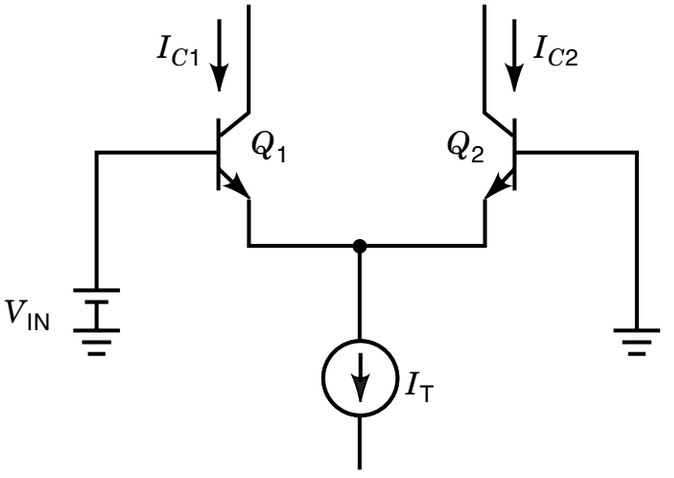


Figure 5. The BJT differential pair.

sion, where the choice of bias currents and W/L ratios for the devices, and back-gate bias, strongly affect the overall function.

The output current of a BJT differential-pair has precisely the same reliable form for any I_T, involving the hyperbolic tangent function:

$$I_{out} = I_{C1} - I_{C2} = I_T \tanh\left(\frac{V_{in}}{2V_T}\right) \quad V_T = \frac{kT}{q} \tag{2}$$

The transconductance is

$$g_m = \frac{\partial I_{out}}{\partial V_{in}} = \left(\frac{I_T}{2V_T}\right) \operatorname{sech}^2\left(\frac{V_{in}}{2V_T}\right) \tag{3}$$

A related class of TN cells provides the basis for low-noise, wideband, ultralinear, current-programmable transductors, useful in high-performance mixers and variable-gain cells. They are also of value in continuous-time filters and in oscillators whose frequency can be rendered proportional to bias current over a ratio of at least a million by the rigorous application of translinear principles.

An excellent example of a translinear network is the *multitanh* cell (10), the term referring to the use of a multiplicity of basic cells similar to Fig. 5, each exhibiting a hyperbolic tangent response between input voltage and output current. By introducing a set of offset voltages between the pairs of bases, and summing the pairs of collector currents (Fig. 6), the overlapping tanh functions can generate a very linear g_m function which, unlike a resistive degenerated cell, remains electronically controllable, being proportional to the currents I_T. A thorough treatment of these cells, including a variety of practical means to generate the offset voltages, is provided in Ref. 10. It is interesting to note that the same basic form as in Fig. 6, but having the pairs of collector currents connected in alternating antiphase, can provide a very exact synthesis of the sine function over an angular range of $\pm 720°$ (9).

Other adaptations are characterized by having multiple emitters tied to a common node and biased by one current (33,34). Such cells can also provide precise synthesis of the sine function; an example is shown in Fig. 7. When embedded in a larger structure, all the trigonometric functions, including the inverse functions (35), may be accurately generated at high speeds.

The TN view even extends to such unlikely circuits as the low-noise amplifiers (LNAs) used in modern communications systems (whose impedance-matching and intermodulation performance can be conveniently analyzed using a translinear approach); to ΔV_{BE} cells, used to generate a voltage proportional to absolute temperature (PTAT), and an integral part of band-gap voltage references; to CML logic gates; to special types of current mirrors; and much else.

The essential idea in all these cases is the way in which a device current I_X is exponentially related to an applied voltage V_X, thus: $I_X = I_O \exp(x)$. In this equation I_O is some normalizing current and $x = V_X/V_T$, where $V_T = kT/q$ evaluates to 25.86 mV. (Unless stated, data are for $T = 27°C$). The inverse logarithmic relationship $V_X = V_T \log(y)$, where $y = I_X/I_O$, is equally valuable in TN cells. This is used in the logarithmic amplifier shown in Fig. 8; here, the important scaling parameter I_O is provided by the saturation current, I_S, of the transistor. The TN approach to the design of such cells treats the BJT as a voltage-controlled current source, rather than relying on the nonrigorous and obsolete "beta-view" of a current-controlled current source.

TRANSLINEAR AMPLIFIERS

Translinear design first arose in the field of monolithic wideband fixed- and variable-gain amplifiers for oscilloscopes. Prevalent discrete-transistor amplifiers used balanced topologies. Methods were sought to implement fully integrated amplifiers also based on differential structures, but in a way better suited to a monolithic medium, such as a junction-isolated process having a peak f_T of 600 MHz. Using modern BJT processes having one hundred times higher peak f_Ts (60 GHz), translinear variable-gain amplifiers operating at 13 Gbits/s in optical-fiber receivers (13) and operation at over 30 GHz have been reported (14,15).

A cascade of cells of the sort shown in Fig. 5 can be continued indefinitely without the need for level shifting as shown in Fig. 9. Operation at a collector-emitter bias V_{CE} of >200 mV is usually satisfactory, permitting direct coupling of stages. The incremental voltage gain of each stage is $G_V = I_G R_G / 2V_T$ and thus proportional to each tail current. Using PTAT biasing, the voltage gain can be rendered stable with temperature. More elaborate biasing techniques can also desensitize the gain to variations in, for example, junction resistances and finite current gain and achieve highly robust performance in large-scale production (36).

The input-referred voltage-noise spectral density for an ideal BJT differential pair evaluates to 0.925 $nV/Hz^{1/2}$ at a tail bias I_G of 1 mA. This noise is inversely proportional to the square-root of I_G, being for example 2.9 $nV/Hz^{1/2}$ for $I_G = 100$ μA. Ohmic resistances generate Johnson noise; a base resistance of 50 Ω in each transistor adds a total of 1.29 $nV/Hz^{1/2}$, thus raising the input-referred noise at $I_G = 1$ mA to 1.59 $nV/Hz^{1/2}$.

The high sensitivity and low noise make amplifiers of this sort useful in many communications applications, in particular, in IF subsystems, where very high gain, and often a variable-gain capability, are required. However, the large-signal transfer characteristic of this TN amplifier is nonlinear; con-

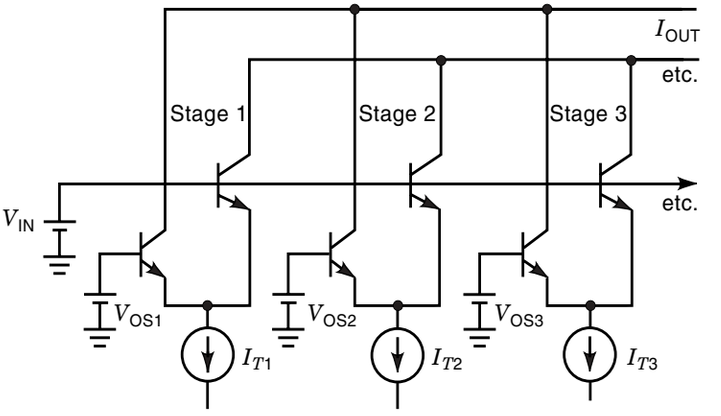


Figure 6. The generalized multi-tanh concept: a translinear network.

version to TL form can render the amplifier linear while preserving the gain-control feature. Each stage generates a differential output voltage $V_{CC'}$ that is related to its differential input voltage $V_{BB'}$ by

$$V_{CC'} = I_G R_G \tanh(V_{BB'}/2V_T) \tag{4}$$

For the overall cell function to be linear, the collector currents need to be a linear function of the input signal. These currents, which may be written as $(1 + X)I_G/2$ and $(1 - X)I_G/2$, where X is called is a modulation factor $-1 < X < 1$, generate a collector-to-collector voltage output of

$$V_{CC'} = R_G \left\{ \frac{(1+X)I_G}{2} - \frac{(1-X)I_G}{2} \right\} = XI_G R_G \tag{5}$$

From Eqs. (4) and (5) it is apparent that the base-to-base voltage $V_{BB'}$ required to result in a modulation factor of X must have the form

$$V_{BB'} = V_T \log \frac{1+X}{1-X} \tag{6}$$

Thus, the input voltage required to generate a certain value of X (typically having peak values of ± 0.75) depends neither on the value of the bias current I_G nor on the transistor geometry. Such a voltage can be generated by current-driving a similar pair of junctions with inputs (which may be the outputs from the preceding amplifier stage) already in current-mode form, as shown in Fig. 10, to generate a voltage of

$$V_{BB'} = V_T \log \frac{1+Z}{1-Z} \tag{7}$$

An input modulation factor of $Z = \pm 0.5$ would correspond to signal components of ± 500 μA for $I_Z = 1$ mA, but only ± 500 nA for $I_Z = 1$ μA. Nevertheless, Eq. (7) states that the voltage swing $V_{BB'}$ will be ± 28.4 mV for all values of I_Z. Thus, the sensitivity of this cell to the magnitude of its input current (that is, the transresistance $4V_T/I_Z$ for small signals) may be raised through control of I_Z.

When this fragment is combined with one of the differential amplifier stages of the sort shown in Fig. 9, we arrive at the simple four-transistor cell (1) shown in Fig. 11, which is noteworthy for several reasons:

1. The signal input, $I_{BB'}$, signal output, $I_{CC'}$, and gain-control means I_G and I_Z, are all in the form of currents, and the signal-induced voltage variations that arise inside the cell are *purely incidental.* The differential voltages

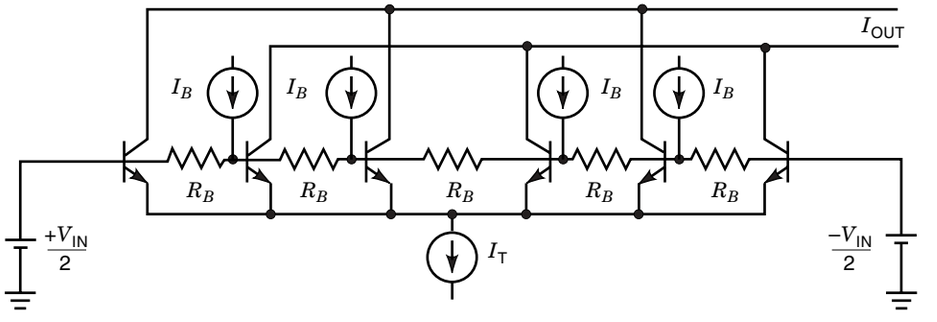


Figure 7. A translinear network for sine synthesis.

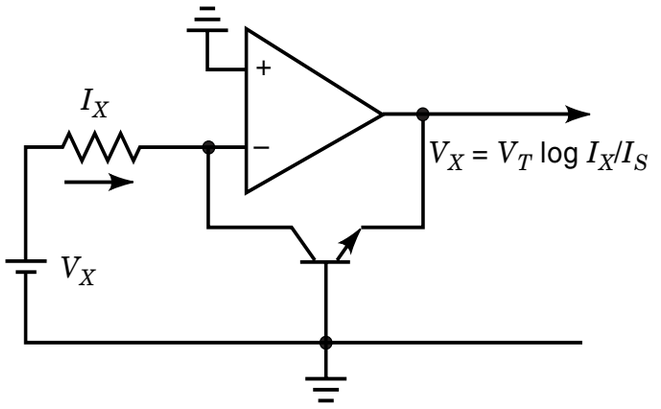


Figure 8. A translinear network for logarithmic conversion.

($V_{BB'}$) associated with the signal path are small, typically only ±50 mV for a full-scale modulation factor $X = \pm 0.75$. Note that, although $V_{BB'}$ is a nonlinear function of the signal, this is quite irrelevant to the accuracy of current-mode circuit function.

2. The current-mode gain G_I is proportional to the bias current I_G and inversely proportional to the bias current I_Z, that is

$$G_I = \frac{\partial I_{CC'}}{\partial I_{BB'}} = \frac{I_G}{I_Z} \tag{8}$$

This ratio can, in principle, be very high, limited only by the finite beta and device saturation at high currents due to internal collector resistance. If I_G and I_Z have the same "shape" over temperature, the gain is completely unaffected by temperature, within the limitations of device imperfections.

3. This is a large-signal result, that is, the transfer function is now fundamentally linear:

$$I_{CC'} = \frac{I_G}{I_Z} I_{BB'} \tag{9}$$

Thus, through an appeal to a current-mode synthesis, the strong nonlinearity of the exponential I_C/V_{BE} relationship has been entirely side-stepped, and relegated to a position of relevance only inside the cell. This large-signal linearity extends from zero current right up to the full bias current limit in each transistor, once again bearing in mind that certain nonideal aspects of real transistors will somewhat modify this result.

4. This cell introduces an important feature, namely, a loop of emitter-base junctions traceable through the four transistors, two of which have their current flow in a clockwise direction, two of them counter-clockwise. This is a necessity in all strictly translinear (TL) circuits, though loops may be of any size (usually between four and ten junctions) and two or more loops may overlap to produce interesting and useful results.

This cell has a further hidden benefit, namely its substantial insensitivity to the finite base currents of the output pair, Q_3/Q_4, with these two provisos: (a) the beta is essentially independent of the collector current; and (b) the base currents always remain less than the available input currents. The reason for this behavior, which is unique to this cell, is that the

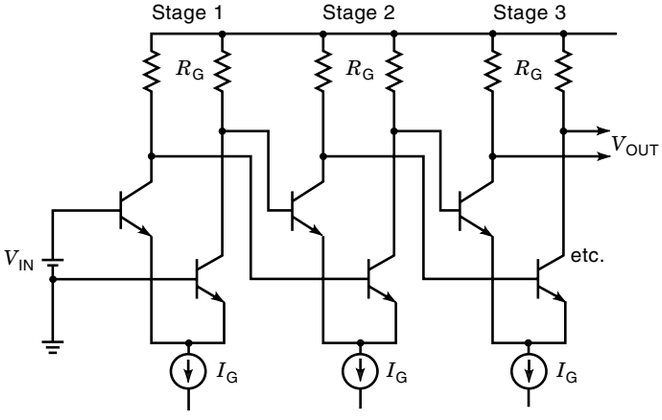


Figure 9. A cascade of translinear network voltage-gain stages.

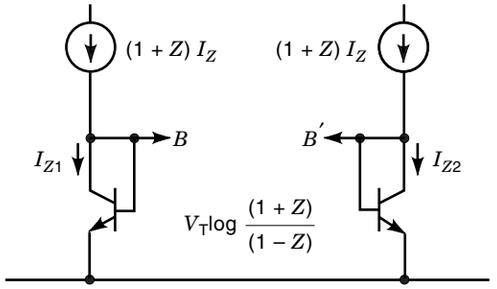


Figure 10. A predistorting cell: stepping stone to a fully translinear amplifier.

base currents are in the same ratio as the drive currents, so the all-important ratio of the currents in the input pair Q_1/Q_2, is unaffected (although of course, the actual currents in these transistors is reduced). The differential cell of Fig. 11 was the first truly current-mode, inherently linear, variable-gain amplifier. This cell could also be viewed as a two-quadrant analog multiplier, and by varying I_Z it could be used as a two-quadrant analog divider.

Once the principles and alluring potential of this elementary cell were grasped, the extension to four-quadrant multiplication followed quickly (2). This entailed simply attaching the linearizing or predistorting cell to a doubly balanced active mixer, already being investigated at the time. (See Ref. 37 for some historical notes about an alternative synthesis path, using current-mirrors as a starting point.)

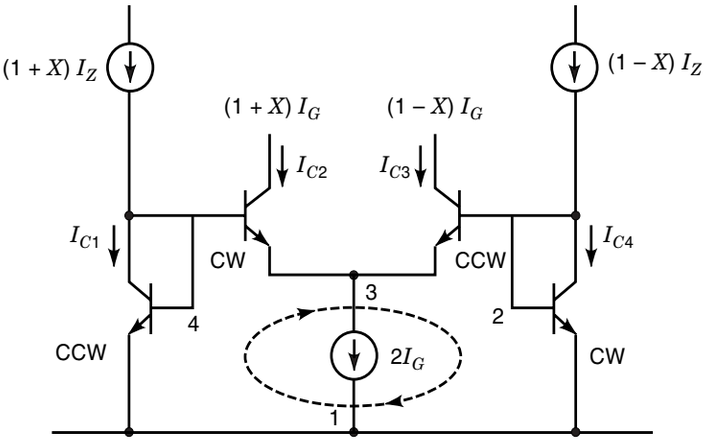
This four-quadrant multiplier topology is shown in Fig. 12. It retained the "beta-immunity" property mentioned above and also allowed operation from low supply voltages (down to 1 V), using appropriate biasing arrangements. In another topology—which later became very popular—the polarity of the linearizing diodes was reversed: they were driven from input currents flowing toward the negative supply, readily provided by an *npn* cell. This alteration forfeited the beta immunity feature; however, because these are multiplier cells, it is a straightforward matter to introduce beta-compensation into the bias currents to achieve high accuracy of the complete monolithic function. Second-generation multipliers using such techniques were later presented in the literature (38).

Since the publication of the first translinear multiplier design (notable for achieving a dc to 500 MHz bandwidth using a 1960s monolithic technology) these basic cells have been used innumerable times and have become familiar textbook entities to analog IC designers.

We now return to the starting point for the early translinear work, namely, wideband linear current-mode amplifiers. One cell does not provide sufficient gain for many practical applications. The next step is therefore to cascade several cells of the form shown in Fig. 11. The resulting topology is indefinitely cascadable and can provide very high current gain; it also provides a wide variable-gain range without using excessively large alterations in the bias currents, thus achieving a more constant bandwidth.

Figure 13 shows a three-stage version of such an indefinitely-cascadable amplifier. The beta-immune form allowed a high current-gain G_I at each stage [in principle, right up to $\beta(\omega)$ without significant gain error] with a bandwidth of approximately f_T/G_I at each stage. The odd-numbered dc bias currents were provided by low-beta lateral *pnp* transistors—the only type available at the time. A minor inconvenience was that the gain law was nonlinear, not only because of the multiplication of linear gain factors, but also because as the tail bias to each cell is raised, the bias to the input diodes of the subsequent cell is lowered. Thus, for the three-stage amplifier, the current gain is

$$G_{\text{I\_TOTAL}} = \frac{I_2}{I_1}\frac{I_4}{(I_3 - I_2)}\frac{I_6}{(I_5 - I_4)} \tag{10}$$



$$I_{BB'} = I_{C1} - I_{C4} = 2XI_Z$$
$$I_{CC'} = I_{C2} - I_{C3} = 2XI_G$$

Figure 11. A current-mode amplifier/multiplier/divider.

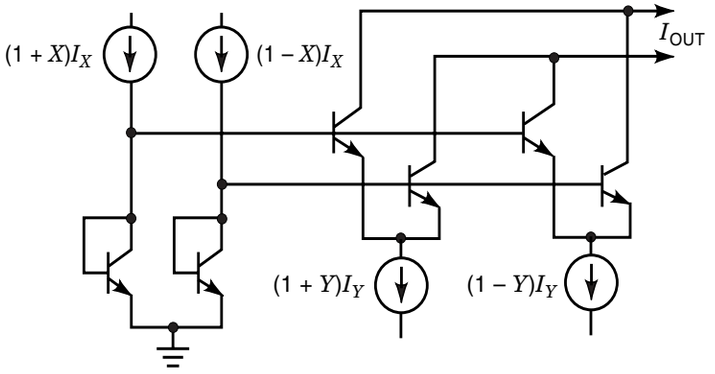


Figure 12. Current-mode (TL) four quadrant multiplier/divider.

The first such multistage TL amplifier built on a 1.2 GHz process (1) exhibited a clean large-signal pulse response and a 20 GHz gain-bandwidth (GBW) product. Recent implementations have achieved GBW values of over 300 GHz.

Another basic TL topology that became quite popular during the early 1970's is shown in Fig. 14. In this so-called "gain cell," also described in Ref. 1, the differential signal currents $(1 + X)I_X$ and $(1 - X)I_X$ are reused at the collectors of Q_1/Q_2 (which now act rather like cascodes) and the additional signal currents $I_{C3} = (1 - X)I_Y$ and $I_{C4} = (1 + X)I_Y$ were added inphase to I_{C1} and I_{C2}. The current gain of this cell is

$$G_I = \left(1 + \frac{I_Y}{I_X}\right) \tag{11}$$

This was again a true current-mode amplifier and exhibited somewhat higher bandwidth, partly because of the reuse of the input currents. It was easy to cascade several such cells across a supply voltage, without the need for the additional bias currents used in the circuit of Fig. 13, although the number of cells was limited by the available voltage. That structure—shown in the first example of a translinear circuit in Figure 1—accumulates both current gain and peak output current capacity at each stage. In an early monolithic amplifier, the ±50 mA output currents were applied directly to a final cascode using a pair of discrete high-breakdown transistors, with the collectors driving the CRT vertical plates in an advanced oscilloscope.

During this period, numerous examples of such true current-mode circuits were developed—having all inputs, outputs, internal signals and control functions fully in current form. Mixed-mode signal-processing TN circuits using a combination of currents and voltages followed in the mid-1970s. In various low-cost rms-dc converters, exemplified by the Analog Devices AD536, the squarer-divider function was implemented in current-mode form, whereas the absolute-value function (which preceded the translinear core) and the low-pass filter (used to extract the mean value of the squared input) were performed in voltage mode (28). Recent translinear developments have led to rms-dc converters capable of accurate operation up to 10 GHz, providing true-power (waveform independent) measurement in such applications as radio frequency power amplifier control.

Translinear network techniques are also exploited in the design of low phase-noise quadrature voltage-controlled oscillators (VCOs) having a wide-range, current-controlled fre-

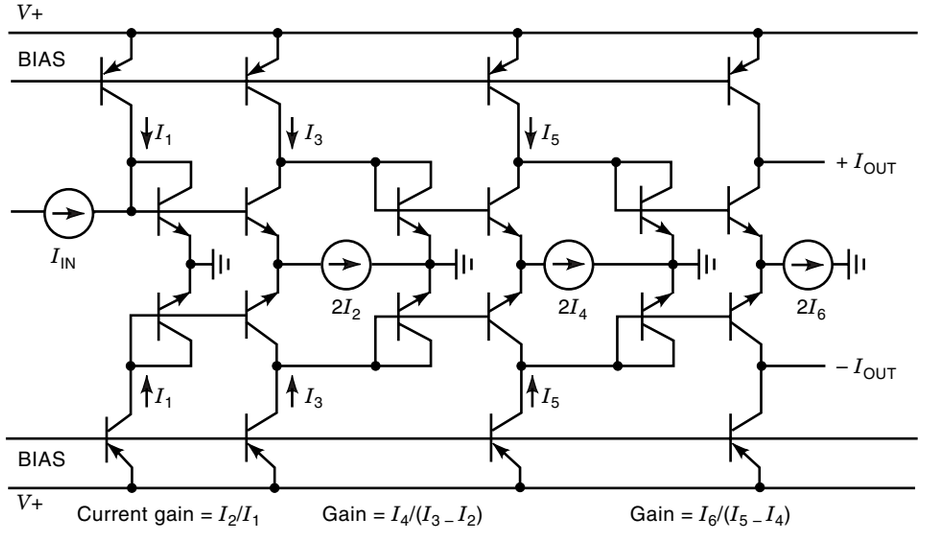


Figure 13. Indefinitely-cascadable current-code amplifier.

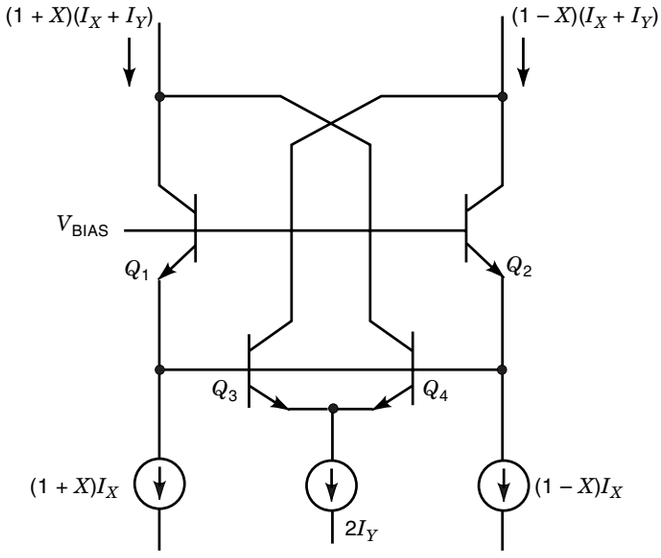


Figure 14. Current-mode gain-cell.

quency. In one useful implementation of a dual-integrator loop, multi-tanh doublets are used to provide linear, programmable transconductance elements for frequency control. The differential currents charge capacitors to generate the differential voltages that drive the opposite g_m cell in the loop. Clearly, such circuits cannot be called current mode, because of the equal importance of both currents and voltages. Yet the strict proportionality of the g_m to the control current is precisely translinear. A further departure from the purity of the original strictly TL loop concepts was the idea of introducing fixed PTAT voltages within the loop to modify its behavior in deliberate and useful ways. A simple example of this would be the use of a sub-millivolt laser-trimmed voltage to null the distortion caused by emitter-area mismatches in high-performance analog multipliers, such as the AD734 produced by Analog Devices Inc.

The practical necessity of interfacing with voltage-mode signals at the perimeters of translinear signal-processing cores, such as the four-quadrant multiplier cell of Fig. 12, has been vigorously addressed, with special emphasis on preserving the excellent linearity and bandwidth inherent in the current-mode core. In low-frequency instrumentation applications, translinear cells can be augmented by op-amps to force collector currents; but to realize the intrinsic speed of TL circuits, other types of interfaces are needed. The translinear cross-quad, described later, is useful in this regard.

Reports of "poor accuracy" were sometimes noted by early experimenters with translinear current-mode circuits. These were invariably due to a failure to appreciate the critical importance of using well-matched, isothermal transistors, for which a monolithic technology was essential, implemented using careful layout techniques. Even among contemporary designers of monolithic ICs, the importance of avoiding spurious sub-millivolt errors in metalization paths is still not fully appreciated.

TRANSLINEAR DESIGN PRINCIPLES

We next review the foundations of translinear design from a fundamental starting point, namely, the relationship between I_C and V_{BE}, which is the heart of the BJT. Figure 15 shows that this relationship can be viewed in reciprocal ways. In Fig. 15 the base-emitter junction of the transistor is driven by an applied voltage, V_{BE}, resulting in a collector current, I_C:

$$I_C = A_E J_S(T) \exp(V_{BE}/nV_T) \tag{12}$$

where A_E is the emitter area and $J_S(T)$ is the saturation current density. The factor n is the emission coefficient, generally close to unity (typically 1.001 to 1.01) for an analog-quality bipolar transistor operated in its normal forward active mode at moderate currents (over the range of, say, I_C = 1 nA to 1 mA, a ratio of one million). We are generally safe in assuming that n is constant over the working current range; its exact value is usually unimportant in TL synthesis.

The saturation current $I_S(T) = A_E J_S(T)$ is a scaling parameter arising from a multiplicity of process-related quantities, including doping levels and profiles, and base thickness, as well as several fundamental constants, most notably, E_{GO}, the band-gap energy. The quantity I_S cannot be easily measured directly, except at high temperatures; in practice, it is deduced through measurement of the V_{BE} of a transistor operating at some collector current $I_C = I_R$ and temperature $T = T_R$. It exhibits notorious temperature sensitivity, varying by a factor of roughly 10^{13} from −55°C to +125°C (for a typical small transistor, from approximately 10^{-24} A to 10^{-11} A).

The collector current, I_C, being proportional to $I_S(T)$ and $\exp(T_R/T)$, would also vary enormously if V_{BE} were held at a fixed value. For example, applying a fixed V_{BE} of 650 mV to a BJT having $I_S = 5 \times 10^{-17}$ A at 27°C would result in an I_C of roughly 1 nA to 1 mA over this temperature range. It is therefore hardly surprising that the early applications of discrete transistors strenuously avoided hard voltage biasing of the E-B junction, because it seemed dangerously inappropriate. Design at that time emphasized instead the safer notion of a current-controlled current source—the "beta view"—because beta varies only mildly over temperature. As we shall see, TL circuits are dramatically immune to this immense variation in I_S, which has little direct importance.

A plot of $\log(I_C)$ versus V_{BE} for a modern monolithic npn transistor shows extraordinary linearity over eight or more decades (Fig. 16). Differentiating Eq. (12) we find

$$\frac{\partial I_C}{\partial V_{BE}} = g_m = \frac{I_C}{V_T} \tag{13}$$

that is, the transconductance of an ideal BJT is a linear function of its collector current. Although this property of the BJT is widely known to be useful in general circuit design, it is absolutely pivotal to the translinear view.

The literature on BJT circuit design makes generous reference to g_m; however, it is not uncommon to find the emphasis still placed on the current gain, β, recalling the pre-monolithic period in which discrete transistors could not be trusted to have accurate and matching V_{BE}s, or operate under isothermal conditions. Even today, translinearity is rarely presented as the key to comprehending the behavior of the majority of BJT circuits, in which the base-emitter voltage and collector current are the dominant parameters.

In Fig. 15 the transistor is operated in a reciprocal fashion by forcing I_C and observing the resulting V_{BE}. (The amplifier

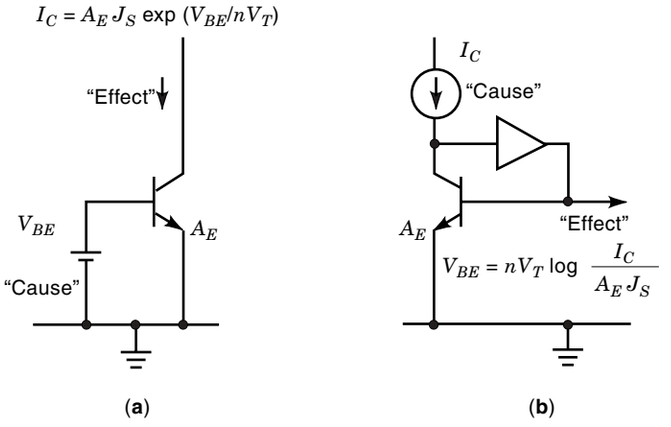


Figure 15. Reciprocal views of the BJT's V_{BE}-I_C relationship.

represented by the triangle, usually realized by a simple emitter-follower or NMOS source-follower, ensures that I_C is independent of the base current). In this case, the circuit "output" (V_{BE}) is now a mild, almost-linear, function of temperature:

$$V_{BE} = nV_T \log \frac{I_C}{A_E J_S(T)} \tag{14}$$

Using an alternative formulation (39):

$$V_{BE} \approx E_{GE} - \frac{T}{T_R}(E_{GE} - V_{BER}) + nV_T \log \frac{I_C}{I_R} \tag{15}$$

where E_{GE} is typically 1.15 V, slightly less than the intrinsic band-gap voltage E_{GO}, and V_{BER} is the V_{BE} at a reference temperature T_R and current I_R. This important relationship comes directly from fundamental considerations and is the basis of the band-gap reference cell. Figure 17 shows the simulated $V_{BE}(T)$ for a library transistor, over the extreme temperature range from −250°C to +400°C; the slight curvature in $V_{BE}(T)$, an artifact not included in Eq. (15), is quite apparent in the simulated result. It is typically +0/−2 mV over the range −55°C to 125°C.

Translinear Loops

The interplay of current, voltage, and temperature is fundamental to transistor operation. Nevertheless, there exists an extensive class of circuits whose function depends on the use of currents as signals or functional variables. These can be designed using methods in which voltages need not be considered at all and in which temperature effects are completely

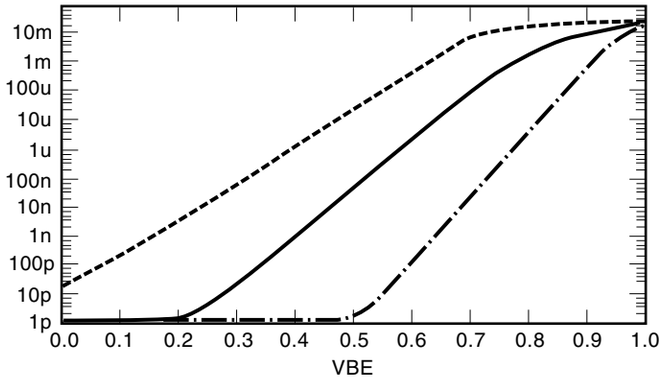


Figure 16. log(I_C) vs. V_{BE} at −55°C, 35°C and 125°C for an NPN Transistor (A_E = 45 μ^2).

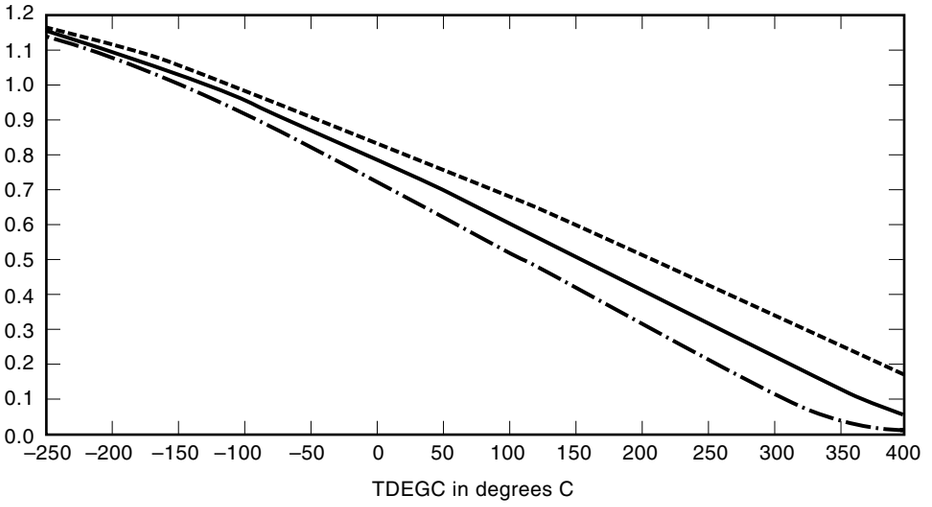


Figure 17. V_{BE}(T) for an NPN Transistor (A_E = 45 μ^2) at I_C = 10 μA, 100 μA and 1 mA.

canceled and are comprised exclusively of BJTs arranged in one or more closed loops of junctions, augmented by various biasing means. Cells of this type are called *strictly TL,* or just TL.

The simplest TL circuit is the current mirror (Fig. 18). It can be viewed as a combination of the current-in/voltage-out subcircuit of Fig. 16 driving the voltage-in/current-out subcircuit of Fig. 15. However, one does not generally think of the current mirror in this fragmented way; rather, it is immediately recognizable as a current-mode configuration. The base-emitter voltage is of merely incidental interest and one intuitively understands that the output current will be scaled by the ratio of the emitter areas.

Numerous elaborations of BJT current mirrors can be found in the literature (40). Note that it is not essential that the transistors exhibit an exponential I_C/V_{BE} relationship. Thus, the current mirror was one of the few bipolar cell concepts that could be immediately converted to MOS form, where its current-mode nature was equally apparent, although the incidental voltage swings were now much larger and could not be overlooked so easily.

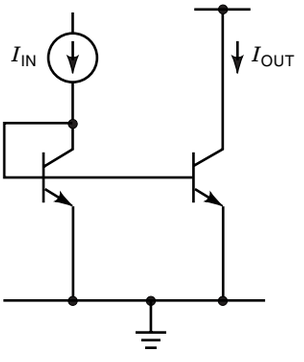


Figure 18. A Current Mirror: The Simplest Translinear-Loop (TL) Cell.

In more sophisticated TL circuits, involving overlapping loops of four, six, or more transistors, the cell function may be less readily apparent. Traditional analyses using full circuit equations, relating voltages and currents, become needlessly burdened with factors that do not appear in the final result. Such factors include the temperature-dependent V_T (increasing by 0.33%/°C at 27°C) and the saturation current I_S. On the other hand, they can be quickly understood when the translinear principle is applied, making analysis simple and direct.

The Translinear Principle

Although subject to numerous detailed caveats when the crucial but somewhat ambiguous qualification of ideal is violated to varying degrees, the following statement is true in broad terms and has proven to be a reliable design rule in hundreds of case histories. The wording here is not quite all-embracing in that it does not yet allow for the use of MOS devices operating in weak inversion; such might be anticipated by substituting the term *exponential element* for *junction,* although this tends to detract from the basic simplicity of the idea.

In a closed loop containing an even number of ideal junctions, arranged so that there are an equal number of clockwise-facing and counterclockwise-facing polarities, with no further voltage generations inside this loop, the product of the current densities in the clockwise direction is equal to the product of the current densities in the counterclockwise direction.

We will now provide a brief proof, based on the analysis of a general closed loop containing N junction devices. Figure 19 shows an example in which N = 8; the junctions are biased into forward conduction by some means.

The junction voltages, V_{Fk}, must algebraically sum to zero:

$$\sum_{k=1}^{k=N} (-1)^k V_{Fk} = 0 \tag{16}$$

The *pn* junctions here will usually represent the base-emitter terminals of the BJTs in the loop, so that each V_{Fk} is actually the V_{BE} of a transistor and the currents shown in each junc-

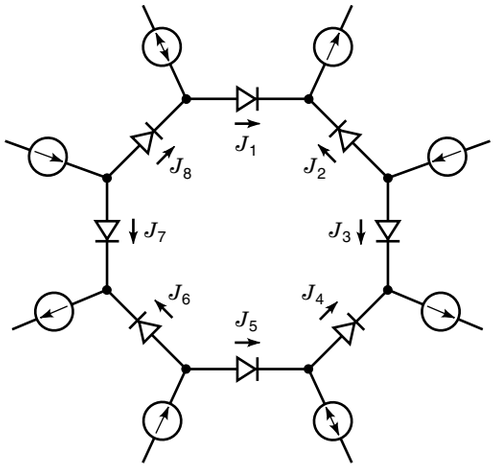


Figure 19. An Illustrative Translinear Loop.

tion represent the collector currents, I_{Ck} (sometimes I_{Ek}). Accordingly, we can replace V_{Fk} by the value given for V_{BE} in Eq. (14):

$$\sum_{k=1}^{k=N} (-1)^k n V_T \log \frac{I_{Ck}}{I_{Sk}} = 0 \tag{17}$$

The use of a separate I_S for each junction recognizes the possibility that the junctions may have different areas or even be made as different device types (for example, a mixture of *npn* and *pnp* transistors). The quantity nV_T appears in all terms; we can generally assume that it is equal for isothermal junctions of the same polarity.

With this assumption and noting that the summation of a series of logarithmic terms can be written as a product and that zero may be written as log(1), we can rewrite Eq. (17) as

$$\prod_{k=1}^{k=N} \left(\frac{I_{Ck}}{I_{Sk}} \right)^{(-1)^k} = 1 \tag{18}$$

Now, every practical circuit will operate with $I_C/I_S \gg 1$. For example, even at a collector current as low as 1 nA, this ratio will typically be $>10^6$ at 27°C. Thus, for the product to remain unity while maintaining sensible operating currents, there must be

1. An even number of junctions in the loop.
2. An equal number forward-biased in the clockwise (CW) and counterclockwise (CCW) directions.

Any mix of junction devices of different polarities, such as *npn* and *pnp* transistors, including SiGe heterojunction bipolar transistors (HBTs), or even Schottky diodes may be used, provided they appear in opposing pairs, since the saturation currents of differing device types may have significantly disparate temperature behavior. Given this need for symmetry, Eq. (18) can be stated as

$$\prod_{CW} \frac{I_{Ck}}{I_{Sk}} = \prod_{CCW} \frac{I_{Ck}}{I_{Sk}} \tag{19}$$

The saturation currents I_{Sk} are proportional to the effective emitter areas. We can replace I_{Sk} in Eq. (19) by factors of the form $A_k J_{Sk}$. Since the saturation current density J_{Sk} equally weights both sides of the equation, we are left with

$$\prod_{CW} \frac{I_{Ck}}{A_{Sk}} = \prod_{CCW} \frac{I_{Ck}}{A_{Sk}} \tag{20}$$

The ratios I_{Ck}/A_k are simply the current densities in each device. Thus, we can write the *Translinear Principle* in its most compact form:

$$\prod_{CW} J = \prod_{CCW} J \tag{21}$$

which reads as in the verbal definition above. It is the elegance and simplicity of this principle, and the reliability with which it can be implemented in a modern analog IC process, that renders it so powerful. It is also a rather wonderful manifestation of the underlying semiconductor physics and the carrier statistics that determine junction currents: the elimination of not only all the thermal sensitivities, the dependence on doping levels and absolute device size, but also the exponential function that so strongly characterizes junction behavior in the usual modes of operation suggest that Eq. (21) is perhaps the most fundamental relationship of all in BJT circuits.

Effect of Emitter-Junction Area

Although absolute size is not very important in translinear circuits, the ratio of emitter areas between pairs of devices in a TL circuit is crucial, and may be exploited to realize a variety of useful effects. For example, in a current mirror, the emitter-area ratio directly scales the current gain. Deliberate use of emitter area ratios is often helpful in reducing, or even eliminating, errors (most often, distortion) due to finite junction resistance; for example, carefully chosen nonunity ratios can improve the accuracy of an rms-dc converter for signals of high crest factor, while leaving the scale-factor unchanged (28). On the other hand, unwanted random deviations from a nominal emitter-area ratio can represent a significant practical limit to the accuracy of TL cells.

In a small-geometry transistor, there will be a significant component of I_S due to carrier injection from the emitter sidewall; also, other effects mitigate against a simple proportionality of I_S to the drawn emitter area in an IC layout. Therefore, it is generally essential in TL practice to realize area ratios by repeating a fixed, unit geometry an integral number of times, rather than by altering either the length or width of the emitter. In TL schematics, the small letter "e" beside an emitter is sometimes used to show the use of a unit emitter, whereas multiple repetitions of this unit emitter are shown as 2e, 4e, and so on. Consolidating the emitter areas into a

composite term, we find

$$\prod_{\mathrm{CW}} \frac{1}{A_k} \prod_{\mathrm{CW}} I_{Ck} = \prod_{\mathrm{CCW}} \frac{1}{A_k} \prod_{\mathrm{CCW}} I_{Ck} \tag{22}$$

hence

$$\prod_{\mathrm{CW}} J = \lambda \prod_{\mathrm{CCW}} J \tag{23}$$

where λ, the area-ratio factor, has the value

$$\lambda = \frac{\prod_{\mathrm{CW}} A_k}{\prod_{\mathrm{CCW}} A_k} \tag{24}$$

Unintentional errors in the effective emitter area ratios are caused by random variations in junction doping (affecting J_S) and in the delineation of the emitter (affecting A_k). Mismatches can also be caused by thermal gradients on the chip. V_{BE} varies by about -2 mV/°C, and 2 mV is equivalent to an emitter-area ratio mismatch of 8% [that is, exp(2 mV/26 mV) = 1.08], so small variations in temperature can cause significant errors in TL circuits. For example, the heat from a power output stage in a mixed-function chip will generate both fixed and signal-dependent thermal gradients, which may affect operation of a TL core function.

High-accuracy monolithic circuits invariably use a symmetrical layout in which critical pairs of transistors are cross-connected in quads. This practice is even more important in TL circuits. In the well-known six-transistor multiplier, a residual V_{BE} mismatch of only 20 μV—equivalent to roughly one-hundredth of a degree Celsius—will result in parabolic nonlinearity of approximately 0.04%. Mechanical stresses in the silicon die, arising from poor layout and assembly techniques, can also cause the V_{BE} of adjacent transistors to differ in various anomalous ways.

It is for these reasons that one occasionally still meets with some skepticism about the accuracy potential of TL circuits. Nevertheless, the practical problems can be surmounted, as evidenced by the many high-precision circuits that are now commercially available. For example, the Analog Devices AD734 Multiplier can exhibit a nonlinearity of 0.01%, equivalent to a 5 μV V_{BE} offset around each of the two overlapping loops in the four-quadrant cell.

The deliberate use of emitter-area ratios is readily illustrated by one of the earliest TL circuits, the one-quadrant multiplier/divider cell shown in Fig. 20. If we neglect base currents, it is apparent from Eq. (21) that

$$J_1 J_2 \underset{\mathrm{CCW}}{=} J_3 J_4 \underset{\mathrm{CW}}{}$$

thus

$$I_4 = \frac{I_1 I_2}{I_3} \tag{25}$$

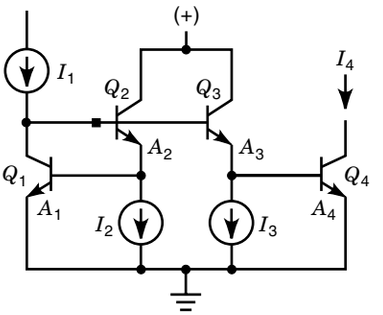


Figure 20. A Simple TL Multiplier/Divider.

when

$$A_1 A_2 = A_3 A_4 \quad \text{that is, } \lambda = 1$$

It is not necessary for all the emitters to be fabricated with identical areas for the overall scaling to be unity. For example, one could choose $A_1 = 1$, $A_2 = 6$, $A_3 = 2$, $A_4 = 3$, which still yields $\lambda = 1$. A common use of unequal areas is in minimizing errors caused by the junction resistance using devices having sizes in close approximation to the nominal currents. Often, the overall scaling factor needs to be something other than unity. A significant limitation to the use of large values of λ in this particular cell is the effect of base currents due to finite beta; this can be addressed by various topological enhancements.

Multiple TL Loops

The above theory involved just one translinear loop, but there is no limit to how many loops may overlap in a cell. The Translinear Principle (TLP) stated in Eq. (21) will apply to each of them independently. Because signal currents are now shared between these loops, interesting and often valuable effects can be achieved. The TLP does not require any modification to address this possibility. It is only necessary to use the appropriate value of currents for the devices contained in more than one loop. Thus, the four-quadrant multiplier, already shown in Figure 11, contains two overlapping loops: Q_1-Q_2-Q_3-Q_4 and Q_1-Q_2-Q_5-Q_6. In this case, however, the loops are essentially noninteractive (completely so if base currents are ignored).

The cell shown in Fig. 21 also contains two overlapping loops, but the function is now less apparent, because the current in Q_7 is shared by the two loops. Devised in the early 1970s, this was one of several cells often used as an excellent didactic example of the remarkable functional sophistication that could be elicited from just a few transistors; these examples also amply demonstrated the power of TLP to rapidly reveal the behavior of TL cells.

We might try to determine the function of this cell by noting that when I_Y is zero, Q_3, Q_4, and Q_6 are nonconducting, whereas Q_1, Q_2 and Q_5, Q_7 form an extended current mirror; thus I_W will just be a linear replication of I_X. Likewise, when I_X is zero, Q_1, Q_2, and Q_5 are nonconducting, whereas Q_3, Q_4 and Q_6, Q_7 act as a current mirror and simply replicates I_Y. It is not immediately obvious, however, what happens when

both I_X and I_Y are applied. Using TLP the full analysis is so easy that such beating-around-the-bush is quite unnecessary. Applying TLP to Loop A:

$$\underset{\text{CCW}}{I_X I_X} = w \underset{\text{CW}}{I_W I_W} \tag{26}$$

where w is a temporary variable (see figure). For Loop B

$$\underset{\text{CW}}{I_Y I_Y} = (1-w) \underset{\text{CCW}}{I_W I_W} \tag{27}$$

Adding these two equations and solving, we immediately find

$$I_W = \sqrt{(I_X^2 + I_Y^2)} \tag{28}$$

that is, the circuit performs the vector-summation function. This simple two-dimensional processor can be readily extended to generate the three-dimensional vector sum (the cubic diagonal) with the addition of just three more transistors driven by a third current I_Z. It is equally apparent that any number of input cells can be added in the horizontal direction to provide n-dimensional operation, and that the function $\sqrt[m]{\sum I_K^m}$, for $m > 2$, can be realized by adding further diode-connected transistors in the vertical branches.

In a modern BJT technology an accurate solution can be available within less than a nanosecond, and even in a microprocessor-rich culture this simple cell deserves consideration where real-time processing is required. A solution based on *digital-signal-processing* (DSP) could perhaps be more accurate, if the basic signal sources and the associated A/D and D/A operations were impeccable, but it could not be as fast. There are applications for vector summation in modern communications systems where this rapid response is valuable.

This is a one-quadrant vector summing circuit, that is, I_X, $I_Y > 0$. Frequently, this function is required to operate in all four quadrants, for example, in finding the radius amplitude of a pair of bipolarity in-phase and quadrature (I and Q) signals. This can be achieved using a different, but equally elegant, translinear approach. The inputs to this cell must be currents. Since to this day most signals outside of an IC remain in the voltage domain, conversion of the inputs current form is needed. Furthermore, these currents flow from the supply, which implies the use of p-type (pnp or PMOS) transistors in a single-supply context. Finally, I_W will usually be converted back to a voltage, which may require the use of a p-type mirror. The potential accuracy and speed of the basic translinear core may thus quickly become compromised by the auxiliary circuitry. This cell can be embedded into a extended framework, using feedback amplifiers to preserve accuracy. A translinear cross-quad can be very effective in bridging the gap between voltage-mode and current-mode signals while maintaining high accuracy and bandwidth (41).

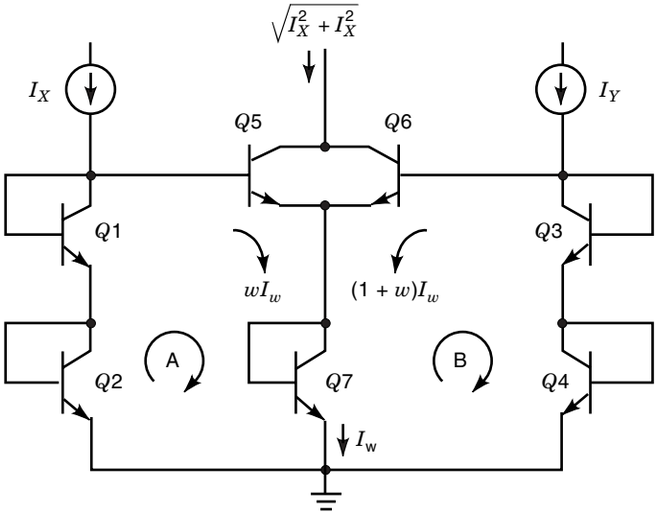


Figure 21. A TL Cell Containing Two Loops.

Figure 22 shows two more examples of dual-loop vector-manipulation cells; nonunity emitter-area ratios are invoked to achieve the correct function. The analysis has been presented elsewhere (42) but proceeds along the same lines as used for the previous circuit.

Figure 23 shows an interesting example of a multiple-loop TL circuit, in which all loops overlap and two nodes are common to all loops. It is noteworthy that this cell was also included in the first published paper on translinear techniques (21). Here again, the remarkable processing power that can be accomplished within the confines of a very rudimentary circuit, the hallmark of this design methodology, is demonstrated. Using M loops coupled in the tightest possible topology, it performs the M-dimensional array normalization:

$$I_{\text{out\_}k} = I_{\text{E}} \frac{I_{\text{in\_}k}}{\sum_{j=1}^{j=M} I_{\text{in\_}j}} \tag{29}$$

that is, it continuously computes the ratio of each input in the array to the sum of all the inputs and then multiplies the result by the output scaling current I_{E}. With attention to certain practical details (not included in Fig. 23) the inputs can span a dynamic range of 80 dB and generate the solution within nanoseconds.

This sophisticated analog computation proceeds in an extraordinarily compact fashion, being mediated through little else than the wire connecting all the emitters together. An IC embodiment of this cell (43) provided a 16-wide input, expandable without limit through three expansion pins. Using a simple modification, the IC also provided the alternative function

$$I_{\text{out\_}k} = I_{\text{E}} \frac{I_{\text{in\_}k}}{\max(I_{\text{in\_}j})} \tag{30}$$

which results in one of the I_{OUT} values always being at full-scale (I_{E}), whereas the mode shown in Eq. (29) results in a peak output dynamic range of $M:1$. As might be expected, multiple-loop TL cells have significant potential in executing the near-instantaneous solution of simultaneous equations having a large number of variables. Numerous examples of such highly compact "equation solvers" have been envisaged over the years and are routinely utilized in contemporary commercial ICs.

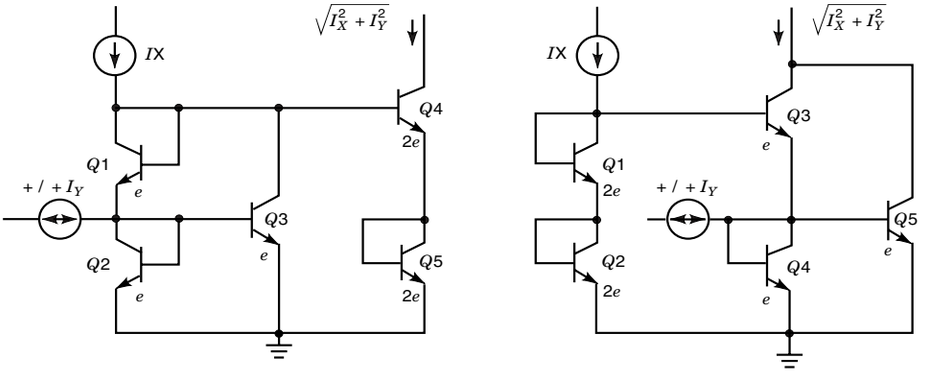


Figure 22. TL Cells for Two-Quadrant Vector-Difference (left) and Vector-Sum (right).

The Ratiometric Viewpoint

The concept of variables embedded in chained products of current having the dimension of $(\text{Amps})^M$, where $M = N/2$ is the number of junctions in each (CW and CCW) direction, is somewhat counterintuitive. An alternative way of thinking about TL loop behavior is in terms of the current ratios between junctions taken in opposing pairs. These are dimensionless and often within an order of magnitude of unity (0.1 to 10).

Indeed, the great practical value of TL circuits stems from this ratiometric behavior, which is fundamentally independent of the general magnitude of the bias current or the process on which the devices are made (with appropriate reservations about matching device structures), or the operating temperature, since the nV_T factors canceled in Eq. (18) and the basic I_S factors in Eq. (20). These general expectations about ratiometric behavior have been proven reliable over a wide range of circumstances. Such a view is readily applied to the array normalizer of Fig. 23, where

$$\frac{I_{\text{out\_1}}}{I_{\text{in\_1}}} = \cdots \frac{I_{\text{out\_}k}}{I_{\text{in\_}k}} = \cdots \frac{I_{\text{out\_}M}}{I_{\text{in\_}M}} \tag{31}$$

but it is equally applicable to the single loop cells shown in Figs. 10, 11 and 13 by taking the junctions in opposing pairs, with due regard for the junction area. In basic TL circuits, this strict ratiometric behavior arises from setting the net loop voltage to zero. However, it is certainly possible, and occasionally even useful, to include one or more voltage sources in a loop, when the governing equation becomes

$$\sum_{k=1}^{k=N} V_T \log \frac{I_{Ck}}{I_{Sk}} = V_L \tag{32}$$

where V_L is the net voltage inserted into the loop (using one or more sources) and the n of nV_T is assumed to be unity. This voltage radically alters the behavior of the circuit, but can be cast into a form that shows its potential utility. With simple manipulation, it can be shown to be equivalent to the modification of the emitter-area scaling factor, λ, that is,

$$\lambda' = \lambda \exp \frac{2V_L}{NV_T} \tag{33}$$

It follows that if a temperature-stable function is desired, V_L must be PTAT (proportional to absolute temperature). A practical use of such a voltage is to null out the V_{BE} mismatch in a TL loop where this would degrade accuracy. These mismatches amount to much less than 100 μV in a modern BJT process, using appropriate layout techniques, which is another way of saying that the emitter area ratio of critical pairs can be held to within better than $\pm 0.4\%$. Nevertheless, this is quite inadequate matching for a high-performance, low-distortion analog multiplier such as the AD734. This product achieves very high scaling accuracy and low even-order distortion first by using careful cross-quadding of critical pairs and second by laser-trimming the V_{BE} mismatch, corresponding the factor λ, by introducing a V_L of up to ± 200 μV, using synchronous demodulation techniques to measure minuscule levels of distortion (-120 dBc).

In an alternate design approach, one may rely solely on correct-as-fabricated devices, using extensive interdigitation of transistors to minimize statistical fluctuations in the effective value of λ. This has the advantage of requiring no trimming and further reduces the sensitivity to on-chip thermal gradients and stress-induced errors (particularly those due to post-packaging stress). On the other hand, this approach will usually consume more chip area and may result in reduced bandwidth from the much higher parasitic capacitances of the large transistors and their lower current densities.

It is often possible to use a short length of the aluminum interconnect as an approximately PTAT resistor of a few ohms to generate the needed correction voltage when driven by a temperature-stable current. This has a temperature coef-

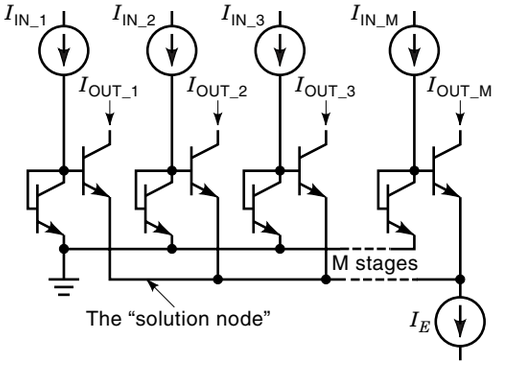


Figure 23. An Infinitely-Expandable Analog Array Normalizer.

ficient of roughly 3900 ppm/°C, which makes it almost right for this purpose. Alternatively, it is a simple matter to generate a PTAT voltage using a ΔV_{BE} cell for this purpose, as is utilized in the AD734. An example of the use of an inserted voltage used to bring about a much larger change in circuit function is shown in Figure 22. Here, the current-gain G_I of a somewhat-elaborated mirror, using complementary transistors, can be altered over a wide range by the voltage V_G:

$$G_I = A \exp \frac{V_G}{2V_T} \tag{34}$$

This complementary bipolar (CB) cell conveniently provides a differential pair of nodes, of moderately high impedance, at which to apply the control voltage, V_G. Using CB cells of alternating polarity, a simple wideband current-mode variable-gain amplifier can be built.

There has been considerable recent interest in so-called *log-domain* filters (16), which seek to advantageously exploit the bipolar transistor's unique exponential properties. In the work described by Perry and Roberts (17), the cell shown in Fig. 24 is used as for the *log* and *antilog* operations. In another approach, Seevinck (44) adapts the basic multiplier/divider cell shown in Fig. 10. Log-domain filters are attractive because they offer an alternative to the use of the linear transductors needed in g_m/C filters, which are complicated by the additional requirement that the g_m must invariably be programmable to effect tuning (in a master/slave configuration). They also provide a wide tuning range.

Figure 25 shows a further example of a TL cell in which an inserted voltage is used to strongly modify the cell function. I_{C1} is forced to I_O—a primary bias current, which is PTAT—by the emitter follower (or NMOS device) Q_2. I_G is a gain-control current, which should also be PTAT for stable gain-scaling. R_B serves only to ensure that Q_2 is always biased and absorbs the nonconstant I_G. The inserted voltage in this case is V_G, generated across the resistor R_G, which lowers the collector current of Q_3:

$$I_{C3} = AI_0 \exp(-V_G/V_T) \tag{35}$$

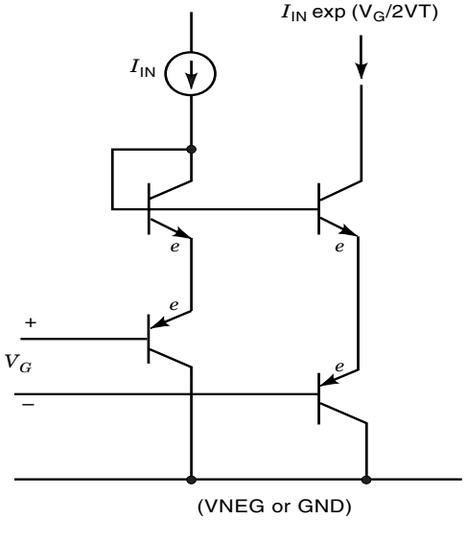


Figure 24. A Voltage-Programmable Current-Mirror.

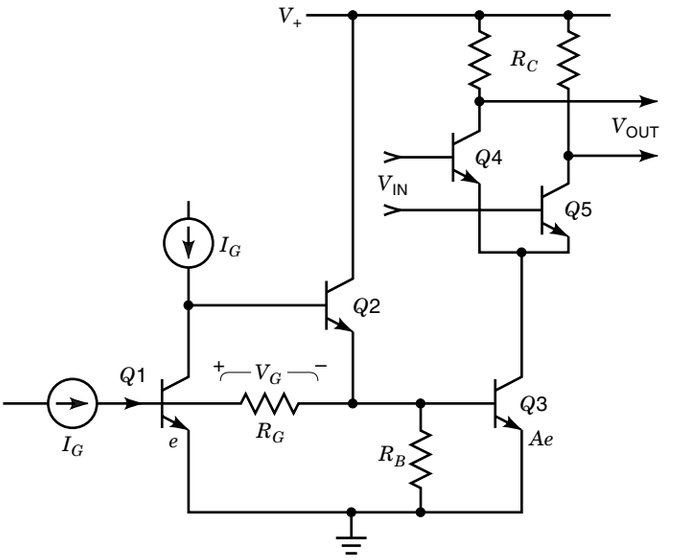


Figure 25. A Linear-in-dB Current-Programmable Gain-Cell.

Thus, I_G controls the gain of the associated differential pair, Q_4/Q_5. The exponential relationship results in a linear-in-decibels gain function. The scaling is easily calculated: at T = 27°C, 1 mV of V_G lowers I_{C3}, and thus the gain, by the factor exp(1 mV/25.86 mV) or 1.0394, which expressed in decibels is 0.336 dB. When R_G = 1 kΩ, the scaling is approximately 3 μA/dB. Several gain cells can be driven from the same basic interface simply by adding current-source transistors like Q_3; the same linear-in-decibels gain form results.

Mixed TL and TN Cells

Strictly translinear (TL) subcells can be combined with translinear network (TN) subcells in numerous ways. In the variable-gain amplifier (VGA) shown in Figure 26, Q_1–Q_4 form a translinear cross-quad (41). Here, *pnp* devices are used for Q_1/Q_2 and *npn* devices for Q_3/Q_4. The input current $I_{in} < I_O$ modulates the collector currents. Tracing the build-up of

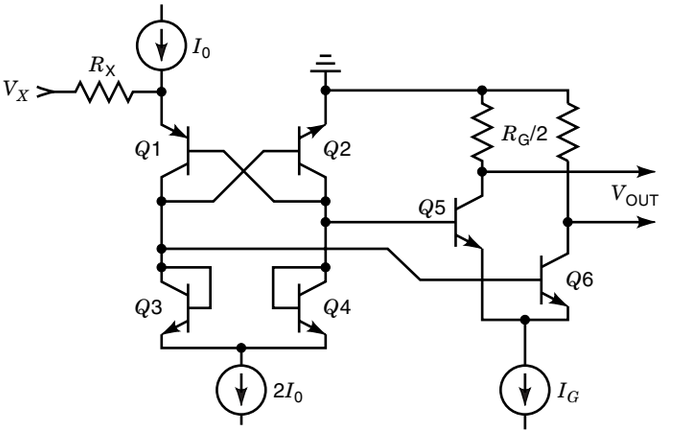


Figure 26. A Mixed TN/TL Structure: A Voltage-Input/Output VGA.

V_{BE}'s through these four transistors from the input node back to the ground node, we find that they fully cancel. [This is not exactly true when finite current gain $\beta(\omega)$ is taken into account, but it is a good approximation.] If we neglect the base currents of Q_5/Q_6 at low frequencies, we find that $r_{in} = 4kT/\beta qI_O$, or approximately 1 Ω at $I_O = 1$ mA. Thus, the input voltage V_X is accurately converted to the current $I_X = V_X/R_X$ even for quite small values of R_X (say, 50 Ω).

The currents in Q_3 and Q_4 have exactly the required form to act as the input pair to a linear multiplier (compare this with Fig. 10), completed by the addition of the transconductance pair Q_5, Q_6. Using simple current-to-voltage conversion, the overall structure can be viewed as a linear VGA, whose numerical gain is readily shown to be

$$G = \frac{I_G R_G}{I_0 R_X} \tag{36}$$

This scheme integrates the required high-linearity, wideband voltage-current conversion step with the predistorting devices (Q_3, Q_4), while the V_{BE}'s of Q_1/Q_2 usefully provide level-shifting for the output pair. Note also that the cell Q_3-Q_4-Q_5-Q_6 preserves the desirable beta-immune form. By adding a second output pair and a suitable interface for the second input variable a four-quadrant multiplier can be realized.

Effect of Device Nonidealities

The reference value of V_{BE} usually assumes a V_{BC} of zero, when I_S is defined in accordance with generally agreed modeling practices. Base-width modulation increases I_C by the factor $(1 + V_{BC}/V_{AF})$, where V_{AF} is the forward Early voltage. Thus, the basic equations need to be amended, to read

$$I_C = \left(1 + \frac{V_{BC}}{V_{AF}}\right) I_S(T) \exp \frac{V_{BE}}{nV_T} \tag{37}$$

or

$$V_{BE} = nV_T \log \frac{I_C}{I_S(T)(1 + V_{BC}/V_{AF})} \tag{38}$$

For high-frequency transistors, V_{AF} is generally quite low. To minimize errors, devices should be biased in *pairs,* so that the V_{CB} effects cancel (recall that the operation of TL circuits is invariably based on current *ratios,* not the absolute currents). It is often possible to use a cascode stage or a specially provided bias line designed to keep V_{CB} at or near zero. It is unusual in strict-TL circuits to find the full supply voltage across any device inside a TL loop.

The increase in V_{BE} due to the junction resistances, most notably, the base resistance, $r_{BB'}$ and the emitter resistance $r_{EE'}$ (particularly in transistor processes using polysilicon emitters) is often a major limitation to accuracy, since it does not introduce simple factors into the equations, as for base-width modulation. Rather, it results in a V_{BE} which is now a mixture of linear and logarithmic terms:

$$V_{BE} = V_T \log \frac{I_C}{I_S(T)} + I_C \left(\frac{r_{BB'}}{\beta} + r_{EE'}\right) \tag{39}$$

where β is the appropriate value for the current gain, and is a function of I_C, V_{CB}, frequency, temperature and production tolerances. As evidence of the complications that $r_{BB'}$ introduces into TL analysis, note that one can no longer write a closed-form equation for I_C as a function of V_{BE}.

The effect of the junction resistances on cell behavior are capricious. In four-transistor two-quadrant multipliers (variable-gain cells) they introduce odd-order distortion, which can vary strongly with the gain. This distortion can be made to vanish at one specific value of gain by the judicious use of emitter area sizing (determining $r_{BB'}$), but cannot be eliminated completely. On the other hand, the six-transistor four-quadrant multiplier cell can be designed to exhibit essentially zero odd-order distortion even in the presence of very large ohmic errors (2).

Thus, ohmic errors are not readily quantified in general terms. Analysis is complicated by the fact that $r_{BB'}$ is current and temperature dependent: the subemitter portion of $r_{BB'}$ typically increases by about 1%/°C, whereas the extrinsic portion has a temperature coefficient of approximately 0.15 %/°C. Analysis is further complicated by the role of finite beta, as well as its current and temperature dependence.

The value of bipolar translinear circuits is now well established. The voltage-controlled current-source view of the BJT, which is captured in the notion of "translinearity," is a more useful one than the older idea of a current-controlled current source (the beta view) in a modern monolithic context. Many of the limitations and obstacles that once stood in the way of actually realizing the full potential of these cells have long since been removed.

The largest utilization of translinear concepts has been in analog multiplication. Once a very important general challenge, this function is now more likely to be found in various specialized forms. Multipliers are used in RF power management (29,45), modulation–demodulation, and gain-control applications at frequencies up to 30 GHz. There are few alternatives to translinear techniques where speed and high accuracy are required. Heterojunction transistors, often used in these high-speed applications, also conform to the translinear principle; thus, all of the cell concepts developed for homojunction transistors are fully realizable in HBT form.

Operating in subthreshold, MOS transistors are also translinear, although the generally low currents in this domain limit the operating speed to much less than the full capabilities of a given technology. This mode of operation may become of importance in analog neural networks. In a simple theory of field-effect devices, the transconductance of an MOS transistor in strong inversion is a linear function of the gate-source bias. This has led to the adoption of the term translinear in this context, and various TL-like cells have been proposed. The term *MOS-translinear* (MTL) has been used for such circuits. Since there is a growing number of ways in which this word is now being applied, this particular class of circuits, differing so markedly from bipolar TL and TN circuits, should be called voltage-translinear, or VTL.

BIBLIOGRAPHY

1. B. Gilbert, A new wideband amplifier technique, *IEEE J. Solid-State Circuits,* **SC-3** (4): 353–365, 1968.

2. B. Gilbert, A precise four-quadrant multiplier with subnanosecond response, *IEEE J. Solid-State Circuits,* **SC-3** (4): 365–373, 1968.
3. B. Gilbert, Translinear circuits: A proposed classification, *Electron. Lett.,* **11** (1): 14–16; errata: **11** (6), 136, 1975.
4. E. Seevinck, *Analysis and Synthesis of Translinear Integrated Circuits,* Ser. Stud. Electr. Electron. Eng., Amsterdam: Elsevier, 1988.
5. C. Toumazou, F. J. Lidgey, and D. G. Haigh (eds.), *Analogue IC Design: The Current-Mode Approach,* IEE Circuits Syst. Ser., London: Peter Perigrinus, 1990, Vol. 2.
6. B. E. Andersen, The 'multi-tanh' technique for linearizing the transconductance of emitter coupled pairs, M.Sc. thesis, Washington State University, Seattle, 1978.
7. W. Mack, Wideband transconductance amplifiers, M.Sc. thesis, University of California, Berkeley, 1979.
8. S. Gold, A programmable continuous-time filter, M.Sc. thesis, Boston University, Boston, 1988.
9. B. Gilbert, Circuits for the precise synthesis of the sine-function, *Electron. Lett.,* **13** (17): 506–508, 1977.
10. B. Gilbert, The multi-tanh principle: A tutorial overview, *IEEE J. Solid-State Circuits,* **33** (1): 2–16, 1998.
11. B. Gilbert et al., Build fast VCAs and VCFs with analog multipliers, *EDN* , pp. 289–299, October 18, 1984.
12. B. Gilbert, A low-noise wideband variable-gain amplifier using an interpolated ladder attenuator, *IEEE ISSCC Tech. Dig.,* 1991, pp. 280–281, 330.
13. Moller et al., 13 Gb/s Si-bipolar AGC amplifier IC with high gain and wide dynamic range for optical-fiber receivers, *IEEE J. Solid-State Circuits,* **29** (7): 815–822, 1994.
14. T. Masuda et al., 40 Gb/s analog IC chipset for optical receiver using SiGe HBTs, *IEEE ISSCC Tech. Dig.,* 1998, pp. 314–315.
15. R. Yu et al., A packaged broadband monolithic variable gain amplifier implemented in AlGaAs/GaAs HBT technology, *IEEE Gallium Arsenide Integr. Circuits Symp. Tech. Dig., 1995,* pp. 197–200.
16. R. W. Adams, Filtering in the log domain, *63rd AES Conf.,* New York, 1979, Prep. No. 1470.
17. D. Perry and G. W. Roberts, Log-domain filters based on LC-ladder synthesis, *Proc. IEEE Int. Sym. Circuits Syst.,* pp. 311–314, 1995.
18. E. Seevinck and R. J. Wiegerink, Generalized translinear principle, *IEEE J. Solid-State Circuits,* **26** (8): 1198–1102, 1991.
19. R. J. Wiegerink, Computer aided analysis and design of MOS translinear circuits, *Analog Integr. Circuits Signal Process.,* **9** (2): 181–187, 1996.
20. A. G. Andreou and K. A. Boahen, Translinear circuits in subthreshold MOS, *Analog Integr. Circuits Signal Process.,* **9** (2): 141–166, 1996.
21. B. Gilbert, A DC-500 MHz amplifier/multiplier principle, *ISSCC Dig. Tech. Pap.,* 1968, pp. 114–115.
22. H. E. Jones, U.S. Patent No. 3,241,078, "Dual Output Synchronous Detector Utilizing Transistorized Differential Amplifiers," Issued Mar. 15, 1966.
23. B. Gilbert, Design considerations for active BJT mixers, in G. Machado (ed.), *Low-power HF Microelectronics; A Unified Approach,* London: IEE Circuits and Systems, 1996, Ser. 8, Ch. 23, pp. 837–927.
24. B. Gilbert, IF amplifiers for monolithic bipolar communications systems, *EPFL Electron. Lab. Adv. Eng. Course RF Des. Wireless Commun. Syst.,* Lausanne, 1996.
25. P. G. Van Lieshout and R. Van de Plassche, A monolithic wideband variable-gain amplifier with a high gain range and low distortion, *ISSCC Tech. Dig.,* 1996, pp. 358–359.
26. J. O. Voorman, Analog integrated filters, *Eur. Solid-State Circuits Conf. Rec.,* 1985, pp. 292–292C.
27. H. Tanimoto et al., Realization of a 1-V active filter using a linearization technique employing plurality of emitter-coupled pairs, *IEEE J. Solid-State Circuits,* **26**: 937–945, 1991.
28. B. Gilbert, A monolithic RMS-DC converter with crest-factor compensation, *ISSCC Dig. Tech. Pap.,* 1976, pp. 110–111.
29. B. Gilbert, Novel method for amplitude measurement of signals up to microwave frequencies, *Electron. Lett.,* **13** (4): 107–108, 1977.
30. B. Gilbert, High-accuracy vector-difference and vector-sum circuits, *Electron. Lett.,* **12** (11): 293–294, 1976.
31. C. A. Mead, *Analog VLSI and Neural Systems,* Reading, MA: Addison-Wesley, 1989.
32. B. Gilbert, Nanopower nonlinear circuits based on the translinear principle, *Workshop on Hardware Implement. Neural Networks,* San Diego, CA, 1988.
33. B. Gilbert, Monolithic analog READ-ONLY memory for character generation, *IEEE J. Solid-State Circuits,* **SC-6** (1): 45–55, 1971.
34. B. Gilbert, A monolithic 16-channel analog array processor, *IEEE J. Solid-State Circuits,* **SC-19** (6): 956–963, 1984.
35. B. Gilbert, A monolithic microsystem for the analog synthesis of trigonometric functions and their inverses, *IEEE J. Solid-State Circuits,* **SC-17** (6): 1179–1191, 1982.
36. B. Gilbert, Advances in BJT techniques for high-performance transceiver, *Eur. Solid-State Circuits Conf. Rec.,* 1997, pp. 31–38.
37. B. Gilbert, Where do little circuits come from?, in J. Williams (ed.), *Analog Circuit Design: Art, Science and Personalities,* EDN Ser. Des. Eng., Stoneham, MA: Butterworth-Heinemann, 1991, Ch. 19.
38. B. Gilbert, A high-performance monolithic multiplier using active feedback, *IEEE J. Solid-State Circuits,* **SC-9** (6): 364–373, 1974.
39. R. J. Widlar, An exact expression for the thermal variation of the emitter base voltage of bi-polar (sic) transistors, *Proc. IEEE (Lett.),* **55**: 96–97, 1967.
40. B. Gilbert, Bipolar current mirrors, in C. Toumazou, F. J. Lidgey, and D. G. Haigh (eds.), *Analogue IC Design: The Current-Mode Approach,* IEE Circuits Syst. Ser., London: Peter Peregrinus, 1990, Vol. 2, pp. 239–296.
41. B. Gilbert, Translinear circuits: An historical overview, *Analog Integr. Circuits Signal Process.,* **9**: 95–118, 1996.
42. B. Gilbert, Current-mode circuits from a translinear viewpoint: A tutorial (Use of op-amps to augment TL cells), in C. Toumazou, J. Lidgey, and D. G. Haigh (eds.), *Analogue IC Design: The Current-Mode Approach,* IEE Circuits Syst. Ser., London: Peter Peregrinus, 1990, Vol. 2, p. 51.
43. B. Gilbert, An analog array processor, *ISSCC Dig. Tech. Pap.,* 1984, pp. 286–287.
44. E. Seevinck, Companding current-mode integrator: A new circuit principle for continuous-time monolithic filters, *Electron. Lett.,* **26** (24), 2046–2947, 1990.
45. B. Gilbert, Novel technique for RMS-DC conversion based on the difference of squares, *Electron. Lett.,* **11** (8).

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