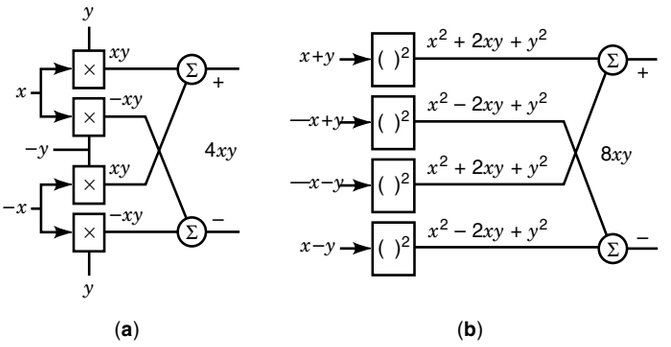

Figure 1. Pictorial explanations of cancellation method used in MOS multipliers. (a) Using single-quadrant multipliers and (b) using square devices correspond to Eqs. (1) and (2) respectively. X and Y are not shown in the figures for simplicity.

OPERATION PRINCIPLES

Despite many reported MOS multipliers, only two cancellation methods for the four-quadrant multiplication are known. A fully differential configuration is necessary in a sound multiplier topology to achieve complete cancellation. As a multiplier has two inputs, there are four combinations of two differential signals, i.e., (x, y), $(-x, y)$, $(-x, -y)$, and $(x, -y)$. Then, the multiplication can be obtained based on the following equalities.

$$\begin{aligned}&[(X+x)(Y+y)+(X-x)(Y-y)]\\&-[(X-x)(Y+y)+(X+x)(Y-y)]=4xy\end{aligned} \tag{1}$$

or

$$\begin{aligned}&[\{(X+x)+(Y+y)\}^2+\{(X-x)+(Y-y)\}^2]\\&-[\{(X-x)+(Y+y)\}^2+\{(X+x)+(Y-y)\}^2]=8xy\end{aligned} \tag{2}$$

X and Y are constant terms that include a common mode signal, and any constant terms in device characteristics. Figure 1 depicts an explanation of the above equations. The simple MOS transistor model expressed for its linear and saturation regions, as

$$I_d = K\left[V_{gs}-V_t-\frac{V_{ds}}{2}\right]V_{ds} = K\left[V_{gs}V_{ds}-V_tV_{ds}-\frac{V_{ds}^2}{2}\right] \tag{3}$$
$$\text{for } |V_{gs}|>|V_t|,\ |V_{ds}|<|V_{gs}-V_t|$$

$$I_d = \frac{K}{2}[V_{gs}-V_t]^2 = \frac{K}{2}[V_{gs}^2-2V_{gs}V_t-V_t^2] \tag{4}$$
$$\text{for } |V_{gs}|>|V_t|,\ |V_{ds}|>|V_{gs}-V_t|$$

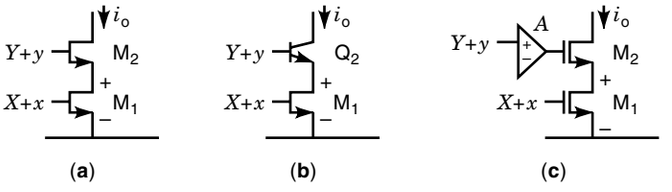

Figure 2. Programmable transconductor (one-quadrant multiplier). M_1 is operating in linear region while M_2 is operating in saturation region.

MULTIPLIERS, ANALOG CMOS

Multipliers produce linear products of two signals x and y yielding an output $z = Kxy$, where K is a multiplication constant with suitable dimension. Historically, a complete analog multiplier was invented by Gilbert (1,2) using BJT. Because digital technology dominates in modern electronics, analog circuits are required to share the same standard digital CMOS process for low cost fabrication. Thus, the popular BJT Gilbert Cell is not suitable in an MOS digital process, and designers must address low power supply voltage requirements. The Gilbert cell is implemented using lateral BJT in the CMOS process in Ref. 3. The MOS version of Gilbert multipliers is reported in Ref. 4. Because its linearity is poor, several modified versions including linearization schemes (4–6), folded structures (6–8), and active attenuators (9) have been reported. However, none of the above multipliers has been adopted in any commercial product. Many other MOS multipliers that are not based on Gilbert cell structure are reported in the literature. MOS multipliers can be categorized into two major groups based on its MOS operating region, linear (10–25) and saturation (3–9,26–48). Beside above major categories multipliers operating in the weak inversion region (49–51), dynamic multipliers for sampled signal system or neural networks (52–57), has been reported. Here, only the MOS multiplier architectures that have practical performance are discussed.

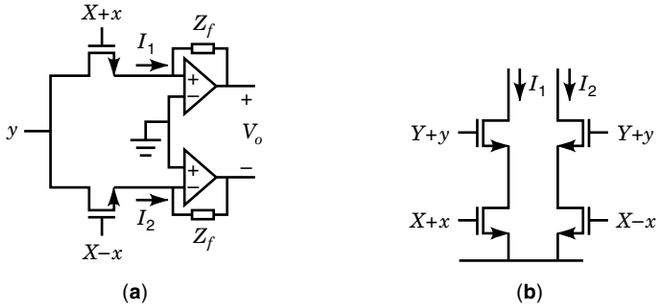

Figure 3. Four-quadrant multipliers with two programmable transconductors.

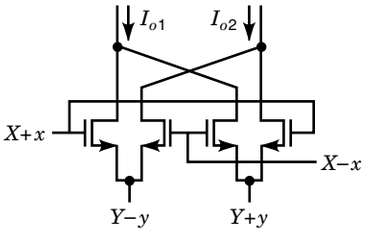

Figure 5. Four cross coupled FETs with gate and source signal application.

where $K = \mu_o C_{ox} W/L$ and V_t are the conventional notation for the transconductance parameter and the threshold voltage of the MOS transistor, respectively. The terms $V_{gs}V_{ds}$ in Eq. (3), or V_{gs}^2 in Eq. (4) are commonly used to implement Eqs. (1) and (2), respectively.

Using V_{gs} V_{ds} in Linear Region

First we introduce a programmable linear transconductor and show how it can be used to implement a multiplier. In Fig. 2, transistor M_1 is forced to operate in the linear region while M_2 operates in saturation with proper bias voltage, X and Y. In Fig. 2(a) (58), $v_{ds;M_1}$ is controlled by y through the source follower M_2 when the transconductance of the source follower is much larger than that of M_1. The source follower can be replaced with the BJT emitter follower (59) [Fig. 2(b)] or the gain enhanced MOS source follower (60–62).

A multiplier is realized by combining two programmable transconductors as shown in Fig. 3(a). The output current is obtained from Eq. (3) where $X \pm x = v_{gs}$ and $y = v_{ds}$.

$$\begin{cases} I_1 = K_1\left(X + x - V_t - \dfrac{y}{2}\right)y \\ I_2 = K_1\left(X - x - V_t - \dfrac{y}{2}\right)y \end{cases} \tag{5}$$

The difference of output currents yields

$$I_o = I_1 - I_2 = 2K_1xy \tag{6}$$

In Fig. 3(a), the op amp keeps the sources of the FETs virtually grounded. This approach has been used in conjunction with switched-capacitor circuits to implement a weighted-sum

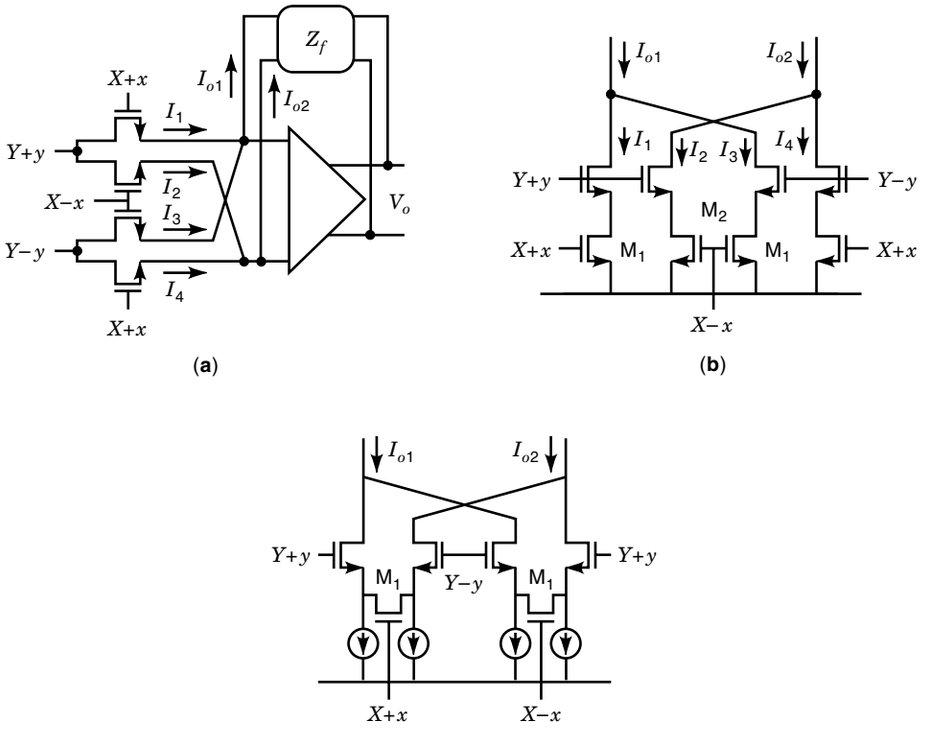

Figure 4. Fully-differential four-quadrant multipliers using $V_{gs}V_{ds}$ term.

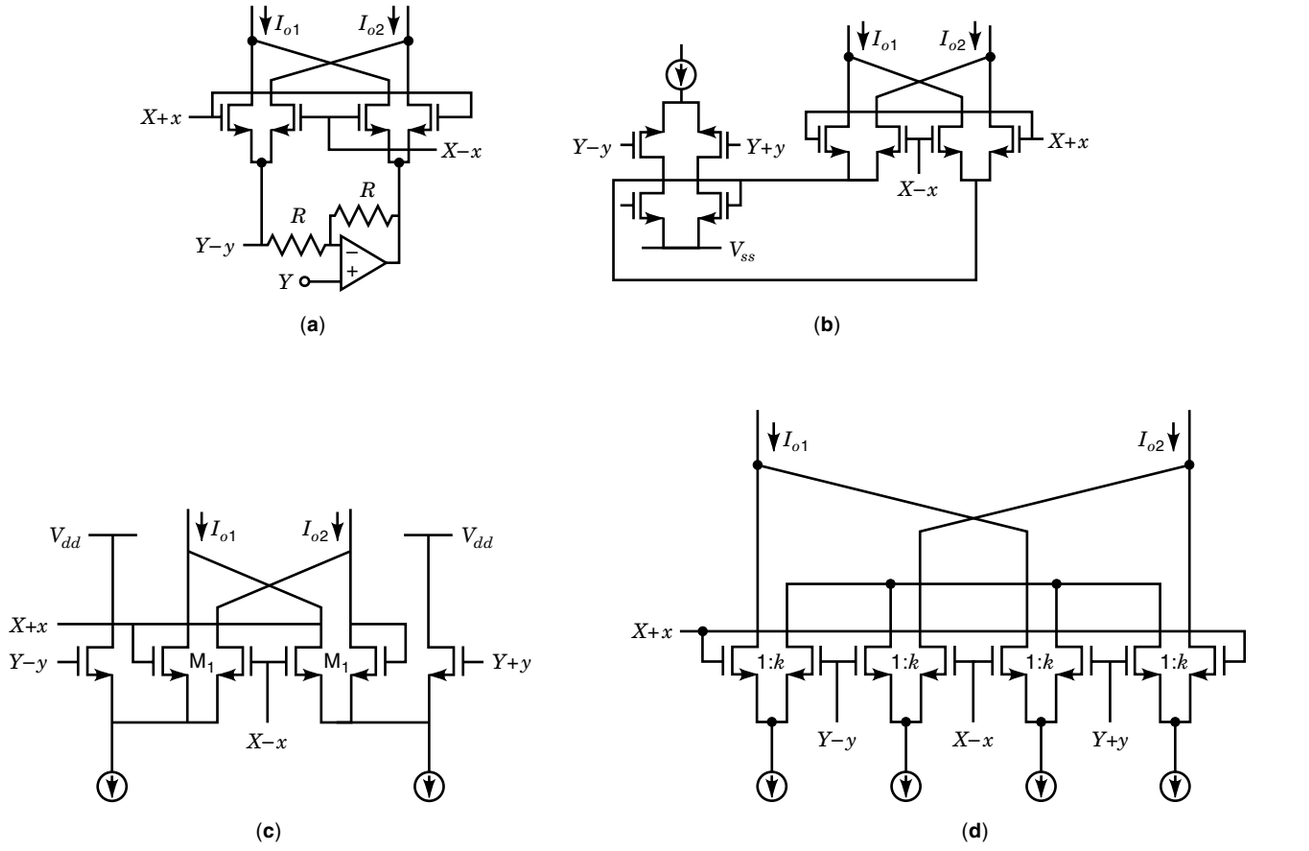

Figure 6. Source signal injection methods for multiplier using v_{gs}^2 term.

or a weighted-integrator (9–12). The configuration in Fig. 3(b) uses MOS source followers and achieves multiplication as in Eq. (5) except y in Eq. (5) is replaced with $Y \pm y - V_t$. This configuration is reported in (13–17) with gain enhanced source follower.

A fully differential extension shown in Fig. 4 achieves complete common mode and power supply dependency cancellation and yields

$$I_o = I_{o1} - I_{o2} = (I_1 + I_3) - (I_2 + I_4) = 4K_1xy \tag{7}$$

or

$$V_o = -Z_f I_o = -4K_1 Z_f xy \tag{8}$$

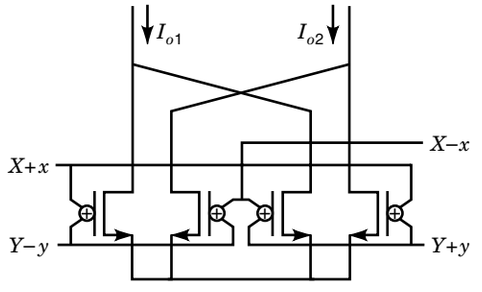

Figure 7. Multiplier that utilizes V_{gs}^2 using voltage adder. $\oplus$ represents voltage adder circuit.

The variations of Fig. 4(a) are reported in Refs. 18–21 and the circuit in Fig. 4(b) is reported in Ref. 22. The V_{ds} of M_1, which is operating in linear region, also can be applied by two source followers as shown in Fig. 4(c) (23,24).

Using V_{gs}^2 with Gate and Source Injection

A four-quadrant multiplier based on the topology in Fig. 1(b) can be realized by four cross-coupled transistors as shown in Fig. 5 whose output current, I_o, is

$$I_o = I_{o1} - I_{o2} = 4Kxy \tag{9}$$

Varieties of source signal application methods are reported in the literature. Figure 6(a) uses an op-amp (26), (b) uses a linear differential amplifier (27), and (c) uses source followers. A separate source follower, as shown in Fig. 6(d) (28), can be provided to each transistor in cross-coupled transistors. A gain-enhanced source follower (29–34) or a BJT buffer (35) can be used to apply the source signal. This type is the most widely implemented multiplier structure.

Using V_{gs}^2 with Voltage Adder

Another way to utilize the V_{gs}^2 term of MOS transistor operating in saturation region is to apply the sum or difference of two input signals to the gate of MOS transistor while the source voltage is fixed, as shown in Fig. 7(a). This configuration is reported in (36–38) using a capacitive adder, in Ref. 39 using resistive adder, in Refs. 40–43 using an active adder,

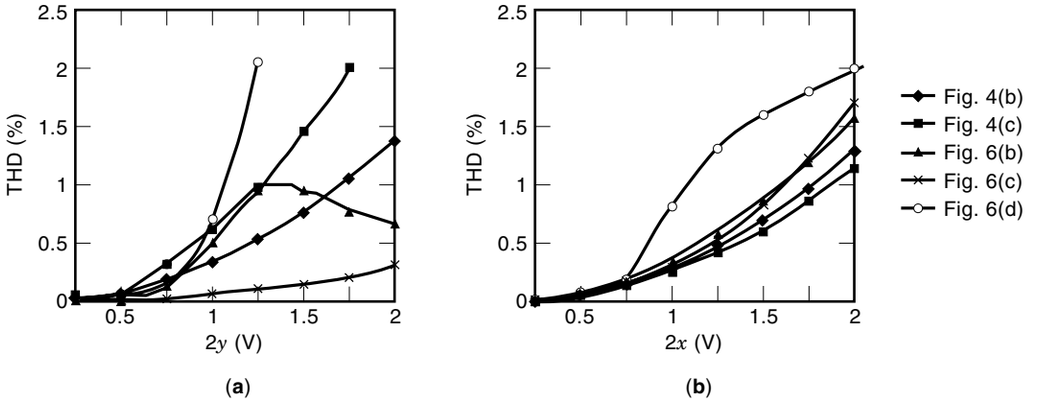

Figure 8. Simulated total harmonic distortion for W/L = 10 μm/10 μm for all transistor. The X and Y are set to allow IV input range for x, y. (a) $2x$ = 1 V; (b) $2y$ = 1 V.

and in Refs. 44–46 using programmable floating voltage source. This type has the following output:

$$I_o = 4KK_a xy \tag{10}$$

where K_a is the gain of the voltage summing circuit and K is the transconductance coefficient as usual. Reference 47 provides a summary of this multiplier type.

REMARKS ON MULTIPLIER STRUCTURES

None of the above analyses includes higher order effects such as the γ-effect, λ-effect, and mobility degradation effect. These effects are more severe in short channel devices. Besides the higher order effect of MOS in the multiplier core, the nonidealities of the source follower and voltage adder were not considered. Another practical limitation of the multiplier is the component mismatch that causes nonlinearity and offset.

The measurements of multiplier performance can include input range, linearity, common mode effects, minimum power supply voltage, power consumption, silicon area, frequency range noise, and so on. Since all these performance measures are strongly design dependent there is not an absolute standard comparison metric. However, the circuits in Fig. 4(a), Fig. 6(a), and Fig. 7 require additional circuitry and there is no clear theoretical advantage. These circuits are not discussed further in this article. Following detailed analysis for the rest of circuits will suggest the most recommended analog MOS multiplier structure.

Linearity. The linearity simulation result in Fig. 8 shows that circuit Fig. 4(c) and Fig. 6(d) have poor linearity. The performances of the circuits in Fig. 4(b) and Fig. 6(c) are strongly dependent on the ideality of source follower. Figure 9 shows that the linearity of circuit Fig. 4(b) improves as the source follower uses larger W/L ratio. On the contrary, this effect is not clear for circuit Fig. 6(c). This result implies that circuit Fig. 4(b) can outperform circuit Fig. 6(c) when K_2 is large enough (at least three times larger than K_1). Although the simulated linearity in Fig. 8 of the circuit Fig. 6(b) is comparable with others, Monte Carlo analysis reveals that high sensitivity to process variation causes poor linearity.

Figure 10 shows the linearity error measured from the fabricated multiplier using Orbit 2μm N-well process. These multipliers were designed with identical transistor size [$(W/L)_1$ = 4 μm/17 μm and 50 μm/10 μm for all others], transconductance, power consumption (360 μW), and input range ($\pm$2 V differential input range for both x and y). The linearity error of the circuit Fig. 4(b) is lower than 0.5%. It is much better than the other because the W/L ratio of the source follower is much larger than that of M_1. These results agree well with the simulation results discussed above.

Input Range and Minimum Power Supply Voltage. Input ranges of circuits Fig. 4(b) and Fig. 6(c) are obtained from their bias conditions shown in Fig. 11. The conditions for circuit Fig. 4(b) are

$$\begin{cases} V_t < X \pm x \\ V_1 = Y \pm y - V_t < X \pm x - V_t \\ V_t < Y \pm y \\ Y \pm y - V_t < V_d \end{cases} \tag{11}$$

These conditions are depicted in Fig. 12(a). The conditions for circuit Fig. 6(c) are

$$\begin{cases} V_{dssat} < V_1 = Y \pm y - V_t \\ V_1 + V_t = Y \pm y < X \pm x \\ X \pm x - V_t < V_d \end{cases} \tag{12}$$

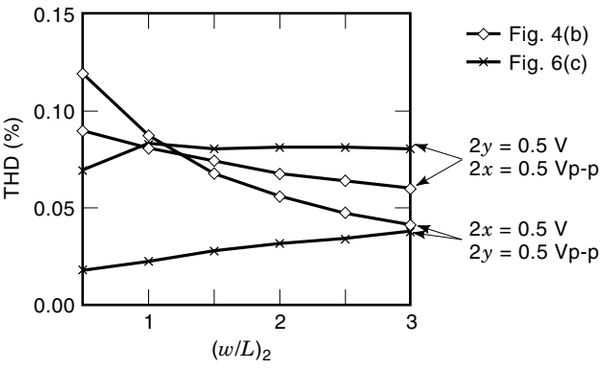

Figure 9. The effect of source follower transistor W/L ratio on THD. The length of the source follower is fixed to 10 μm. All other transistors have W/L = 10 μm/10 μm. The linearity of circuit Fig. 4(b) improves as the source follower uses larger W/L ratio.

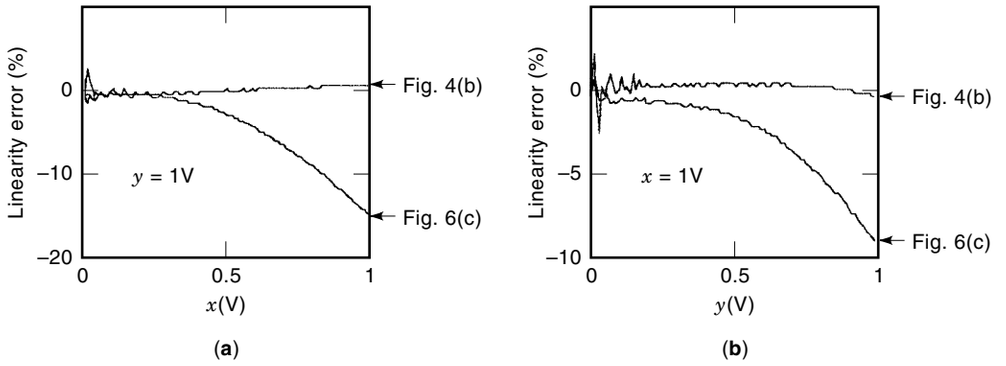

Figure 10. Measured linearity error from a fabricated chip. $(W/L)_1 = 5\ \mu m/17\ \mu m$ and $(W/L)_2 = 50\ \mu m/10\ \mu m$. For simplicity, only one quadrant is shown. (a) Linearity error for fixed y; (b) Linearity error for fixed x.

These conditions are depicted in Fig. 12(b). For the same input range and output node voltage swing, V_o, circuit Fig. 4(b) requires much lower power supply voltage than Fig. 6(c).

Noise. Another performance measure of a multiplier is noise, especially for small signal applications where the input range is not a major concern. A thermal noise current power density of a MOS transistor is conventionally modeled as

$$\begin{cases} \overline{i^2_{n;lin}} = 4kTg_{ds}df \\ \overline{i^2_{n;sat}} = \dfrac{8}{3}kTg_m df \end{cases} \tag{13}$$

for transistor operating in linear and saturation, respectively. In the case of circuit Fig. 4(b), total output noise current is given

$$\begin{aligned} \overline{i^2_{n;o}} &= 4\left(\overline{i^2_{n;lin}} + \overline{i^2_{n;sat}}\right) = 4\left(4kTg_{ds1}df + \frac{8}{3}kTg_{m2}df\right) \\ &= 16kT\left(g_{ds1} + \frac{2}{3}g_{m2}\right)df \end{aligned} \tag{14}$$

where

$$\begin{aligned} g_{ds1} &= K_1(V_{GS1} - V_t - V_{DS1}) \\ &= K_1(X - V_t - (Y - V_t)) = K_1(X - Y) \end{aligned} \tag{15}$$

$$g_{m2} = \sqrt{2K_2I_{DQ}} = \sqrt{2K_2K_1\left(X - V_t - \frac{Y - V_t}{2}\right)(Y - V_t)} \tag{16}$$

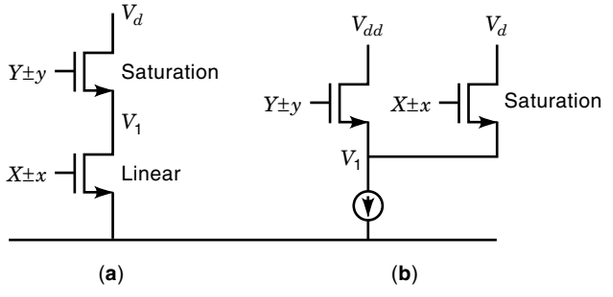

Figure 11. Bias conditions. (a) Circuit Fig. 4(b); (b) Circuit Fig. 6(c).

In the case of the circuit in Fig. 6(c), if the current source has the same transistor size as the source follower, then the total output noise current is given

$$\overline{i^2_{n;o}} = 4\left(\overline{i^2_{n;M2}} + \overline{i^2_{n;M1}}\right) = 4^*\frac{8}{3}kT(g_{m2} + g_{m1})\,df \tag{17}$$

As g_{m1} in Eq. (17) is much larger than g_{ds1} in Eq. (14), the circuit in Fig. 6(c) has higher output noise. The output noise floors of fabricated multipliers are measured with 1 KΩ resistor at 1 Khz. The circuit in Fig. 4(b) shows 26 dB lower noise floor than the circuit in Fig. 6(c).

DESIGN ISSUES OF THE CIRCUIT IN FIG. 4(b)

Table 1 summarizes the above comparisons and proposes that the circuit in Fig. 4(b) is the most suitable analog CMOS multiplier structure. The circuit in Fig. 4(b) has a clear tradeoff

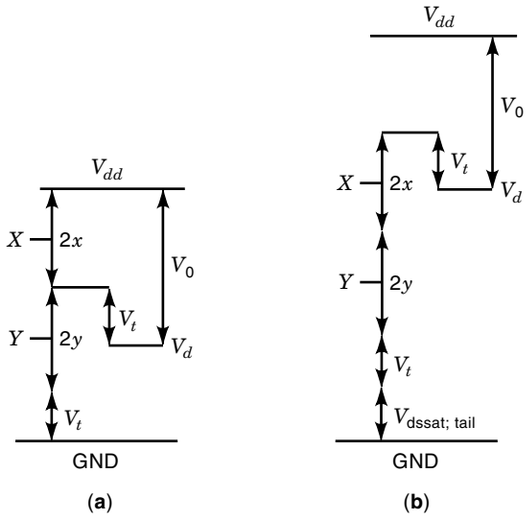

Figure 12. Input range and power supply voltage. When input range is 1 V for both x and y, threshold voltage $V_t = 1$ V, and output signal swing is 2 V, the minimum power supply voltages are 3 and 4 V, respectively for the circuits in Fig. 4(b) and Fig. 6(c). (a) Circuit Fig. 4(b); (b) Circuit Fig. 6(c).

Table 1. Summary of Comparisons[a]

Circuit	Operating Region	Complexity	Linearity	Sensitivity	Minimum Power Supply	Noise
Fig. 4(a)	Linear	bad				
Fig. 4(b)						
Fig. 4(c)			bad			
Fig. 6(a)	Saturation	bad				
Fig. 6(b)				bad		
Fig. 6(c)					bad	bad
Fig. 6(d)			bad			
Fig. 7(a)		bad				
Fig. 7(b)		bad				

[a] Gray areas were not analyzed because circuit had already shown poor performance.

between noise and linearity. The input reflected equivalent noise voltage of the circuit in Fig. 4(b) is obtained by dividing Eq. (14) by the square of transconductance of multiplier, G_m, which is determined by K_1 as in Eq. (7), yielding

$$\overline{v_{n;i}^2} = \frac{\overline{i_{n;o}^2}}{G_m^2} = \frac{\overline{i_{n;o}^2}}{16K_1^2} = \frac{kT}{K_1^2}\left(g_{ds1} + \frac{2}{3}g_{m2}\right)df \tag{18}$$

when other input is unity. Substituting g_{ds1} and g_{m2} in Eq. (18) with Eqs. (15) and (16) results in

$$\overline{v_{n;i}^2} = \frac{kT}{K_1}\left((X-Y) + \frac{2}{3}\sqrt{2\frac{K_2}{K_1}\left(X - \frac{Y+V_t}{2}\right)(Y-V_t)}\right)df \tag{19}$$

This analysis suggests that $(X - Y)$ and K_2/K_1 should be reduced to improve the noise performance for given K_1. This is the direct tradeoff with linearity and input range because K_2/K_1 should be increased to improve linearity as illustrated in Fig. 9 and $(X - Y)$ determines the input range as shown in Fig. 12(a).

Figure 13 shows the noise simulation result. The output noise is a linear function of K_1 as in Eqs. (14)–(16). When the source follower's transconductance is large enough [$(W/L)_2$ = 20], the input reflected noise is inversely proportional to $(W/L)_1$ as in Eq. (19) because Eq. (19) is based on the assumption that the source follower is an ideal one. If the source follower is not large enough [$(W/L)_2$ = 10], Eq. (19) is no longer valid, as shown in Fig. 13(b). The noise performance begins to degrade when K_2/K_1 ratio is smaller than 3 [$(W/L)_2$ = 10 and $(W/L)_1$ = 3]. Figure 14 shows the noise dependency on source follower size and suggests that the K_2/K_1 ratio should be larger than 3. These analyses lead to two conflicting observations as follows:

1. From Fig. 13(b) and Fig. 14, the K_2/K_1 ratio should be larger than 3 to make Eq. (19) valid.
2. From Eq. (19), the K_2/K_1 ratio should be minimized for low input reflected noise.

These two observations lead us to the conclusion that the optimal K_2/K_1 ratio for low noise design is around 3 in this specific process. Note that the K_2/K_1 ratio should be maximized for high linearity.

Figure 15 shows that the input noise is almost a linear function of the difference of two input common-mode voltages, $(X - Y)$, as expected in Eq. (19). This difference is equivalent to the summation over half of the input range. Therefore, for low noise design, the input range should be minimized.

In designing the circuit Fig. 4(b), K_2/K_1 ratio $(X - Y)$ are key design parameters that determine the direct tradeoffs among noise, linearity and input range.

CONCLUSION

Although a large number of MOS transconductance multipliers are reported in the literature only few practical MOS multiplier structures are discussed here. As the current trend of circuit design is low voltage and low power, the circuit shown in Fig. 4(b) seems to be one of the most attractive low voltage and high performance MOS transconductance multipliers. A BiCMOS version that uses BJT instead of source follower, or a careful design, will improve its performance further.

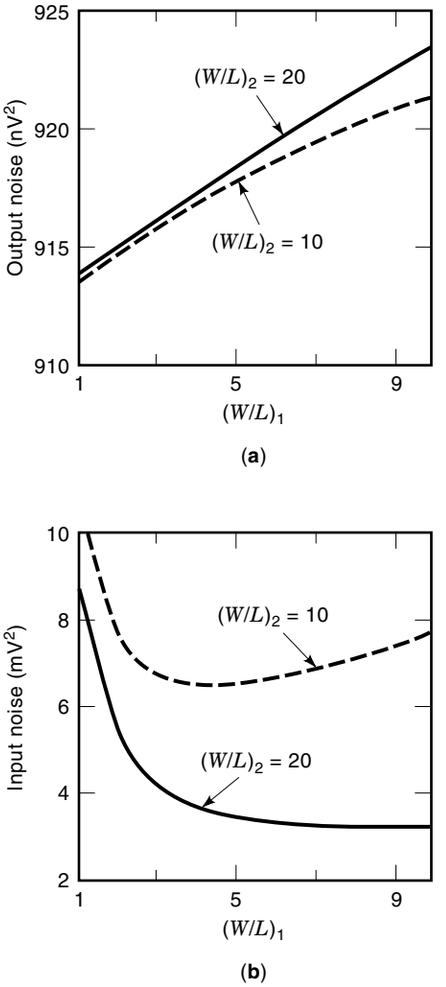

Figure 13. Noise dependency on W_1. $L_{1,2}$ = 10 μm, $(X + Y)/2$ = 4 V and $X - Y$ = 2 V. The output noise is measured at the one of the output node with 50 Ω load resistor and integrated within 1 MHz ~ 2 MHz range. (a) Output noise. The output noise is almost a linear function of W_1. (b) Input reflected noise. Input reflected equivalent noise is inversely proportional to W_1.

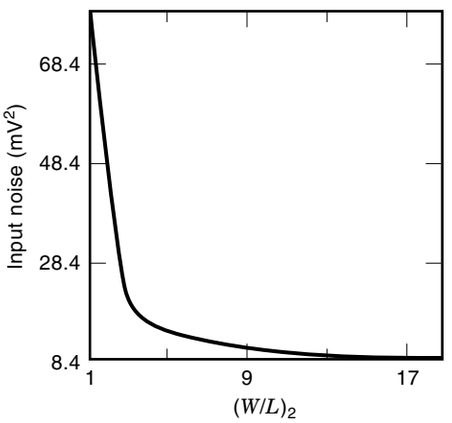

Figure 14. Input noise dependency on $(W/L)_2$: $(W/L)_1$ = 10 μm/10 μm, $V_{com} = (X + Y)/2$ = 4 V and $X - Y$ = 2 V. $(W/L)_2$ should be larger than 3 for low noise design.

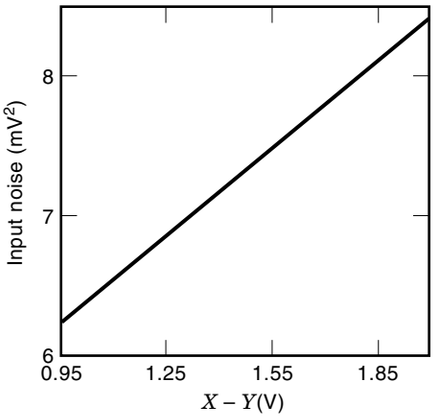

Figure 15. Noise dependency on $(X - Y)$ for L = 10 μm, W_1 = 10 μm, W_2 = 200 μm and V_{com} = 4 V. Input reflected noise is a linear function of input range, $(X - Y)$.

The reader should be aware that this conclusion might not hold for all cases. The choice of circuit topology is completely dependent on design specifications. The reader also should note that, in general, a BJT multiplier outperforms any MOS multipliers and no commercial discrete MOS multiplier has been produced.

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