TUNNEL DIODE CIRCUITS

TUNNEL DIODE OSCILLATORS. SEE TUNNEL DIODE CIRCUITS. TUNNEL DIODE AMPLIFIERS. SEE TUNNEL DIODE CIRCUITS.

Tunnel diodes are important two-terminal p–n junction devices, since they give a negative incremental resistance. This characteristic is obtained by tunneling due to a very high doping level and allows them to be used for such things as amplification, creation of oscillations, modulation and demodulation, logic, and memory. They were first introduced in the 1958 paper of Leo Esaki (1) and consequently are often called Esaki diodes. The circuit symbol is shown in Fig. 1(a), and a typical dc current-versus-voltage curve in Fig. 1(b), where the local peak and valley values are indicated. In Fig. 1(b) the initial (positive) slope near the origin is due to the tunneling, and the positive slope further out is due to the normal diode action of a p–n junction diode. The transition between these two regions is seen to give a negative slope and is the reason for the utility of the tunnel diode.

MODELS AND EQUIVALENT CIRCUITS

Theoretical models for the tunnel-diode $i(v)$ characteristics give the general shape, but the values are somewhat off (2, p. 44; 3, p. 47). Consequently, it is more useful in circuit designs to use curve-fitted models. A meaningful one is the piecewise linear model (4, p. 1049)

$$i(v) = P_0 + P_1 v + P_2|v - V_\mathrm{p}| + P_3|v - V_\mathrm{v}| \tag{1}$$

where V_p is the peak voltage, V_v is the valley voltage, and the vector of coefficient constants $P = [P_0, P_1, P_2, P_3]^\mathrm{T}$, (using $^\mathrm{T}$ for transpose) can be found by choosing i,v pairs at four independent points and solving the four resulting linear equtions; good choices are at $v = 0$, V_p, V_v, $2V_\mathrm{v}$. Different currents can be obtained by design of the junction area; typical values are $V_\mathrm{p} = 50$ mV (with $I_\mathrm{p} = 2$ mA) and $V_\mathrm{v} = 200$ mV (with $I_\mathrm{v} = 0.3$ mA) (3, p. 49). If we set

$$A = \begin{bmatrix} 1 & 0 & V_\mathrm{p} & V_\mathrm{v} \\ 1 & V_\mathrm{p} & 0 & V_\mathrm{v} - V_\mathrm{p} \\ 1 & V_\mathrm{v} & V_\mathrm{v} - V_\mathrm{p} & 0 \\ 1 & 2V_\mathrm{v} & 2V_\mathrm{v} - V_\mathrm{p} & V_\mathrm{v} \end{bmatrix} \tag{2}$$

then by assembling the currents at these points into the vector I of currents

$$I = [0, I_\mathrm{p}, I_\mathrm{v}, I_{2\mathrm{v}}]^\mathrm{T} \tag{3}$$

we have

$$P = A^{-1} I \tag{4}$$

Figure 1c shows the curve obtained from Eq. (1) for (V_p, I_p) = (0.05 V, 2 mA), (V_v, I_v) = (0.2 V, 0.3 mA), and ($2V_\mathrm{v}$, $\mathrm{I}_{2\mathrm{v}}$) = (0.4 V, 2 mA), giving $P = [-0.0007, 0.024, -0.026, 0.009917]^\mathrm{T}$. In actual fact a better curve fit is found by replacing I_p with $1.1I_\mathrm{p}$ and I_v with $0.9I_\mathrm{v}$.

When used in small-signal amplifiers, the diode is normally biased to operate in the middle of the negative-resistance region (at the inflection point). There the small-signal equivalent circuit is as shown in Fig. 2 (5, p. 310), where the main element of interest is the negative conductance, $-g$, the other elements being parasitics, which generally limit the frequency response. C_j is the junction

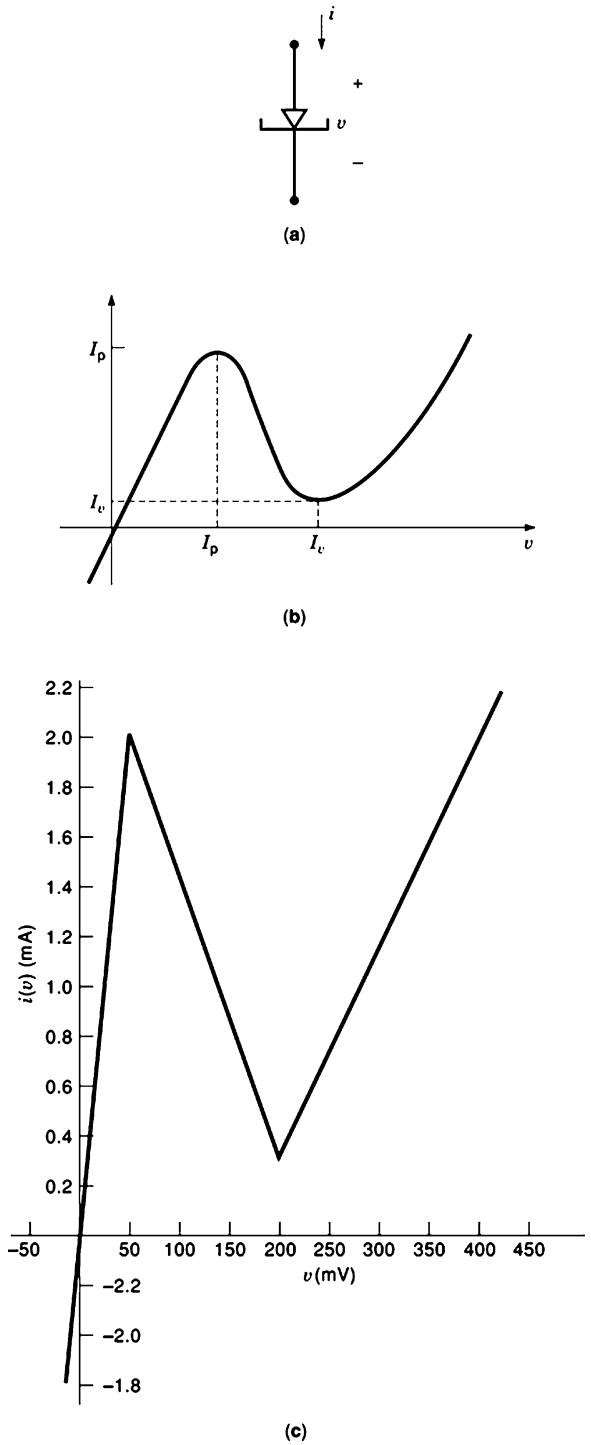

Figure 1. Tunnel diode: (a) symbol; (b) typical dc characteristic; (c) piecewise approximation to characteristic.

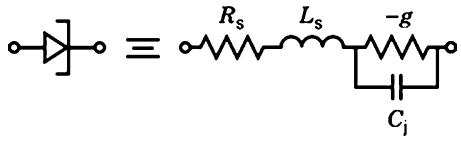

Figure 2. Equivalent circuit.

capacitance at the bias point, this being given by (3, p. 67)

$$C_j = C_{jv}\left(\frac{V_j - V_v}{V_j - V_{bias}}\right)^{1/2} \tag{5}$$

where C_{jv} is the capacitance at the valley and V_j is the internal junction voltage at V_{bias}. Typical values of C_{jv} are in the range of 0.1 pF to 10 pF. R_s and L_s are the lead resistance and inductance, normally on the order of 1 Ω and 100 pH.

As can be seen from Fig. 1(b), when the peak current is made larger (by a using bigger junction area), the diode negative resistance decreases (diode conductance g increases), since the peak and valley voltages V_p and V_v are fixed. Thus, increasing the power-handling capability of a tunnel diode, by designing for larger peak currents, normally decreases the efficiency of conversion of bias into signal power.

OSCILLATOR

The negative resistance region of the tunnel diode can be used in the design of several circuits such as oscillators and pulse generators. In this section, applications to pulse and sinusoidal oscillators are introduced. First we give the basic circuit and set up the differential equation that illustrates the concepts. Consider Fig. 3, where the voltage source E biases the tunnel diode into the negative-resistance region. The inductor and capacitor are set to give the fundamental frequency of oscillation, ω_0, and the signal is generated across the load resistor R_L. In order for the circuit to oscillate, the negative conductance should be larger than the load conductance $G_L = 1/R_L$. Since the tunnel-diode curve has positive slope for signals outside the negative-resistance region, the oscillations become limited by the range of voltage from V_v to V_p, in which case the circuit is really a relaxation oscillator. Assuming the inductor and capacitor are without loss, the describing state equations for Fig. 3 are

$$L\frac{di_L}{dt} = v - E \tag{6a}$$

$$C\frac{dv}{dt} = -i_L - f(v) - G_L v, \qquad \text{where} \quad G_L = 1/R_L \tag{6b}$$

Differentiating the second equation and substituting into it the first, setting $x = v - E$ and $F(x) = df(v)/dv$ with v replaced by $x + E$, and noting that $dx/dt = dv/dt$, we get the Van der Pol equation

$$\frac{d^2x}{dt^2} + [F(x) + G_L]\frac{dx}{dt} + \frac{x}{LC} = 0 \tag{7}$$

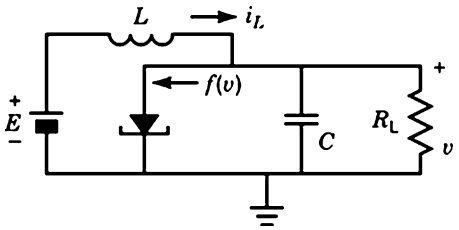

Figure 3. Tunnel-diode oscillator.

Here the undamped natural frequency, that obtained when $F(x) = -G_L$, is $\omega_0^2 = 1/LC$. But because $F(x)$ is nonlinear and both positive and negative, the actual frequency is only approximately ω_0 and is difficult to obtain analytically, so it is best found from simulations.

When $F(x) + G_L$ is negative (in the negative-resistance region of the tunnel diode), this system is a relaxation oscillator and exhibits a unique limit cycle. When $F(x) + G_L$ is only slightly negative, the response is very close to a sinusoidal one, since the limit cycle is bounded to almost within the negative-resistance portion of $F(x) + G_L$. But if G_L is small (that is, the load resistance is large), then the limit cycle covers a much larger portion of the positive-resistance portion of $F(x) + G_L$, in which case the output becomes more pulselike. Thus, by adjusting the parallel resistance one can produce different classes of oscillations with this tunnel-diode oscillator. The situation is illustrated by the time-domain curves of Fig. 4 for the tunnel diode using the approximation of Fig. 2 with $C = 1$ nF, $L = 10$ μH, and $E = (V_p + V_v)/2 = 1.25$ V. In Fig. 4 are shown inductor currents and capacitor voltages for two values of the load resistor. In the case where the positive load resistor (here 85 Ω) almost cancels the negative resistance (−84 Ω) of the tunnel diode, designated by subscripts 1, we obtain a sinusoidal output voltage, while when the load resistor is very large (100 MΩ), designated by subscripts 2, the output voltage is more pulselike. The limit cycles and effective conductances (tunnel diode in parallel with R_L) seen by the LC circuit are shown in Fig. 5(a), for the 85 Ω, and (b), for the 100 MΩ, cases. As seen from Fig. 5(a), the sinusoidal case results when the load resistance is effectively canceled by the tunnel-diode negative resistance.

Other circuits and results can be found in Ref. 6, pp. 810–811.

AMPLIFIERS

Because the negative incremental resistance can be used to cancel losses in a circuit, the tunnel diode can be used to achieve gain. In practice such tunnel-diode amplifiers are used at microwave frequencies, where there are two main classes of amplifiers designed with tunnel diodes: transmission and reflection amplifiers. Figure 6 shows the basic configurations for both types, where a Norton equivalent input source is shown for convenience in treating previous transistorized stages. Since these are small-signal amplifiers, the equivalent circuit of Fig. 2 replaces the tunnel diode, for most designs the series resistance and inductance are assumed negligible. Various alternative config-

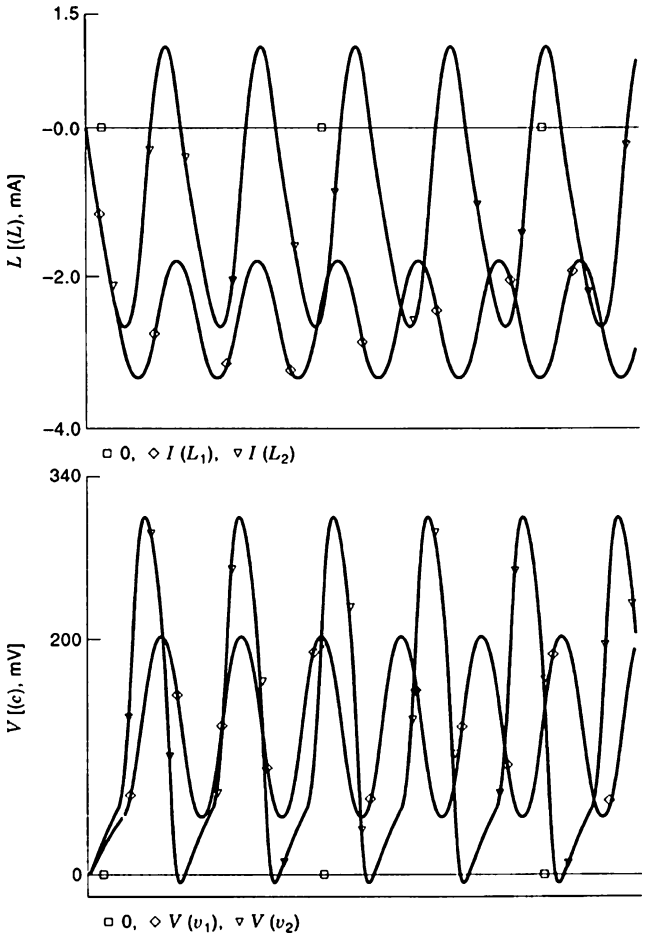

Figure 4. Oscillations of the oscillator.

urations are shown in Fig. 7, which includes two other types of transmission amplifiers and one other reflection one. In both Figs. 6 and 7 the designated 2-ports are taken to be lossless, in which case the tunnel-diode parasitic capacitance, which is a lossless component, is absorbed in them during design. And since microwave frequencies are most often involved, the circuit descriptions are most conveniently expressed through scattering matrices. Consequently, before discussing the amplifiers further, we review a bit of the necessary scattering theory.

Consider the 2-port of Fig. 8, where we define 2-vectors of port currents i and voltages v. Using s for the complex frequency variable, these are used to define the 2×2 scattering matrix $S(s)$ through the incident (v^{i}), and reflected, (v^{r}), scattering variables, with respect to the positive reference port resistances R_1 and R_2, which form the diagonal matrix $R = \mathrm{diag}[R_1, R_2]$, by

$$2v^{\mathrm{i}} = v + Ri, \qquad 2v^{\mathrm{r}} = v - Ri \tag{8a,b}$$

$$v^{\mathrm{r}} = Sv^{\mathrm{i}} \tag{8c}$$

Since the designs are actually based on the input impedance, we note that, for $v = Zi$,

$$S = (Z - R)(Z + R)^{-1} = R(Z + R)^{-1}(Z - R)R^{-1} \tag{9a,b}$$

and, using 1_2 for the 2×2 identity matrix,

$$ZR^{-1} = (1_2 + S)(1_2 - S)^{-1} = (1_2 - S)^{-1}(1_2 + S) \tag{10a,b}$$

The lossless condition is important for the design and physically means that the total input power is zero in the sinusoidal steady state; this is expressed (7, p. 122) in terms of S as

$$\mathrm{SS}_* = 1_2 \tag{11}$$

where the lower asterisk denotes matrix transposition along with complex conjugation (s replaced by its negative and complex conjugated; for circuits with real elements this means transpose and replace s by $-s$). Loading a 2-port with a 1-port scattering variable (reflection coefficient) S_{L} gives the input reflection coefficient in terms of the 2-port S as

$$S_{\mathrm{i}} = \frac{\det \mathrm{S} + s_{11}S_{\mathrm{L}}}{s_{22} + S_{\mathrm{L}}} \tag{12}$$

In the case of a tunnel diode load of resistance $-R_{\mathrm{td}}$, as in Fig. 6, then

$$S_{\mathrm{L}} = \frac{-R_{\mathrm{td}} - R}{-R_{\mathrm{td}} + R} = \frac{R_{\mathrm{td}} + R}{R_{\mathrm{td}} - R} = \frac{1}{\bar{\bar{S}}_{\mathrm{L}}} \tag{13}$$

where $\bar{\bar{S}}_L$ is the reflection coefficient of a positive resistor of value R_{td}. Substituting Eq. (13) into (10a,b), and using Eq. (11), for which the determinants satisfy $\det(S) = 1/\det(S_*)$, yields the input reflection coefficient

$$\bar{\bar{S}}_{\mathrm{i}}(s) = \frac{\det S + s_{11}/S_{\mathrm{L}}}{s_{22} + 1/S_{\mathrm{L}}} = \frac{S_{\mathrm{L}} + s_{11*}}{s_{22*}S_{\mathrm{L}} + \det \mathrm{S}_*} = \frac{1}{S_{\mathrm{i}}(-s)} \tag{14}$$

Equation (15) says that to synthesize the 2-port with a negative resistance (tunnel diode) for the load we synthesize $1/S_{\mathrm{i}}(-s)$ with a positive load resistor equal in magnitude to that of the negative resistance and then turn the 2-port around and load it with the tunnel diode to get the desired $S_{\mathrm{i}}(s)$.

Tunnel-diode amplifiers are primarily designed through specification of the transducer power gain $G(\omega)$ in the sinusoidal steady state, $s = j\omega$, this being defined as

$$G = \frac{\text{power delivered to the load}}{\text{power available from the source}} \tag{15a}$$

$$= 4(G_{\mathrm{L}}G_{\mathrm{s}})\left|\frac{V_{\mathrm{o}}}{I_{\mathrm{s}}}\right|^2 = \frac{G_{\mathrm{L}}}{G_{\mathrm{s}}}\left|\frac{V_{\mathrm{o}}}{v_1{}^{\mathrm{i}}}\right|^2 \tag{15b}$$

since $|I_{\mathrm{s}}|^2/(4G_{\mathrm{s}})$ is the power available from the source, and the power into the load is $G_{\mathrm{L}}|V_0|^2$ for the circuit of Fig. 6, while $v_1{}^{\mathrm{i}} = I_{\mathrm{s}}/G_{\mathrm{s}}$ as in Eq. (4) if $R_1 = R_{\mathrm{s}}$ is chosen.

Considering first the transmission amplifier, the results depend upon the size of the load resistor versus the tunnel diode resistance. Usually $G_{\mathrm{L}} > G_{\mathrm{td}}$ for load stability, so assume that $R_2 = 1/(G_{\mathrm{L}} - G_{\mathrm{td}}) > 0$. Since $-R_2I_2 = V_2$ we have $V_{\mathrm{o}} = v_2{}^{\mathrm{r}}$ and $v_2{}^{\mathrm{i}} = 0$, as seen from Eq. (8a,b), giving $V_{\mathrm{o}}/v_1{}^{\mathrm{i}} = v_2{}^{\mathrm{r}}/v_1{}^{\mathrm{i}} = s_{21}$. For the reflection amplifier, the 3-port circulator is described by the following 3×3 scattering matrix, where we choose as its reference matrix $R = \mathrm{diag}[R_{\mathrm{s}},$

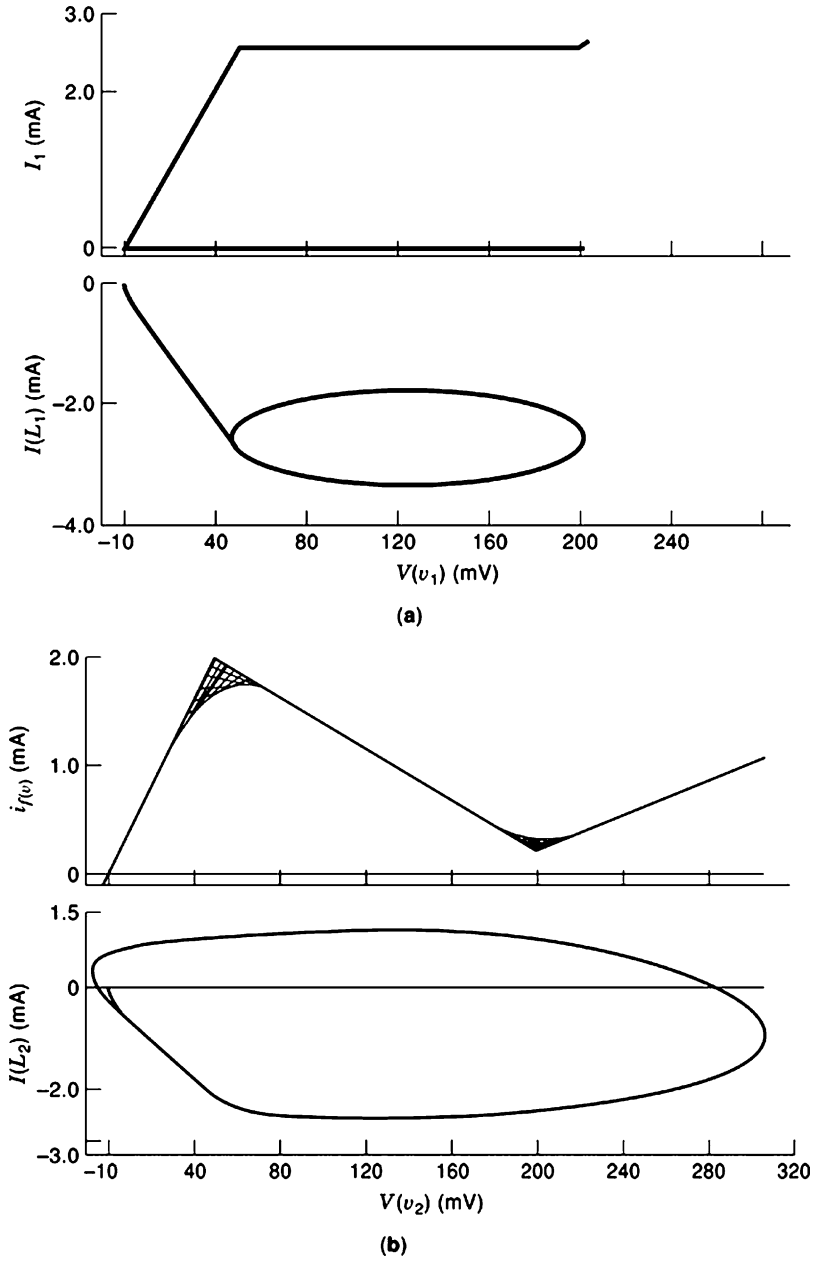

Figure 5. Limit cycles and effective conductances: (a) $R_L = 85\ \Omega$; (b) $R_L = 100\ M\Omega$.

R_1, R_L]:

$$\mathbf{S}_{\text{circ}} = \begin{bmatrix} 0 & 0 & 1 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \tag{16}$$

in which case $V_o = v_{3\text{circ}}{}^r = v_{2\text{circ}}{}^i = v_{1,2\text{port}}{}^r = S_{i,2\text{port}} v_{1,2\text{port}}{}^i = S_{i,2\text{port}} v_{2\text{circ}}{}^r = S_{i,2\text{port}} v_{1\text{circ}}{}^i$; we also have $v_{1\text{circ}}{}^i = R_s I_s/2$. For the 2-port, though, if we choose its reference $R_2 = -R_{td}$, then $v_2{}^r = 0$ and hence $s_{21} v_1{}^i = -s_{22} v_2{}^i$, from Eq. (1), from which $v_1{}^r = (s_{11} - s_{12}s_{21}/s_{22}) v_1{}^i = (\det S/s_{22}) v_1{}^i = (1/s_{11}) v_{1i}$; that is, $S_{i,2\text{port}} = 1/s_{11}$, where s_{11} is the (1,1) entry of the lossless 2-port scattering matrix and $S_{i,2\text{port}}$ is the input reflection coefficient seen at port 1 when the tunnel diode is at port 2. We obtain $V_o/I_s = (R_s/2) S_{i,2\text{port}}(s) = (R_s/2)[1/s_{11}(s)] = (R_s/2)[1/S_{i,\text{port}}(-s)]$, the last by Eq. (14). Summarizing,

$$G(\omega) = \begin{cases} (G_L/G_s)|s_{21}(j\omega)|^2 & \text{for transmission amplifier } (G_L > G_{td}) \\ (G_L/G_s)|1/s_{11}(j\omega)|^2 & \text{for reflection amplifier} \end{cases} \tag{17}$$

Since synthesis is based on s_{11}, in the case of the transmission amplifier we convert to s_{11} via the (1,1) entry of the lossless constraint: $|s_{11}(j\omega)|^2 = 1 - |s_{21}(j\omega)|^2$; while for the reflectance amplifier we use $\bar{S}_L(s) = 1/s_{11}(-s)$ as derived above. Because the lossless 2-ports will be synthesized with passive components, we require $s_{11}(s)$, for the transmission amplifier, and $\bar{\bar{s}}_{11}(s)$ for the reflection amplifier, to be bounded real. Since we desire the tunnel-diode capacitance to be extracted from the lossless 2-port, we place a minus sign on the ratio of the highest powers of s in these reflection coefficients. Then the synthesis follows stan-

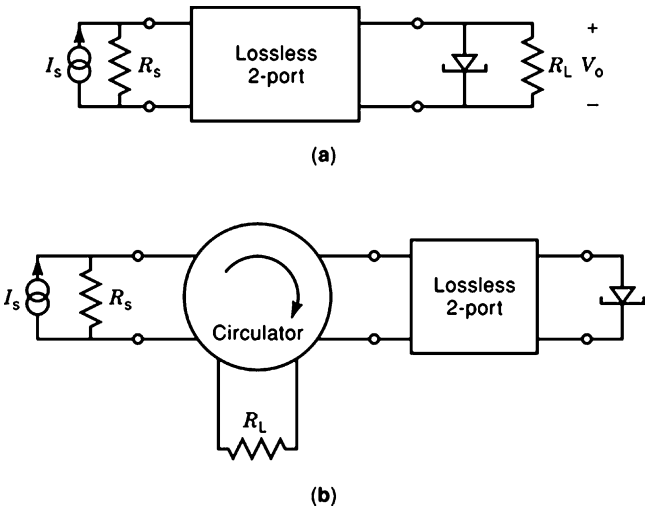

Figure 6. Basic tunnel-diode amplifiers: (a) transmission; (b) reflection.

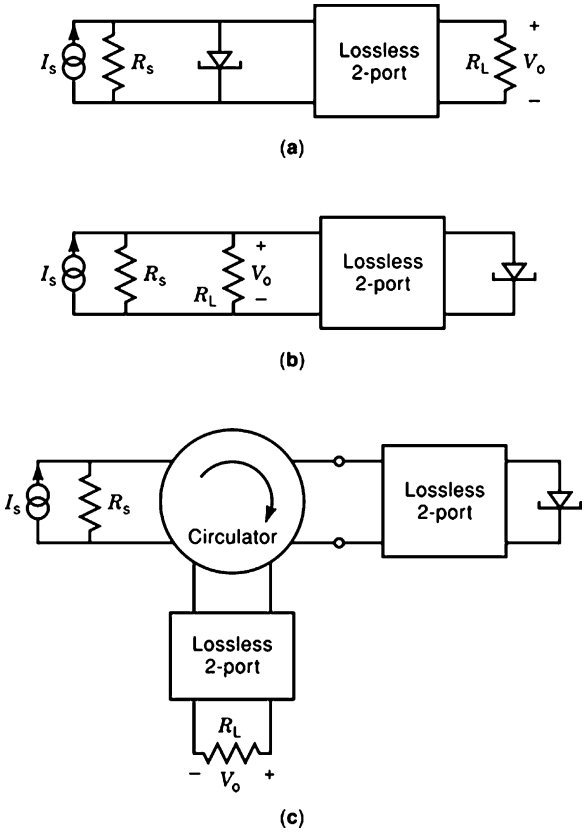

Figure 7. Alternative amplifier types: (a,b) transmission; (c) reflection.

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lossless 2-ports; a number of references for this are in Ref. 2, pp. 204–205.

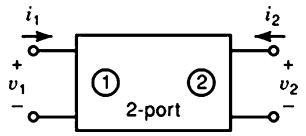

Figure 8. 2-port for discussion of scattering theory.

MEMORY

A computer system or any digital processing system requires memory. Usually, within each system, there are many different types of memory components. In the digital-circuit and computer jargons the two acronyms *RAM* and *ROM* is used to distinguish between two main classes of memory. ROM is read-only memory, whereas RAM usually refers to the kind of read and/or write memory that is called random-access memory. Basically, there are two types of MOS RAMs: static RAMs (*SRAM*s) and dynamic RAMs (*DRAM*s). SRAMs use bistable circuits such as latches to store binary data. On the other hand, DRAMs use capacitors to store binary data in the form of capacitor charges. Of course, storing binary data on a capacitor requires much less area than storing the same information on latches. However, due to capacitor discharges over time (leakage current), DRAMs require periodic refreshing to maintain and/or regenerate their data. It should also be noted that both dynamic and static RAMs are dependent on their dc power supply voltages, and therefore, in the absence of power supply, all stored data will be lost; hence RAM is *called volatile* memory (8, p. 1113; 9, p. 573).

Tunneling-based SRAM (*TSRAM*), in its simplest form, consists of a pass transistor and a pair of tunnel diodes. The first tunnel-diode SRAM was introduced by Goto et al. (.10, pp. 25–29], as shown in Fig. 9 (9, p. 578]. In Fig. 10, a load-line graph illustrates the two stable points for V_N(low) and V_N(high). As can be seen on the figure, these stable points (voltages V_N) are close to the supply voltages 0 and V_{dd}. A large restoring current will stabilize any perturbation about these two stationary points. Assume the stored datum is zero, and therefore the TSRAM is at its left stable point. This point corresponds to the low (almost zero) voltage V_N. At this point the restoring current I_1 is much larger than its opposing current I_2. Therefore any deviation from this stable point, $I_1 = I_2$, will cause more restoring current (discharging current) than opposing current (charging current) to flow through node N Therefore, the net current through node N will be discharging and will reduce the voltage at node N, V_N, to its stable zero value. On the other hand, assume a high bit is stored, which means V_N is almost equal to V_{dd}. In this case too, any reduction in V_N will be opposed by the restoring current (charging current) I_2. As can be seen in the Fig. 10, the restoring current I_2 is larger than its opposing current I_1. Therefore the net current, $I_2 - I_1$, will be a charging current, which will tend to restore the voltage V_N to it original value V_{dd}.

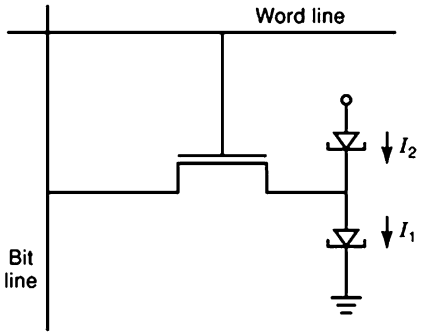

Figure 9. Tunneling-based SRAM.

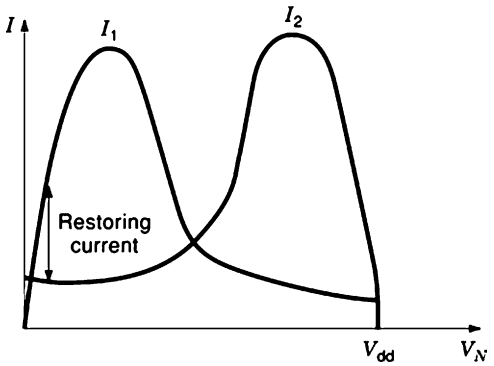

Figure 10. Operating principle of tunneling-based SRAM.

LOGIC-CIRCUIT APPLICATIONS

Introduction

The growth of technology demands larger, faster, and more efficient integrated circuits (*IC*s) on a single chip. Engineers and scientists have answered this demand by continually scaling down the size of transistors in fabrication. As a result, the newer IC chips have more transistors, faster switching speed, and less power consumption due to the size and supply voltage reduction. As this reduction in size continues, engineers are looking for alternative approaches. New and preliminary applications of resonant tunneling diodes in (*RTD*s) IC technology suggests that this device can help electrical engineers to design faster logic gates with fewer active devices (11,12). In addition to high speed, logic circuits using RTDs have fewer active elements and therefore are less complex in design and consume less power. Since the RTD is a latching structure, it can replace traditional latching structures; this would further reduce the total number of gates in the design.

Logic Circuits

Recent developments in semiconductor technology, such as molecular-beam epitaxy, have made it possible to integrate RTDs with conventional semiconductor devices. Here, the principle of operation of a logic circuit with RTDs and heterojunction bipolar transistors (*HBT*s) is discussed (11). Figure 11 shows such a RTD + HBT bistable logic circuit (11). There are m inputs $IN_1, \ldots, IN_m$, and one clock transistor CLK. All transistors, connected in parallel, are driving a single RTD load. Input transistors Q_1 to Q_m which are either on or off depending on the gate voltage, yield collector currents of I_h or zero respectively. The clock transistor will have two current states, I_{clkh} and I_{clkq} respectively for the high and quiescent conditions respectively. A global reset state is when all collector inputs are zero. Figure 12 shows the operation of this circuit. It shows the RTD load curve and all possible collector currents. It shows two groups of possible input currents, one for the quiescent clock transistor current (CLK Q), and the other for the high clock transistor current (CLK H). In each of the two groups, all possible total input-transistor collector currents are shown. Considering there are m input transistors, this means there are m levels of total transistor collector current one for each. When the clock transistor cur-

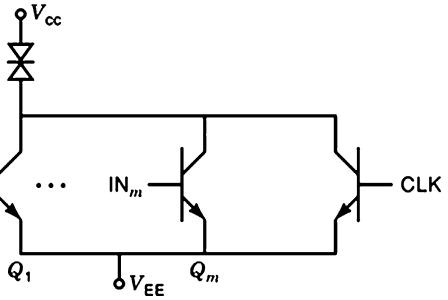

Figure 11. Schematic of the bistable RTD + HBT logic gate (11).

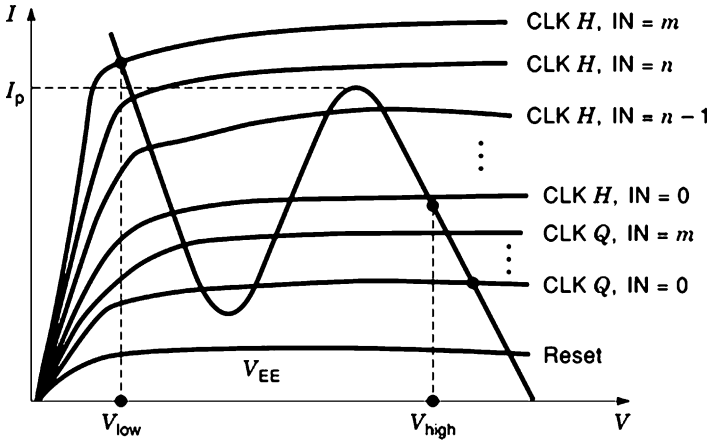

Figure 12. Operating principle of the bistable RTD + HBT logic gate (11).

rent is I_{clkq}, Fig. 12 shows that there are two stable states, a low and a high, for any possible input combination. When clock transistor current is I_{clkh}, Fig. 12 shows that there is exactly one, low stable state for any n or more high inputs. In other words, there is exactly one stable operating point when the RTD current is $nI_h + I_{clkh}$ or more. The operating sequence is as follows: First, reset the logic gate by resetting all collector currents to zero; this will cause the output to go high. Second, remove the reset signal and set the clock to high. Then, if n or more inputs are high, then the logic will go to low; otherwise it will be high. Third, change the clock to its quiescent level. This will reduce the clock current while the output logic remains the same.

Consider a three-input logic circuit. Now suppose n is 1. The output $f(x_1, x_2, x_3)$ is low (logic zero) if and only if one or more of the inputs x_1, x_2, x_3 are high. This by definition is a three-input NOR gate. Now assume n is 3. Then the output $f(x_1, x_2, x_3)$ is low (logic zero) if and only if all three inputs x_1, x_2, x_3 are high. This by definition is a three-input NAND gate. For $n = 2$, we obtain an inverted majority or inverted carry function.

This design scheme can be easily extended to consider weighted inputs. In such a case the output will be low if $w_1x_1 + w_2x_2 + \ldots + w_mx_m > n$. The circuit of Fig. 11 can be used to implement the above weighted function when the collector current of each transistor is weighted by a factor. This can be accomplished by using different transistors.

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