SWITCHED CAPACITOR NETWORKS

The requirement for fully integrated analog circuits prompted circuit designers two decades ago to explore alternatives to conventional discrete component circuits. A sound alternative was developed, a switched-capacitor (SC). The basic idea was replacing a resistor by a switched-capacitor C_R simulating a resistor. Thus, this equivalent resistor could be implemented with a capacitor and two switches operating with a two-phase clock. This equivalent resistor is equal to $1/f_C C_R$, where f_C is the sampling (clock) frequency. SC circuits consist of switches, capacitors, and operational amplifiers (op amps). They are described by difference equations in contrast to differential equations for continuous-time circuits. Concurrently

the mathematical operator to handle sample-data systems, such as switched-capacitor circuits is the z-transform, and the Laplace transform for continuous-time circuits. A host of practical properties of SC circuits have made them very popular in industry:

1. The time constants (RC products) from active-RC circuits become capacitor ratios multiplied by the clock period T_C, that is,

$$\tau = \frac{1}{f_C}\frac{C}{C_R} = T_C\left(\frac{C}{C_R}\right) \tag{1a}$$

where $T = T_c = 1/f_C$ is the sampling frequency. The accuracy of τ is expressed as

$$\frac{d\tau}{\tau} = \frac{dT_C}{T_C} + \frac{dC}{C} - \frac{dC_R}{C_R} \tag{1b}$$

Assuming that T_C is perfectly accurate gives

$$\frac{d\tau}{\tau} = \frac{dC}{C} - \frac{dC_R}{C_R} \tag{1c}$$

Because the two capacitors C and C_R are built close together, $d\tau/\tau$ compatible with conventional CMOS technologies is in the neighborhood of 0.1%.

2. Ordinarily the load of an SC circuit is mainly capacitive. Therefore the required low-impedance output-stage op amp is no longer required. This allows the use of a single-stage operational transconductance amplifier (OTA) which is especially useful in high-speed applications. Op amp and OTA are not differentiated in the rest of this article.
3. Reduced silicon area, because the equivalent of large resistors is simulated by small capacitors. Moreover, positive and/or negative equivalent resistors are easily implemented with SC techniques.
4. Switched-capacitor circuits are implemented in a digital circuit process technology. Thus, useful mixed-mode signal circuits are economically realized in standard MOS technology with available double-poly.
5. The SC design technique has matured. In the audio range, SC design techniques are the dominant design approach. Furthermore, many practical analog/digital (A/D) converters use SC implementations.

FUNDAMENTAL BUILDING BLOCKS

The fundamental building blocks in SC circuits are voltage-gain amplifiers, sample/holds integrators, and multipliers. A combination of these blocks is interconnected to yield a number of useful circuits.

Gain Amplifiers

The gain amplifier is a fundamental building block in switched-capacitor circuits. A voltage amplifier is implemented as shown in Fig. 1(a). The switched-capacitor resistor gives a dc path for leakage current but reduces further the low-frequency gain. A detailed analysis of this topology shows that the dc output voltage is equal to $-I_{\text{leak}}\,T/C_{\text{P}}$, with C_{P} the parasitic capacitor associated with the feedback path. The leakage current I_{leak} in switched-capacitor circuits is a result of the diodes associated with the bottom plate of the capacitors and the switches (drain and source junctions). This leakage current is about 1 nA/cm^2. Using typical analytical methods for switched-capacitor networks, it can be shown that the z-domain transfer function of this topology becomes

$$\begin{aligned} H(z) = \frac{V_0(z)}{V_i(z)} &\cong -\frac{C_S}{C_I}\frac{1-z^{-1}}{1-\left(1-\frac{C_P}{C_I}\right)z^{-1}} \\ &= -\frac{C_S}{C_I}\frac{z-1}{z-(1-C_P/C_I)} \end{aligned} \tag{2}$$

with $z = e^{j2\pi fT}$. For low frequencies, $z \approx 1$, the transfer function is very small, and only for higher frequencies does the circuit behave as a voltage amplifier.

A practical version is shown in Fig. 1(b). During Φ_2, the op amp output voltage is equal to the previous voltage plus the op amp offset voltage plus V_0/A_V, where A_V is the open-loop dc gain of the op amp. In this clock phase, both capacitors, C_{I} and C_{S}, are charged to the voltage at the inverting terminal of the op amp. This voltage is approximately equal to the op amp offset voltage plus V_0/A_V. During the next clock phase, the sampling capacitor is charged to $C_S(V_I - V_-)$, but because it was precharged to $-C_SV_-$, the injected charge to C_I is equal

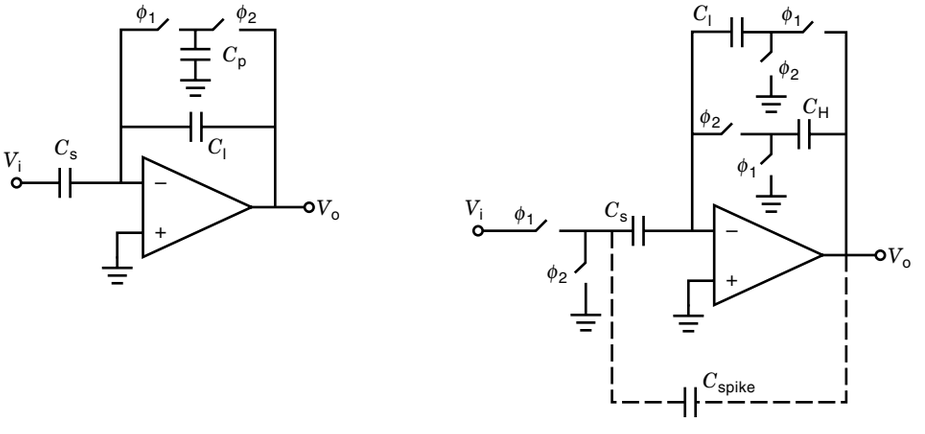


Figure 1. Voltage gain amplifiers: (a) with dc feedback; (b) available during both clock phases.

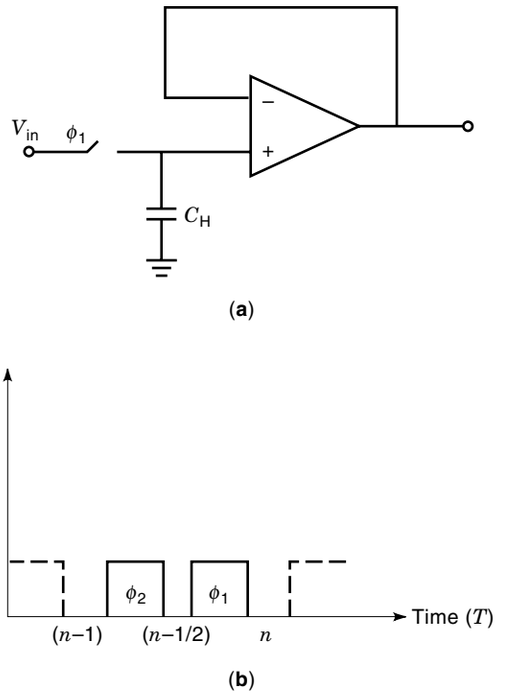


Figure 2. Open-loop S/H: (a) simple S/H buffer; (b) timing diagram.

to $C_S V_I$. As a result of this, the op amp output voltage is equal to $-(C_I/C_S)V_I$. Therefore, this topology has low sensitivity to the op amp offset voltage and to the op amp finite DC gain. A minor drawback of this topology is that the op amp stays in the open loop during the nonoverlapping phase transitions, producing spikes during these time intervals. A solution for this is to connect a small capacitor between the op amp output and the left-hand plate of C_S.

Sample-and-Hold

The function of a sample/hold (S/H) is to transform a continuous-time signal into a discrete-time version. A simple S/H circuit is shown in Fig. 2(a). Its clock phases are shown in Fig. 2(b). This open-loop architecture is attractive because of its simplicity and potential speed. It is often convenient to add an input buffer stage to the S/H circuit. The acquisition time depends on the tracking speed and input impedance of the input buffer, the on-resistance of the switch, and the value of the holding capacitor. The hold settling time is governed by the settling behavior of the buffer. A drawback of this architecture is the linearity requirements imposed on the buffers as a consequence. This limits the speed. Moreover, the input-dependent charge injected by the sampling switch onto the hold capacitor yields an undesirable source of nonlinearity. This type of S/H architecture achieves a linearity to nearly 8 bits. A full-period S/H signal is obtained by either a cascade of two S/H circuits of Fig. 2, driven by opposite clock phases, or by a parallel connection of two simple S/H circuits, output sampling switches, and a third (output) buffer as illustrated in Fig. 3. Structures with closed-loop connections are also used. Figure 4(a) illustrates a popular architecture often encountered in pipelined A/D converters. In the acquisition mode, switches associated with ϕ_1 and ϕ_1' are on whereas ϕ_2 is off, and the transconductance amplifier acts as a unity-gain amplifier. Thus the voltage across C_H is the input voltage and the virtual ground. In the transition to the hold mode, the switches associated with ϕ_1' and ϕ_1 turn off one after the other. Then ϕ_2 turns on. One advantage of this architecture is that because ϕ_1' turns off first, the input-dependent charge injected by ϕ_1 onto C_H does not appear in the held output voltage. Besides, because of the virtual ground, the channel charge associated with ϕ_1' does not depend on the input signal. Yet another advantage is that the offset voltage is not added to the output. A disadvantage is that a high-slew-rate transconductance amplifier is required. Figure 4(b) shows a double-sampling S/H circuit. The S/H operation is valid for both clock phases.

Multipliers

One difficulty in an SC multiplication technique is that continuous programmability or multiplication of two signals is not available. A digitally programmable coefficient is realized with a capacitor bank, as shown in Fig. 5. The resolution of this technique is limited because the capacitor size increases by 2^k where k is the number of programming bits.

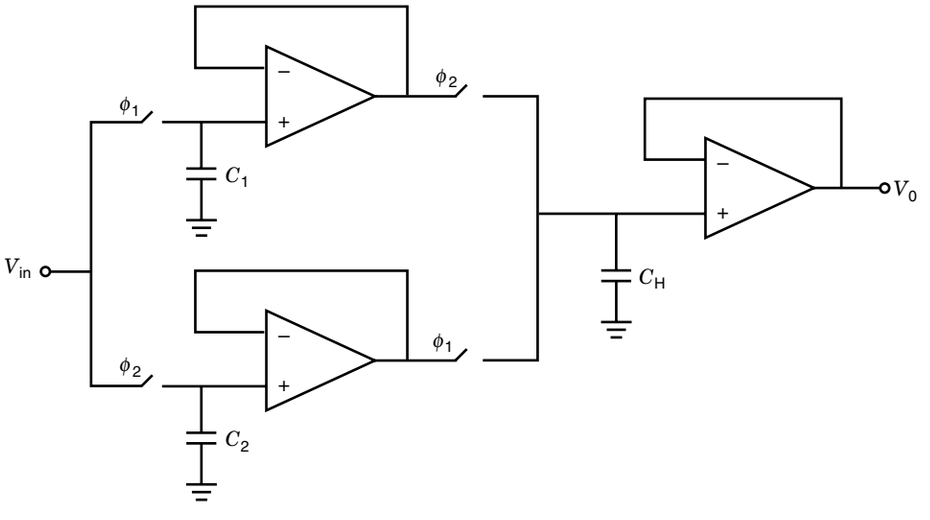


Figure 3. Double-sampling S/H architecture.

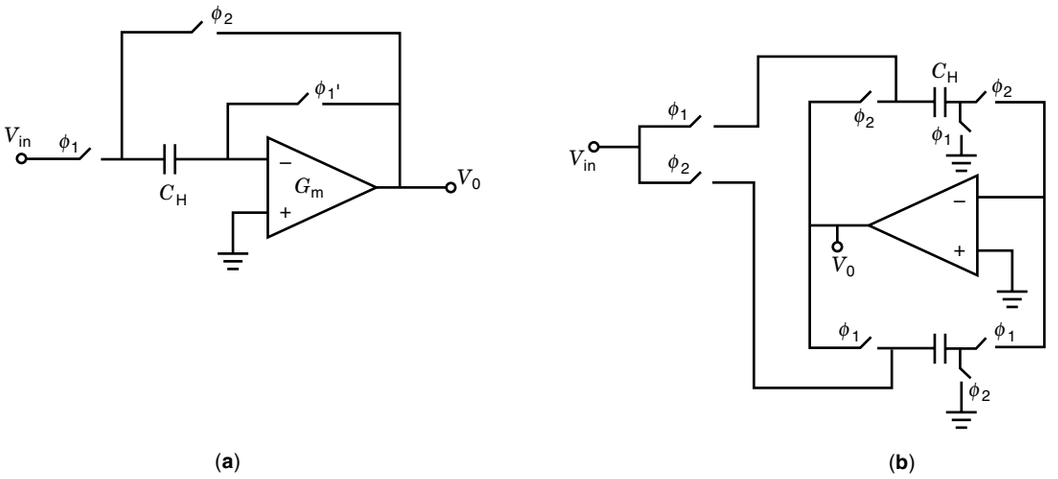


Figure 4. (a) SC S/H single-ended. (b) Double-sampling S/H.

When continuous programmability is required, a continuous multiplier is used. Despite many reported multiplier circuits, only two cancellation methods for four-quadrant multiplication are known. Because a single-ended configuration does not completely cancel nonlinearity and has poor PSRR, a fully differential configuration is often necessary in a sound multiplier topology. The multiplier has two inputs. Therefore there are four combinations of two differential signals, that is (x, y), $(-x, y)$, $(-x, -y)$, and $(x, -y)$. The multiplication and cancellation of an unwanted component are achieved by either of the following two equalities:

$$4xy = [(X+x)(Y+y) + (X-x)(Y-y)] - [(X-x)(Y+y) + (X+x)(Y-y)] \quad (3a)$$

or

$$8xy = \{[(X+x)+(Y+y)]^2 + [(X-x)+(Y-y)]^2\} - \{[(X-x)+(Y+y)]^2 + [(X+x)+(Y-y)]^2\} \quad (3b)$$

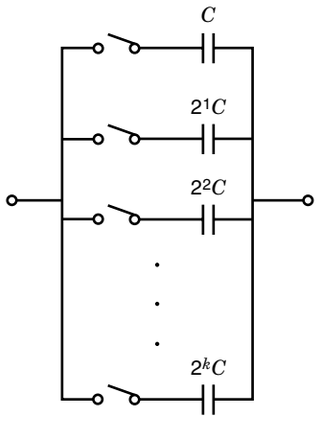


Figure 5. Digitally programmable capacitor bank.

These two approaches are depicted in Fig. 6. The topology of Fig. 6(a) is based on two-quadrant multipliers. Fig. 6(b) is based on square law devices. X and Y are arbitrary constant terms and are not shown in Fig. 6.

MOS transistors are used to implement these cancellation schemes. Let us consider a simple MOS transistor model characterized in its linear and saturation regions, respectively by the following equations:

$$I_d = K\left(V_{gs} - V_T - \frac{V_{ds}}{2}\right)V_{ds} \quad \text{for } |V_{gs}| > |V_T|, |V_{ds}| < |V_{gs} - V_T| \quad (4a)$$

$$I_d = \frac{K}{2}(V_{gs} - V_T)^2 \quad \text{for } |V_{gs}| > |V_T|, |V_{ds}| > |V_{gs} - V_T| \quad (4b)$$

where $K = \mu_o C_{ox}\, W/L$ and V_T are the conventional notations for the transconductance parameter and the threshold voltage of the MOS transistor, respectively. The terms $V_{gs}V_{ds}$ in Eq. (4a) or V_{gs}^2 in Eq. (4b) are used to implement Eqs. (3a) and (3b), respectively. Next we discuss a sound combination of a continuous-time multiplier and an SC integrator. In an SC circuit, the multiplier precedes the integrator, thus forming a weighted integrator. The output of the multiplier is a voltage signal or a current signal. In the case of a voltage-mode multiplier, the configuration of the SC integrator is identical with a conventional integrator, as shown in Fig. 7. The transconductance multiplier is connected directly to the op amp, as shown in Fig. 8. A common drawback in a weighted integrator is the multiplier offset because it is accumulated in the integrator. This problem is more serious for the transconductance mode.

The topology in Fig. 8 with the multiplier implemented by a FET transistor operating in the linear region is known as MOSFET-C implementation. Instead of using a single transistor, a linearizing scheme uses four transistors as shown in Fig. 9.

The four FETs in Fig. 9(a) are operating in the linear region, and depletion FETs are often used in many cases to

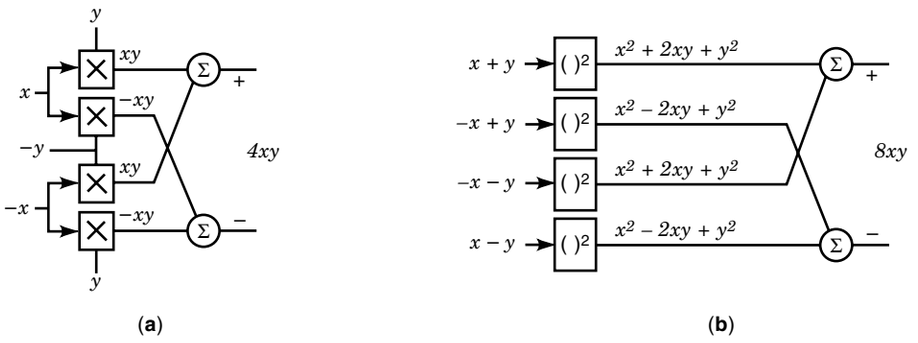


Figure 6. Four-quadrant multiplier topologies: (a) using single-quadrant multipliers; (b) Using square devices.

overcome the transistor threshold limit. The drain current of each FET is given by

$$\begin{aligned} i_{d1} &= K\left(v_y^+ - v_x^+ - V_T - \frac{v_d^+ - v_x^+}{2}\right)(v_d^+ - v_x^+) \\ i_{d2} &= K\left(v_y^- - v_x^+ - V_T - \frac{v_d^- - v_x^+}{2}\right)(v_d^- - v_x^+) \\ i_{d3} &= K\left(v_y^- - v_x^- - V_T - \frac{v_d^+ - v_x^-}{2}\right)(v_d^+ - v_x^-) \end{aligned} \tag{5}$$

and

$$i_{d4} = K\left(v_y^+ - v_x^- - V_T - \frac{v_d^- - v_x^-}{2}\right)(v_d^- - v_x^-)$$

Because of the closed loop, the voltages v_d^+ and v_d^- are virtually equal and fixed by the common-mode feedback circuit in the op amp. The differential current applied to the integrator is expressed by

$$i_d = (i_{d1} + i_{d3}) - (i_{d2} + i_{d4}) = K(v_x^+ - v_x^-)(v_y^+ - v_y^-) \tag{6}$$

The common-mode current injected into the integrator is canceled out by the common-mode feedback. The integrator output is given by

$$v_o(t) = v_o^+(t) - v_o^-(t) = \frac{K}{C}\int_0^t v_x(\tau)v_y(\tau)\,d\tau \tag{7}$$

where $v_x = v_x^+ - v_x^-$, $v_x = v_x^+ - v_x^-$, and $\mathrm{v_y} = \mathrm{v_y^+} - \mathrm{v_y^-}$. If v_x and v_y are sampled signals, then the circuit operates as a discrete-time MOSFET-C circuit. The integrator output yields

$$v_o(nT) = \frac{KT}{C}\sum_{k=0}^{n} v_x(k)v_y(k) \tag{8}$$

where T is the time period of the sampled system.

Several modifications are possible from this prototype. In the balanced differential op amp, the drain voltage v_d is virtually grounded because the common-mode voltage is fixed to ground. In this case, only two FETs are required, as shown in Fig. 9(b). The drain current of each FET is given by

$$\begin{aligned} i_{d1} &= K\left(v_y^- - v_x - V_T - \frac{-v_x}{2}\right)(-v_x) \\ i_{d2} &= K\left(v_y^+ - v_x - V_T - \frac{-v_x}{2}\right)(-v_x) \end{aligned} \tag{9}$$

and the differential current is given by

$$i_d = (i_{d1} - i_{d2}) = Kv_x(v_y^+ - v_y^-) \tag{10}$$

If depletion-mode FETs are used, then the v_y is referred to the ground, as shown in Fig. 10. The differential current is given by

$$i_d = (i_{d1} - i_{d2}) = Kv_xv_y \tag{11}$$

A switched, single-ended implementation using three op amps is achieved, as shown in Fig. 11. C_1 is reset at φ_1, and then the difference of the two integrators is sampled at φ_2. The charge on C_2 is transferred at the next φ_1. The output voltages of the two integrators are given by

$$\begin{aligned} v_1 &= \frac{-1}{C_1}\int_T K\left(v_y - v_x - V_T - \frac{-v_x}{2}\right)(-v_x)\,dt \\ &= \frac{TK}{C_1}\left[v_xv_y - \left(v_x + V_T - \frac{v_x}{2}\right)v_x\right] \\ v_2 &= \frac{-1}{C_1}\int_T K\left(-v_x - V_T - \frac{-v_x}{2}\right)(-v_x)\,dt \\ &= \frac{TK}{C_1}\left[-\left(v_x + V_T - \frac{v_x}{2}\right)v_x\right] \end{aligned} \tag{12}$$

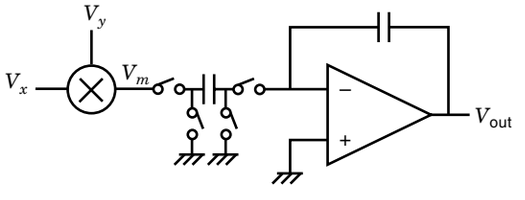


Figure 7. Weighted integrator with voltage-mode multiplier.

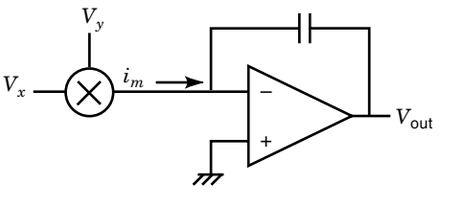
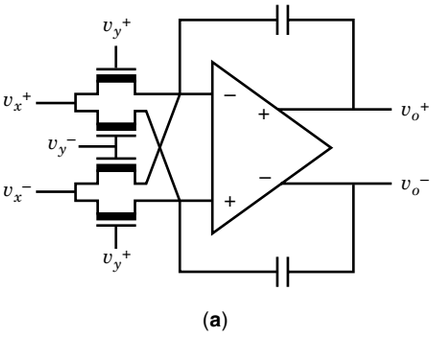
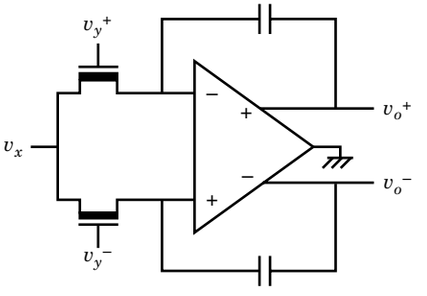


Figure 8. Weighted integrators with transconductance multiplier.



(a)



(b)

Figure 9. (a) Multiplier implemented by MOSFET-C techniques. (b) A MOSFET-C multiplier with balanced differential op amp.

where T is the period defined as the time difference between the end of φ_1 and the end of φ_2. The voltage across C_2 is given by

$$v_{C_2} = \frac{TK}{C_1} v_x v_y \tag{13}$$

At φ_1, the charge in C_2 is transferred to C_3. The output of the integrator becomes

$$v_o = \frac{TKC_2}{C_1 C_3} \frac{z^{-1/2}}{1 - z^{-1}} v_x(z) v_y(z) \tag{14}$$

A weighted integrator is also implemented with two op amps and one FET. It requires several additional clocks. Basically, it multiplexes the FET and the op amp by substituting two FETs and two integrators, as shown in Fig. 12.

The operation involves two additional clock phases. During phase φ_A, the gate input is connected to v_y. Integrator A is

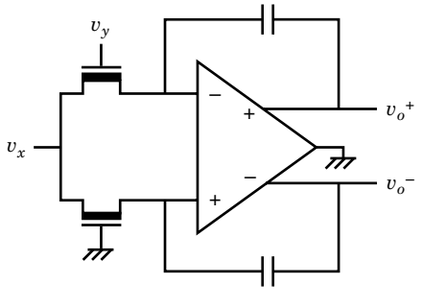


Figure 10. Ground-referenced MOSFET-C multiplier.

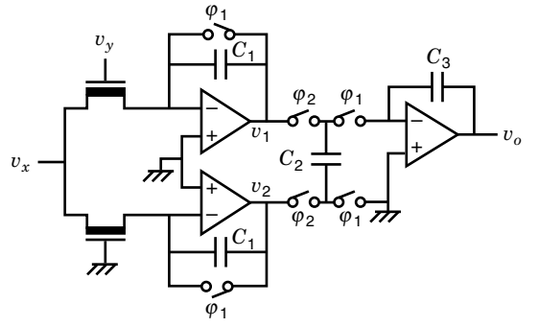


Figure 11. An SC weighted integrator.

reset at φ_1. Its output is sampled at φ_2. Then, the voltage sampled in C_2 yields the expression

$$\begin{aligned} v_{C_2}(\varphi_A) &= \frac{-1}{C_1} \int_T K \left(v_y - v_x - V_T - \frac{-v_x}{2} \right) (-v_x)\, dt \\ &= \frac{TK}{C_1} \left[v_x v_y - \left(v_x + V_T - \frac{v_x}{2} \right) v_x \right] \end{aligned} \tag{15}$$

During the second phase φ_B, T the gate input is connected to v_y. Integrator A is reset at φ_1. At φ_2, v_1 becomes

$$v_{C_2}(\varphi_B) = \frac{TK}{C_1} \left[- \left(v_x + V_t - \frac{v_x}{2} \right) v_x \right] \tag{16}$$

One node of C_2 is connected to integrator A and the other node is connected to integrator B. The total charge into integrator B is given by

$$Q_2 = C_2[v_1(\varphi_B) - v_1(\varphi_B)] = \frac{TKC_2}{C_1} v_x v_y \tag{17}$$

A single FET SC weighted integrator does not have an offset due to an FET mismatch. However, all transconductance-weighted integrators depend on the clock period T. Unfortunately, a jitter-free clock is impossible to implement. This jitter causes offset and incomplete cancellation, even in the circuit shown in Fig. 12. Next an SC weighted integrator with voltage-mode offset cancellation is described.

The multiplier offset caused by device mismatch in the multiplier is the most critical limitation in continuous-time weighted SC integrators. A simple and effective offset cancel-

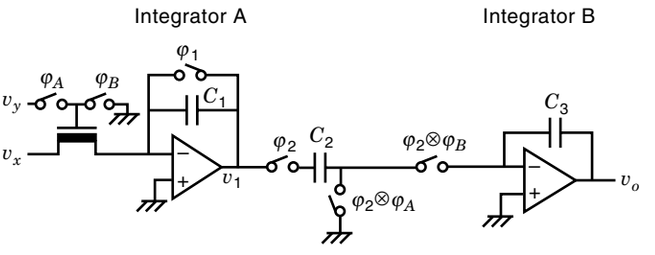


Figure 12. Single FET SC weighted integrator.

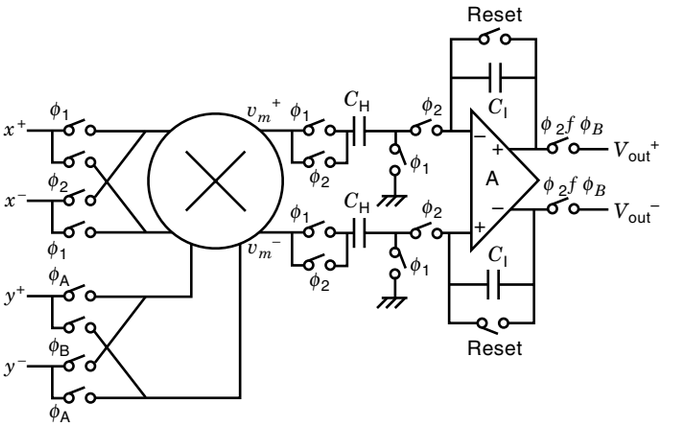


Figure 13. A switched-capacitor weighted integrator with offset cancellation.

lation scheme using SC techniques is discussed next. The multiplier offset is modeled by

$$z = K(x + x_o)(y + y_o) + z_o \tag{18}$$

where K is a multiplication constant, x_o and y_o are offset-related device mismatches at the input stage of the x and y signals, respectively, and z_o is the offset caused by device mismatch at the output stage. This offset is canceled by four combinations of input signal polarity as follows:

$$\begin{aligned} z_{x,y} &= K(\ \ x + x_o)(\ \ y + y_o) + z_o \\ z_{-x,y} &= K(-x + x_o)(\ \ y + y_o) + z_o \\ z_{-x,-y} &= K(-x + x_o)(-y + y_o) + z_o \\ z_{x,-y} &= K(\ \ x + x_o)(-y + y_o) + z_o \end{aligned} \tag{19}$$

Then the offset is canceled out similarly to a nonlinearity cancellation in a multiplier, that is,

$$(z_{x,y} - z_{-x,y}) + (z_{-x,-y} - z_{x,-y}) = 4Kxy \tag{20}$$

This scheme is implemented with a switched-capacitor circuit, as shown in Fig. 13. ϕ_1 and ϕ_2 are nonoverlapping clock phases. At ϕ_1, the multiplier output is sampled and is held in C_H. At ϕ_2, one node of C_H is connected to the multiplier output whereas the other node is connected to the integrator input. Then, the charge is injected into the integrating capacitor C_I. The voltage across C_I, after the clock ϕ_2, becomes $[v_m(\phi_2) - v_m(\phi_1)]$ where v_m is the multiplier output voltage at the given clock phase. The switches ($\phi_1 - \phi_2$ and $\phi_A - \phi_B$), at the multiplier input nodes, change input signal polarities. Using clocks shown in Fig. 14, the multiplier input is given as a sequence

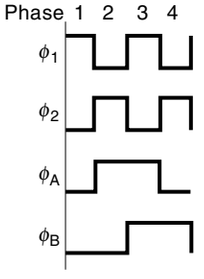


Figure 14. Clock phase diagram.

of $\{(x, y), (-x, y), (-x, -y), (x, -y)\}$ at each clock phase 1, 2, 3, 4, respectively.

At the end of phase 4, C_I contains

$$v_{out}(phase\,4) = 4K\frac{C_H}{C_1}xy \tag{21}$$

x and y should be kept constant during the four phases. If the four phases are considered unit time period than the weighted integrator is characterized as follows:

$$v_{out}(z) = 4K\frac{C_H}{C_1}\frac{1}{1 - z^{-1}}x(z)y(z) \tag{22}$$

Note that multiplier offset cancellation is obtained in the integrator.

Integrators

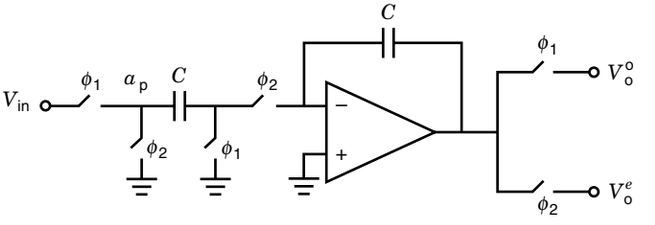
Standard stray-insensitive integrators are shown in Fig. 15. In sampled data systems, input and output signals are sampled at different times. This yields different transfer functions. We assume two-phase nonoverlapping clocks, an odd clock phase ϕ_1 and an even clock phase ϕ_2. Thus, for a noninverting integrator, the following transfer functions are often used:

$$H^{oo}(z) = \frac{V_o^o(z)}{V_{\text{in}}^o(z)} = \frac{a_p z^{-1}}{1 - z^{-1}} = \frac{a_p}{z - 1} \tag{23a}$$

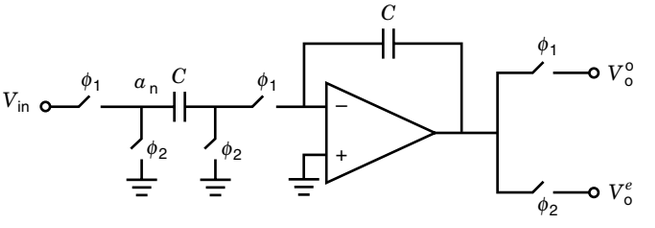
$$H^{oe}(z) = \frac{V_o^e(z)}{V_{\text{in}}^o(z)} = \frac{a_p z^{-1/2}}{1 - z^{-1}} = \frac{a_p}{z^{1/2} - z^{-1/2}} \tag{24a}$$

For an inverting integrator,

$$H^{oo}(z) = \frac{V_o^o(z)}{V_{\text{in}}^o(z)} = -\frac{a_n}{1 - z^{-1}} = -\frac{a_n z}{z - 1} \tag{23b}$$



(**a**)



(**b**)

Figure 15. Conventional stray-insensitive SC integrators: (a) noninverting; (b) inverting.

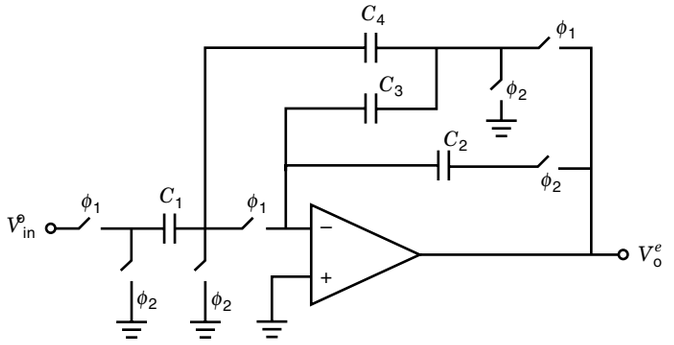


Figure 16. An inverting SC integrator with reduced capacitance spread.

and

$$H^{oe}(z) = \frac{V_o^e(z)}{V_{\text{in}}^o(z)} = -\frac{a_n z^{-1/2}}{1 - z^{-1}} = -\frac{a_n}{z^{1/2} - z^{-1/2}} \tag{24b}$$

where z^{-1} represents a unit delay. A crude demonstration, showing the integrative nature of these SC integrators in the s-domain, is to consider a high sampling rate, that is, a clock frequency ($f_c = 1/T$) much higher than the operating signal frequencies. Thus, let us consider Eq. (23a) and, assuming a high sampling rate, we can write a mapping from the z- to the s-domain:

$$z \approx 1 + sT \tag{25}$$

Then

$$H(s) = \frac{a_p}{z - 1}\bigg|_{z \cong 1 + sT} \cong \frac{1}{(T/a_p)s} \tag{26}$$

This last expression corresponds to a continuous-time, noninverting integrator with a time constant of $T/a_p = 1/f_c a_p$, that is, a capacitance ratio times the clock period.

In many applications the capacitor ratios associated with integrators are very large, thus the total capacitance becomes excessive. This is particularly critical for biquadratic filters with high Q, where the ratio between the largest and smallest capacitance is proportional to the quality factor Q. A suitable inverting SC integrator for high Q applications is shown in Fig. 16. The corresponding transfer function is given by

$$H^{oe}(z) = \frac{V_o^e(z)}{V_{\text{in}}^o(z)} = \frac{-C_1 C_3}{C_2 C_4'} \frac{1}{1 - z^{-1}} Z^{-1/2} \tag{27}$$

where $C_4' = C_4 + C_3$. This integrator is comparable in performance to the conventional circuit of Fig. 15, in terms of stray sensitivity and finite-gain error. Note from Eq. (27) that the transfer function is defined only during ϕ_2. During ϕ_1, the circuit behaves as a voltage amplifier. Thus high slew-rate op amps could be required. A serious drawback in the integrator of Fig. 16 is the increased offset compared with standard SC integrators. In typical two-integrator loop filters, however, the other integrator is chosen to be offset and low dc gain-compensated, as shown in Fig. 17. The SC integrator integrates by C_1 and C_B, and the hold capacitor C_h stores the offset voltage. The voltage across C_h compensates for the offset voltage and the dc gain error of the op amp. Note that the SC integrator of Fig. 17 can operate as a noninverting integrator if the clocking in parenthesis is employed. C_M provides a time-continuous feedback around the op amp. The transfer function, for infinite op amp gain, is given by

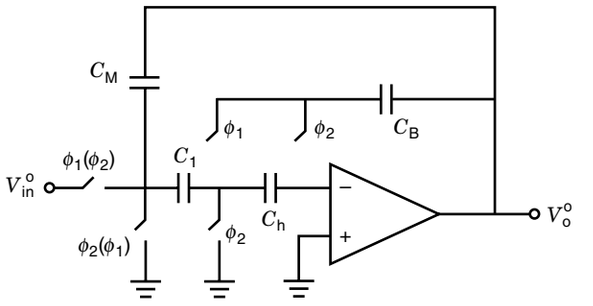


Figure 17. Offset and gain-compensated integrator.

$$H^{oo}(z) = \frac{V_o^o(z)}{V_{\text{in}}^o(z)} = \frac{-C_1}{C_B(1 - z^{-1})} \tag{28}$$

Furthermore, if the dc offset is tolerated in certain applications, an autozeroing method is used to compensate for the dc offset. Next we discuss a general form of a first-order building block (see Fig. 18). The output voltage is expressed as

$$V_0^e = -\frac{C_1}{C_F} V_{i_1}^e - \frac{C_2}{C_F} \frac{1}{1 - z^{-1}} V_{i_2}^e + \frac{C_3}{C_F} \frac{z^{-1}}{1 - z^{-1}} V_{i_3}^e \tag{29}$$

Observe that the capacitor C_3, and switches are the implementation of a negative resistor. Also note that if $V_{i_2}^e$ is equal to V_0^e, this connection makes the integrator a lossy one. In that case Eq. (29) is written

$$V_0^e \frac{\left(1 + \dfrac{C_2}{C_F}\right) z - 1}{z - 1} = -\frac{C_1}{C_F} V_{i_1}^e + \frac{C_3}{C_F} \frac{1}{z - 1} V_{i_3}^e \qquad \text{for } V_{i_2}^e = V_0^e \tag{30}$$

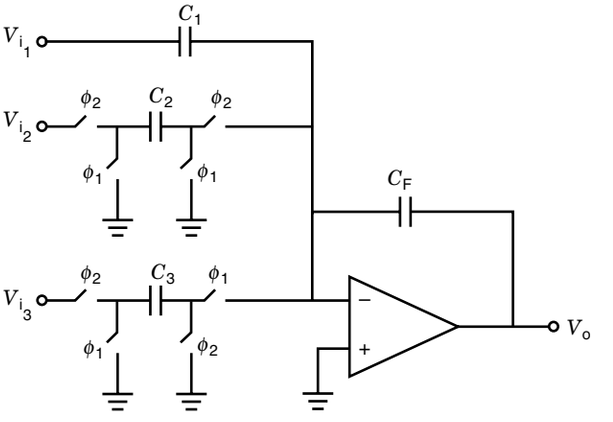


Figure 18. General form of a first-order building block.

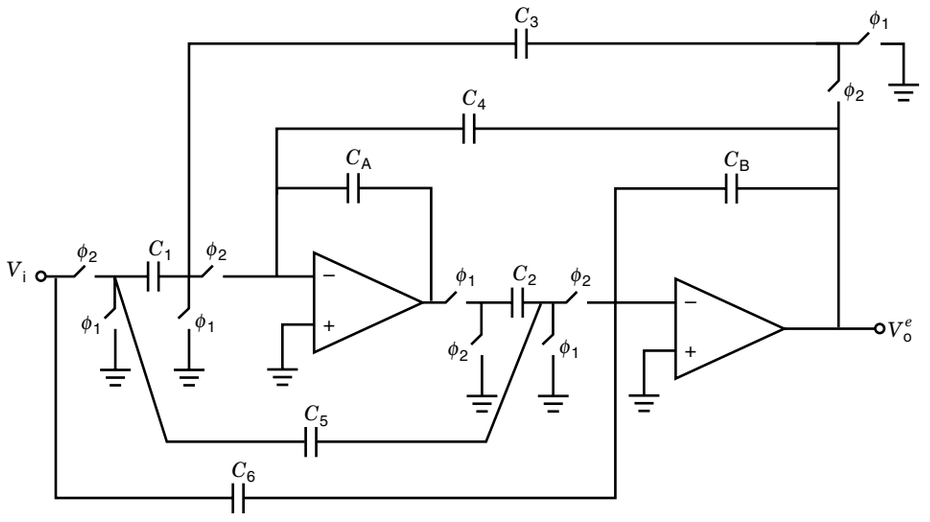


Figure 19. An SC biquadratic section.

The building block of Fig. 18 is the basis of higher order filters. An illustrative example follows.

SC Biquadratic Sections

The circuit shown in Fig. 19 implements any pair of poles and zeros in the z-domain. For $C_A = C_B = 1$,

$$H^{ee}(z) = \frac{V_0^e(z)}{V_{\text{in}}^e(z)} = -\frac{(C_5+C_6)z^2 + (C_1C_2 - C_5 - 2C_6)z + C_6}{z^2 + (C_2C_3 + C_2C_4 - 2)z + (1 - C_2C_4)} \tag{31}$$

Simple design equations follow:

Low-pass	$C_5 = C_6 = 0$
High-pass	$C_1 = C_5 = 0$
Band-pass	$C_1 = C_6 = 0$

Comparing the coefficients of the denominator of Eq. (31) with the general expression $z^2 - 2\,r\cos\theta + r^2$, we obtain the following expressions:

$$C_2C_4 = 1 - r^2 \tag{32a}$$

$$C_2C_3 = 1 - 2r\cos\theta + r^2 \tag{32b}$$

For equal voltages at the two integrator outputs and assuming that Q is greater than 3 and a high sampling rate ($\theta = \omega_{0_d}T \ll 1$),

$$C_2 = C_3 = \sqrt{1 + r^2 - 2r\cos\theta} \cong \omega_{0_d}T \tag{32c}$$

$$C_4 = \frac{1 - r^2}{C_2} \cong \frac{1}{Q} \tag{32d}$$

The capacitance spread for a high sampling rate, $C_A = 1$, and a high Q is expressed as

$$\frac{C_{\max}}{C_{\min}} = \max\left[\frac{C_1}{C_2}, \frac{C_1}{C_4}\right] = \max\left\{\frac{1}{\omega_{0_d}T}, Q\right\} \tag{33}$$

In particular cases, this capacitance spread is prohibited. For such cases the SC integrators shown in Figs. 16 and 17 replace the conventional building blocks. This combination yields the practical SC biquadratic section shown in Fig. 20. This structure offers reduced total capacitance and also reduces the effect of the offset voltage of the op amps. Note that the capacitor C_h does not play an important role in the design, and can be chosen with a small value. For the poles, comparing $z^2 - (2\,r\cos\theta)z + r^2$ and the analysis of Fig. 20,

$$\frac{C_2C_3}{C_A + C_B} = 1 + r^2 - 2r\cos\theta \tag{34a}$$

$$\frac{C'_AC_2C_4}{C_{A_1}C_AC_B} = 1 - r^2 \tag{34b}$$

where $C_{A_1} = C'_A + C''_A$. Simple design equations are obtained by assuming a high sampling rate, a large Q, and $C_2 = C_3 = C_4 = C'_A = C_h = 1$. Then

$$C_A + C_B \cong \frac{1}{\omega_{0d}T} \tag{35a}$$

and

$$C''_A \cong Q\omega_{0d}T - 1 \tag{35b}$$

Another common use of SC filters is high-frequency applications. In such cases a structure with a minimum gain-bandwidth product (GB = ω_u) is desirable. This structure is shown in Fig. 21 and is often called a decoupled structure. It is worth mentioning that two SC architectures can have ideally the same transfer function, but with real op amps, their frequency (and time) response can differ significantly. A rule of thumb for reducing GB effects in SC filters is to avoid a direct connection between the output of one op amp to the input of another op amp. It is desirable to transfer the output of an op amp to a grounded capacitor and, in the next clock phase, transfer the capacitor charge into the op amp input. More dis-

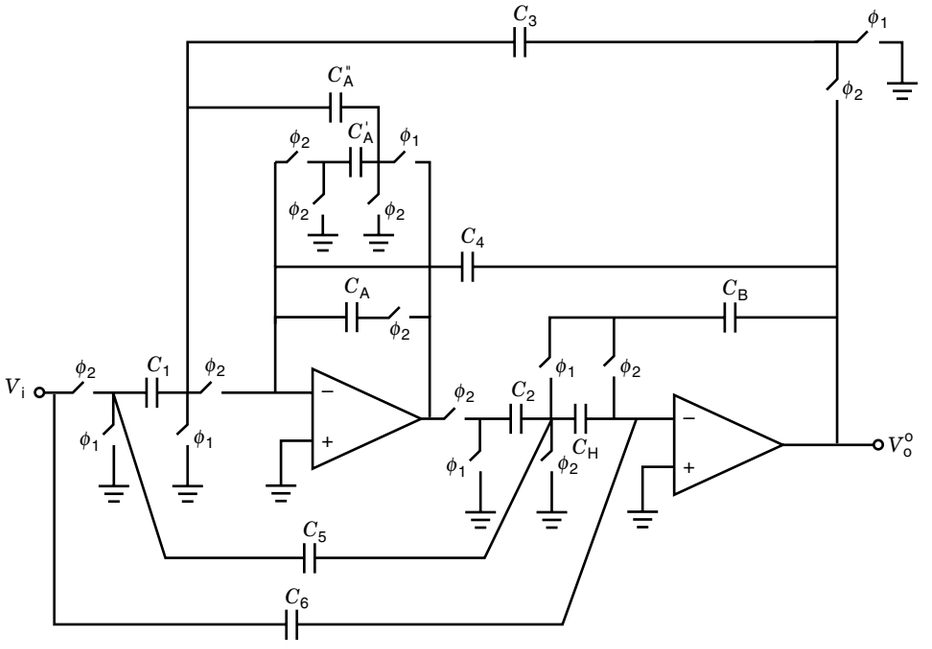


Figure 20. An improved capacitance area SC biquadratic section.

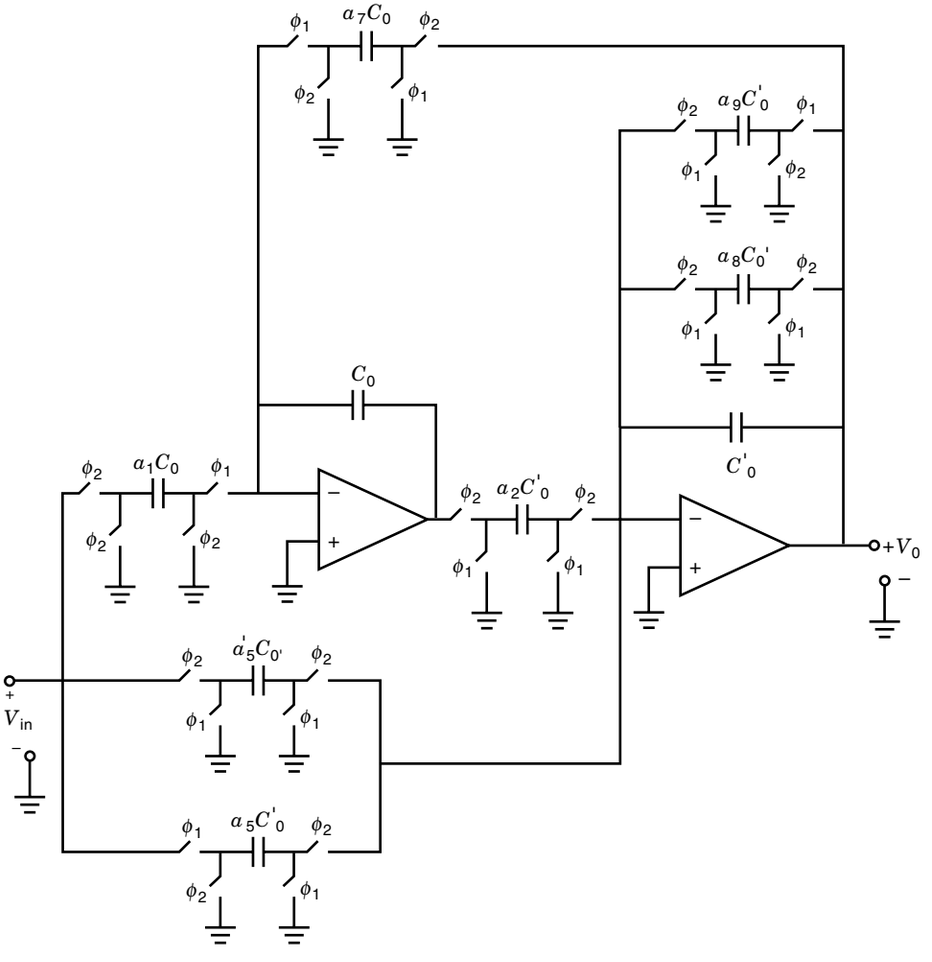


Figure 21. A decoupled SC biquadratic section.

cussion on ω_u effects is in the next section. Analysis of Fig. 21 yields the following expressions:

$$r^2 = \frac{1+a_9}{1+a_8} \tag{36a}$$

$$2r\cos\theta = \frac{2+a_8+a_9-a_2a_7}{1+a_8} \tag{36b}$$

If the input is sampled during ϕ_2 and held during ϕ_1, the ideal transfer function is given by

$$H^e(z) = \frac{V_0^e(z)}{V_i^e(z)} = \left(\frac{-a_5'}{1+a_8}\right)\left(\frac{z^2 - z(a_5'+a_5-a_1a_2)/a_5' + a_5/a_5'}{z^2 - z\dfrac{2+a_8+a_9-a_2a_7}{1+a_8} + \dfrac{1+a_9}{1+a_8}}\right) \tag{37}$$

The capacitor a_9C_0' can be used as a design parameter to optimize the biquad performance. A simple set of design equations follows:

$$a_8 = \frac{(1+a_9)-r^2}{r^2} \tag{38a}$$

$$a_2 = a_7 = \sqrt{\frac{1+r^2-2r\cos\theta}{r^2}(1+a_9)} \tag{38b}$$

Under a high sampling rate and high Q, the following expressions are obtained:

$$\omega_0 \cong f_c\sqrt{\frac{a_2a_7}{1+a_8}} \tag{39a}$$

and

$$Q \cong \sqrt{\frac{a_2a_7(1+a_8)}{a_8-a_9}} \tag{39b}$$

A tradeoff between Q-sensitivity and total capacitance is given by a_8 and a_9.

EFFECTS OF THE OP AMP FINITE PARAMETERS

Finite Op Amp dc Gain Effects

The effect of finite op amp dc voltage gain A_0 in a lossless SC integrator is to transform a lossless integrator into a lossy one. This degrades the transfer function in amplitude and phase. Typically the magnitude of deviation due to the integrator amplitude variation is not critical. By contrast, the phase deviation from the ideal integrator has a very important influence on overall performance. When real SC integrators are used to build a two-integrator biquadratic filter, the actual quality factor becomes

$$Q_A = \frac{1}{\dfrac{1}{Q}+\dfrac{2}{A_0}} \cong \left(1-\frac{2Q}{A_0}\right)Q \tag{40}$$

The actual center frequency suffers small deviations:

$$\omega_{o_A} = \frac{A_0}{1+A_0}\omega_o \tag{41}$$

We can conclude that the ω_o deviations are negligible. However, the Q deviations are significant depending on the Q and A_0 values.

Finite OP AMP Gain-Bandwidth Product. The op amp bandwidth is very critical for high-frequency applications. The analysis is carried out when the op amp voltage gain is modeled with one dominant pole that is,

$$A_V(s) = \frac{A_0}{1+s/\omega_3} = \frac{A_0\omega_3}{s+\omega_3} = \frac{\omega_u}{s+\omega_3} \cong \frac{\omega_u}{s} \tag{42}$$

where A_0 is the dc gain, ω_u is approximately the unity-gain bandwidth, and ω_3 is the op amp bandwidth. Also, it is assumed that the op amp output impedance is equal to zero. The analysis taking into account $A_V(s)$ is rather cumbersome because the op amp input-output characterization is a continuous-time system modeled by a first-order differential equation and the rest of the SC circuit is characterized by discrete-time systems modeled by difference equations. The step response of a single op amp SC circuit to a step input applied at $t = t_1$ is given by

$$V_o(t) = V_o(t_1)e^{-(t-t_1)\alpha\omega_u} + V_{od}\{1-e^{-(t-t_1)\alpha\omega_u}\} \tag{43}$$

where V_{od} is the desired output which is a function of the initial conditions, inputs, and filter architecture and α is a topology-dependent voltage divider, $0 < \alpha \leq 1$.

$$\alpha = \frac{\sum C_f}{\sum_i C_i} \tag{44}$$

where the C_f sum consists of all feedback capacitors connected directly between the op amp output and the negative input terminal and the C_i sum is over all capacitors connected to the negative op amp terminal. Note that the $\alpha\omega_u$ product determines the rise time of the response, therefore both α and ω_u should be maximized. For the multiple op amp case, the basic concept prevails. For the common case where $t - t_1 = T/2$ at the end of any clock phase, the figure of merit to be maximized becomes $\alpha T\omega_u/2$. This means that a rule of thumb for reduced gain-bandwidth effects requires that

$$\alpha T\omega_u/2 \geq 5 \tag{45}$$

This rule is based on the fact that five times constants are required to obtain a steady-state response with a magnitude of error of less than 1%.

Noise and Clock Feedthrough

The lower range of signals processed by electronic devices is limited by several unwanted signals at the circuit output. The rms values of these electrical signals determine the noise level of the system, and it represents the lowest limit for the incoming signals to be processed. Input signals smaller than

the noise level, in most of the cases, cannot be driven by the circuit. The most critical noise sources are those due to (1) the elements used (transistors, diodes, resistors, etc.); (2) the noise induced by the clocks; (3) the harmonic distortion components generated by the intrinsic nonlinear characteristics of the devices; and (4) the noise induced by the surrounding circuitry. In this section, types (1), (2) and (3) are considered. The noise generated by the surrounding circuitry and coupled to the output of the switched-capacitor circuit is further reduced by using fully differential structures.

Noise Due to the MOSFET. In an MOS transistor, noise is generated by different mechanisms but there are two dominant noise sources, channel thermal noise and $1/f$ or flicker noise. A discussion of the nature of these noise sources follows.

Thermal Noise. The flow of the carriers caused by drain-source voltage takes place on the source-drain channel, most like in a typical resistor. Therefore, thermal noise is generated because of the random flow of the carriers. For an MOS transistor biased in the linear region, the spectral density of the input referred thermal noise is approximated by

$$V_{\text{eqth}}^2 = 4kTR_{\text{on}} \tag{46}$$

where R_{on}, k, and T are the drain-source resistance of the transistor, the Boltzmann constant, and the temperature (in degrees Kelvin), respectively. In saturation, the spectral noise density is calculated by the same expression but with R_{on} equal to $2/3g_m$, where g_m is the small signal transconductance of the transistor.

$1/f$ Noise

This type of noise is mainly caused by the imperfections in the silicon-silicon oxide interface. The surface states and the traps in this interface randomly interfere with the charges flowing through the channel. Hence the noise generated is strongly dependent on the technology. The $1/f$ noise (flicker noise) is also inversely proportional to the gate area because with larger areas, more traps and surface states are present and some averaging occurs. The spectral density of the input referred $1/f$ noise is commonly characterized by

$$V_{\text{eq1/f}}^2 = \frac{k_F}{WLf} \tag{47}$$

where the product of WL, f, and k_F are the gate area of the transistor, the frequency in hertz, and the flicker constant, respectively. The spectral noise density of an MOS transistor is composed of both components. Therefore the input referred spectral noise density of a transistor operating in its saturation region becomes

$$V_{\text{eq}}^2 = \frac{8}{3}\frac{kT}{g_m} + \frac{k_F}{WLf} \tag{48}$$

Op Amp Noise Contributions. In an op amp, the output referred noise density is composed of the noise contribution of all transistors. Hence the noise level is a function of the op amp architecture. A typical unbuffered folded-cascade op amp

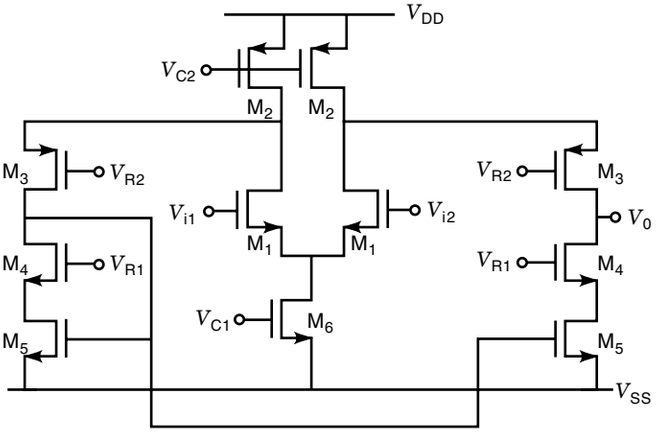


Figure 22. A folded-cascade operational transconductance amplifier.

(folded cascade OTA) is shown in Fig. 22. To compute the noise level, the contribution of each transistor must be evaluated. This can be done by obtaining the OTA output current generated by the gate referred noise of all the transistors. For instance, the spectral density of the output referred noise current due to M_1 is straightforwardly determined because the gate referred noise is at the input of the OTA, leading to

$$i_{\text{o1}}^2 = G_m^2 V_{\text{eq1}}^2 \tag{49}$$

where G_m (equal to g_{m1} at low frequencies) is the OTA transconductance and v_{eq1} is the input referred noise density of M_1. Similarly, the contributions of M_2 and M_5 to the spectral density of the output referred noise current are given by

$$\begin{aligned} i_{\text{o2}}^2 &= g_{m2}^2 v_{\text{eq2}}^2 \\ i_{\text{o5}}^2 &= g_{m5}^2 v_{\text{eq5}}^2 \end{aligned} \tag{50}$$

The noise contributions of transistors M_3 and M_4 are very small compared with the other components because their noise drain current, due to the source degeneration implicit in these transistors, is determined by the equivalent conductance associated with their sources instead of by their transconductance. Because the equivalent conductance in a saturated MOS transistor is much smaller than the transistor transconductance, this noise drain current contribution can be neglected. The noise contribution of M_6 is mainly common-mode noise. Therefore it is almost canceled at the OTA input because of current substraction. The spectral density of the total output referred noise current is approximated by

$$i_0^2 = 2[G_m^2 v_{\text{eq1}}^2 + g_{m2}^2 v_{\text{eq2}}^2 + g_{m5}^2 v_{\text{eq5}}^2] \tag{51}$$

The factor 2 is the result of the pairs of transistors M_1, M_2, and M_5. From this equation, the OTA input referred noise density becomes

$$V_{\text{OTAin}}^2 = 2v_{\text{eq1}}^2 \left[1 + \frac{g_m^2 2v_{\text{eq2}}^2 + g_{m5}^2 v_{\text{eq5}}^2}{G_m^2 v_{\text{eq1}}^2}\right] \tag{52}$$

According to this result, if G_m is larger than g_{m2} and g_{m5}, the OTA input referred noise density is mainly determined by the OTA input stage. In that case and using Eq. (48), Eq. (52) yields

$$V_{\text{OTAin}}^2 \cong 2V_{\text{eq1}}^2 = V_{\text{equ1}/f}^2 + 4kTR_{\text{eqth}} \tag{53}$$

where the factor 2 has been included in $V_{\text{eq1}/f}$ and R_{eqth}. In Eq. (47), $v_{\text{eq1}/f}$ is the equivalent $1/f$ noise density and R_{eqth} is the equivalent resistance for noise, equal to $4/3g_{\text{m}}$.

Noise in a Switched-Capacitor Integrator

In a switched-capacitor lossless integrator, the output referred noise density component due to the OTA is frequency limited by the gain-bandwidth product of the OTA. To avoid misunderstandings, in this section f_u (the unity gain frequency of the OTA in Hertz) is used instead of ω_u (in radians per second). Because f_u must be higher than the clock frequency f_c and because of the sampled nature of the SC integrator, the OTA high-frequency noise is folded back into the integrator baseband. In the case of the SC integrator and assuming that the flicker noise is not folded back, the output referred spectral noise density becomes

$$v_{\text{oeq1}}^2 = \left[v_{\text{eq1}/f}^2 + 4kTR_{\text{eqth}}\left(1 + \frac{2f_u}{f_c}\right)\right]|1 + H(z)|^2 \tag{54}$$

where the folding factor is equal to f_u/f_c) and $H(z)$ is the z-domain transfer function of the integrator. The factor $2f_u/f_c$ is the result of both positive and negative foldings. Typically, the frequency range of the signal to be processed is around and below the unity-gain frequency of the integrator. Therefore $H(z) > 1$ and Eq. (54) are approximated by

$$v_{\text{oeq1}}^2 = \left[v_{\text{eq1}/f}^2 + 4kTR_{\text{eqth}}\left(1 + \frac{2f_u}{f_c}\right)\right]|H(z)|^2 \tag{54b}$$

Noise from Switches. In switched-capacitor networks, switches are implemented by single or complementary MOS transistors. These transistors are biased in the cutoff and ohmic region for open and closed operations, respectively. In the cutoff region, the drain-source resistance of the MOS transistor is very high. Then the noise contribution of the switch is confined to very low frequencies and it can be considered a dc offset. This noise contribution is one of the most fundamental limits for the signal-to-noise ratio of switched-capacitor networks.

Clock Feedthrough

Another factor that limits the accuracy of switched-capacitor networks is the charge induced by the switch clocking. These charges are induced by the gate-source capacitance, the gate-drain capacitance, and the charge stored in the channel when the switch is in the on state. Furthermore, some of these charges depend on the input signal and introduce distortion in the circuit. Although these errors cannot be canceled, there are some techniques to reduce these effects.

Analysis of clock feedthrough is very difficult because it depends on the order of the clock phases, the relative delay of the clock phases, and also on the speed of the clock transitions. For instance, in Fig. 23 let us consider the case when

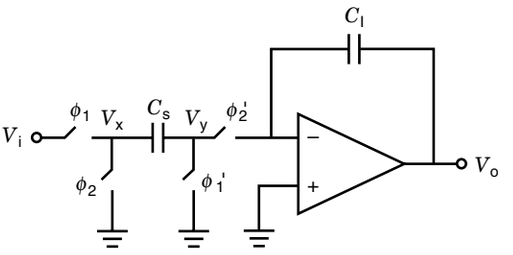


Figure 23. Typical switched-capacitor, lossless integrator.

ϕ_1 goes down before ϕ_1'. This is shown in Fig. 24. Although C_{P1} is connected between two low-impedance nodes, C_{P2} is connected between ϕ_1, a low impedance node, and the capacitor C_S. For $\phi_1 > v_i + V_T$, the transistor M_1 is on, and the current injected by C_{P2} is absorbed by the drain-source resistance. Then v_x remains at a voltage equal to v_i.When M_1 is turned off, $\phi_1 < v_i + V_T$, and charge conservation at node v_x leads to

$$v_x = v_i + \frac{C_{P2}}{C_S + C_{P2}}(V_{\text{SS}} - v_i - V_T) \tag{55}$$

where V_{SS} is the low level of ϕ_1 and ϕ_2. During the next clock phase, and both capacitors C_{P2} and C_S are charged to v_x, and this charge is injected to C_I. Thus, an integrator time constant error proportional to $C_P2/(C_S + C_{P2})$ is induced by C_{P2}. In addition, an offset voltage proportional to $V_{\text{SS}} - V_T$ is also generated. Because the threshold voltage V_T is a nonlinear function of v_i, an additional error in the transfer function and harmonic distortion components appears at the output of the integrator. The same effect occurs when clock phases ϕ_2 and ϕ_2' have a similar sequence.

Let us consider the case when ϕ_1 is opened before ϕ_1', as shown in Fig. 24(b). Before M_1 turns off, $V_x = -v_i$, and $v_Y = 0$. When M_1 is off, $V_{\text{SS}} < \phi_1 < v_i + V_T$, the charge is recombined among C_S, C_{P1}, C_{P2}, and C_{P3}. After the charge redistribution, the charge conservation at node v_Y leads to

$$C_S[v_x(t) - v_Y(t)] - C_{P3}v_Y(t) = C_S v_i(t_0) \tag{56}$$

where $v_i(t_0)$ is the input voltage just at the end of the previous clock phase. Observe from Eq. (56) that the addition of the charges stored on C_S and C_{P3} is conserved. During the next clock phase, $v_x(t) = 0$, and both capacitors C_S and C_{P3} transfer the ideal charge $-C_S v_i(t_0)$ to C_1, making the clock-feedthrough-induced error negligible. The conclusion is that if the clock

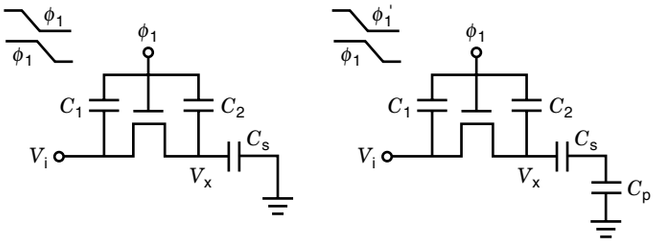


Figure 24. MOS Switches: Charge induced due to the clocks: (a) if ϕ_1 goes down before ϕ_1' and (b) if ϕ_1' goes down before ϕ_1.

phase ϕ_1' is a bit delayed, then ϕ_1 the clock-induced error is negligible. This is also true for clock phases ϕ_2 and ϕ_2'.

In Fig. 23, the right hand switches also introduce clock feedthrough but unlike the clock feedthrough previously analyzed, which is input-signal-independent. When clock phase ϕ_2' decreases, the gate-source overlap capacitor extracts the following charge from the summing node:

$$\Delta Q = C_{GS0}(V_{SS} - V_T) \tag{57}$$

In this case, V_T does not introduce distortion because v_y is almost at zero voltage for both clock phases. The main effect of C_{GS0} is to introduce an offset voltage. The same analysis reveals that the bottom right-hand switch introduces a similar offset voltage.

From the previous analysis it can be seen that the clock feedthrough is reduced by using transistors of minimum dimension. This implies minimum parasitic capacitors and minimum induced charge from the channel. If possible, the clock phases should be arranged for minimum clock feedthrough. The effect of the charge stored in the channel has not been considered.

Dynamic Range

Dynamic range is defined as the ratio of the maximum signal that the circuit drives without significantly distorting the noise level. The maximum distortion tolerated by the circuit depends on the application, but −60 dB is commonly used. Because the linearity of the capacitors is good enough and if the harmonic distortion components introduced by the OTA input stage are small, the major limitation for distortion is determined by the output stage of the OTA. For the folded cascade OTA of Fig. 22 this limit is given by

$$v_{o\max} \cong V_{R2} + V_{TP3} \tag{58}$$

If the reference voltage V_{R2} is maximized, Eq. (45) yields

$$v_{o\max} \cong V_{DD} - 2V_{DSATP} \tag{59}$$

where V_{DSATP} is the source-drain saturation voltage for the P transistors M_2 (M_3) and M_3. A similar expression is obtained for the lowest limit. Assuming a symmetrical output stage, from Eq. (59), the maximum rms value of the OTA output voltage is given by

$$v_{ORMS} \cong (V_{DD} - 2V_{DSATP})/\sqrt{2} \tag{60}$$

If the in-band noise, integrated up to $\omega = 1/R_{int}C_I$ is considered and if the most important term of Eq. (60) is retained, the dynamic range of the single-ended, switched-capacitor integrator becomes

$$DR \cong \frac{(V_{DD} - 2V_{DSATP})}{2\sqrt{2kT/C_I}} \tag{61}$$

At room temperature operation, this equation reduces to the following expression

$$DR \cong 5.5 \times 10^9 \sqrt{C_I}(V_{DD} - 2V_{DSATP}) \tag{62}$$

According to this result, the dynamic range of the switched-capacitor integrator is reduced when power supplies are scaled down and a minimum number of capacitors are employed. Clearly, there is a compromise between power consumption, silicon area, and dynamic range. As an example, for the case of $C_I = 1.0$ pF, supply voltages of ±1.5 V, and neglecting V_{DSATP}, the dynamic range of a single integrator is around 78 dB. For low-frequency applications, however, the dynamic range is lower because of the low-frequency flicker noise component.

DESIGN CONSIDERATIONS FOR LOW-VOLTAGE, SWITCHED-CAPACITOR CIRCUITS

For the typical digital supply voltages of 0–5V, switched-capacitor networks achieve dynamic ranges of the order of 80 to 100 dB. As long as power supplies are reduced, the swing of the signal decreases and the resistance of the switches increases further. Both effects reduce the dynamic range of switched-capacitor networks. For very low supply voltages, however, the main limitation on the dynamic range of the switched-capacitor circuit is from analog switches. A discussion of these topics follows.

Low-Voltage Operational Amplifiers

The implementation of op amps for low voltage applications is not a fundamental limitation as long as the transistor threshold voltage is smaller than $(V_{DD} - V_{SS})/2$. This limitation becomes clear in the design example presented in this section. The design of the operational amplifier is strongly dependent on the application. For high-frequency circuits, the folded-cascade is suitable but the swing of the signals at the output stage is limited by the cascade transistors. If a large output voltage swing is needed, a complementary output stage is desirable. To illustrate the design tradeoffs involved in a design of a low-voltage OTA, let us consider the folded cascade OTA of Fig. 22. For low-voltage applications and small signals, the transistors must be biased with very low $V_{GS} - V_T$. For ±0.75 V applications and $V_T = 0.5$ V, $V_{GS1} - V_{T1} + V_{DSAT6}$ must be lower than 0.25 V, otherwise the transistor M_6 goes to the triode region. For large signals, however, the variations of the input signal produce variations at the source voltage of M_1. These variations are of the order of $\pm 1.44(V_{GS1} - V_{T1})$. Hence, for a proper operation of the OTA input stage it is desirable to satisfy the following equation:

$$0.25 > 2.44(V_{GS1} - V_{T1}) + V_{DSAT6} \tag{63}$$

The increases in threshold voltage of M_1 because of body effects have to be taken into account. In critical applications,

Table 1. Dimension and Bias Current for the Transistors

Transistor	W, μm/L, μm	I_{BIAS}, mA
M_1	48/2.4	2.5
M_2	120/2.4	5.0
M_3	60/2.4	2.5
M_4	60/4.2	2.5
M_5	60/4.2	2.5
M_6	60/4.2	5.0

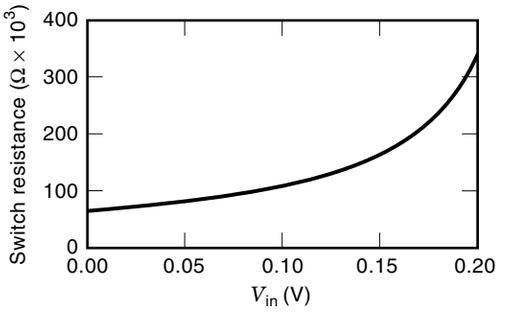


Figure 25. Typical switch resistance for an NMOS transistor.

PMOS transistors fabricated in a different well with their source tied to their own well are used. The dimensioning of the transistors and the bias conditions are directly related to the application. For instance, if the switched-capacitor integrator must slew 1 volt in 4 ns and the sampling capacitor is of the order of 20 pF, the OTA output current must be equal to or higher than 2.5 mA. Typically, for the folded cascade OTA, the DC current of the output and the input stages are the same. Therefore, the bias current for M_1, M_3, M_4, and M_5 equals 2.5 mA. The bias current for M_2 and M_6 is 5 mA. If $V_{GS1} - V_{T1}$ equals 0.06 V the dimensions of M_1 can be computed. Similarly, the dimensions of the transistors can be calculated, most of them designed to maximize the output range of the OTA. The dimensions and the bias condition for the OTA are given in Table 1.

A very important issue in the design of low-voltage amplifiers is the reference voltage. In the folded-cascade of Fig. 22, the values of the reference voltages V_{R1} and V_{R2} must be optimized for maximum swing of the output signal.

Analog Switches

For low-voltage applications, the highest voltage processed is limited by the analog switches rather than by the op amps. For a single NMOS transistor, the switch resistance is approximated by

$$R_{DS} = \frac{1}{m_n C_{OX} \dfrac{W}{L}(V_{GS} - V_T)} \tag{64}$$

where m_n and C_{OX} are technological parameters. According to Eq. (44), the switch resistance increases further when V_{GS} approaches V_T. This effect is shown in Fig. 25 for the case $V_{DD} = -V_{SS} = 0.75$ V and $V_T = 0.5$ V. From this figure, the switch resistance is higher than 300 kΩ for input signals of 0.2 V. However, for a drain-source voltage higher than $V_{GS} - V_T$, the transistor saturates and no longer behaves as a switch. This limitation clearly further reduces the dynamic range of switched-capacitor circuits.

A possible solution to this drawback is to generate the clocks from higher voltage supplies. A simplified diagram of a voltage doubler is depicted in Fig. 26a. During the clock phase ϕ_1, the capacitor C_1 is charged to V_{DD}, and, during the next clock phase, its negative plate is connected to V_{DD}. Hence, at the beginning of ϕ_2, the voltage at the top plate of C_1 is equal to $2(V_{DD}) - (V_{SS})$. Hence, C_1 is connected to C_{LOAD} and, after several clock cycles, if C_{LOAD} is not further discharged, the charge is recombined leading to an output voltage equal to $2(V_{DD} - V_{SS})$. An implementation for an N-well process is shown in Fig. 26(b). In this circuit, the transistors M_1, M_2, M_3, and M_4 behave as the switches S_1, S_2, S_3, and S_4 of Fig. 26(a). Whereas normal clocks are used for M_1 and M_2, special clock phases are generated for M_3 and M_4 because they drive higher voltages. The circuit operates as follows.

During ϕ_1, M_8 is opened because ϕ_2' is high. The voltage at node v_y is higher than V_{DD} because the capacitors C_3 and C_P were charged to V_{DD} during the previous clock phase ϕ_2. At the beginning of ϕ_1, when the voltage goes up, charge is injected to the node through the capacitor C_3. Because the bottom plate of C_2 is connected to ground by M_6, C_2 is charged to $V_{DD} - V_{SS}$ through M_7. Also, C_1 is charged to $V_{DD} - V_{SS}$. Dur-

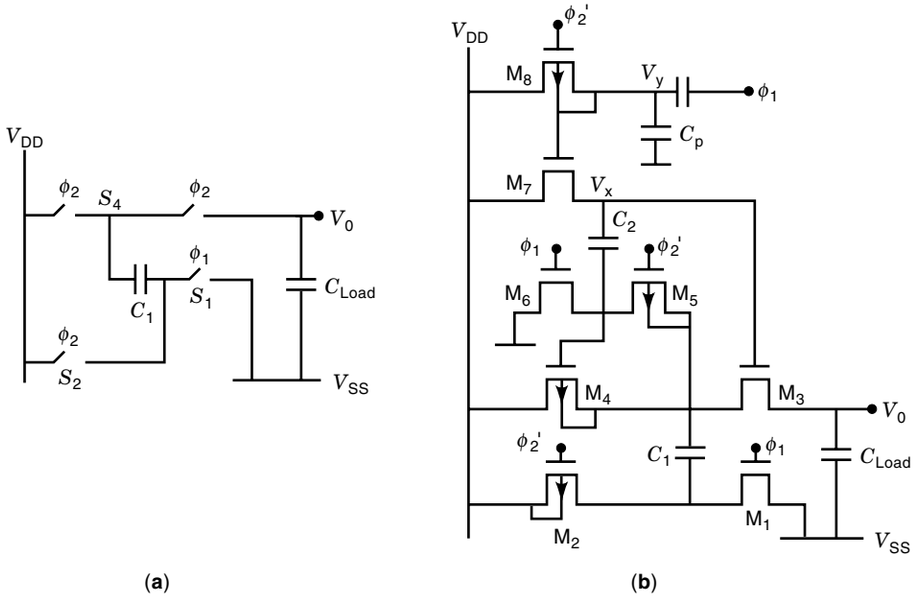


Figure 26. Voltage doubler: (a) simplified diagram and (b) transistor level diagram.

ing ϕ_2, the refresh clock phase, the bottom plate of C_1 is connected to V_{DD} by the PMOS transistor M_2. Note that if an NMOS transistor is employed, the voltage at the bottom plate of C_1 is equal to $V_{DD} - V_T$ resulting in lower output voltage. If C_1 is not discharged, the voltage at its top plate is $2V_{DD} - V_{SS}$ The voltage at node v_x approaches $3V_{DD} - 2V_{SS}$ volts turning M_3 on and enabling the charge recombination of C_1 and C_{LOAD}. As a result, after several clock periods, the output voltage v_0 is equal to $2V_{DD} - V_{SS}$. It has to be noted that v_Y is precharged to V_{DD} during this clock phase and that M_7 is off, keeping the voltage v_x high. To avoid discharges, the gate of M_4 is also connected to the bottom plate of C_2. Thus, M_4 is turned off during the refresh phase.

Some results are shown in Fig. 27. For this figure, the voltage at the nodes v_X, v_Y, and v_0 are depicted. The supply voltages used are $V_{DD} = 0.75$ V and $V_{SS} = -0.75$ V. The voltage at node v_x is nearly equal to $3V_{DD} - 2V_{SS}$, for this example, equal to 3.75 V. The output voltage nearly equals 2.25 V.

Design Example

Biquadratic filter. In this section, a second-order band-pass filter is designed. Following are the specifications for this biquad:

Center frequency:	1.63 kHz
Quality factor:	16
Peak gain:	10 dB
Clock frequency:	8 kHz

A transfer function that realizes this filter is given by the following expression:

$$H(z) = \frac{0.1953(z-1)z}{z^2 - 0.5455z + 0.9229} \tag{65}$$

This transfer function is implemented by using the biquad presented before. For the biquad of Fig. 21 and employing $a_1 = a_5 = a_9 = 0$, the circuit behaves as a band-pass filter.

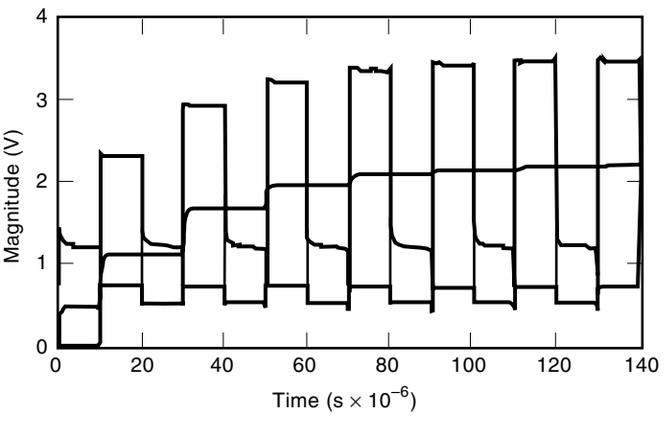


Figure 27. Time response of the voltage doubler at start-up.

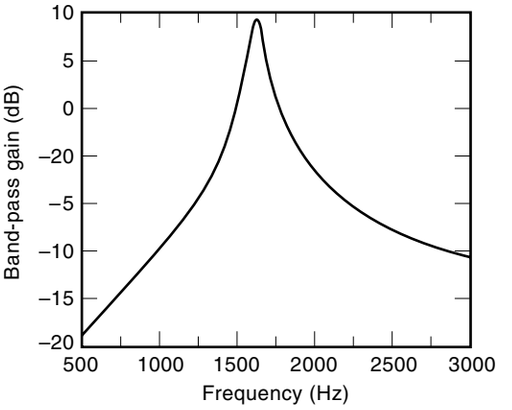


Figure 28. Frequency response of the second-order, band-pass filter.

Equating the terms of Eq. (65) with the terms of Eq. (37), the following equations are obtained:

$$\begin{aligned} a_8 &= \frac{1}{0.9229} - 1 \\ a_5' &= \frac{0.1953}{0.9229} \\ a_2 a_7 &= 2 + a_8 - \frac{0.5455}{0.9229} \end{aligned} \tag{66}$$

Solving these equations, the following values are obtained:

$$\begin{aligned} a_8 &= 0.0835 \\ a_5' &= 0.2116 \\ a_2 a_7 &= 1.4924 \end{aligned}$$

A typical design procedure employs $a_2 = 1$. For this case, the total capacitance is of the order of 32 unity capacitances. The frequency response of the filter is shown in Fig. 28.

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SWITCHED-CURRENT TECHNIQUE. See ANALOG INTEGRATED CIRCUITS.

SWITCHED FILTERS. See DISCRETE TIME FILTERS.

SWITCHED NETWORKS. See DISCRETE TIME FILTERS; TELEPHONE NETWORKS.