J. Webster (ed.), *Wiley Encyclopedia of Electrical and Electronics Engineering*

PHASE-LOCKED LOOPS, APPLICATIONS

Phase-locked loops (*PLL*s) are used for a variety of functions, all of which may be incorporated in a generic *PLL* form. The fundamentals of *PLL* systems are actually rather straightforward, but are typically enshrouded in mystery. This mystery stems in part from the difficulty of identifying the basic signal components in the loop and of understanding the unit as a feedback system with the peculiarities related to its phase-detector properties. This article provides a foundation of principles, including those of tracking and acquisition. From this foundation, several applications will be explored with the intent of providing an approach toward extending the concepts and not simply being able to replicate the analysis and design discussed.

The *PLL* has wide application. The majority of its applications fall into the four main categories frequency synthesis, frequency (*FM*) and phase (*PM*) modulation and demodulation, data and carrier recovery, and tracking filters. Applications for each category will be considered.

The Generic Phase-Locked Loop

Definition. The basic *PLL* is rather simple in concept. However, we extend it a bit to include most of the features of interest in a loop. The generic loop is shown in Fig. 15. Features that have been included are frequency synthesis, frequency offset, and modulation and detection. The phase detector is shown as a multiplier, since many classic phase detectors actually use the process of multiplication to extract phase information about a nominal phase shift of 90°. Many of the loop effects may be absorbed into the simpler model of Fig. 1 without any loss of generality. This basic *PLL* includes all the behavioral blocks needed for analysis of loops. The components of the basic loop are a phase detector (*PD*), a low-pass filter (*LPF*), and a voltage-controlled oscillator (*VCO*). In reality, the oscillator may be current-controlled and may be preceeded by an amplifier to adjust the range of performance of the oscillator or make a filter active. It is not uncommon to have to allow for additional delays and for low-pass filter effects at the input of the oscillator. Such delays and filtering increase the need for adequate phase and amplitude margins of the open-loop gain compared to unity at −180°, in order to prevent oscillation of the feedback system. The latter would cause either a highly undesired frequency modulation of the *VCO* or a total loss of frequency lock in the loop.

An aspect that causes much grief for newcomers to *PLL* systems is the varied notation. We will use typical notation and explain the meaning of each item as we proceed through the concepts. Many of the terms lend themselves to approximations that offer excellent predictions of system results.

A *PLL* is generally analyzed as a linear, feedback-control system with a transfer function $H(s)$ representing the relationship between the input phase θ_s and the *VCO* phase θ_o. This transfer function is one of the most confusing features of *PLL* analysis to the newcomer. In the signal sense, we have phase as a signal, not voltage or current amplitude. Thus, the frequency response is that of a time-varying phase, not of the amplitude variations in a typical input signal. Once this dual-frequency concept is understood, the analysis of a *PLL* is

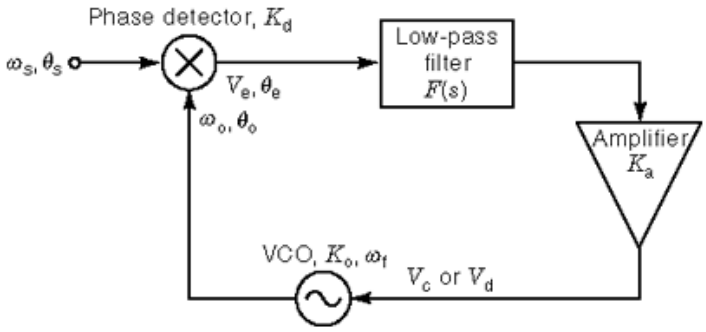

Fig. 1. Basic PPL, offering the most basic structure of a *PLL* needed for analysis, and consisting of a *VCO*, phase detector, loop filter, and possible amplifier.

rather straightforward. The transfer function just mentioned is written as

$$H(s) = \frac{\Theta_o(s)}{\Theta_s(s)} \tag{1}$$

This transfer behavior is typically written in terms of the linear transfer characteristics of the control-system open-loop transfer function $G(s)$. From Fig. 1 we have

$$H(s) = \frac{G(s)}{1 + G(s)}, \qquad G(s) = K_d F(s) K_a \frac{K_o}{s} = F(s)\frac{K}{s} \tag{2}$$

where the *VCO* is modeled as an integrator (the *VCO* converts the control voltage V_c into an instantaneous frequency, which is then integrated to obtain the phase). The gain terms provide the appropriate conversion, such as voltage to frequency for the *VCO*. The overall gain K is found with a variety of subscripts in the literature, which we have chosen not to use. In the control-theory context, the phase detector acts as a difference block—comparing the phase of the incoming signal with that of the *VCO*. The units used throughout the loop are the radian and the volt. In some cases, the ampere is appropriate for a particular device, simply requiring a change of the appropriate terms.

The filter used in a *PLL* is basically a low-pass filter designed to reject harmonics and spurious frequencies generated in the phase-detection process, a design requirement not typically found in control systems. This cutoff of the filter should be greater than the bandwidth of the *PLL*. However, additional filter shaping may also used to enhance the bandwidth and performance of the *PLL*. A simple lag–lead filter may be used to narrow the loop bandwidth, followed by a lag (or low pass) to provide the out-of-band low-pass filtering. In discussing filters, we will generally neglect this latter out-of-band lag filter, which should always be added to a *PLL*.

The use of integrators in the filter facilitates tracking of velocity and acceleration signals (velocity signals have a constant offset frequency, while acceleration signals have a changing offset frequency over time, typical of the Doppler shift in a low-earth-orbit satellite system). These integrators allow the steady-state phase error to be zero for specific applications, an important feature for many phase-demodulation processes.

Since the filters and the loop *VCO* response are generally monotonically decreasing in amplitude with increasing frequency, it is obvious that $H(s)$ may be simply approximated in two separate ranges as

$$H(s) \approx \begin{cases} 1, & \omega < \Delta\omega \\ G(s), & \omega > \Delta\omega \end{cases} \tag{3}$$

where $\Delta\omega$ is the bandwidth of the loop. A major problem in *PLL* design is ensuring that $G(s)$ does not approach -1 near the bandwidth of the loop. If the latter occurs, then substantial ringing or possible instability of the loop should be expected. To avoid this stability difficulty, the loop is specified with a sufficient damping factor, phase margin, or gain margin at $\omega = \Delta\omega$. The analytical treatment of the stability must take account of possible stray delays in the system caused by low-pass coupling of oscillator control lines and related connections needed for circuit isolation. It is common to simply add some extra margin to allow for common stray effects, but such actions should be taken carefully, since they may add substantial switching delays and performance degradation in an operational system. It should be noted that the *PLL* bandwidth $\Delta\omega$ is not the bandwidth of a filter inserted in the loop, but rather comes from an interaction of the loop filter with the entire loop, particularly the feedback filter effects of the *VCO*.

A secondary transfer function that is important for evaluating the limitations of the system is the error transfer function relating the phase error to the input phase. This function may be written as

$$H_e(s) = \frac{\Theta_s(s) - \Theta_o(s)}{\Theta_s(s)} = 1 - H(s) \approx \begin{cases} 1/G(s), & \omega < \Delta\omega \\ 1 & \omega > \Delta\omega \end{cases} \tag{4}$$

This error function is critical in the determination of the limits beyond which the signal may cause the loop to lose lock, or simply to exceed the linear range of the components of the loop—most commonly the phase detector or active filters. Additional transfer functions may be defined to describe the modulation and demodulation processes of both *FM* and *PM* systems, as will be considered with specific applications. For *FM*, the product of the modulation signal and the error transfer function tends to peak at $\Delta\omega$. This peak substantially increases the probability of the phase range of the detector being exceeded, causing a loss of lock in the vicinity of $\Delta\omega$. This peaking suggests that $\Delta\omega$ would be a good frequency to be check during loop testing.

Simple Phase-Locked-Loop Analysis. The simple linear analysis of a *PLL* starts with Eq. (2) written as

$$H(s) = \frac{KF(s)}{s + KF(s)} \tag{5}$$

Thus the basic analysis and design stem from the choice of the open-loop gain K and the filter function F. It is common to assume that F is monotonically decreasing in frequency, though this need not be the case. If $F = 1$, then the transfer function is simply a low-pass filter defined by a radian bandwidth of K. In practice, an additional filter pole is added above the loop bandwidth for rejection of spurious signals created by the phase-detector process (generally a form of multiplication) and will only increase the rejection of higher frequencies in the loop, not having a substantial effect on the in-lock performance. If this additional filtering is not used with multivibrator *VCO*s, the resultant output of the *VCO* will have a duty cycle related to the phase error.

Let us consider the poor choice of a lag filter to control the bandwidth by adjusting the filter bandwidth relative to K. In this case we would have

$$F(s) = \frac{1}{1+s\tau} \quad \text{and} \quad H(s) = \frac{\dfrac{K}{\tau}}{s^2 + \dfrac{1}{\tau}s + \dfrac{K}{\tau}} \tag{6}$$

The new transfer function is commonly written as

$$H(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{7}$$

where ω_n is called the natural frequency and ζ is the damping factor. In controls, ζ takes on an important role in the stability of the system. Generally speaking, ζ should not be chosen any smaller than about $1/\sqrt{2}$. That exact value leads to optimal coupling for the system, in the sense that smaller coupling values lead to transient ringing, while larger values lead to longer transient times or slower responses. Actual choices of ζ must also allow for spurious delays in the system. The corresponding response of such a transfer function to a step change in phase is easily obtained using Laplace transforms and is given by Blanchard (1) as

$$\theta_o(t) = \theta e^{-\zeta\omega_n t}\left(\cos\omega_n\sqrt{1-\zeta^2}t + \frac{\zeta}{\sqrt{1-\zeta^2}}\sin\omega_n\sqrt{1-\zeta^2}t\right) \tag{8}$$

where θ_o represents the transient phase equivalent of the output phase, Θ_o. For $\zeta < 0.707$, substantial oscillatory behavior near ω_n is created that dies out at the rate $1/\tau$ (τ being the filter time constant), slower than K. For larger ζ, the trigonometric functions become hyperbolic and the solution becomes a double exponential in $1/\tau$ and K. This connection with the actual parameters being selected is sometimes scaled out of the problem, leaving the designer in a bit of a quandary about how to make some of the choices. In this case, it is clear that the decay at the rate of K is the limiting feature of the loop. If K is not adjustable, the only consideration with a lag filter is setting τ for good rejection of the spurious output frequencies created by the detector outside of the bandwidth of K.

A lag–lead filter offers a reasonable alternative to adjustment of the loop gain constant. The lag–lead filter and response are given by

$$F(s) = \frac{1+s\tau_2}{1+\tau_1} \quad \text{and} \quad H(s) = \frac{\dfrac{K}{\tau_1}(1+s\tau_2)}{s^2 + \dfrac{1+K\tau_2}{\tau_1}s + \dfrac{K}{\tau_1}} \tag{9}$$

The step response for this loop is similar to the last case and is given by Blanchard as (1)

$$\theta_o(t) = \theta e^{-\zeta\omega_n t}\left(\cos\omega_n\sqrt{1-\zeta^2}t + \frac{\frac{\omega_n}{K} - \zeta}{\sqrt{1-\zeta^2}}\sin\omega_n\sqrt{1-\zeta^2}t\right) \tag{10}$$

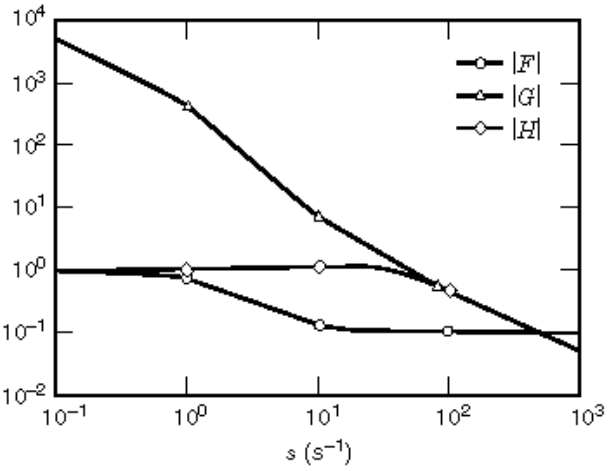

Fig. 2. Bode plot of a second-order filter and the associated G and H magnitudes. The lag–lead properties of the filter are seen in the two breakpoints of the filter response $|F|$. The filter behavior produces $|G|$ as $|F/s|$, resulting in a transfer function H with response of unity within the passband and G outside the passband.

where $\omega_n = \frac{|\omega_o' \pm \omega_{offset}|}{N} = \omega_{ref}$ and $\zeta = (1 + K\tau_2)/(2\frac{|\omega_o' \pm \omega_{offset}|}{N} = \omega_{ref})$. This response has a key τ_1 that was missing with the simple lag filter. As τ_1 is increased to narrow the filter response, the zero of the filter may also be changed. In essence, the effective gain of the loop is changed to $K\tau_2/\tau_1$, with a fundamental pole at $-K\tau_2/\tau_1$ and a second pole at about $-1/\tau_2$ as long as the response of F changes almost entirely within the bandwidth of the loop. This is easily seen in a Bode plot of H along with the plots of $|F|$ and $|G|$, as in Fig. 2 with $\tau_1 = 0.1$ s, $\tau_2 = 1$ s, and $K = 500$ rad/s. In this instance, the bandwidth of the loop has been reduced to 50 rad/s, from 500 rad/s with no filter. The inclusion of an additional pole in the filter at 200 rad/s ($\tau_3 = 0.005$ s) helps to filter out the spurious output frequencies of the detector without much change to the in-band response of the *PLL*, as shown in Fig. 3. There is a slight increase in the bandwidth due to the proximity of the pole to the 50-rad/s bandwidth, but with improved rejection. The values of the other filter parameters may be adjusted slightly to bring the bandwidth back to the desired value.

This Bode-plot viewpoint has been provided to emphasize the design information that is directly available from the Bode plot for many *PLL* situations. The Bode plot often provides a faster approach to the design needs while still maintaining reasonable accuracy. Evaluating the phase margin (phase of G relative to -180° when $|G| = 1$) is an alternate method for estimating the stability of the loop. With the extra pole, the margin in this example becomes 65.8° rather than 80°. The advantage to this approach is a quick look at a design based on the physical system rather than the scaled control system variables. In addition, once the Bode-plot approach is adopted, the extension to higher-order systems is straightforward, not requiring information for Nyquist or root-locus plots. The latter are useful tools, but do not substantially speed the design of a well-designed *PLL*.

The criteria for the Bode design is that the slope of G about the bandwidth should be approximately 20 dB/decade, similar to a simple integrator. A phase margin of 90° is desirable to minimize peaking in the passband response. A 65.6° phase margin corresponds to a damping factor of $1/\frac{N\phi_o}{N\phi_{ref}} = \frac{N\omega_o}{N\omega_{ref}} = \frac{\phi_o'}{N\phi_{ref}} = \frac{\omega_o'}{N\omega_{ref}} = H(j\omega_n)$, often found to give the fastest settling of transient responses with no ringing. A damping factor of 1/2 creates a phase margin of 52° with a peaking at the band edge of about 1.2 dB above the nominal passband response. This slight peaking in the response is often a reasonable compromise for faster transient response times, though with some damped ringing. Additional filtering may be added above the bandwidth to reject spurious detector

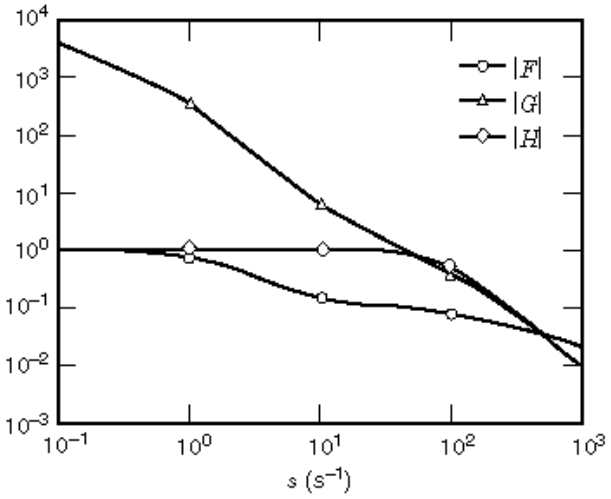

Fig. 3. Bode plot of the second-order filter with an additional rejection pole. The performance within the passband is equivalent to the filter of Fig. 2, but with additional rejection for higher frequencies.

output. Such filtering may even include notch filters. With the additional filtering design guidelines placed above the loop bandwidth, the transient response of the system approaches that of a simple low-pass filter with a bandwidth set from the Bode analysis. If a designer hedges on the phase margin by bringing these higher-frequency filter poles closer to the passband, the *PLL* response peaks at the bandwidth limit as suggested. Such a slight peak was seen in the response of Fig. 3 and is considered acceptable for many applications if kept below 1 dB. A large collection of typical transient response plots is provided by Blanchard (1).

Components

Phase Detector. The critical component of a *PLL* is the phase detector. In control theory, it becomes simply a difference block as previously suggested. However, the difference in phase between the two incoming signals or frequencies is typically obtained by multiplying the two signals together and filtering the resulting frequency-difference product. A multiplier is an ideal mixer that produces a phase detector whose output voltage is proportional to the sine of the phase difference θ_e. The multiplier-type phase detector is one of four basic forms. The basic detector forms give error output voltages as

$$V_e = K_d \begin{cases} \sin\theta_e & \text{(sinusoidal)} \\ \begin{cases} \theta_e - n2\pi, & |\theta_e - n2\pi| < \pi/2 \\ \pi - (\theta_e - n2\pi), & |\theta_e - n2\pi - \pi| < \pi/2 \end{cases} & \text{(triangular)} \\ \theta_e - n2\pi, \quad |\theta_e - n2\pi| < \pi & \text{(ramp)} \\ \theta_e - n2\pi, \quad |\theta_e - n2\pi| < 2\pi & \text{(extended ramp, phase–frequency)} \end{cases} \tag{11}$$

which are depicted graphically in Fig. 4. The arrows in Fig. 4(d) emphasize that the transitions at the voltage extremes are directed back to the zero value as a one-way transition, not to the opposite extreme as with

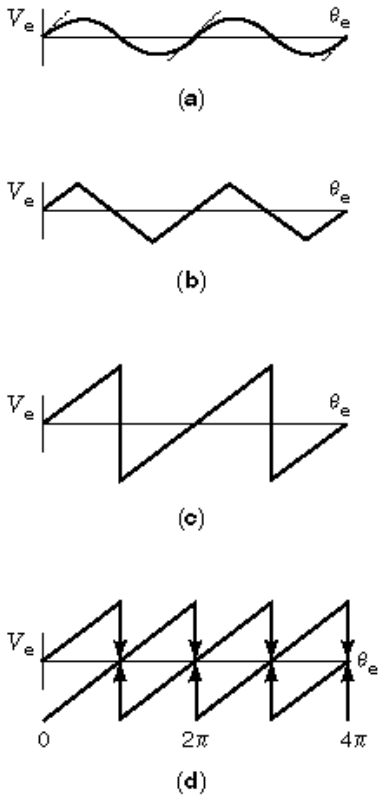

Fig. 4. Phase detector characteristics: (a) sinusoidal, (b) triangular, (c) ramp, and (d) extended ramp. The arrows of (d) are to emphasize the one-way transition to the zero output state rather than the opposite extreme of the output.

the two-way transition of the ramp detector. The one-way transition of the extended ramp is critical to the development of a dc offset level to aid in acquisition when the loop is out of lock.

How are these results obtained? They are obtained through basic mixing processes creating a product of the two signals in question. Consider the input frequencies to be given by

$$\omega_s = \omega_f + \frac{d\phi_s}{dt} = \omega_f + \Omega s$$
$$\omega_o = \omega_f + \frac{d\phi_o}{dt} = \omega_f + \Omega_o \qquad (12)$$

where ϕ has been used to represent the phase difference from a reference oscillator at frequency ω_f. This frequency ω_f is often called the free-running frequency and is indeed just that for several of the detectors. For the other detectors, which use integrating filters, it is typically chosen as the center of the frequency range.

The corresponding input signals are

$$\begin{aligned} \upsilon_{\mathrm{s}}(t) &= V_{\mathrm{s}} \cos(\omega_{\mathrm{f}} t + \phi_{\mathrm{s}}) \\ \upsilon_{\mathrm{o}}(t) &= V_{\mathrm{o}} \cos(\omega_{\mathrm{f}} t + \phi_{\mathrm{o}}) \end{aligned} \tag{13}$$

If we use an ideal multiplier followed by a low-pass filter, we obtain

$$\upsilon_{\mathrm{e}} = \mathrm{LPF}(\upsilon_{\mathrm{s}}\upsilon_{\mathrm{o}}) = \mathrm{LPF}\left(\frac{V_{\mathrm{s}}V_{\mathrm{o}}}{2}[\cos(\phi_{\mathrm{s}} - \phi_{\mathrm{o}}) + \cos(2\omega_{\mathrm{f}} t + \phi_{\mathrm{s}} + \phi_{\mathrm{o}})]\right) \tag{14}$$

Using a low-pass rejection filter for the second harmonic, we take the output as

$$\begin{aligned} \upsilon_{\mathrm{e}} &= \frac{V_{\mathrm{s}}V_{\mathrm{o}}}{2} \cos(\phi_{\mathrm{s}} - \phi_{\mathrm{o}}) \\ &= \frac{V_{\mathrm{s}}V_{\mathrm{o}}}{2} \sin\left(\phi_{\mathrm{s}} - \phi_{\mathrm{o}} + \frac{\pi}{2}\right) \end{aligned} \tag{15}$$

To obtain the *sinusoidal* form we have to include a $\pi/2$ phase shift, θ_{offset}. Thus if we define $\theta_{\mathrm{s}} = \phi_{\mathrm{s}}$ and $\theta_{\mathrm{o}} = \phi_{\mathrm{o}} - \pi/2$, we have the sinusoidal error form. An important aspect of the sinusoidal detector is the need for amplitude control of the input signals to avoid gain variations due to the signal amplitude changes. The needed product may be obtained using a variety of mixer configurations. See Egan (2) for an analysis of the various types of mixers used as phase detectors.

The simplest way of considering the *triangular* detector is to replace the cosine inputs of the sinusoidal detector with pure square waves. Then the phase-detector response is simply the convolution of two square waves, providing the triangular response after filtering. Due to the multiplication process, the same $\pi/2$ phase shift is required as used for the sinusoidal detector. A simple square-wave phase detector is a logic AND, OR, or exclusive-OR gate. If we filter the output of the gate, we obtain the logical product with a dc voltage offset, the latter describing the linear variation of the two waves from in phase to totally out of phase. For the AND gate, the dc offset is $\frac{1}{4}$ the maximum output voltage, the variation between between 0 and one-half the maximum output voltage. The OR gate simply raises the average voltage of the AND gate to three-fourths the maximum output voltage of the gate. Relative to the center of this voltage variation, we have triangular-wave performance of the offset voltage with respect to the phase difference of the two signals.

A *ramp* detector has a phase offset of 180° (π rad). This form of detector is obtained by using the two input signals to set and reset an edge-triggered RS flip-flop, followed by appropriate low-pass filtering.

The *extended ramp* requires no phase offset and obtains its output from a tristate logic circuit that has a cycle memory to extend the range beyond a single cycle. This detector is one of the most commonly used phase detectors in integrated systems. The extended ramp is simply a transient-logic combination of ramp-type detectors and is commonly called a phase–frequency detector. A fundamental problem that has been overcome in recent years is its zero-phase residual error. The transition through the zero-phase crossing involves several state changes, which may cause random behavior. The frequency-detection properties of the detector occur when the *PLL* is not in lock, creating a high or low triangular waveform with one-way transitions shown by the arrows of Fig. 4(d). This high–low feature causes an additional dc offset that aids in frequency acquisition. The detector is generally followed by an integrating low-pass filter in order to reach a zero steady-state error with no frequency or phase error. Further information on these detectors are given by Egan (2), Best (3), and Rohde (4).

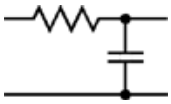

Fig. 5. Filter for spurious-output rejection. This simple low-pass filter is the minimum filtering that should be used with a *PLL* to rejected unwanted frequency products produced in the phase-detection process.

A final phase detector that should be noted is the *sample-and-hold*. The classic sample-and-hold extracts a sample of an oscillator signal and holds it until the next sample, at which time the hold is simply updated. This technique operates much like a sinusoidal detector for a sinusoidal input signal, having the digital equivalent of a D flip-flop phase detector. The sample-and-hold can offer a major advantage in feedthrough reduction for the pulsed phase–frequency detector. To take advantage of such a use in a synthesizer, the sample is held off one or more clock cycles of the *VCO* frequency. Thus, the sample is taken after the integrated output of the phase–frequency detector has settled. In so doing, the feedthrough signal is reduced to a correction step rather than a short pulse, substantially reducing the sideband generation in the system. The sample-and-hold detector is not restricted to following another detector, but may be used directly as the phase detector. It is sometimes advantageous in a synthesizer application to cascade two sample-and-hold phase detectors to obtain even further sideband reduction. Further filtering should still be used, but with reduced rejection requirements on the filter.

A second significant use of the sample-and-hold detector is in microwave frequency synthesis and stabilization. For this application, the sample is taken on every N th cycle of an input sinusoidal waveform from the *VCO*. The result is to effectively treat the input signal as though it were N times smaller, acting as a synthesizer with a frequency that is N times the reference frequency. For many applications, the primary purpose of this multiplying loop is to stabilize a microwave oscillator that may otherwise drift in frequency with temperature and power.

Filters. The filters of the phase-locked loop provide two vital functions. First, the *PLL* filter provides the necessary feedback frequency response to control the gain and bandwidth of the system. An additional low-pass characteristic that should always be included provides the needed spurious rejection of mixing products that result from the phase-detector operation. In frequency synthesis applications, the feedthrough of the spurious frequencies of the phase detector is the major cause of sideband modulation components in the oscillator output. These sidebands are usually severely restricted by governmental regulation to prevent interference with other spectrum users. Thus the regulatory issue is a major concern that must be added to the problem, where the spurious products usually have little effect on the *PLL* performance other than the sideband generation. On reception, interference rejection of adjacent-channel signals, produced by the conversion with the spurious sidebands generated in the *VCO*, is also a potential problem.

It is a good rule to make the filter only as sophisticated as needed for the particular application. If no bandwidth control is needed, then a simple low-pass filter for eliminating the spurious frequencies may be all that is used. In such a case, the filter bandwidth will be above the *PLL* bandwidth and may be obtained with a simple *RC* low-pass filter. In such a case, the *PLL* operates in a first-order mode within the bandwidth of operation.

The filters used in the *PLL* define the system type and order. The *order* refers to the degree of the system polynomial in the denominator of the transfer function, while the *type* refers to the number of integrators in the loop. By default, a *PLL* is at least a type-I loop. An ideal first-order loop would have no filter. In reality, we use a filter (Fig. 5) to eliminate the spurious outputs of the phase detectors. However, as long as the filter bandwidth is much greater that the loop bandwidth (which is K for this case), the linear system analysis of the loop is closely approximated by a first-order loop with no filter.

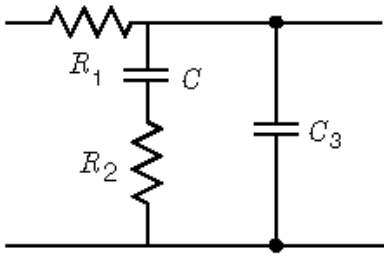

Fig. 6. Lag–lead passive filter with spurious-frequency rejection. The lead produced by R_2 returns the filter response to a constant for transition through the bandwidth limit, reducing the potential instability due to a small phase margin. The capacitor C_3 is added to provide high-frequency rejection of the undesired phase-detection products.

The lag–lead filter is easily implemented in discrete form with the addition of a single resistor as shown in Fig. 6. The extra capacitor, C_3, provides the spurious-sideband rejection and is not directly a part of the lag–lead circuit. This filter is described by

$$F(s) = \frac{1 + sR_2C}{1 + s[(R_1 + R_2)C + R_1C_3] + s^2R_1R_2CC_3} \approx \frac{1 + sR_2C}{1 + s(R_1 + R_2)C} \qquad (16)$$

where the approximation occurs when the extra capacitor is ignored. A second lag–lead filter may be cascaded with this filter to obtain an approximation to a double-pole, double-zero filter for use in a third-order system. Third-order systems find use in tracking of low-earth-orbit satellites, which have an acceleration profile that causes a continuously changing frequency. The third-order system is necessary to minimize the steady-state phase error in the received signal and is typically implemented as a type-II loop.

Active filter systems are useful for implementing many filter functions. A major advantage of active filters is their ability to make the denominator of the filter function a simple s and thus yield an integrator. Such a configuration is shown in Fig. 7, giving

$$F(s) = -\frac{1 + sR_2C}{sR_{\text{in}}(C + C_3)\left(1 + sR_2\dfrac{CC_3}{C + C_3}\right)} \qquad (17)$$

The new difficulty added by active filters is a phase inversion in the path that must be correctly taken into account in the feedback analysis. An additional filter is simply cascaded if needed.

One must take care that the high-frequency response of the operational amplifier used does not allow undesired pulse streams through the device. It is often wise to add passive rejection filters within the active-filter design to guard against such problems. In practice, the frequency response of the operational amplifier limits the ability to reject the transmission of the higher-frequency spurious signals, for which C_3 is added. To aid in the rejection and reduce the potential for overdrive of the operational amplifier, C_3 may be relocated as part of an input T network as shown in Fig. 8, giving

$$F(s) = -\frac{1 + sR_2C}{sR_{\text{in}}C[1 + s(R_{\text{in}}/4)C_3]} \qquad (18)$$

Additional factors that must often be adjusted in practical systems are offset voltages within the filters and other components.

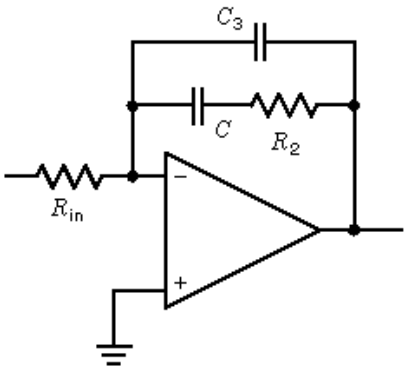

Fig. 7. Integrating operational-amplifier filter with spurious-signal rejection, providing the desired zero to control the phase margin while still providing high-frequency rejection with C_3.

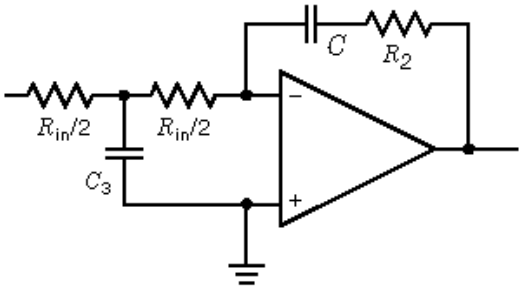

Fig. 8. Modified filter for improved spurious-signal rejection. This filter is a modified version of Fig. 7, designed to reduce possible high-frequency feedthrough in the filter due to inadequate operational-amplifier performance and to also avoid overdrive of the amplifier.

Oscillators. The type of oscillator depends strongly on the application at hand. For low-frequency applications, the oscillator that forms the *VCO* in the loop is often a simple multivibrator, typically constructed with a balanced pair of devices and current-controlled in frequency. As frequencies are increased into the radio and microwave realms, the oscillators are generally tuned circuits (resonant *LC* combination, cavity, or *YIG* structure) with varactor frequency adjustment. The circuits are often balanced to reduce harmonic content, and varactors are often used in pairs to reduce noise effects. Care must be used in providing the bias to varactors. These units are part of a tuned circuit that effectively forms a low-pass filter with the bias resistor to the control signal, producing an unwanted lag filter in the loop. In addition, the resistor must be sufficiently large not to reduce the *Q* (or bandwidth) of the tuned circuit and yet not so large as to become a substantial noise source in the loop. Noise is a critical item of concern in the design of synthesizer systems.

The tuning of the *VCO* is often nonlinear, even with some multivibrators. It is sometimes desirable to linearize the voltage-to-frequency response, improving the linear system performance of the loop. Such linearization is generally done with a diode switching network for selective loading that creates a piecewise compensation of the *VCO* transfer function to obtain an effective linearization of the transfer. One drawback to such piecewise loading systems is the inherent noise that may be created in the process.

In power and related applications, the oscillator may not always be obvious. The effective oscillator may be a variable-speed motor that must be controlled or be a fully mechanical system such as the combustion engine of an automobile with a speed sensor on the shaft. The specific design of oscillators is not the goal of

this section, but rather a brief consideration of the types of units that might compose an oscillator in a *PLL* system. For the purposes of analysis, the oscillator, frequency divider, and offset oscillator to be considered in the applications may be considered as a single oscillator. Keep your mind open, and you may be surprised at the systems that might be considered as oscillators in a *PLL*.

Acquisition

Analytic Approach. The first step in the operation of a *PLL* is the acquisition phase. In the previous sections we considered the *PLL* as a linear system, always in lock. We begin the consideration of achieving this locked state by assuming the *VCO* is running at a free-running frequency and the input is offset from the free-running frequency by an amount Ω_0. The analysis that follows provides a basic viewpoint of acquisition for the generic loop with a sinusoidal phase detector. If the detector is a triangular or ramp type, the same basic mechanism occurs with a slight increase in the effective detector gain for the beat-frequency component of the system. The analysis for the phase-frequency detector is a bit simpler due to the built-in offset voltage when the frequencies are different. Other considerations must also be taken if the filter is an integrator that is likely sitting on a power-supply rail when out of lock.

This analytical derivation is approximate, but gives surprisingly useful guidelines to the acquisition process of phase-locked loops with lag–lead filters. We assume that only a sinusoidal term plus a slowly varying offset need be considered at the control terminal of the *VCO*. With this in mind, we will look at the operation of the loop for frequency differences in the various frequency ranges of the loop filter in order to obtain limits on acquisition as well as an estimate of the time for acquisition.

For the nonintegrating lag–lead filter used with nearly all but the phase–frequency detector, the output of the detector will be dominated by a beat frequency between the two detector inputs and a small low-frequency (approximately dc) part that provides the locking mechanism. For such an output, we may write the control voltage of the loop as approximately

$$v_c(t) \approx u + \Delta u \sin \Omega t \tag{19}$$

From this voltage we may write the output of a sinusoidal detector as

$$\begin{aligned} v_e &= K_d \sin\left((\Omega_o - K_o u)t + \frac{K_o \Delta u}{\Omega}\cos \Omega t + \theta\right) \\ &= K_d\Big[\sin[(\Omega_o - K_o u)t + \theta]\cos\left(\frac{K_o \Delta u}{\Omega}\cos \Omega t\right) \\ &\quad + \cos[(\Omega_o - K_o u)t + \theta]\sin\left(\frac{K_o \Delta u}{\Omega}\cos \Omega t\right)\Big] \\ &\approx K_d \sin[(\Omega_o - K_o u)t + \theta] \\ &\quad + \frac{K_d K_o \Delta u}{2\Omega}\cos[(\Omega_o - K_o u - \Omega)t + \theta], \\ &\quad \left|\frac{K_o \Delta u}{\Omega}\right| \ll 1 \end{aligned} \tag{20}$$

The quantity θ is an unknown phase offset of the *VCO*. We have chosen to use simple Taylor expansions of the trigonometric functions rather than taking the additional step of using Bessel functions before taking a Taylor series.

For the analysis we will assume the first term of Eq. (20) is above the filter breakpoints and is simply reduced in amplitude by the high-frequency response of τ_2/τ_1 of the filter. The second term is considered slowly varying and is the term we shall consider for the filter interaction. Thus we have

$$\begin{aligned} v_c(t) \approx K_d K_a \Bigg(& \frac{\tau_2}{\tau_1} \sin[(\Omega_o - K_o u)t + \theta] \\ & + K_o \Delta u f(t) \otimes \frac{\cos[(\Omega_o - K_o u - \Omega)t + \theta]}{2\Omega} \Bigg) \end{aligned} \tag{21}$$

where the $\otimes$ denotes convolution in time. Assuming the second term is a low-frequency term as previously mentioned, we can determine coefficients by comparison with the original v_c to give

$$\begin{aligned} \Delta u &= K_d K_a \frac{\tau_2}{\tau_1} \\ \Omega &= \Omega_o - K_o u \\ \theta &= 0 \\ u &= \frac{K \Delta u}{2} f(t) \otimes \frac{1}{\Omega} \end{aligned} \tag{22}$$

Thus we may write a summary equation as

$$\Omega_o - \Omega = \frac{K^2}{2} \frac{\tau_2}{\tau_1} f(t) \otimes \frac{1}{\Omega} \tag{23}$$

Rather than work with the full $f(t)$, we may consider each frequency range of the filter separately. The purpose of checking each region to search for a possible solution and or limit on the operation. First, consider $f(t) \approx \tau_2/\tau_1$ (the high-frequency response). Equation (23) becomes

$$\Omega_o - \Omega = \left(K \frac{\tau_2}{\tau_1} \right)^2 \frac{1}{2\Omega} \tag{24}$$

with solution

$$\Omega = \frac{\Omega_o}{2} \pm \sqrt{\left(\frac{\Omega_o}{2} \right)^2 - \frac{1}{2} \left(K \frac{\tau_2}{\tau_1} \right)^2} \tag{25}$$

There are two cases of interest. First, if $\Omega_o \geq \frac{N\phi_o}{N\phi_{ref}} = \frac{N\omega_o}{N\omega_{ref}} = \frac{\phi'_o}{N\phi_{ref}} = \frac{\omega'_o}{N\omega_{ref}} = H(j\omega_m) K \tau_2/\tau_1$, the solution provides for a constant difference frequency as well as a low-frequency term at zero frequency, not above $1/\tau_2$, which is an invalid solution. If $\Omega_o \leq \frac{N\phi_o}{N\phi_{ref}} = \frac{N\omega_o}{N\omega_{ref}} = \frac{\phi'_o}{N\phi_{ref}} = \frac{\omega'_o}{N\omega_{ref}} = H(j\omega_m) K \tau_2/\tau_1$, the solution is nonphysical and we have

chosen the wrong region of the filter for the analysis. Thus this frequency range of operation is not possible within the constraints of the model.

For the second low-frequency, unity-transmission region, we have

$$\Omega_o - \Omega = K^2 \frac{\tau_2}{\tau_1} \frac{1}{2\Omega} \tag{26}$$

or

$$\Omega = \frac{\Omega_o}{2} \pm \sqrt{\left(\frac{\Omega_o}{2}\right)^2 - \frac{1}{2} K^2 \frac{\tau_2}{\tau_1}} \tag{27}$$

Again there are two cases of interest. First, if $\Omega_o \geq |1 - H(j\omega_m)| \approx 1 \quad \text{for} \quad \omega_m > (\text{loop bandwith})$, the solution is a constant difference frequency along with a low-frequency term at zero frequency, an out-of-lock condition. This limit becomes our basic limit of frequency pull-in, $\Delta\omega_p$, the range within which the *PLL* is able to lock eventually. If $\Omega_o \leq |1 - H(j\omega_m)| \approx 1 \quad \text{for} \quad \omega_m > (\text{loop bandwith})$, the solution is nonphysical and we have again chosen the wrong region of the filter for the analysis.

The third midrange frequency region gives an integration of the detector output that is needed for acquisition as

$$\Omega_o - \Omega = \frac{K^2}{2} \frac{\tau_2}{\tau_1} \frac{1}{\tau_1} \int_0^t \left(\frac{1}{\Omega}\right) d\tau \tag{28}$$

with a solution given by

$$\Omega = \sqrt{\Omega_o^2 - K^2 \frac{\tau_2}{\tau_1} t} \tag{29}$$

In this analysis we have used the smallness restriction that

$$\left|\frac{K_o \Delta u}{\Omega}\right| = \left|\frac{K\tau_2/\tau_1}{\Omega}\right| \ll 1 \tag{30}$$

At the limit of this restriction, the *PLL* has reached the system bandwidth and ceases the pull-in process of acquiring lock we have just identified, locking in without further cycle slippage. This latter process is the basic transient response of the system and is referred to as lock-in; it occurs over a range $\Delta\omega_L$. The time it takes for this process to move the *VCO* from the starting offset frequency to the loop bandwidth comes from Eq. (29) as

$$t \approx \left[\left(\frac{\Omega_o}{K\tau_2/\tau_1}\right)^2 - 1\right] \tau_2 \tag{31}$$

The pull-in transient occurs in about τ_2 seconds, giving a total acquisition time of

$$T_{acq} \approx \left(\frac{\Omega_o}{K\tau_2/\tau_1}\right)^2 \tau_2 \tag{32}$$

Thus τ_2 has a major role in setting the acquisition time of a loop. For the largest frequency of pull-in, called the pull-in range, we have

$$\Delta\omega_p = \sqrt{2K\left(K\frac{\tau_2}{\tau_1}\right)} \tag{33}$$

If the frequency difference of the loop is within this range, the loop will eventually pull in to the locked condition. After the pull-in process error reaches the loop bandwidth, the transient effects of a well-designed loop will take over and complete the locking process with no further cycle slippage. The smaller range over which this occurs is the *lock-in range*; it is approximately equal to the loop bandwidth and given by

$$\Delta\omega_L = K\frac{\tau_2}{\tau_1} \tag{34}$$

The integrating filter does not have a low-frequency, unity-gain region. Thus the pull-in range for the integrating filter is not limited by the detector, but rather by the filter, amplifier, or *VCO*. Unfortunately, an integrator also tends to send an unlocked *PLL* to a supply limit of one of the components rather than to the free-running frequency for an initial value, so that it requires an acquisition-process initialization. With active filters, the initialization may simply be a Schmidt trigger arrangement that reverses the bias voltage on the reference terminal to begin integration back across the active region of the device. As long as the desired frequency is within the tuning range, this integration process should pick up the locking process. In the case of the phase–frequency detector, the detector has a built-in bias that is added to the loop-filter input if the frequencies of the inputs differ. This bias results from the phase–frequency detector being reset to the center of the phase range rather than the opposite phase limit when the range is exceeded [refer to Fig. 4(d)].

Phase-Plane Approach. In the phase-plane approach, it is desired to relate the time derivative of the phase error to the instantaneous phase error. In relating these two properties, a plot may be made of the phase error versus time. In a numerical sense, you would simply start with the current phase error, determine the time derivative, and estimate the new phase error at the next time step. In stepping through the process, acquisition will occur if the process converges to smaller phase errors as time progresses and the phase error cycles through multiple cycles. These plots are interesting, and the reader is referred to Blanchard (1) for further information.

Noise Fundamentals

Noise can be a problem in *PLL* systems, though it can be alleviated by the proper use of *PLL*s. Slightly different problems are encountered for low and for high signal-to-noise ratios. For the small-signal case, many of the small-signal approximations relating amplitude and phase may be used. For the large-signal case, the nonlinearities of the system must often be considered, particularly with respect to the the potential for loss

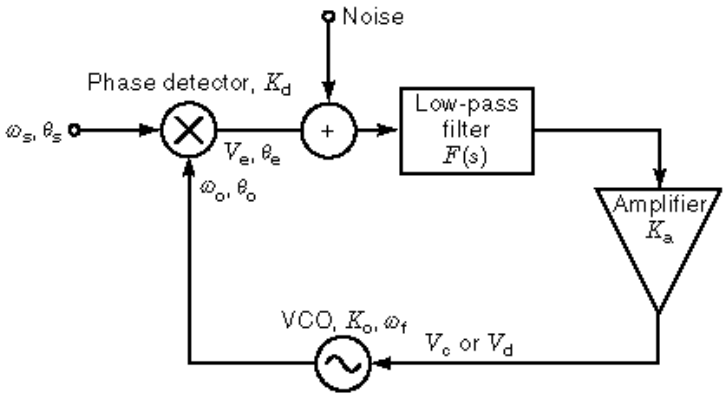

Fig. 9. Simple noise model of a *PLL*, with a generic noise being added at a single point just after the detector. This location is most suited to the analysis of the noise in a *PLL* used as a receiving system, yet represents the fundamental concepts of general noise analysis.

of lock and cycle slipping. This overview of noise will provide a basic knowledge of the noise effects in *PLL* systems, and further comments will be made in other sections.

A Simple Noise Model. The basic model typically adds a noise source in summation with the output of the phase detector as shown in Fig. 9. Both Gardner (5) and Blanchard (1) discuss the case of additive Gaussian noise at the model input. Rohde (4) adds substantial information on noise sources within the *PLL* itself. Manassewitsch (6) concentrates on the determination of noise bandwidth. Approaches to high-level noise are built around nonlinear system descriptions, often incorporating Monto Carlo techniques for analysis of the noise statistics and determination of the potential for loss of lock. We refer the reader to the classic papers by La Frieda and Lindsey (7) and by Viterbi (8) for details on high-level noise problems.

The level of noise in the model is determined by the translation of the input statistics due to the additive noise conversion in the detector process and by the noise figures of the remaining components in the loop, referenced to the detector output. We may typically treat the noise as a broadband noise voltage and simply evaluate the transfer of this noise to the appropriate point of the loop. This explanation is slightly oversimplified, but contains all of the basic analysis needs of the problem. If we consider the output point of interest to be the θ_0 at the output of the *VCO*, the appropriate transfer function is simply $H(s)/K_d$. Thus the noise properties are determined by the amplitude of the noise-source power density times the noise bandwidth. The latter is not necessarily the 3 dB bandwidth; is often found to be 1.5 times larger than the 3 dB bandwidth, and is obtained through integration of the transfer function.

A major source of noise is semiconductor junctions, which create partition and shot noise. Any resistive component in the loop is a source of wideband thermal noise proportional to kTB (k being Boltzmann's constant, 1.38×10^{-23} J/K; T being the absolute temperature, often taken as 290 K; and B being the bandwidth in hertz). Such thermal noise was mentioned in connection with the choice of the isolation resistor used with varactors. The spurious output of the detector may also be treated as noise, though by no means Gaussian. Other low-frequency noise results from active device flicker (a low-frequency noise particularly important in the phase detector, filter, and amplifier) and poorly chosen feedback levels in the *VCO*. Stability and microphonics (frequency variations due to mechanical vibrations of the *VCO* components) are also critical aspects of the *VCO*. People often forget that a *VCO* is mounted in a hostile environment where it may be subject to severe vibration, particularly in the 1000 Hz range for automobiles and aircraft. Such periodic noise can cause havoc through unwanted modulation on the *VCO* and is not corrected by the *PLL* for higher frequencies.

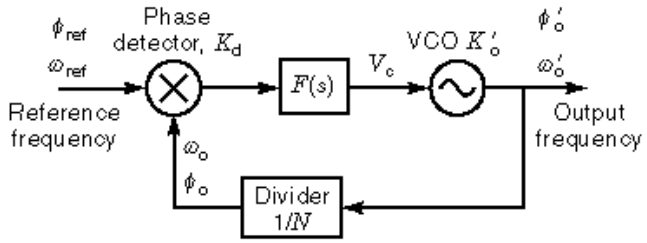

Fig. 10. *PLL* with a frequency divider in the feedback loop, forming a basic, divider-type frequency synthesizer.

All of these sources, as suggested, may typically be lumped together as a single source at the output of the detector and the noise analysis done by simply considering each of them as independent and feeding the system transfer function. Improvement in noise performance involves improving the noise filtering properties of the transfer function or reducing the noise contribution of individual components to the system. Though simple in concept, this noise reduction process is often tedious and is considered by many to be an art.

Though this noise discussion has been brief, it should point to the potential sources of noise and the fundamental analysis process for determining their contributions to the system noise. It is also wise to remind the reader that the uncorrelated noise power adds, not the noise voltage. Pure random noise has zero correlation with other noise sources. A few comments are offered on noise throughout the applications, but to only suggest the correct path to consider in design.

Applications of Phase-Locked Loops

The *PLL* has wide application. The majority of its applications fall into four main categories:

- Frequency synthesis
- Frequency (*FM*) and phase (*PM*) modulation and demodulation
- Data and carrier recovery
- Tracking filters

Frequency Synthesis. Frequency synthesis is one of the most widely used applications for *PLL*s. The local oscillators in most cell phones, land mobile radios, television sets, and broadcast radios are built around *PLL*s. Frequency-synthesizer integrated circuits are available from a number of manufacturers (3). The basic topology of the *PLL* frequency synthesizer is shown in Fig. 10.

The phase difference between a reference signal, ω_{ref}, and a divided sample of the output frequency, ω'_{o}, is measured at the phase detector. In a synthesizer, the signal frequency previously used is replaced by a frequency standard referred to as the reference signal. When phase lock is achieved, the output frequency from the divider must be equal to

$$\omega'_{\text{o}} = N\omega_{\text{ref}} \tag{35}$$

where N is the divider ratio and ω_{ref} is the reference frequency. The basic frequency synthesizer acts as a frequency multiplier. Since the phase comparison is done at the reference frequency, the effective *VCO* gain is

given by

$$K_o = \frac{K'_o}{N} \tag{36}$$

A synthesizer loop can be analyzed as a conventional loop where the *VCO* gain above is substituted into the calculations.

The value of N is often made programmable. N is an integer; so changing it has the effect of increasing or decreasing the output frequency, ω'_o, in steps that are a multiple of ω_{ref}. It is also important to recognize that changing the value of N has the effect of changing the loop dynamics. Since the *VCO* gain K_o is a function of N in a synthesizer, changing N will change the critical parameters ω_n and ζ in second-order loops and the phase margin in third and higher-order loops.

The value of N influences the loop transfer function $H(s)$. Consider the situation where $s = j\omega_m$ and ω_m is a modulating frequency:

$$\frac{N\phi_o}{N\phi_{ref}} = \frac{N\omega_o}{N\omega_{ref}} = \frac{\phi'_o}{N\phi_{ref}} = \frac{\omega'_o}{N\omega_{ref}} = H(j\omega_m)$$

or

$$\frac{N\phi_o}{\phi_{ref}} = \frac{\phi'_o}{\phi_{ref}} = \frac{N\omega_o}{\omega_{ref}} = \frac{\omega'_o}{\omega_{ref}} = NH(j\omega_m) \tag{37}$$

Any phase or frequency deviation on the reference is multiplied N times for the output by the synthesizer.

Figure 10 shows a simple synthesizer with a divider in the loop. It is also possible to put a mixer in the loop. This configuration is called an offset loop, and it is shown in Fig. 11. In order for the loop to be locked, the following must be true:

$$\frac{|\omega'_o \pm \omega_{offset}|}{N} = \omega_{ref}$$

or

$$\omega'_o = |N\omega_{ref} \pm \omega_{offset}| \tag{38}$$

The offset oscillator can operate either above or below the output oscillator frequency, and the filter can select either the sum or the difference of the two oscillator frequencies. In the case of the offset loop, the loop gain is unaffected by the frequency translation, expect for a possible phase inversion. The divider in Fig. 11 can be bypassed. In such a case N is set to one.

In most synthesizers, the reference frequency ω_{ref} must be significantly higher than the loop bandwidth. The reason for this requirement is that the output of most phase detectors is not a pure dc signal. The signal is pulses whose duty cycle and/or polarity are proportional to the phase difference. The loop filter not only sets loop dynamics, but it must reject the ac component of the phase-detector output, passing only the dc value to the *VCO*. The attenuation of the loop filter is finite, so some of the ac component does make its way to the *VCO*. The

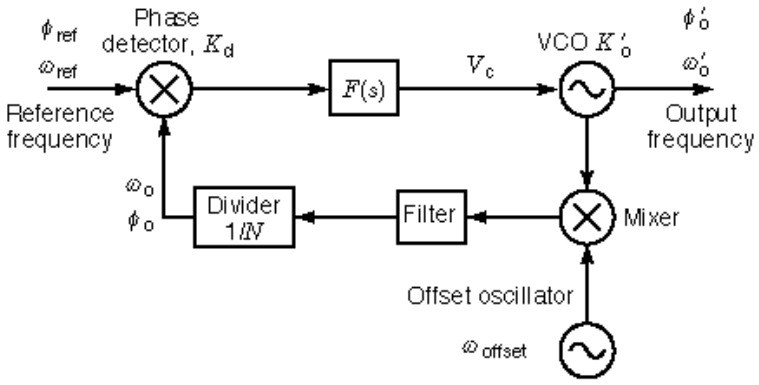

Fig. 11. Offset-loop frequency synthesizer. The offset oscillator is often used to lower the frequency requirements on the divider.

result is undesired phase modulation sidebands at the reference frequency on the output signal. Narrow-band loop filters provide better suppression of this reference feedthrough, but narrow-band filters exact a cost. Notch filters are also used to filter out the reference frequency components.

Consider this example: The channel spacing in the *FM* broadcast band is 200 kHz. A synthesizer with a reference frequency of 200 kHz will produce steps at the channel spacing. A second-order type-II synthesizer loop, $\zeta = 1$, $\omega_n = 2\pi$ (200 Hz), will settle in approximately 10 ms to within 100 Hz of its target frequency after a 200 kHz step. A similar loop with a reference frequency of 200 Hz will produce 200 Hz steps but, everything else being the same, will require that $\omega_n = 2\pi$ (0.2 Hz) to produce the same level of reference suppression. This loop will take almost 8 s to settle to the same accuracy after being commanded to change frequency by 200 kHz.

Most cell-phone, television, and broadcast radio receivers employ simple offset or divider-type synthesizers. For these applications, the required step size is usually much greater then the loop bandwidth required for the desired dynamics. In order to produce small steps and at the same time obtain acceptable reference suppression and settling time, it is often necessary to resort to multiloop synthesizers.

An example of a multiloop synthesizer is shown in Fig. 12. It was designed for an upconverting HF (0 to 30 MHz) in a communications receiver with a 75 MHz IF (4). This synthesizer will produce 10 Hz steps, but it is much more complex than a simple offset or divider-type synthesizer. Loop 1 in Fig. 12 is a simple divider-type synthesizer. It tunes from 50 MHz to 60 MHz in 1 kHz steps. The output of this loop is divided by 100, and the resulting 0.5 MHz to 0.6 MHz output changes by 10 Hz each time the divider in loop 1 is incremented or decremented by 1. Loop 2 is also a divider synthesizer, but it tunes from 75.5 MHz to 106.5 MHz in 100 kHz steps. Loop 3 is an offset loop without a divider. This loop forces the difference between the loop-3 *VCO* and the loop-2 *VCO* to be equal to the divided output of loop 1. Loop 1 can tune loop 3 over a 100 kHz range in 10 Hz steps, while loop 2 tunes loop 3 from 75 MHz to 105 MHz in 100 kHz steps. By proper choice of divider programming, it is possible to continuously tune the loop-3 *VCO* from 75 MHz to 105.1 MHz in 10 Hz steps.

The multiloop synthesizer in Fig. 12 employs a combination of divider and offset loops. Another technique, called fractional N, permits a synthesizer to produce steps smaller than the reference frequency. Details on fractional-N synthesizers can be found in Refs. 9 and 10. A particularly simple implementation of a fractional-N synthesizer can be found in Ref. 11.

The design of frequency synthesizers is often a careful balancing act that requires minimizing the lock time, the reference feedthrough, and the spurious outputs generated by mixing and dividing, while at the same

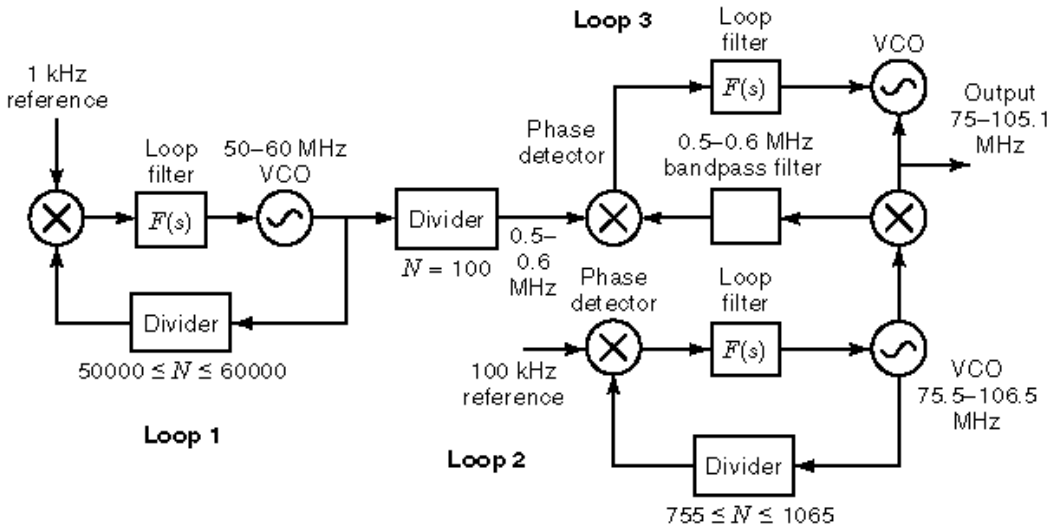

Fig. 12. This triple-loop frequency synthesizer of Rohde can tune from 75 MHz to 105.1 MHz in 10 Hz steps (4). Loop 1 is used to obtain a stable 10 Hz step interval for use in locking loop 3 to 10 Hz steps.

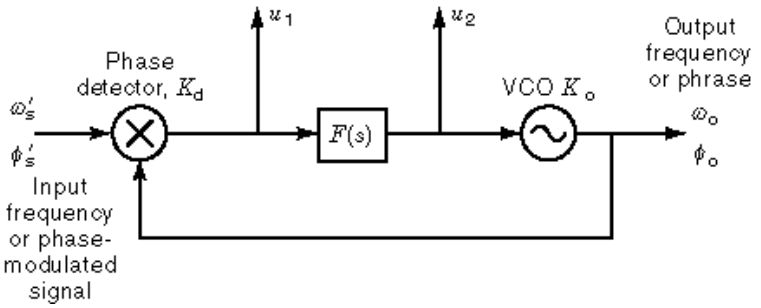

Fig. 13. *PLL* configured as a frequency or phase demodulator. The outputs at u_1 and u_2 offer tracking alternatives for demodulation, allowing output for frequencies both above and below the loop bandwidth.

time meeting power, size, frequency, and step-size requirements. The literature contains additional information on these design tradeoffs (4,9,10,12).

Modulation/Demodulation. A *PLL* can be used for phase or frequency modulation and demodulation. Before presenting the analysis, it maybe valuable to obtain an intuitive understanding of the modulation–demodulation process.

Figure 13 contains the block diagram of a *PLL* configured as a demodulator. If the modulating frequency ω_m is inside the loop bandwidth, the loop follows the phase and frequency of the incoming signal with little error. The phase (and thus the instantaneous frequency) of the *VCO* follows that of the input signal. The *VCO* control voltage u_2 must be an exact replica of the modulating voltage for this to be true. It is generally assumed that there is a linear relation between the control voltage and the *VCO* frequency. If the relation is nonlinear, the *VCO* will still track the input frequency, but the control voltage will be a distorted replica of the modulation voltage.

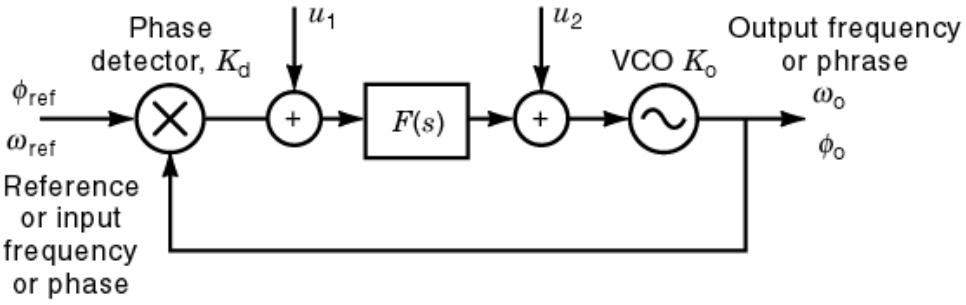

Fig. 14. *PLL* configured as a frequency/phase modulator. As in Fig. 13, this configurations offers alternative modulation inputs for modulation frequencies both above and below the loop bandwidth.

When the modulation frequency is outside the loop bandwidth, the *VCO* phase will no longer track the instantaneous input signal phase. The loop can only track the average frequency of the incoming signal. This causes the average *VCO* phase to remain constant. The instantaneous output voltage of the phase detector will be a function of the difference between the applied phase modulation and the average *VCO* phase. Thus, the phase-detector output voltage will be a replica of the source modulating voltage.

The output voltage for a *FM* demodulator is given by

$$u_2 = \frac{\Delta\omega_s(\omega_m)}{K_o} H(j\omega_m) \tag{39}$$

Here $\Delta\omega_s(\omega_m)$ is the frequency deviation of the input signal and ω_m is the modulating frequency. Recall that $H(j\omega_m) \approx 1$ for ω_m less than the loop bandwidth. For the phase demodulator, the output voltage can be obtained at u_1 as

$$u_1 = \Delta\phi_s(\omega_m)[1 - H(j\omega_m)]K_d = \Delta\phi_s(\omega_m)H_e(j\omega_m)K_d \tag{40}$$

where $\Delta\phi_s(\omega_m)$ is the phase deviation of the input signal. Note that

$$|1 - H(j\omega_m)| \approx 1 \qquad \text{for} \quad \omega_m > \text{(loop bandwith)}$$

The situation is reversed for the *PLL* modulator shown in Fig. 14. Here a modulating voltage is added to the loop. In the case of frequency modulation, the *VCO* control voltage is the sum of the voltage from the loop filter, $F(s)$, and the modulating voltage, u_2. If the modulating frequency is less than the loop bandwidth, the loop will interpret any change of frequency due to u_2 as an error and produce an equal and opposite correction voltage at the loop filter output. The result is no change in the output frequency. If, however, the modulating frequency is greater then the loop bandwidth, the loop can only follow the average frequency. The instantaneous frequency will be controlled by u_2, and frequency modulation will result.

Phase modulation can be generated by introducing the modulation voltage at u_1. When the modulating frequency is less than the loop bandwidth, the modulating voltage will cause a phase change at the *VCO*, which the loop will track. The *VCO* phase must be adjusted to produce a phase difference at the phase detector that cancels u_1. The *VCO* phase is now forced to track u_1; thus the *VCO* output is phase-modulated. Beyond the loop bandwidth, the loop can no longer track the error introduced by u_1 and no modulation will occur.

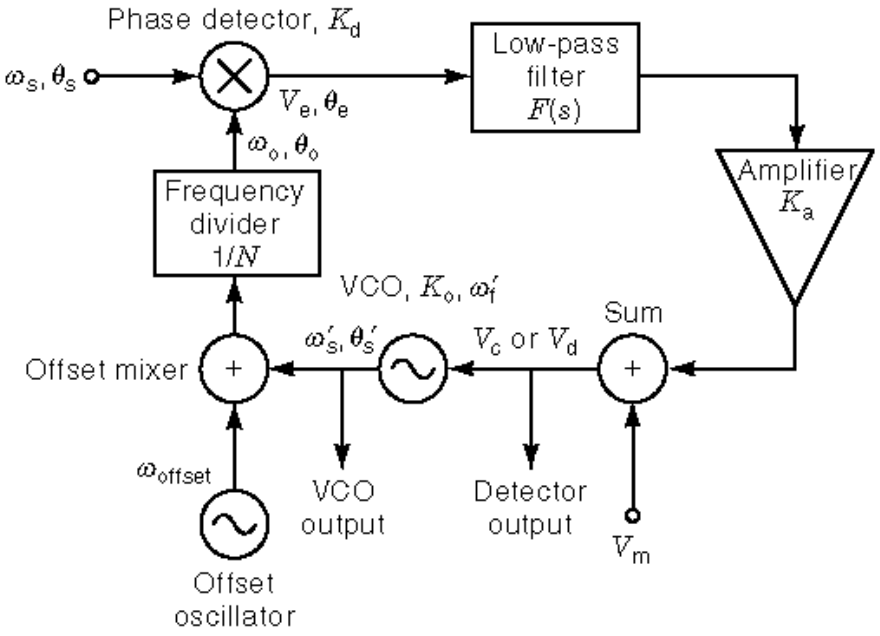

Fig. 15. Generic phase-locked loop with options. The options include frequency offset, frequency division, and modulation and demodulation terminals.

The output deviation of the *FM* modulator is given by

$$\Delta\omega_o(\omega_m) = u_2[1 - H(j\omega_m)]K_o \tag{41}$$

Here $\Delta\omega_o(\omega_m)$ is the frequency deviation of the input signal and f_m is the modulating frequency. We have

$$|1 - H(j\omega_m)| \approx 1 \quad \text{for} \quad \omega_m \quad > (\text{loop bandwidth})$$

For the phase modulator, the output phase deviation can be obtained by

$$\Delta\phi_o(\omega_m) = u_1[H(j\omega_m)]/K_d \tag{42}$$

where $\Delta\phi_o(\omega_m)$ is the phase deviation of the output signal and $H(j\omega_m) \approx 1$ for ω_m less than the loop bandwidth.

For *FM* the loop acts as a high-pass filter, and for *PM* the loop acts as a low-pass filter. Loop-bandwidth considerations driven by loop dynamics and reference suppression may prevent *FM* at low modulating frequencies or *PM* at high modulating frequencies. It is possible to overcome some of this limitation by applying the modulating voltage at both u_1 and u_2. Low-frequency *FM* can be generated by applying the modulating signal to u_2 in the conventional manner and applying an integrated version of the modulating voltage to u_1. Details of this process can be found in Ref. 2.

It is also possible to obtain low-frequency *FM* by modulating the reference. For frequencies less than the loop bandwidth the instantaneous phase and frequency are transferred to the output. This technique is used

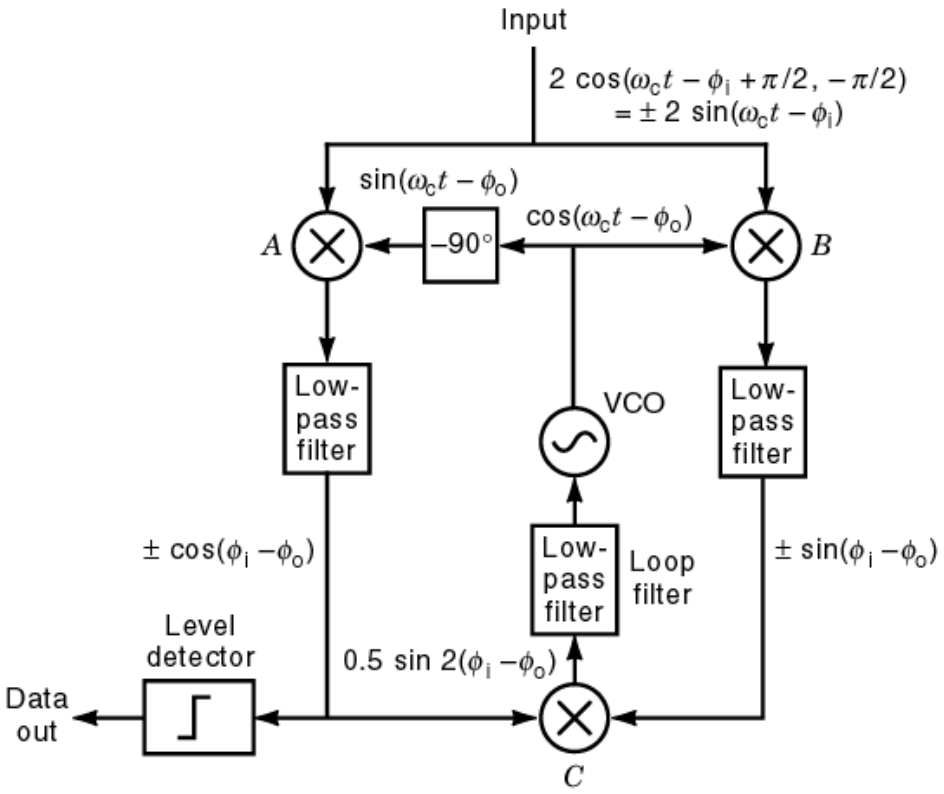

Fig. 16. The Costas loop for BPSK demodulation specifically locks to the carrier so that the modulation data may be recovered. In this role, it is a carrier recovery loop.

in land mobile and cellular phone transmitters in conjunction with divider-type synthesizers. The synthesizer acts as a multiplier, and a small amount of modulation applied to the reference is multiplied at the output.

All real oscillators are phase-modulated with noise. This noise modulation results from the finite-*Q* resonators in the oscillators and the inherent noise of the active devices used in oscillators. While a full noise analysis is beyond the scope of this article, combining the multiplier effect with the loop modulation response gives insight into the noise performance of synthesizers. A more complete analysis can be found in the literature (6,10,13).

Phase noise in oscillators is often described by a single-sided power spectral density L_ϕ. Below the loop bandwidth, the loop follows a multiplied replica of the noise on the reference signal. The phase noise on the *VCO* is suppressed, as the *VCO* phase is forced to follow the reference phase. Beyond the loop bandwidth, the *VCO* phase no longer follows the reference phase, the error between the *VCO* and the reference increases, and the noise output becomes the noise of the *VCO*. This effect can be expressed by

$$L_{\phi\,\mathrm{out}} = N^2|H(j\omega_\mathrm{m})|^2 L_{\phi\,\mathrm{ref}} + |1 - H(j\omega_\mathrm{m})|^2 L_{\phi\,\mathrm{VCO}} \qquad (43)$$

A careful choice of loop bandwidth can minimize the total noise output. An example of this can be seen in many microwave synthesizers. Well-designed microwave oscillators such as YIG oscillators have very low phase noise at large offsets ω_m from the center frequency, but close to the center frequency their phase noise

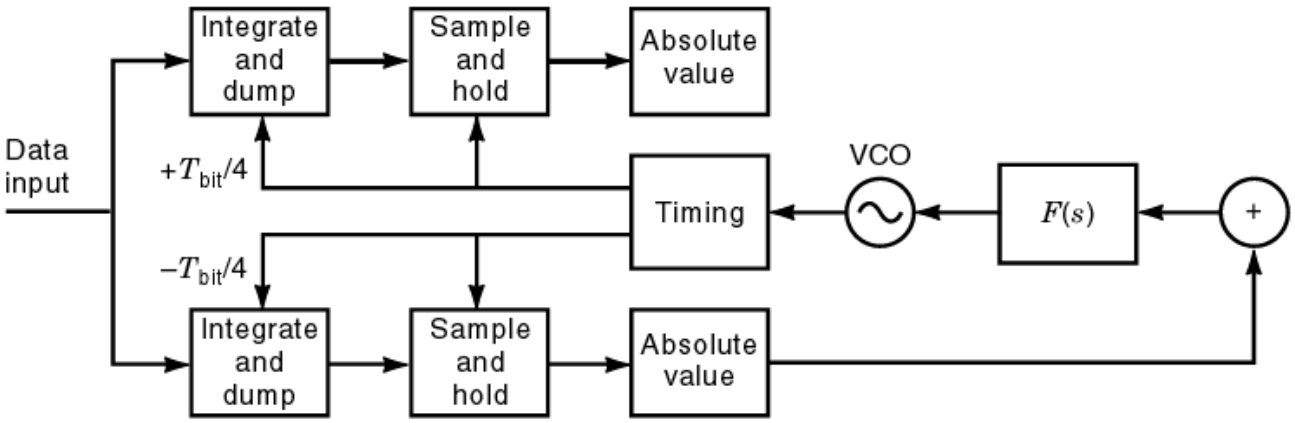

Fig. 17. Early–late data synchronizer that offers the ability to synchronize with a data stream in order to have reliable recovery of the data stream in a sampled detection system.

is relatively high. Crystal oscillators multiplied into the microwave region, on the other hand, have very low noise close to the center frequency, but the multiplication process tends to bring up the noise far removed from the center frequency. The loop bandwidth can be chosen so the crystal-oscillator noise dominates close to the center and the microwave oscillator noise dominates at large offsets from the center frequency. Such a loop is referred to as a *cleanup* loop.

Data and Carrier Phase Recovery. Synchronization is probably one of the oldest applications for the *PLL*. The timing and phase synchronization of 60 Hz power generating plants can be analyzed as a kind of *PLL*. Television, and particularly color TV, would not be possible without *PLL*s to extract timing and phase information from the TV signal. The growth of digital systems that employ various types of phase and phase-difference modulation has brought renewed interest in *PLL*s to extract phase and timing information from a data stream.

An example of a carrier phase recovery loop is the Costas loop. A Costas loop is shown in Fig. 16. The Costas loop can coherently demodulate binary phase-shift keying (*BPSK*) signals. With a BPSK signal, a phase shift of $-\pi/2$ or $\pi/2$ rad represents a data 0 or 1.

The input to the loop is $2\cos(\omega_c + \phi_i \pm \pi/2) = \pm 2\sin(\omega_c + \phi_i)$, where ω_c is the carrier frequency and ϕ_i is the carrier phase. The $\pm \pi/2$ represents the data modulation. The input is equally split and multiplied by the quadrature of a locally generated carrier, $\cos(\omega_c t + \phi_o)$, in multipliers A and B. The low-pass filters extract the difference signals from the product. The result is a quadrature of the phase difference between the locally generated carrier and the incoming signal, $\pm\cos(\phi_i - \phi_o)$ and $\pm\sin(\phi_i - \phi_o)$. These quadrature outputs are multiplied together in multiplier C. The result is a doubling of the quadrature component arguments as $0.5\sin[2(\phi_i - \phi_o)]$. The modulation disappears, and the resulting phase difference between the input and the output is used to steer the *VCO*. While this example is for simple BPSK, it is possible to design similar loops for N-phase modulation (5).

Another data synchronizer is the early–late gate (5). The circuit works well for rectangular pulses. Figure 17 contains a block diagram of an early–late gate synchronizer. Figure 18 shows the timing.

Integration from $+T_{bit}/4$ to the data transition is controlled by the late timing. This integration will produce an equal and opposite value for the integration controlled by the early timing from $-T_{bit}/4$ to the data transition only if the data transition occurs halfway between $+T_{bit}/4$ and $-T_{bit}/4$. The *VCO* is steered to this point by the difference of the absolute values of the integration products.

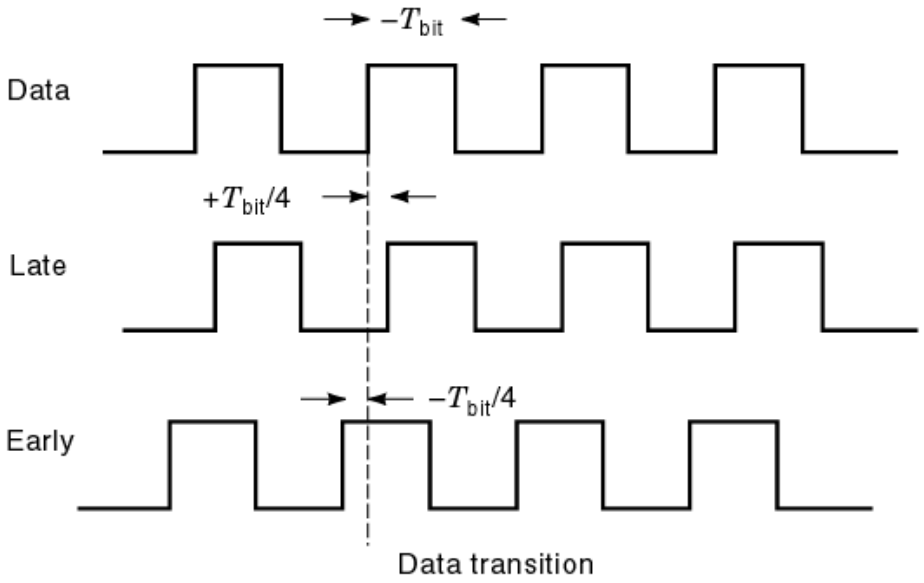

Fig. 18. Early–late data synchronizer timing, showing the balance of the early and late pulses used to center the data stream.

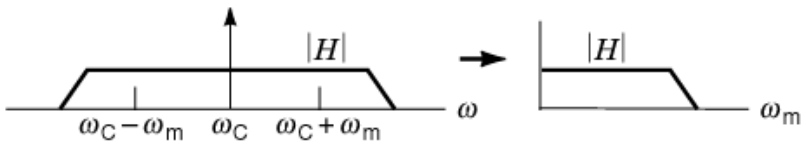

Fig. 19. Bandpass and low-pass representation of a *PLL*, emphasizing the relationship between the transmitted signal and the baseband representation of the signal used for detection.

Tracking Filters. Tracking filters are another early application for the *PLL*. The early space program used *PLL* receivers to track weak satellite signals that were accompanied by changing Doppler shift.

The loop transfer function, $H(j\omega_m)$, is almost always represented by its baseband representation, but phase measurement is actually accomplished at some carrier frequency. The loop appears as a bandpass filter centered at ω_c with bandwidth twice that of $H(j\omega_m)$. See Fig. 19. The unique property of this filter is that it can track ω_c as it changes. A signal with large frequency excursions can be passed through a filter that would be otherwise too narrow to accommodate the frequency changes by using *PLL* tracking-filter technology.

Since it is desired to follow Doppler-shifted signals or signals that change frequency, loop dynamics are an important consideration. The loop dynamics are related to the loop order and loop type. Loop type is determined by the number of poles at zero in the open-loop transfer function. Table 1 shows the dynamic behavior of various loops. The table shows the loop phase error after the loop reaches steady state following a phase step, a frequency step, or a frequency ramp. The frequency ramp can be used to describe the loop's performance in tracking a satellite signal as the satellite passed from horizon to horizon.

Table 1. Loop Error for a Step Change in Phase ϕ, a Phase Ramp or Frequency Step, and a Frequency Ramp as Time Goes to Infinity

Order	Filter Type	Phase Loop Type	Phase Step	Ramp or Freq. Step	Freq. Ramp
1st	None	None	Zero	Constant	∞
2nd	Lag	I	Zero	Constant	∞
	Lag–lead	I	Zero	Constant	∞
	Integrator with lead	II	Zero	Zero	Constant
3rd	Integrator with lead	II	Zero	Zero	Zero

Conclusions

This article has provided the fundamentals of *PLL* analysis and several examples to illustrate typical applications. There are many extensions that may be made to a *PLL* for a particular application. The emphasis of this article has been to highlight the process of the analysis and operation so that such extensions are easily handled. The examples of frequency synthesis, frequency and phase modulation and demodulation, data and carrier recovery, and tracking filters have provided extensions to suggest the variety of configurations that may be considered. In all cases, the extensions may be brought back to the form of the basic *PLL* for analysis, giving the reader the fundamental tools needed to design effective phase-locked systems.

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