MULTIPLIERS, ANALOG

The multiplication of continuous-time continuous-amplitude analog signals has been of fundamental importance since the earliest days of electronic systems, notably in computing and nonlinear control systems, modulation, correlation, the determination of signal power, variable-gain amplifiers, and other signal management functions. Many ingenious multiplier methods have been devised during the past fifty years, most of which have fallen into obsolescence (1,2).

In contemporary electronics, two-variable analog multiplication, and the closely related function of division, are invariably implemented by inexpensive monolithic integrated circuits whenever cost, low power consumption, small size, accuracy, and high speed are essential requirements. By far the largest proportion of current commercial products utilize bipolar junction transistor (BJT) technologies and invoke *translinear* principles (3), providing dependable, accurate, complete solutions that are easy to use. When optimized for accuracy, using special circuit techniques and laser trimming, static errors may be $\pm 0.05\%$ full scale (FS) or better, with nonlinearity errors (deviation from the ideal function) as low as $\pm 0.01\%$. Translinear multipliers may also be optimized for very high speed, which can extend up to the limits of the technology; a 3 dB bandwidth of over 30 GHz is nowadays possible in special applications such as wideband variable-gain cells.

In principle, monolithic multipliers can provide both very high static accuracy and very high bandwidth in a single device, but such a need is rare, and products providing this capability are not generally available. A typical *integrated circuit* (IC) *four-quadrant* multiplier (one that generates the true algebraic product for inputs of either polarity) usually provides a compromise solution, with accuracy–bandwidth combinations of the order of 0.1% and 10 MHz (found, for example, in the Analog Devices AD734), or 3% and 1 GHz (AD834).

Analog multiplier techniques are widely used in gain-control applications. *Two-quadrant* multipliers often serve this function, with careful optimization to meet difficult and conflicting performance objectives. Occasionally, dual-channel operation is provided, as in the 60 MHz AD539. The *voltage-controlled amplifier* (VCA) function is often better addressed by a different class of circuits, particularly those that provide an exponential relationship between the control variable and the resulting gain, thus providing a *linear-in-dB* control law.

Other multiplier applications require a response only to inputs of one polarity. These are called *one-quadrant* multipliers. Many of the cells proposed in contemporary research papers are in this class and need considerable elaboration with auxiliary circuitry to permit operation in two or four quadrants. The careful choice and optimization of the *root structure* is therefore of critical importance, and a few solutions have gained preeminence.

A *mixer* is sometimes regarded as an analog multiplier, optimized by close attention to noise and intermodulation for use in frequency-translation applications. While this view is useful in thinking about the basic *function,* mixer *designs* differ markedly. For example, the response to one of its two inputs (the signal at the local oscillator port) desirably approximates a binary (switching) function, and the mixer ideally performs only the sign-reversal (or phase-alternation) function on the other input (the *carrier*). This can also be viewed as the multiplication of the analog input signal by all the terms in the Fourier expansion of a square wave.

While the time-domain and amplitude-domain behavior of analog multipliers are usually of greatest interest, mixers are more often assessed by their performance in the frequency and power domain, with a strong emphasis on two dominant imperatives: the minimization of spurious intermodulation terms, and the minimization of noise. Thus, from a practical perspective, it is unwise to view mixers in the same terms as analog multipliers. The term *modulator* is often used, though modulators (and demodulators) may be fully linear multipliers.

Multiplication of two *binary* variables is implemented by the exclusive-OR logic function, and this operation is at the heart of a modern digital multiplier–accumulator cell. With the advent of inexpensive analog-to-digital and digital-to-analog converters and the microprocessor, many applications formerly solved in the analog domain have migrated to digital implementations. The benefits include greater stability, reconfigurability and increased flexibility, and easy integration into a software-governed hierarchy. Modern *digital signal processing* (DSP), using specialized very large scale integration (VLSI) multiplication algorithms, has taken this trend a step further. However, the time quantization of DSP approaches precludes operation at high speeds.

MULTIPLIER BASICS

An ideal multiplier generates the product of two time-varying input variables (rarely more), historically identified as X and Y. In most practical multipliers, the inputs and output (here labeled W) are voltages. Occasionally the *exterior* variables are in the form of currents; however, the *interior* variables are very often in this form. The function is described by the equation

$$V_W = \frac{V_X}{V_U} V_Y \tag{1}$$

where V_W is the output, V_X and V_Y are the two inputs, and V_U will here be called the *scaling voltage.* V_U is of critical importance in establishing the accuracy of the function. Equation (1) is written in a way which emphasizes that V_X is the variable whose voltage range is determined by V_U. A more useful multiplier structure allows the addition of a further variable, V_Z, to the output:

$$V_W = \frac{V_X}{V_U} V_Y + V_Z \tag{2}$$

V_U may also be varied from an input interface in some IC multipliers. Thus, in its most general implementation, Eq. (2) describes a versatile *multiplier–divider–adder* element. Its practical value depends on the speed and accuracy with which it implements this function, the noise levels at input and output, the harmonic distortion under various drive conditions, and detailed practical issues such as the impedance at its interfaces (often differential), its ability to drive a load, the supply voltage and current-consumption requirements, its size, its cost, and the like.

A basic consideration relates to the number of quadrants in which a multiplier can operate (Fig. 1). Some multipliers provide operation in only *one quadrant,* that is, all variables are unipolar. These are useful in specialized embedded analog computing applications; for example, in certain temperature-compensation applications (4), a unipolar output $V_C'(T)$ must be proportional to absolute temperature (PTAT) as well as to the primary controlling variable V_C, which is independent of temperature:

$$(+)V_C'(T) = \frac{(+)V_C}{(+)V_R} V_0 \frac{T}{T_0} \tag{3}$$

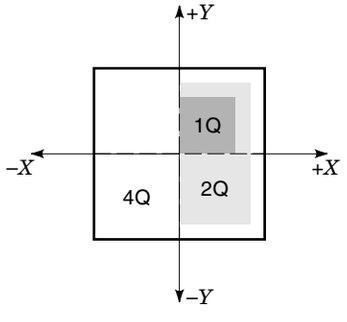

Figure 1. Multiplier operating quadrants.

where V_R is a reference voltage that scales the controlling (input) function while V_0 is a second reference voltage that scales the output, T is the system temperature, and T_0 is a reference temperature, often taken as 300 K (≈27°C). The robust design of all nonlinear analog circuits is characterized by the need for careful consideration of such detailed scaling attributes.

In a *two-quadrant* multiplier, commonly used in gain-control applications, one of the two inputs is unipolar, that is, constrained to a single polarity, while the other input and the output are bipolar, as is the case for a VCA. This functional restriction does not represent a concession to structural complexity, but rather has as its objective the improvement of performance in gain-control applications.

In a *four-quadrant* multiplier, the sign of V_W is algebraically correct for all sign combinations of V_X and V_Y, that is, for the quadrants $(+ \times +)$, $(+ \times -)$, $(- \times +)$, and $(- \times -)$. This may appear to be the most versatile case and could be used in any application, but in practice it will not perform optimally in all of them. For example, a two-quadrant multiplier, used as a VCA, can provide output-referred noise and distortion that is proportional to the magnitude of the unipolar input, while in a four-quadrant type these remain almost constant for a given magnitude of input on the bipolar (signal) channel.

Equation (1) indicated that the input V_X is associated with a divisor V_U, and the full-scale value of V_X will be determined by this denominator. When V_U is arranged to be controllable from an interface, *analog division* is implemented. In some practical IC products, the range of allowable values for V_U may be quite large. For example, the AD734 provides a 1000 : 1 range (+10 mV to +10 V) at its high-impedance V_U interface. As a fixed-scale multiplier a high-precision reference voltage, generated by a buried zener, laser-trimmed to 0.01%, provides V_U. As well as its utility in contemporary analog computing applications, where the value lies in the measurement of a *ratio* of voltages over a wide range of absolute values, the division function may also be used in gain-control applications, where V_X represents the signal and V_U is the (one-quadrant) gain-control voltage, providing a gain range of over 60 dB.

Many monolithic multipliers use a *differential cell topology,* and can process differential signals at their X and Y interfaces, with high common-mode rejection. These versatile devices add features normally only found in instrumentation (differencing) amplifiers, by implementing the even more general function

$$V_W = \frac{V_{X1} - V_{X2}}{V_U}(V_{Y1} - V_{Y2}) + V_Z \tag{4}$$

In the most versatile IC dividers, the V_U input interface would also be differential, and allow this voltage to change sign (that is, support *four-quadrant division*). Because of its limited utility and the basic problem of the singularity at $V_U = 0$, this capability is generally not provided in commercial products. However, the function is practicable, and a method will later be shown for its implementation and use in *filterless demodulation.*

During the 1970s and 1980s, the supply voltages for analog multipliers invariably were ±15 V, the voltage ranges for V_X, V_Y and V_W were ±10 V FS, and V_U was 10 V. During recent years, supply voltages have dropped, first to ±5 V, heralding

FS input and output voltages of typically ±2 V (with a V_U of 1 V to 2 V) and more recently to single supplies of either +5 V or +3 V, necessitating some modification in the approach to full four-quadrant operation, for example, by providing a differential output as well as differential inputs. *Current-mode interfaces* for the signals are sometimes used to cope with these limitations.

Contemporary analog multiplier developments are moving away from generic, textbook objectives toward system-specific embodiments, with increasing emphasis on extending the high-frequency accuracy, lowering spurious nonlinearities, and reducing noise levels. The development of high-performance analog multipliers remains a specialized art; only a few IC companies have the skills to cope with the numerous arcane design details. Cell developments being reported in the professional journals, particularly those promoting the use of complementary metal–oxide–semiconductor (CMOS) technologies, are often not fully in touch with the imperatives of modern systems and their challenging requirements.

MULTIPLIER ERRORS

The absolute accuracy of analog multipliers has traditionally been defined in terms of the error between the actual and ideal output relative to the FS value of the output. This is invariably a more optimistic metric than the error specified in terms of the actual output. Further, it is common practice to emphasize the static accuracy, obtained under dc or low-frequency conditions. The dynamic errors at realistic operating frequencies are then layered over the static specifications, using similar metrics to those for linear amplifiers, such as 3 dB bandwidth, rise and fall times, slew rate, etc. These practices came about largely because of the context within which high-accuracy multipliers were historically developed: in analog simulators, in military applications, and in industrial plant control and various types of instrumentation, prior to the advent of the microprocessor. The FS static accuracy remains a key parameter in defining the performance of a multiplier.

The most accurate monolithic multipliers—using translinear techniques and high-performance *complementary bipolar* (CB) processes with *silicon-on-insulator* (SOI) fabrication, temperature-stable thin-film resistors, and laser trimming for precise calibration against NBS-traceable standards—achieve a guaranteed absolute accuracy of ±0.1% FS, with −80 dBc harmonic distortion. Selected components can maintain a short-term accuracy of ±0.02% FS, which is practically the state of the art in analog multiplication, using any known technique.

Errors arise from many mechanisms, and are of several types. Some, such as the linear errors, can usually be attributed to component mismatches; nonlinear errors can be caused by mismatches in device size and in current density; dynamic errors are due to the finite response time of these devices and to parasitic signal coupling across them. While these may be captured in mathematical expressions, little insight is gained from such, and they become particularly enigmatic when the modeling of all of the nonlinear and dynamic effects is attempted. A more useful approach is to consider the linear, nonlinear, and dynamic errors separately.

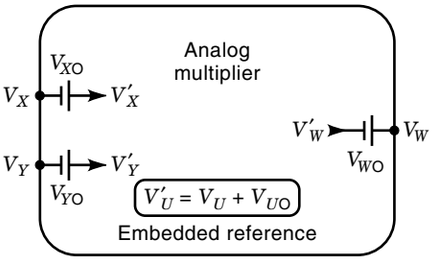

Figure 2. Linear error sources in a multiplier.

LINEAR ERROR SOURCES

There are four linear error sources in an analog multiplier, identified in Fig. 2. First is the uncertainty, V_{UO}, in the scaling voltage V_U, equivalent to a *gain* error. Contemporary monolithic multipliers often use a bandgap reference to provide V_U. Without trimming, these can achieve an absolute accuracy of ±2% and a temperature coefficient of $\pm 50 \times 10^{-6}$/°C. Using trimming, the initial and long-term accuracy may be as high as ±0.1% or better, with a temperature coefficient of under $\pm 5 \times 10^{-6}$/°C. For higher accuracies, some type of breakdown device is used; their use is limited to applications in which at least one supply voltage is available that exceeds the breakdown voltage of the reference element (about 8 V). Monolithic circuits may use a *buried-zener* reference, whose voltage can be adjusted to within ±0.01% using laser-wafer trimming in high-volume production, with commensurate temperature stability and long-term stability.

The second linear error is the dc offset at the *output* of the multiplier, V_{WO}. Consider a multiplier having V_U = 10 V and full-scale X and Y inputs of 10 V. When both inputs are 1 V (that is, 10% of FS), the output should be 100 mV. While an output offset of V_{UO} = 10 mV is only 0.1% of the FS output, it is 10% of the actual output. Some applications of multipliers are severely affected by this output-referred dc error. However, in a VCA, where the output will invariably be ac-coupled, this offset is inconsequential. In considering the specifications of a multiplier, one must pay careful attention to all of the many detailed requirements of each specific application.

The two remaining linear errors are those due to the input offsets, V_{XO} and V_{YO}. An input applied to one of the two inputs will generate a spurious output when the second input is nominally zero. Thus, if a 10 V sinusoid is applied to the X input, and the Y input is set to zero but exhibits an internal offset of V_{YO} = 10 mV, there will be a residual sine output of amplitude 10 mV when V_U = 10 V. This is called *static feedthrough* and is commonly specified either in fractional or decibel terms. In the above case, the feedthrough of 10 mV is 0.1%, or 60 dB below the potential full-scale output of 10 V. It is important, however, to make a distinction between the feedthrough due to dc offsets and that due to parasitic signal coupling at actual operating frequencies. Residual nonlinearities in the multiplier may also cause signal feedthrough.

NONLINEAR ERRORS

When all linear errors have been eliminated by exact calibration of the scaling voltage V_U and by nulling the offsets associ-

ated with V_X, V_Y, and V_W, some errors will remain. These may be called irreducible errors, to the extent that they are difficult for the user to eliminate in most practical applications. However, there are many ways by which these may be lowered in a production context, using careful design and IC layout techniques, laser trimming, and special packaging. They are sometimes addressed using a multiplexed analog-to-digital converter (ADC) for V_X and V_Y, followed by digital multiplication in a microprocessor and digital-to-analog conversion back to the voltage domain, in which case the residual nonlinearities will usually be less than a least-significant bit (LSB). This approach is appealing for low-frequency instrumentation-grade multiplication, but not in applications where bandwidth, power consumption, size, and cost are dominant considerations.

The IC multiplication method most widely used today is based on the *translinear principle,* and the following comments regarding residual nonlinear errors are with this implementation in mind. It is found that, for the commonly used two- and four-quadrant types, one error is essentially quadratic in form, while another is essentially cubic. Quadratic errors can be largely traced to V_{BE} matching errors in the core of the four-quadrant multiplier. Cubic errors arise due to mismatches in current density and are minimized by the optimal choice of topology, device sizes, and bias conditions. High-volume production experience over a period of more than two decades shows that residual nonlinearities of under 0.1% of FS can be routinely achieved without trimming.

Since an analog multiplier has two independent inputs, the output and the error generate *surfaces,* formally requiring three-dimensional representation. Here again, no special insights are gained by using such in examining the behavior of a multiplier. Instead, an excellent practical assessment of static accuracy is provided by a *crossplot* (5). The term arose in a testing context, in which a multiplier of unknown quality was compared with one of impeccable credentials.

In the classical crossplot technique (Fig. 3), both multipliers are excited by the same inputs (whose precise calibration is unimportant), and the difference in the outputs of the two units—that is, the error relative to the internal calibration

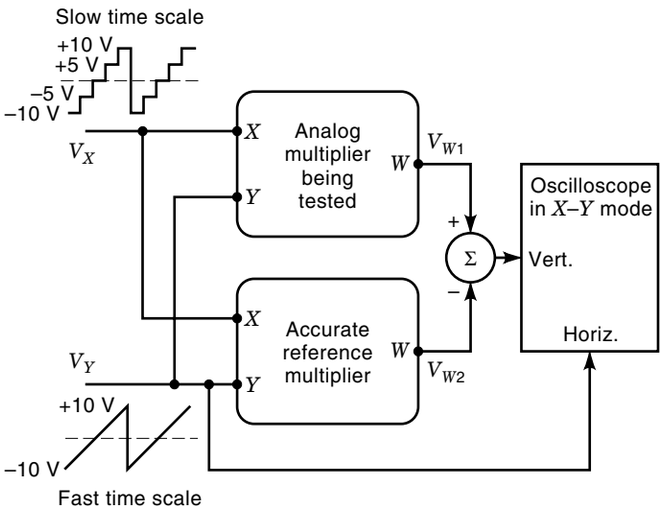

Figure 3. Typical crossplot measurement technique.

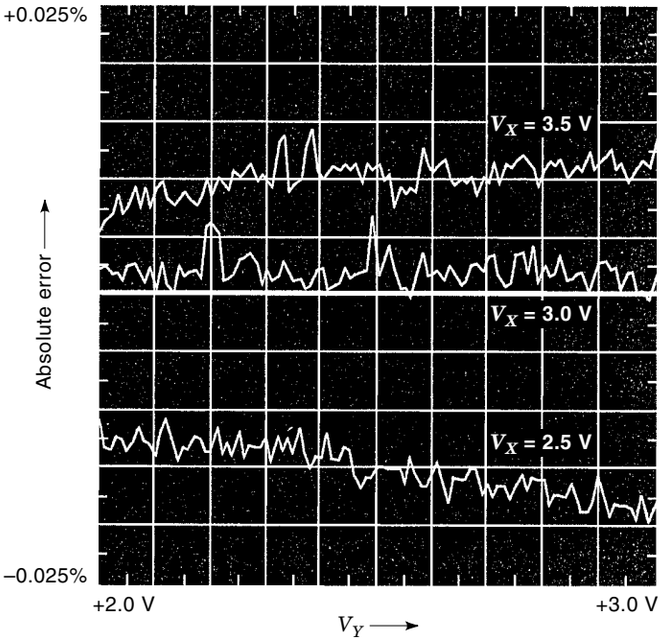

Figure 4. Typical multiplier crossplot.

of the reference multiplier—is displayed on an oscilloscope, generating an insight-rich real-time display. Using a high vertical sensitivity, errors as small as 0.01% of FS are readily visible. One of the two inputs is swept linearly over its full range; this input also provides the horizontal sweep voltage for the oscilloscope. The other input is stepped through several spot values (typically −100%, −50%, zero, +50% and +100% of FS) by automatically incrementing one step for each sweep of the first input. The sweep times are chosen to ensure a flicker-free display, but not much faster, since dynamic errors quickly become dominant, even in a 1 MHz bandwidth multiplier. The X and Y inputs can then be swapped for a different view of the errors. Insight into interpreting the multiplier errors displayed in a crossplot can be acquired rapidly after a little practice.

In contemporary production practice, when multipliers of the highest accuracy are to be characterized, the input voltages are generated by computer-programmable sources traceable to NBS standards, and the output is measured by a high-grade digital voltmeter. The error is then calculated in the host computer, which may generate a crossplot as a graphical entity. Figure 4 shows a typical result for a state-of-the-art laser-trimmed multiplier; the peak error is seen to be within ±0.02% over the range of X and Y input values (6).

DYNAMIC ERRORS

The errors discussed so far relate to slowly varying inputs. Dynamic errors arise when the inputs are varying rapidly and may be generated in the input interfaces of the multiplier, in the core, or in the output stage. Since multipliers may exhibit different response times on the X and Y input channels (that is, different phase angles), their dynamic errors need to be measured separately. When a high degree of phase matching is required in the response from the X and Y inputs, two mul-

tipliers can be used (either in cell form or as complete ICs) with their two pairs of input interfaces cross-connected and their outputs summed. The key dynamic property of a multiplier is its *small-signal bandwidth,* the frequency at which the output amplitude is 3 dB below its midband value. The measurement should be made with one of the input channels receiving the ac test signal, while the other receives a fixed dc level. For modern commercial IC multipliers, values range from 1 MHz to 1 GHz, but operation of bipolar multiplier cells at 13 GHz (7) and 32.7 GHz (8) is currently feasible in automatic gain control (AGC) applications.

The individual bandwidths of the input circuits, the multiplying core, and the output stage are often different, and design optimization depends on the requirements. Consider a signal-squaring application being implemented by a four-quadrant multiplier, with the two input channels connected in parallel and sinusoidally excited. This generates an output from the multiplier core at twice the input frequency, plus a dc component. To extract the ac component, as in a frequency doubler, the output bandwidth must be at least twice that of the input frequency; however, if we wish to determine the mean squared value, as in a power measurement application, the output bandwidth must be much lower, requiring a post-multiplication low-pass filter to perform averaging.

It is often found that the ac response from one of the two multiplier inputs depends in some complex way on the dc value of the other input, due to another type of dynamic error, namely, high-frequency (HF) feedthrough. This occurs when the effective gain of a multiplier is low, and results in the ac output being (usually) larger than the dc gain value would predict. Two-quadrant multipliers may show this problem more noticeably, because they are sometimes designed to provide a very high gain-control range (as much as 80 dB) and will therefore be operating in an *attenuation* mode for much of this range. Even minute parasitic capacitances can lead to large feedthrough errors at, say, 100 MHz and above. The solution lies in the use of special cell topologies for HF multiplication.

The notion of *vector error* arose in computing applications. This is only another way of describing errors due to the finite bandwidth of the device, but taking phase lag into account. In a system characterized by a single-pole response, a dynamic error of 1% will occur at a frequency of 1% of the −3 dB bandwidth, and is closely proportional below this frequency. Thus, a multiplier having a 10 MHz bandwidth exhibits a 0.1% vector error at 10 kHz, while the output *magnitude* is in error by only −0.005%. Practical wideband multipliers rarely conform to a simple one-pole response, however, and this metric is not often invoked in contemporary applications of multipliers.

In multipliers based on pulse-averaging methods, there is a residual periodic ripple on the output, and vector errors are large, due to the use of multipole filters. Further types of dynamic error will be found in multipliers implemented using hybrid analog–digital techniques, due to time quantization. Slew-rate (dV/dt) limitations generate dynamic errors under large-signal conditions, and increase settling time. Overload-recovery effects may also arise: a well-designed multiplier will not "fold over" when the inputs greatly exceed the nominal FS value, and will recover quickly when the overdrive condition is removed.

Finally, multiplier noise needs consideration. This is usually specified in terms of the output noise spectral density (so many $nV/Hz^{1/2}$). In translinear multipliers, the dominant wideband noise source is the core: because of the high effective gain to the output, multiplier noise will invariably be much higher than in typical IC amplifiers. In multipliers using MOS technologies, there is a significant increase at low frequencies, due to $1/f$ mechanisms. In a multiplier used for gain-control purposes, this may cause *modulation noise.*

HISTORICAL TECHNIQUES

The earliest analog multipliers were electromechanical (1). In a *servomultiplier* (Fig. 5) one of the two inputs, V_X, determined the relative angular position X of a shaft. A first potentiometer, P_1, on this shaft, biased by a dc voltage, which can be equated to the denominator voltage V_U in Eq. (1), generated the voltage $V_X = XV_U$. Thus, the shaft angle X was proportional to V_X/V_U. A second potentiometer, P_2, whose excitation was provided by V_Y, generated the output $(V_X/V_U)V_Y$. The static accuracy was determined by V_U and the matching of the X and Y potentiometers. The response time to the X input, typically 100 ms to 1 s, was determined by the inertia of the mechanical system. The response bandwidth of the Y input was limited by the ac behavior of the potentiometers (which were often wire-wound resistance elements, and thus very inductive) and associated circuitry; it extended to at most a few megahertz.

Mechanical servomultipliers are essentially obsolete, but in 1975 Gilbert (9) described a novel solid-state realization, in which the position of a rotating shaft was mimicked by the angular position of a *carrier domain,* a narrow region of highly localized minority carrier injection from a semicircular emitter of a bipolar semiconductor structure. The track of the mechanical potentiometer was replaced by the resistive collector region. Smith described a second-generation rotational design (10). In more recent BiCMOS embodiments of this principle the domain moves linearly, in a long, narrow n-type emitter, in response to the X input. Its position $0 < X < L_E$ is precisely determined by a parabolic voltage profile induced in the p-type base-region, which also serves as a resistor and as the drain of the superintegrated PMOS devices, as shown in

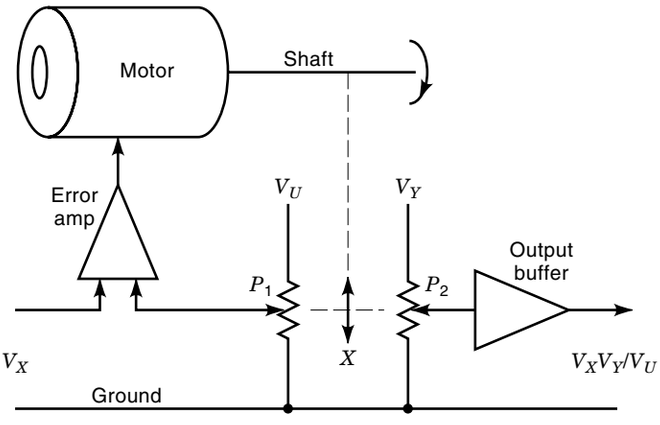

Figure 5. Electromechanical servomultiplier.

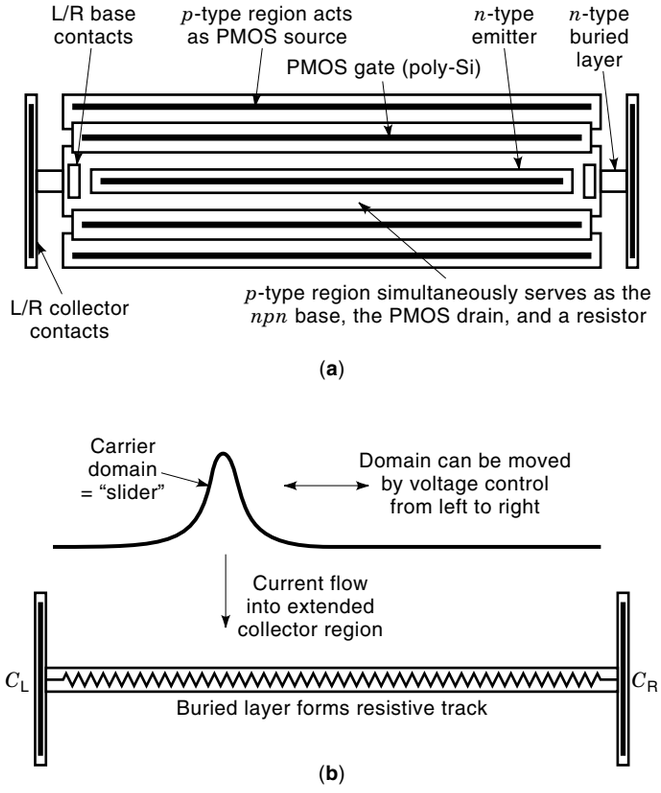

Figure 6. Solid-state servomultiplier: (a) upper regions; (b) detail of subcollector.

Fig. 6(a). An *n*-type buried-collector layer beneath the emitter corresponds to the track of the output potentiometer. The domain, whose current magnitude is controlled by the *Y* input, is analogous to the slider; Fig. 6(b) shows just the collector region.

Two domains may readily be integrated into a single device to realize a four-quadrant multiplier. The response time to the position-controlling *X* input is typically nanoseconds; the *Y* input is even faster, since the extended *npn* transistor behaves essentially as a grounded-base stage. While the performance of these carrier-domain multipliers is excellent, the use of superintegrated structures is deprecated in a commercial context, since they are not amenable to standard modeling and simulation techniques.

With the increased need for speed in analog computers during the mid-1940s, electromechanical multipliers were replaced by vacuum tube circuits. A popular technique of this time was based on cells that generated a square-law function, used in conjunction with summing and differencing circuits to implement a quarter-square multiplier (5), so named because of the algebraic identity

$$XY = \tfrac{1}{4}[(X+Y)^2 - (X-Y)^2] \tag{5}$$

A generic implementation is shown in Fig. 7. The squaring circuits are here presumed to be transconductance (g_m) elements and able to handle *X* and *Y* inputs of either polarity (although in practice it is often necessary to include an absolute-value circuit to allow the use of single-quadrant squarers). The effective value of V_U is determined by these g_m's, the load resistors R_L, and *A*, the voltage gain of the buffer amplifier. Note that the squaring function implies an embedded voltage reference V_R, a fundamental requirement, since the basic scaling demands of Eq. (1) must be met. The source of this voltage, which dominates the accuracy, is not always made clear in some descriptions of circuit operation.

MOS transistors are said to exhibit a square-law relationship between the channel current and the gate–source voltage, when operating in the *saturation region.* Many of the analog multiplier cells devised for CMOS implementation during the 1980s depended on this notion. Here, the denominator V_U is traceable to device parameters that are not accurately known or well controlled. Furthermore, the basic relationship is far from square-law for modern short-channel transistors, which have other error sources (for example, back-gate channel modulation). Other problems arise in MOS cells based on operation in the triode region.

Analog multipliers have also been based on the use of squaring cells made with bipolar transistors, whose practical value is questionable, since they perform only indirectly what can be more efficiently achieved using direct translinear multiplier implementations. Indeed, the appeals to the quarter-square approach in a contemporary context seem to overlook the historical reasons for invoking this principle in the first place, at a time when bipolar transistors and their highly advantageous translinear properties were not yet available.

In an attempt to push the static accuracy to fundamental limits, the use of nonlinear device behavior has often been set aside to explore what might be done using little more than analog switches (11). Invariably, the accuracy of these multipliers is limited more by the auxiliary circuitry required to support the core function, as is true of most practical multipliers, and any theoretical benefits that might be possible using switching techniques are often lost in this way. A more serious limitation, for all but a few specialized low-frequency applications (for example, power measurement at line frequencies), is that the output must be derived from averaging a pulse train whose duty cycle and amplitude vary with the two multiplicands. A considerable time is required to determine the average value, even using an optimal filter.

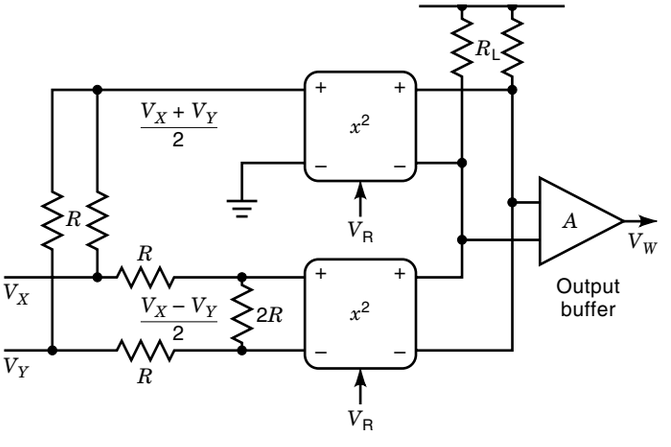

Figure 7. Quarter-square multiplier.

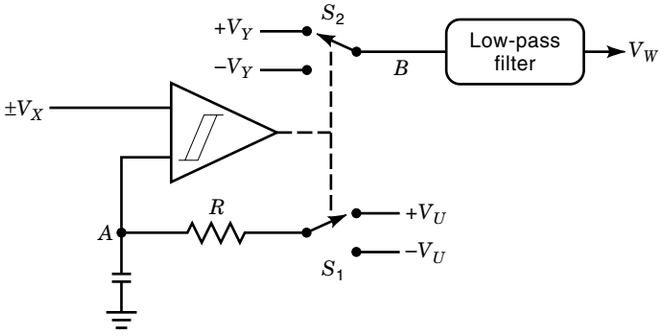

Figure 8. Pulse-averaging multiplier.

An illustrative embodiment of this principle is shown in Fig. 8. The hysteretic comparator, which operates the changeover switch S_1, and the low-pass filter RC constitute an asynchronous delta modulator. This loop generates a pulse sequence whose duty cycle is forced to a value such that the average voltage appearing at node A is equal to the input V_X, which is assumed to be varying only slowly compared to the oscillation period of the loop, which is determined by the hysteresis band of the comparator, V_H, the reference voltages $\pm V_U$, and the time constant $\tau = RC$. It is easily shown that the duty cycle is

$$\mathscr{P} = \frac{t_{hi}}{t_{lo} + t_{hi}} = \frac{V_X + V_U}{2V_U} \tag{6}$$

varying from 0 when $V_X = -V_U$ to 100% when $V_X = +V_U$, independent of V_H, which must be considerably less than V_U. The comparator is arranged to operate a second switch, S_2, to which the Y input voltage is applied, and whose output at node B is a voltage of $+V_Y$ and $-V_Y$, also having the duty cycle $\mathscr{P}$. This is averaged in a multipole low-pass filter to generate the output

$$\begin{aligned} V_W &= \text{ave}\{\mathscr{P}V_Y - (1 - \mathscr{P})V_Y\} \\ &= \frac{V_X}{V_U} V_Y \end{aligned} \tag{7}$$

A clocked comparator may be used to provide synchronous operation. This multiplier offers very high accuracy, arising from a fundamentally sound architecture, which does not depend on any device nonlinearity, such as vacuum tube or MOS square-law behavior, or the exponential junction law. It is well suited to CMOS implementation, where the chief sources of error will be the offset voltage in the comparator (which can be eliminated using doubly correlated sampling) and in the output filter. The fundamental need for averaging, however, severely limits the response bandwidth to the high kilohertz region; if higher oscillation periods are used in the delta modulator, second-order effects due to inaccurate switching eventually become troublesome.

VARIABLE-TRANSCONDUCTANCE MULTIPLIERS

Analog multipliers may be implemented in a true transconductance mode, that is, using cells accepting voltage-mode signals at their input interfaces, and generating a differential output current that ideally, is proportional to the product, and is converted back to a voltage using a simple resistive load. While space precludes a discussion of true g_m-mode multipliers, the underlying device-modeling issues are crucial to the operation of modern multipliers using translinear-loop techniques.

A bipolar junction transistor exhibits an accurate and reliable exponential relationship between its collector current I_C and base–emitter voltage, V_{BE}:

$$I_C = A_E J_S(T) \exp\left(\frac{V_{BE}}{V_T} - 1\right) \approx A_E J_S(T) \exp\left(\frac{V_{BE}}{V_T}\right) \tag{8}$$

A_E is the effective emitter area (never exactly equal to the physical junction area, because of edge effects, though exactly proportional when using replicated *unit* devices). The factor $J_S(T)$ is the saturation current density, a characteristic of the doping in the transistor's base region; it is highly temperature-dependent. The product $A_E J_S$ is usually called I_S, the *saturation current,* and is a key scaling parameter. V_T is the thermal voltage kT/q, where k is Boltzmann's constant, 1.38×10^{-23} C · V/K, T is the absolute temperature, and q is the electron charge, 1.60×10^{-19} C. V_T evaluates to 25.85 mV at $T = 300$ K, which temperature is assumed unless otherwise stated.

Equation (8) is essentially Shockley's junction law, stated in transistor terms, with some concessions to simplicity, inconsequential for most practical purposes. First, the approximation of the quantity $\exp(V_{BE}/V_T) - 1$ by the simpler $\exp(V_{BE}/V_T)$ is readily justified: even at $V_{BE} = 360$ mV, the exponential term is over a million. Second, V_T should be multiplied by a factor, called the *emission coefficient,* which is very close to, but not exactly, unity. Finally, the forward Early voltage V_{AF} and the reverse Early voltage V_{AR}, which do not appear in Eq. (8), have an effect on the I_C–V_{BE} relationship. These and other device effects are of importance in the detailed analysis of high-performance analog multipliers. However, they are truly second-order effects, and the design of practical, robust, and manufacturable multipliers can ignore many of them, or utilize simple compensation techniques to lessen or eliminate their effect on accuracy.

The dual equation is

$$V_{BE} = V_T \log(I_C/I_S) \tag{9}$$

Using $I_S = 3.5 \times 10^{-18}$ A, typical for a modern small transistor, V_{BE} evaluates to 800 mV at 100 μA, and varies by a factor V_T log 10, or 59.5 mV, per decade. These equations describe the most important characteristics of a bipolar junction transistor (BJT), which operates as a *voltage-controlled current source* (VCCS), having an *exponential* form in its collector-current response to an applied base-emitter voltage, or as a *current-controlled voltage source* (CCVS), having a *logarithmic* form in its base-emitter-voltage response to its collector current. The accurate log–antilog properties of bipolar transistors are the basis of innumerable nonlinear circuits, not available from CMOS devices.

An important outcome of Eq. (8) is that the small-signal transconductance g_m is accurately related to the collector current:

$$g_m = \frac{\partial I_C}{\partial V_{BE}} = \frac{I_S(T) \exp(V_{BE}/V_T)}{V_T} = \frac{I_C}{V_T} \tag{10}$$

that is, the *trans*conductance is an exactly *linear* function of the collector current—the origin of the term *translinear.* Even more remarkably, this equation holds true for all bipolar transistors, on any technology (including heterojunction bipolar transistors (HBT) in SiGe, GaAs, etc.) and is independent of I_S, thus being unaffected by doping levels or device size.

These *transconductance multipliers* are best viewed as a subset of the larger class of translinear circuits, and are widely used in contemporary practice where linearity and accuracy are less important than extreme simplicity. It is instructive to review the history from this broader perspective. Regrettably, some confusion has arisen in the nomenclature, and what should be called "translinear multipliers," whose internal operation can be analyzed entirely in the current mode, are often mistakenly classified as "transconductance types," which properly have at least one input in voltage form and generate a current output.

TRANSLINEAR MULTIPLIERS

During the period 1960 to 1970, the planar fabrication process for bipolar junction transistors was being perfected, and it became possible to produce a large number of integrated circuits on a 1 in. (2.5 cm) wafer, each having many transistors with excellent analog characteristics and closely matching parameters. In particular, the base-emitter voltages, for a given device geometry and collector current, were closely matched, partly due to operating at near-identical temperatures. These and other aspects of monolithic fabrication opened the floodgates to stunning new design techniques, hitherto quite impracticable using discrete-transistor implementations. In fact, many related cell concepts were generated within a short period of time. The translinear technique for analog multiplication was one such development.

We will begin with a discussion of cells using loops of junctions, called *strictly translinear,* and identified here as TL (translinear loop) cells. TL multipliers can be readily understood by considering first a simple one-quadrant cell (Fig. 9) using four identical, isothermal transistors (12, p. 51). The collector currents of Q1, Q2 and Q3, which are here assumed to have the same size, are forced to values I_X, I_Y, and I_U respectively. This cell does not, in principle, place any restrictions on the values of these currents, but they are restricted to a single polarity. Summing the V_{BE}'s around the four-transistor loop and assigning a value I_W to the current in Q4, we obtain the equation

$$V_T \log(I_X/I_S) + V_T \log(I_Y/I_S) = V_T \log(I_U/I_S) + V_T \log(I_W/I_S) \tag{11}$$

It is immediately apparent that the thermal voltages V_T may be eliminated from this equation, leaving sums of logarithms. These may be converted to products:

$$\frac{I_X}{I_S}\frac{I_Y}{I_S} = \frac{I_U}{I_S}\frac{I_W}{I_S} \tag{12}$$

The saturation currents I_S may also be eliminated, leaving

$$I_W = \frac{I_X I_Y}{I_U} \tag{13}$$

The most important observations about this result are: (1) temperature sensitivity has been completely eliminated; (2) the product I_W is exactly proportional to I_X and I_Y; (3) the cell also provides analog division; (4) the actual V_{BE}'s are of no interest; that is, we have realized a pure current-mode cell.

This is a simple demonstration of the power of the *translinear-loop principle* (TLP), which describes the relationship between all the currents in a loop of transistors, as in this example, and allows complex nonlinear functions to be synthesized with ease. The TLP states:

$$\prod_{\text{cw}} I_C = \lambda \prod_{\text{ccw}} I_C \tag{14}$$

which reads: "The product of the collector currents in the clockwise direction around a translinear loop is equal to the product of the counterclockwise collector currents, times a factor λ that allows for the possibility that the transistors emitter areas A_E may differ." For present purposes, we will generally assume $\lambda = 1$, except when discussing certain distortion mechanisms. Note that this condition may be achieved using devices of different emitter area, arranged in balanced pairs of equal area, or in many other ways. Any number of loops may overlap, and thus interact, but each loop will independently satisfy this equation.

Figure 10 shows a practical development of the basic cell that retains the pure current-mode operation and can provide

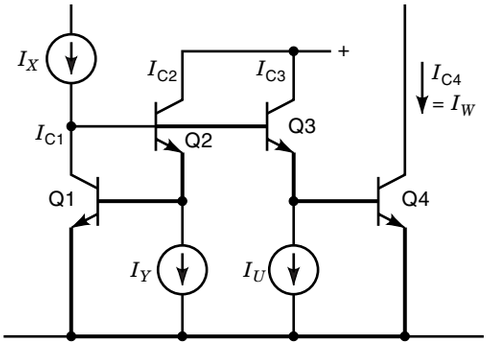

Figure 9. Translinear one-quadrant multiplier–divider cell.

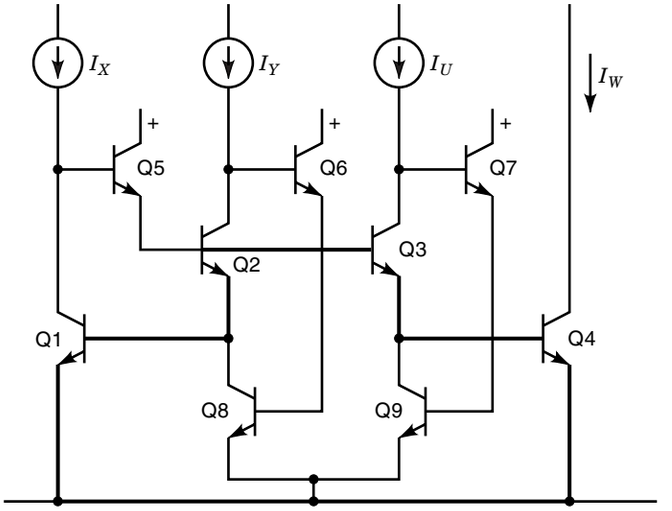

Figure 10. Elaborated current-mode multiplier cell.

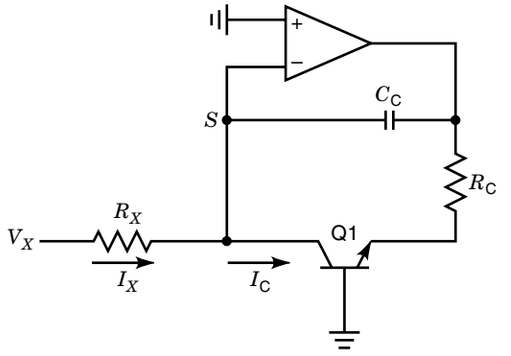

Figure 11. Method for forcing $I_C = I_X = V_X/R_X$ using an OPA.

very accurate operation. Transistors Q5 to Q9 ensure that the collector currents are forced to the desired value, even when the dc current gain β_0 is low; all of the above equations remain accurate in this eventuality. The main sources of static error in this multiplier are (1) emitter-area uncertainties in Q1 to Q4, which cause a simple scaling error, but do not generate nonlinearity; (2) the base and emitter resistances, $r_{bb'}$ and $r_{ee'}$, which will cause nonlinearity, but only at high currents, when the voltage drops across them are a significant fraction of V_T; (3) the modulation of I_W by the collector–base voltage V_{CB} of Q4, due to finite Early voltage.

Many further improvements in current-mode multipliers are possible, and have been developed, but it is generally necessary for a multiplier to receive and generate *voltage-mode* variables. Special-purpose high-bandwidth interface cells can be designed for high-bandwidth voltage-to-current (V–I) and current-to-voltage (I–V) conversion. However, in moderate-speed applications operational amplifier (OPA) interfaces can provide these functions. Figure 11 shows a rudimentary structure for forcing a collector current (5).

The low input offset voltage of the OPA serves two functions. First, it places the current-summing node S close to ground potential (under static conditions), which allows the input current I_X to be generated from a voltage V_X with high accuracy, scaled by R_X, thus: $I_X = V_X/R_X$. Assuming the OPA has very low input current, all of I_X flows in the collector of the transistor. Second, it forces the V_{CB} of Q1 to be zero, eliminating modulation effects due to V_{AF}. The V_{BE} of Q1 bears a logarithmic relationship to $I_C = I_X$ over a very wide dynamic range, specifically, $V_{BE} = V_T \log(V_X/R_X I_S)$; accordingly, this cell may also be used as a logarithmic element (see LOGARITHMIC AMPLIFIERS). R_C and C_C are necessary to ensure that the OPA loop remains stable.

Figure 12 shows a complete one-quadrant multiplier based on this approach. It is traditionally called a log-antilog multiplier, because of the reliance on the dual log-exp relationships of Eqs. (8) and (9). Its function is not, however, predicated on the small-signal transconductance given by Eq. (10), which is also temperature-dependent, but is accurately linear with respect to the X or Y input under large-signal conditions, and temperature-stable. A simpler view is therefore that it is a translinear multiplier, following the principle stated in Eq. (14), aided by operational amplifiers to accurately force the collector currents.

OPA1 to OPA3 provide the input interfaces (the HF compensation has been omitted for clarity). OPA4 converts the current $I_{C3} = I_W$ to a voltage $V_W = I_W R_W$. The op-amps hold the collector voltages of all transistors at ground potential, eliminating Early-voltage errors. From inspection,

$$V_W = \frac{R_U R_W}{R_X R_Y} \frac{V_X V_Y}{V_U} \tag{15}$$

The linear errors are determined by the offset voltages of the amplifiers (a 1 mV offset represents a 0.01% error for a FS input or output of 10 V), by element matching, and by the voltage reference. Nonlinear errors are mainly determined by the junction resistances in Q1 to Q4. The dynamic errors are dominated by the op-amps. This remains a one-quadrant multiplier–divider, useful in specialized contemporary applications. Incidentally, this drawing hints at the care which must be taken in a practical realization with regard to the placement of the current-forcing connections.

More often, multipliers are used as gain-control elements, which require two-quadrant (bipolar) operation of the signal path, with single-polarity operation of the other multiplicand and the divisor. However, a one-quadrant cell can be adapted for two- or four-quadrant operation. The rearrangement shown in Fig. 13 shows the extension to two quadrants; further rearrangements of this same core allow operation in all four quadrants.

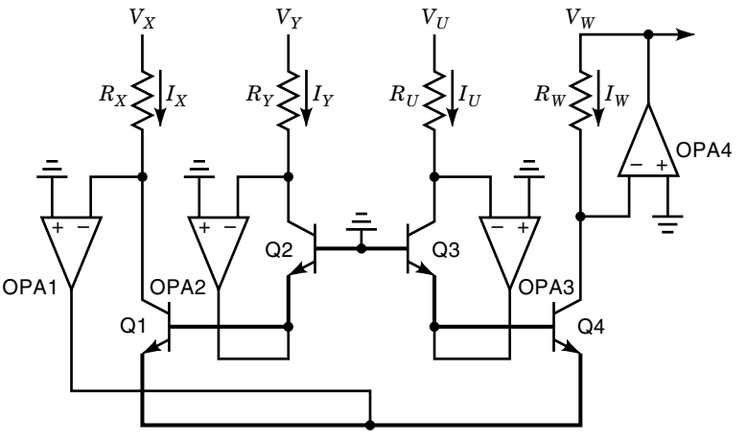

Figure 12. One-quadrant log–antilog multiplier having voltage interfaces.

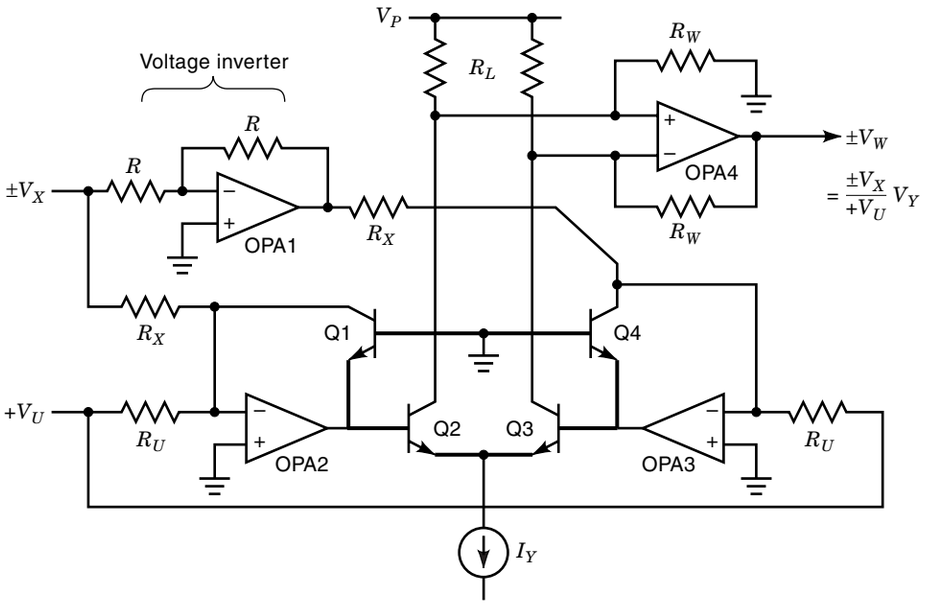

Figure 13. Two-quadrant multiplier/divider.

HIGH-FREQUENCY TRANSLINEAR MULTIPLIERS

The bandwidth of the preceding circuits is severely limited by the operational amplifiers. Some improvement in a fully monolithic design is possible using specialized amplifiers, but in order to realize the full potential of the translinear core, other types of interface—often, though not necessarily, using open-loop rather than feedback techniques, are used. Note that moderately accurate conversion back to voltage mode in a wideband current-mode multiplier may be achieved by the use of simple load impedances.

The first translinear multipliers, described by Gilbert in 1968 (13), achieved a response from dc to 500 MHz, and exhibited a large-signal rise time of 0.7 ns. Two-quadrant types were originally developed for use in oscilloscope vertical deflection amplifiers, to provide interpolation between the 1 : 2 : 5 step attenuator settings that determine the sensitivity, replacing the use of potentiometers, which were formerly used in the signal path. Four-quadrant types were also developed during that period, for use in modulation and demodulation; optimized low-noise mixer cells, including the widely used topology known as the "Gilbert mixer," were developed for use in frequency translation applications, though prior art using discrete devices (14) was discovered in patent searches.

The immediate combination of monolithic simplicity, accuracy, speed, and low cost was unprecedented at that time, and remains unimproved on even to this day. These classic circuit cells have undergone little change in design, and have become the dominant technique for analog multiplication across a broad front.

Numerous commercial products are nowadays available providing one-quadrant, two-quadrant and four-quadrant operation, sometimes supporting the division function. Absolute accuracies may be as high as 0.05%, nonlinear errors as low as 0.01% (roughly corresponding to harmonic distortion levels of −80 dBc) and bandwidths extend from dc, through audio, ultrasonic, IF, RF, and microwave ranges, and as high as 40 GHz in advanced optical receiver AGC applications. No other multiplier technique provides such broad coverage of the applications domain.

To illustrate the principles, Fig. 14 shows a practical two-quadrant translinear multiplier. The bandwidth of the TL core extends from dc to a substantial fraction of the f_T of the transistors, which for a modern BJT process is commonly 25 GHz, and as high as 100 GHz using advanced SiGe heterojunction technologies. The chief practical limitation to overall bandwidth is usually the support circuitry, notably the *V–I* conversion cell at the X input and in the conversion of the differential current-mode outputs to a voltage output.

The input voltage V_X is first converted to a pair of differential currents $(1 + X)I_X$ and $(1 - X)I_X$ by the *V–I* cell; these currents are applied to the diode-connected outer pair of transistors, Q1, Q2. Assume that the *V–I* interface is perfectly linear, that is, $X = V_X/I_X R_X$. For the case of the *pnp*-style interface shown here, X runs from +1 when the value of V_X is

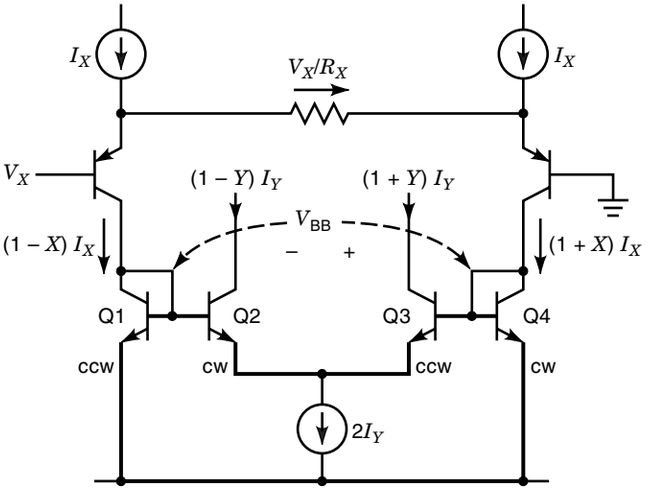

Figure 14. Two-quadrant wideband multiplier cell (type A).

at, or more than, its FS negative limit of $-I_X R_X$, to -1 at the other extreme, when $V_X \geq I_X R_X$.

The variable X, called a *modulation factor,* is frequently useful in describing the operation of these cells. A feature of this multiplier cell (and unique to TL cells) is that operation remains linear up to the extremities of the FS range, in other words, for all values $-1 \leq X \leq +1$. In practice, a moderate peak value of X_{FS} of about ± 0.75 is generally used, first, to ensure that at FS drive, the current densities remain above the point where the instantaneous bandwidth, that is, $f_T(I_C, V_{CB})$, is jeopardized during portions of the signal cycle, and second, to reduce the incidental nonlinearity in the V–I cell. Since the peak input voltage is $V_{XFS} = X_{FS} I_X R_X$, it follows that the bias current must be raised to $I_X = V_{XFS}/X_{FS} R_X$ to provide this overrange capacity. For $X_{FS} = 0.75$ and a FS input of 1 V, the product $I_X R_X$ must be 1.333 V.

To analyze the operation of this *Type A* multiplier cell—so named because the junction polarities *alternate* around the loop, cw–ccw–cw–ccw—we can assign a similar modulation index Y to describe the currents in the driven pair Q3, Q4 and then apply the TLP. To gain rapid insight, we will ignore for the moment the effects of junction resistance, finite base currents, and device mismatches. While these may appear to be naive simplifications, the performance capabilities of TL multipliers are well proven, and the practical errors can in fact be held to very low levels. Applying the TLP, from Eq. (14), we have

$$I_{C2} I_{C4} = I_{C1} I_{C3} \quad \begin{matrix} \text{cw} \\ \text{ccw} \end{matrix} \tag{16}$$

Inserting the actual currents, we have

$$(1-Y) I_X (1+X) I_Y = (1-X) I_X (1+Y) I_Y \tag{17}$$

Thus

$$Y \equiv X \tag{18}$$

independent of I_X and I_Y. That is, the modulation factor in the outer pair has been exactly replicated in the inner pair, and the current-gain is simply I_Y/I_X.

This is a very important result. Note the simplicity of the analysis that results from direct application of the TLP, which completely bypasses considerations involving V_{BE}, its exponential nature, and the temperature-dependent saturation current I_S and thermal voltage kT/q. Equation (18) holds over all temperatures, for all bias currents (from nanoamperes to milliamperes), any device size, either device polarity (pnp or npn), for any material (Si, Ge, SiGe, GaAs), and for any bipolar technology (homojunction or heterojunction).

For this striking reason, the TLP was originally named "the pervasive principle." It is as fundamental a result for translinear circuits as that for g_m stated in Eq. (10) is for a single transistor. Of course, when implementing the principle in robust, high-performance products, many detailed issues need consideration. The differential output current is just

$$\begin{aligned} I_W &= I_{C3} - I_{C2} = (1+X) I_Y - (1-X) I_Y \\ &= 2X I_Y \end{aligned} \tag{19}$$

The differential voltage V_{BB} has the magnitude

$$V_{BB} = V_T \log \frac{1+X}{1-X} \tag{20}$$

and while this voltage, having a peak value of ± 50 mV for $X_{max} = \pm 0.75$, is of only incidental interest, it provides a useful way to assess the wideband noise of a translinear multiplier. For example, when $I_X = I_Y = 1$ mA, the total voltage noise spectral density (NSD) of this four-transistor cell evaluates to about 1.3 nV/Hz$^{1/2}$. Thus, if the FS output is raised to ± 1 V—a factor of 20 times V_{BB}—the lowest possible NSD at this node will be 26 nV/Hz$^{1/2}$. Assuming a 1 MHz signal bandwidth, this amounts to 26 μV rms, providing a dynamic range of 88.7 dB for a 707 mV rms sine-wave output.

More detailed analysis shows that this particular cell is *beta-immune,* that is, finite base currents do not affect the basic operation, provided that the current gain $\beta = I_C/I_B$ is substantially independent of current over the X range. This can be understood by noting that the *fractional* loss of current in the outer transistors due to the base currents I_{B3} and I_{B4} of the inner pair bears a constant-ratio relationship to I_{C3} and I_{C4}; thus, the modulation factor X is unaffected by the base currents, and Y continues to have the same modulation factor as generated by the input V–I converter. Even when the base currents are almost equal to the available drive currents, and Q1, Q2 are operating under starved conditions, the multiplier remains linear—a unique property of this particular circuit. The scaling error due to $\alpha = I_C/I_E$ can be considered as a separate mechanism, even though arising from the same device limitations. Highly refined design techniques address such matters of scaling stability and robustness in mass production.

The most serious nonlinear error sources in this cell are (1) small mismatches in the emitter areas and (2) finite junction resistances. These and other causes of errors in translinear multipliers were fully quantified in the seminal papers published in 1968 (15,16). Mismatches between the ratios A_{E1}/A_{E2} and A_{E3}/A_{E4} cause *even-order* nonlinearities (essentially quadratic), and also linear offsets. The factor λ used in Eq. (14) is here given by

$$\lambda = \frac{A_{E1} A_{E4}}{A_{E2} A_{E3}} \tag{21}$$

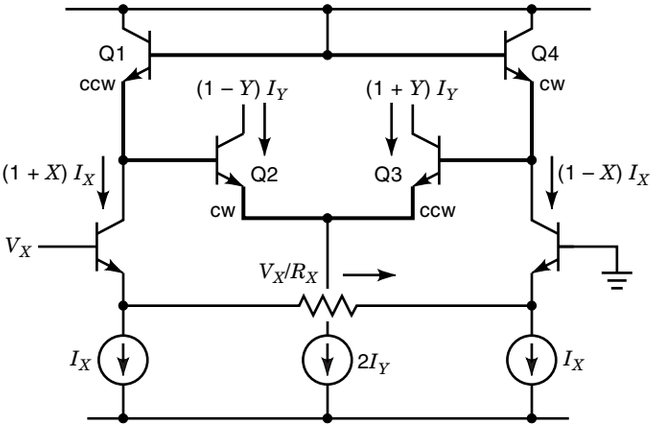

Figure 15. Alternative two-quadrant multiplier cell (type B).

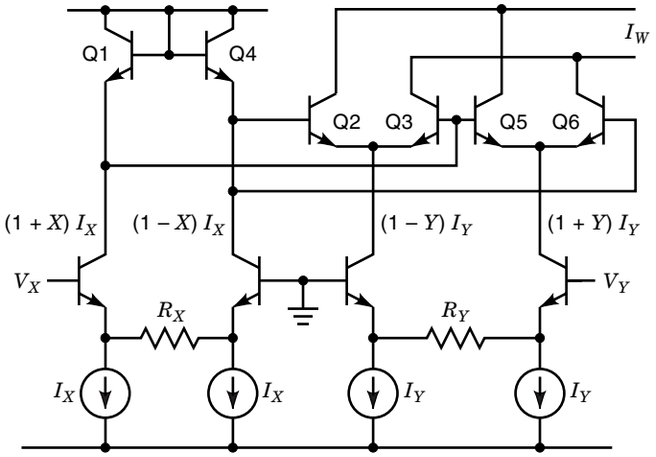

Figure 16. Wideband four-quadrant multiplier cell.

The V_{BE} mismatch around the loop Q1–Q2–Q3–Q4 is V_T log λ. While this *voltage* is a function of temperature, the effects of emitter-area mismatches in translinear circuits are temperature-independent, and the voltage view is irrelevant.

For $X_{max} = \pm 0.75$, it is found that the peak quadratic error is 0.1% of FS output when $\lambda = 1.002$ (V_{BE} mismatch of 52 μV). To minimize this error the transistors should be arranged in a common-centroid manner in the IC layout. This level of quadratic error is routinely achieved in untrimmed multipliers, and may be reduced by a factor of at least ten by using laser trimming to null the second harmonic distortion. This error is independent of device size and bias currents.

Errors due to junction resistance, on the other hand, are dependent on device size (mostly because of the effect on the base resistance $r_{bb'}$) and operating currents. These cause *odd-order* nonlinearity errors (essentially cubic), but no offsets. This source of nonlinearity is particularly troublesome in two-quadrant VCA cells, where current densities vary widely. However, when certain simple criteria are met (16), this distortion can be eliminated in four-quadrant cells, and for this reason they are often used even where only two-quadrant operation is required.

A four-transistor multiplier has only one other topological form, shown in Fig. 15, called a *Type B* (*balanced*) cell. The junctions occur in pairs, cw–cw–ccw–ccw. It can be shown that this circuit does not enjoy the beta immunity of the Type A multiplier, since the currents in the driven transistors Q2, Q3 are now out of phase with those in the input transistors Q1, Q4; the base currents subtract from the drive currents in antiphase. It is nonetheless widely used, because it can be easily driven from all-*npn* interfaces (V–I converters), which until recently were the only available high-speed transistors in a bipolar IC process.

A four-quadrant multiplier is formed by adding a further pair of transistors Q5, Q6, also having their bases driven from Q1, Q2, as shown in Fig. 16, and their outputs connected in parallel antiphase. The common-emitter nodes are driven from a second V–I, handling the Y input and generating a complementary pair of currents $(1 + Y)I_Y$ and $(1 - Y)I_Y$, where $Y = V_Y/I_Y R_Y$.

The operation is an extension of that analyzed for the two-quadrant cell. Elaborating Eq. (19), we have

$$\begin{aligned} I_W &= I_{C3} - I_{C2} + I_{C6} - I_{C5} \\ &= (1-X)(1-Y)I_Y/2 - (1+X)(1-Y)I_Y/2 \\ &\quad + (1+X)(1+Y)I_Y/2 - (1-X)(1+Y)I_Y/2 \\ &= 2XYI_Y \end{aligned} \tag{22}$$

The conversion of the differential currents back to the voltage domain can be accomplished in several ways, depending largely on accuracy and bandwidth considerations. In high-frequency applications, a balanced-to-unbalanced transformer (balun) can be employed, with the working load impedance R_W determining the overall scaling factor.

Substituting the full expressions for X and Y into Eq. (22), we can write

$$V_W = 2XYI_Y = \frac{V_X V_Y I_Y R_W}{I_X R_X I_Y R_Y} = \frac{V_X V_Y}{V_U}\frac{R_W}{R_Y} \tag{23}$$

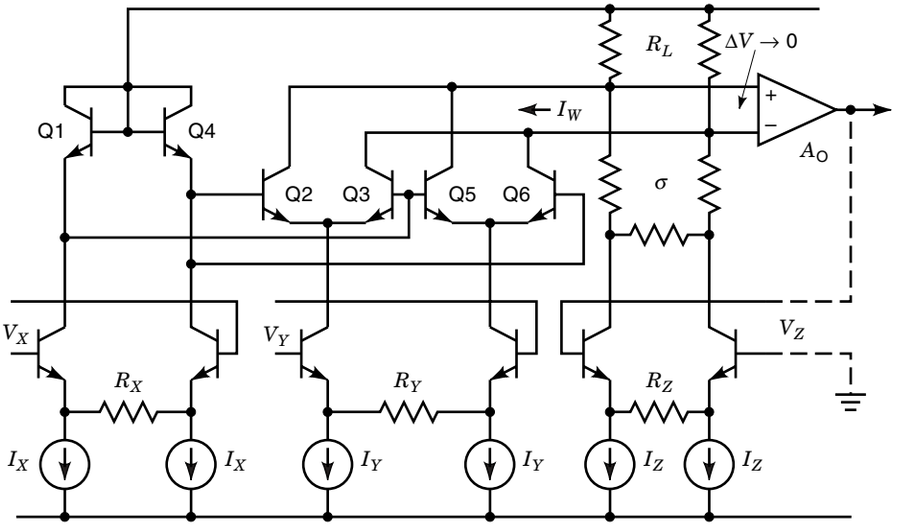

Figure 17. Versatile four-quadrant structure using active feedback.

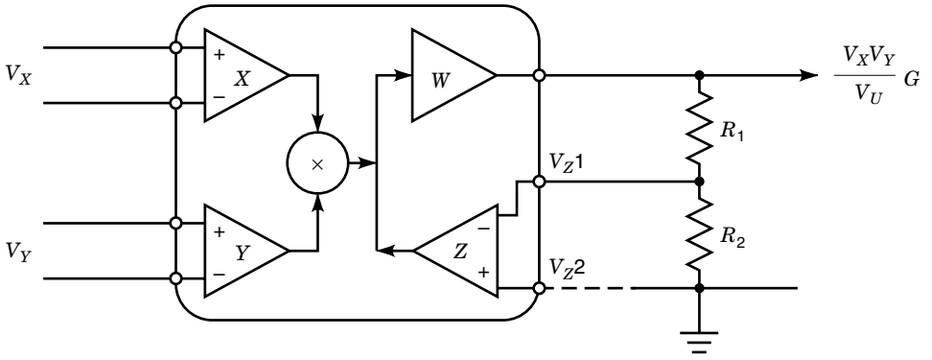

Figure 18. Four-quadrant multiplier with gain.

where $V_U = I_XR_X$ in this implementation. It follows that the biasing arrangements for I_X should be traceable to an accurate, temperature-stable voltage reference. In a complete multiplier, this current will also include compensation for finite beta. The AD834 is a dc to 1 GHz four-quadrant multiplier having essentially this structure, having open-collector outputs; special techniques are employed to linearize the X and Y interfaces.

In low-frequency (<300 MHz) applications, it is possible to provide a more versatile output interface based on feedback around a closed loop. Of particular interest here is the use of *active-feedback* techniques (17) to improve linearity. Figure 17 shows the general structure: a third V–I cell has been added to handle the feedback path; its differential output is V_Z/R_Z. Note that while the currents I_Y and I_Z do not enter into the scaling of this multiplier, they nevertheless affect the FS capacity of the Y and Z interfaces. Resistive loads R_L are used at the collectors of the core, but the high open-loop gain of the output amplifier ensures that the differential voltage swing is very small. The output currents of the Z cell are attenuated by a scaling factor σ; the purpose of this will become clear in a moment.

The output can be expressed as

$$V_W = A_O\left(\frac{V_XV_YI_YR_L}{I_XR_XI_YR_Y} - \frac{\sigma V_ZR_L}{R_Z}\right) \tag{24}$$

As before, the I_Y factors cancel, and when the effective resistance A_OR_L is very high, the two terms inside the brackets must be equal. This condition will always be forced by V_W acting on one of the inputs, by a feedback connection, but it does not have to be the Z input. We will show that in addition to four-quadrant multiplication, this versatile IC structure can be used for two-quadrant squaring, simple one-quadrant square-rooting, absolute-value extraction, two-quadrant square-rooting (with very few external components), two-quadrant division, four-quadrant division (using two ICs), and N-dimensional vector summation (using N multiplier ICs).

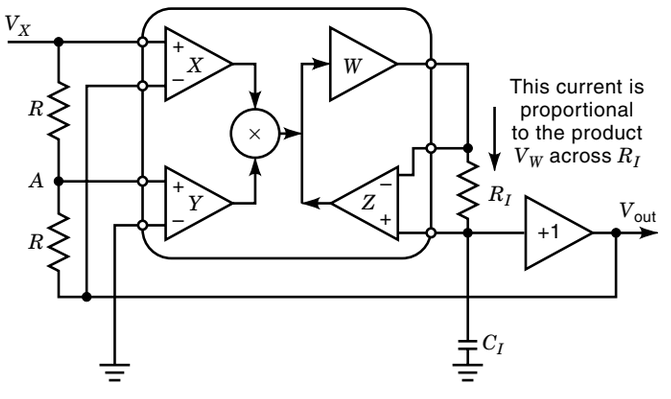

Figure 19. Rms–dc converter using difference-of-squares technique.

The active-feedback structure can also easily generate an accurate bipolar current output having a very high impedance, and thus also provide exact time integration using a capacitor. This structure was first used in the highly successful AD534, a fully calibrated laser-trimmed monolithic multiplier introduced by Analog Devices in 1975, and since then in the AD633, AD734, and AD835, and IC multipliers from other manufacturers. It has become a classic form, having been designed into thousands of systems.

To complete the theory of this multiplier form, we will rewrite the general solution found by nulling the bracketed terms in Eq. (24):

$$\frac{V_XV_Y}{I_XR_XR_Y} = \frac{\sigma V_Z}{R_Z} \tag{25}$$

which can be simply cast as

$$V_XV_Y = V_ZV_U \tag{26}$$

where the scaling voltage is

$$V_U = \sigma I_XR_XR_Y/R_Z \tag{27}$$

It was previously noted that the product I_XR_X needed to be 1.333 times the FS input to result in a FS modulation factor X_{FS} of 0.75. For a FS X input of 10 V, this requires I_XR_X to evaluate to 13.33 V (though no such *explicit* voltage may arise in the IC). Further, it is desirable that $R_Z = R_Y$, so that the nonlinearity arising in the feedback (Z) cell exactly cancels that of the Y-input cell; this is an important advantage of the active feedback scheme. Finally, we wish the scaling voltage to be exactly 10 V. Solving Eq. (27), this requires that the factor σ must be set to 0.75.

These multipliers also provide fully differential, high-impedance X, Y, and Z interfaces, implementing a more compre-

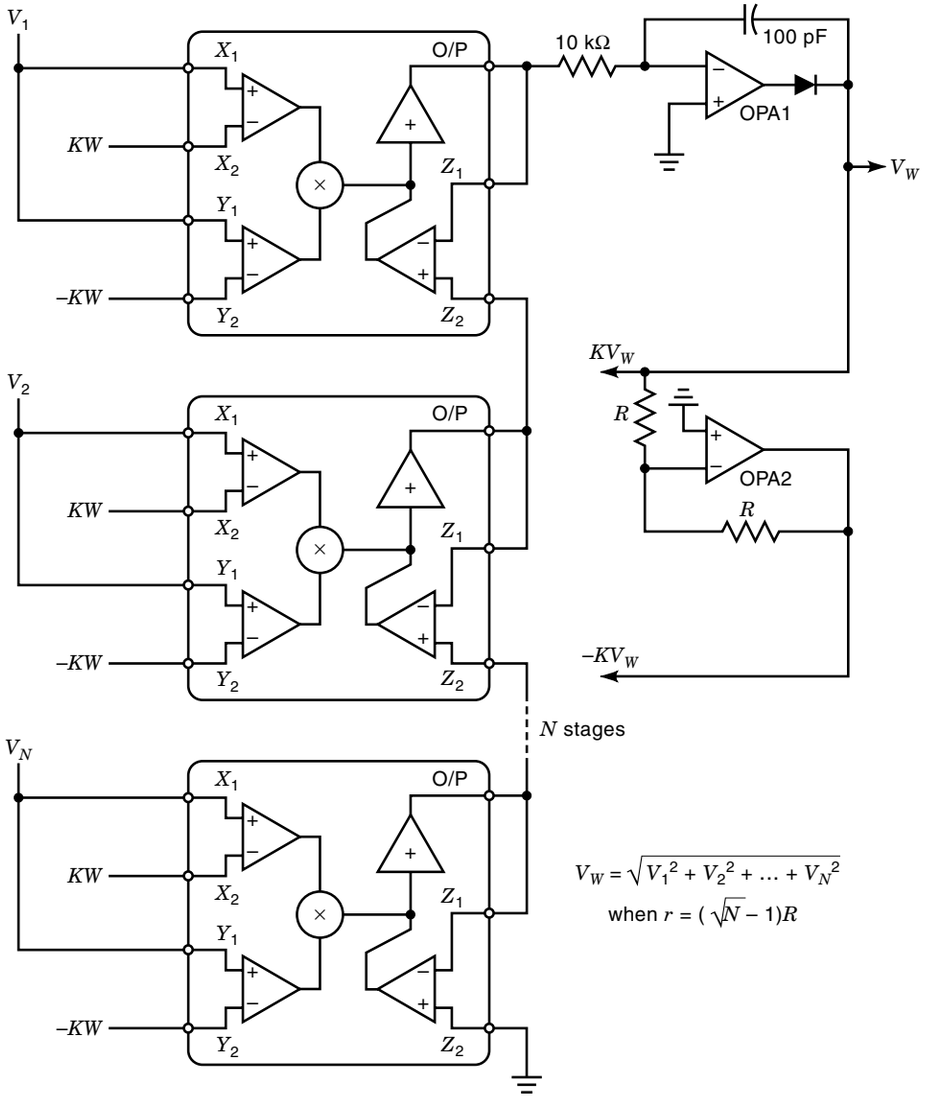

Figure 20. *N*-dimensional vector summation.

hensive function, which can be expressed in terms of the *balance equation*

$$(V_{X1} - V_{X2})(V_{Y1} - V_{Y2}) = V_U(V_{Z1} - V_{Z2}) \tag{28}$$

While many general purpose multipliers support 10 V FS inputs and utilize a denominator voltage V_U of 10 V (such as the AD534, AD633, and AD734), the 250 MHz AD835 has ±2 V FS inputs, with a V_U that is readily trimmed to 1 V, thus providing a ±4 V FS output; the node V_{Z1} is internally connected to V_W, but access to V_{Z2} allows many useful extra functions based on summing at the output. The 1 GHz AD834 provides differential current outputs.

MULTIPLIER APPLICATIONS

The balance equation can be used to implement numerous functions: modulation, demodulation, mean-square and root-mean-square extraction, power measurement, gain control; filterless demodulation, correlation (using the multiply-and-add feature), and many more nonlinear/linear operations, such as trigonometric-function synthesis, rms–dc conversion, and programmable filters. The availability of this *Z* interface is of great practical value, and is used in many of the application examples which follow (18), in most of which either the low-cost AD633 or the AD534 can be used.

Figure 18 shows the basic symbol for versatile multipliers of this class, and demonstrates how one may be connected for basic four-quadrant multiplication. With V_W simply connected to V_{Z1}, the balance equation (28) becomes

$$(V_{X1} - V_{X2})(V_{Y1} - V_{Y2}) = V_U(V_W - V_{Z2}) \tag{29}$$

thus

$$V_W = \frac{V_X V_Y}{V_U} + V_{Z2} \tag{30}$$

In this case, however, only a fraction of V_W is returned to the *Z* interface, invoking familiar feedback techniques, which raises the output gain by the factor $G = (R_1 + R_2)/R_2$, and

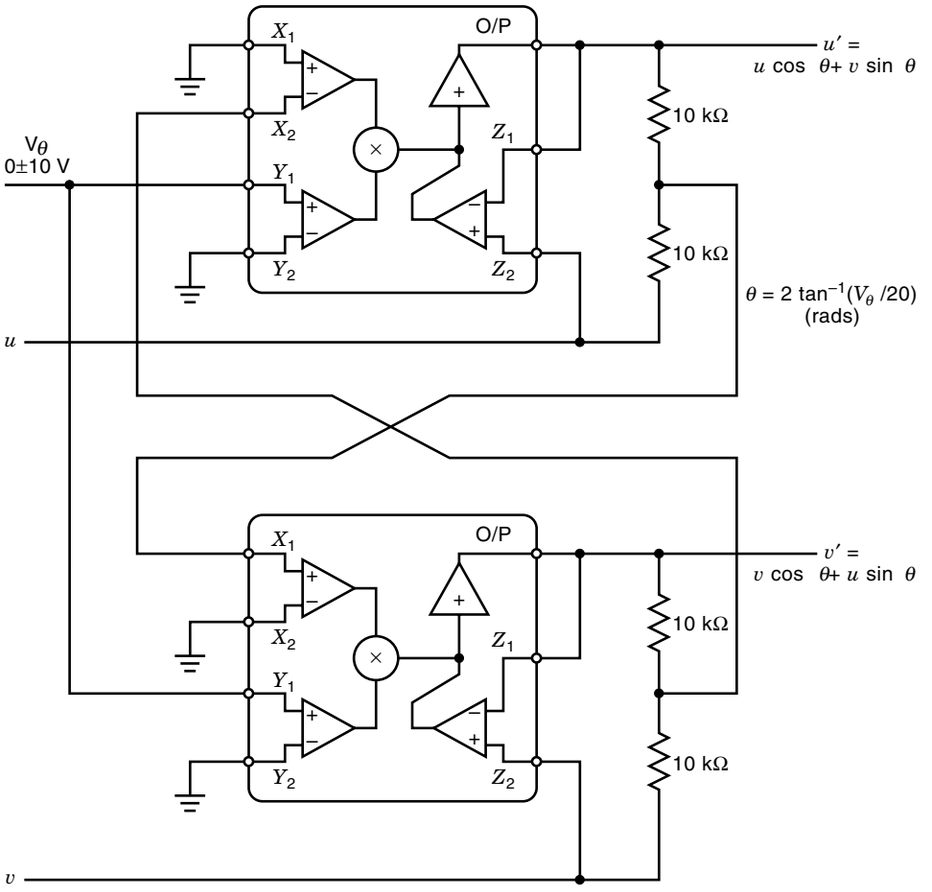

Figure 21. Vector rotation circuit.

thus the effective value of the denominator voltage is V_U/G. A voltage at the lower end of R_2 adds directly to the output, with a scaling factor of unity.

The output may be taken in current-mode form from the V_{Z2} node by a resistor placed from V_W to V_{Z2} since the product voltage $V_X V_Y/V_U$ is forced across this resistor, whatever its value and for any load voltage (for both within a wide range); the output impedance is very high (megohms), being determined by the common-mode rejection ratio of the Z interface. When this current is applied to a grounded capacitor, the time-integration function can be implemented. This is used in the rms–dc converter based on a difference-of-squares technique (19), shown in Fig. 19. This scheme generates the product

$$\frac{V_{\text{in}} + V_{\text{out}}}{2}(V_{\text{in}} - V_{\text{out}}) = \frac{V_{\text{in}}^2 - V_{\text{out}}^2}{2} \tag{31}$$

the long-term average of which is forced to zero by the action of the loop including the integrator, which also serves to average the signal at the multiplier output, V_W. It follows that

$$V_{\text{out}} = \text{ave}(V_{\text{in}}^2) \tag{32}$$

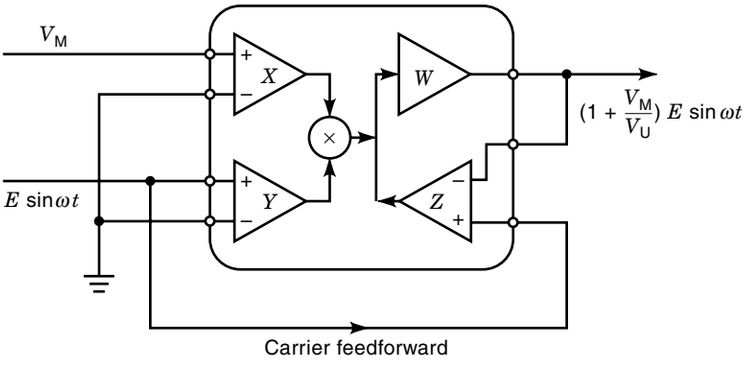

Figure 22. AM modulator.

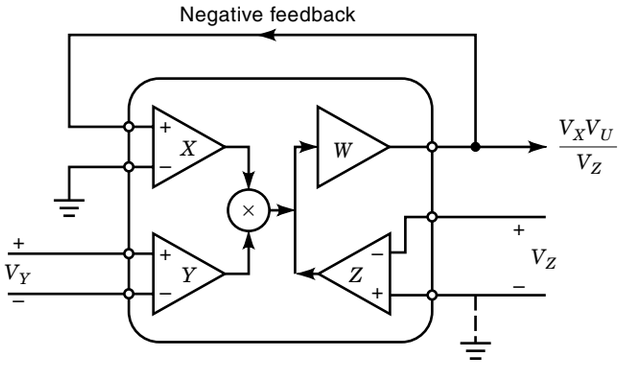

Figure 23. Two-quadrant division.

in other words, the rms value of V_{in} has been generated. Using an integration time constant C_1R_1 of 16 μs, the loop settles to within 1% of the final value after 123 μs for a 10 V sine-wave input, and within 305 μs for a 4 V input. With the capacitor omitted, the circuit provides the absolute-value function.

A further example of the utility of the summation feature is provided by the N-dimensional vector-summing circuit (Fig. 20), where this function is provided by daisy-chaining the multiplier outputs. The inputs V_1 through V_N may have either polarity, and the loop seeks to null the sum of the N independent difference-of-the-squares components. When the factor K is set to $1/\sqrt{N}$, the overall scaling from the inputs is unity, that is

$$V_W = \sqrt{V_1^2 + V_2^2 + \cdots + V_N^2} \tag{33}$$

The integration time, provided by the 10 kΩ resistor and the 100 pF capacitor, will normally be chosen to ensure stable loop operation, but when large enough to implement averaging, the circuit performs the root-mean-sum-of-squares operation.

The use of *normalized* variables is often valuable in analyzing and synthesizing multiplier applications. Thus:

$$x = V_X/V_U; \quad y = V_Y/V_U; \quad w = V_W/V_U; \quad z = V_Z/V_U; \quad \text{etc.}$$

It is sometimes required to rotate a pair of signals representing a two-dimensional vector, for example, in image presentation systems. Figure 21 shows how just two multipliers may be used. The vector ($\boldsymbol{u}$, $\boldsymbol{v}$) is turned through an angle θ controlled by the V_θ input, to generate

$$\boldsymbol{u}' = \boldsymbol{u}\cos\theta + \boldsymbol{v}\sin\theta \tag{34a}$$

$$\boldsymbol{v}' = \boldsymbol{v}\cos\theta + \boldsymbol{u}\sin\theta \tag{34b}$$

where

$$\theta \approx 2\arctan(V_\theta/20) \tag{35}$$

Using AD534 or AD633 multipliers, the rotation scaling is 5.725 deg/V and is $\pm 60°$ at $V_\theta = \pm 11.55$ V; the relative error is -2% at $V_\theta = \pm 5$ V ($\theta = \pm 28°$). The length of the vectors is unchanged. A related scheme for cathode-ray tube (CRT) geometry and focus correction was described in Ref. 18.

In a more commonplace application, the Z interface is also used in the AM modulator shown in Fig. 22, where the carrier E sin ωt is fed forward to the output (which responds as a voltage follower to the Z_2 input) and thus added to the product of the modulation voltage V_M and this carrier.

The Z interface is especially useful in analog division (Fig. 23), since it presents a high-impedance, fully differential input port. From Eq. (28), with V_{X1} now being the output V_W, we have

$$(V_W - V_{X2})(V_{Y1} - V_{Y2}) = V_U(V_{Z1} - V_{Z2}) \tag{36}$$

thus

$$V_W = V_U\frac{V_{Z1} - V_{Z2}}{V_{Y1} - V_{Y2}} + V_{X2} \tag{37}$$

A high-impedance summing input is again available. To maintain negative feedback around the output amplifier, the denominator must be positive, but the numerator may have either polarity. The circuit therefore provides two-quadrant division, with the added advantage of differential signal processing available at both the numerator and denominator inputs.

The determination of the ratio of two voltages, both of which have indeterminate polarity, calls for a divider capable

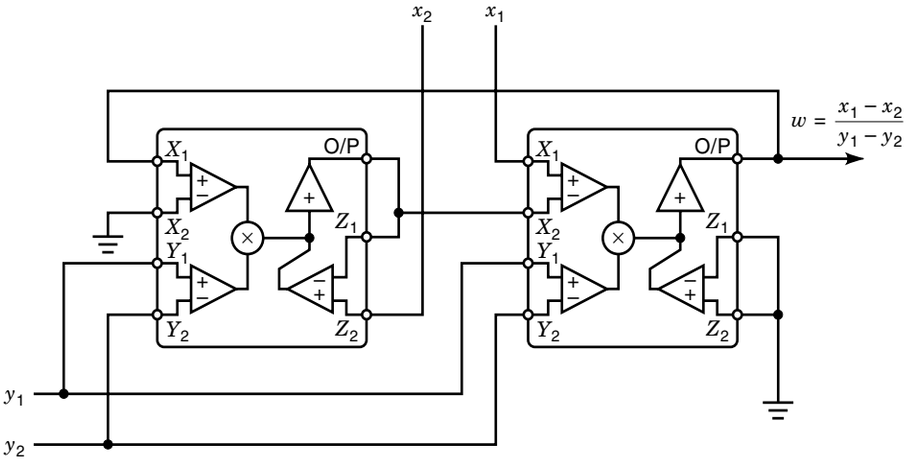

Figure 24. Four-quadrant division.

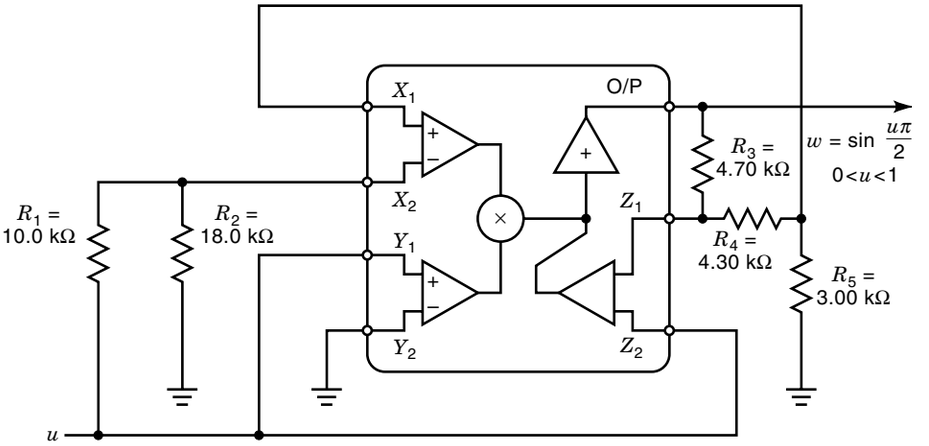

Figure 25. Sine-function synthesis.

of accepting a *bipolar* denominator input. This is the *four-quadrant division* function. Commercial products that perform this function are not in demand, but it is easily implemented using two of these general-purpose multipliers, as shown in Fig. 24. The behavior is benign through the singularity where the denominator is zero, though of course significant errors arise for small values. This circuit is unusual in being able to divide one sine wave by another. In a test in which a 400 Hz, 10 V amplitude sine wave was applied to both numerator and denominator inputs, the output was essentially constant at +10.03 V, with a ripple of only ±50 mV at the zero crossings.

These versatile multipliers allow the implementation of arcane and often complicated nonlinear functions. For example, the sine function can be approximated by

$$\sin\theta \approx \frac{1.0468\theta - 0.4278\theta^2}{1 - 0.2618\theta} \tag{38}$$

over the range $0 \le \theta \le \pi/2$. The theoretical error is ±0.4% of FS. While the synthesis requires considerable elaboration, Fig. 25 shows how simple the implementation becomes, using a single, low-cost multiplier. A better approximation, providing a theoretical error of only ±0.01%, and <0.2% in practice, can be implemented with just two such multipliers and five resistors (18). Cosine synthesis needs only one multiplier and two resistors (18), with a peak error of ±2% at 22° and 73°, and the useful arctangent function may be approximated with a peak error of ±0.46° as shown in Fig. 26.

Many further examples could be provided. These general-purpose voltage-in, voltage-out translinear multipliers cover a very broad range of applications, and their structure is practicable for operation from dc to at least 1 GHz. Contemporary wideband translinear multipliers, implemented using very fast complementary bipolar silicon-on-insulator (CB-SOI) processes and aided by advances in noise and distortion reduction, calibrated to high accuracy using laser-wafer trimming and presented in tiny surface-mount packages, represent the epitome of the analog nonlinear art, while squarely meeting the pragmatic ongoing requirements for a wide variety of nonlinear continuous-time signal-processing tasks, which go far beyond the basic task of multiplication.

All manner of special-purpose multiplier cells, of either transconductance or translinear types, have found their way into numerous IC systems: as gain-control elements, often implementing the AGC function; as power detectors and power controllers; in correlation applications; in analog-programmable filters; as modulators and demodulators, for example, synchronous detectors; and much else. Their simplicity, completeness (no external components are usually required), very high speed combined with excellent accuracy, low supply voltage requirements, and low power, coupled with low cost and very small size, ensure the continued use of these ubiquitous elements.

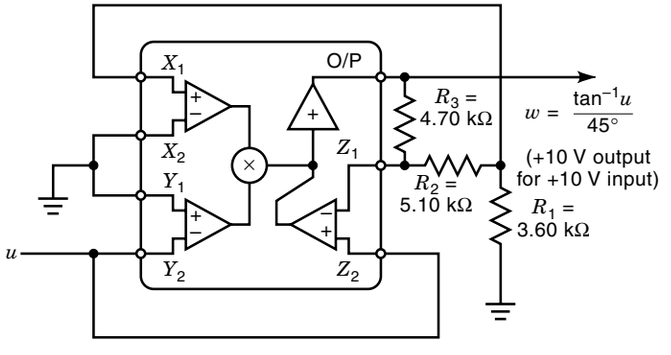

Figure 26. Arctangent synthesis.

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