INTEGRATING CIRCUITS

Since inductors tend to be bulky and expensive (except for applications at frequencies higher than approximately 1 GHz), integrating circuits generally consist of a current signal which is integrated onto a capacitor to form a voltage signal. Cascading one integrating circuit to another requires that the voltage signal be converted to a current signal. An integrating circuit can be realized using an opamp, resistor, and capacitor. The input voltage is converted to an input current which is directly proportional to the input voltage via Ohm's Law. This current is integrated onto the capacitor. The output voltage is produced at the output of the opamp.

The major applications of integrating circuits are in filters, slow analog-to-digital converters, and image sensor circuits. Integrating circuits are the basic building blocks used to synthesize frequency selective circuits, or filters. The complexity of the filter function, in terms of the number of poles, determines the number of integrating circuits that must be included in the circuit. A high precision but low speed technique for analog-to-digital conversion employs an integrating circuit, comparator, and a counter or timer. The integrating capacitor is charged for a specified amount of time by a current which is proportional to the input signal. The capacitor is dis-
charged by a fixed amount of current. The length of time re-
quired to fully discharge the capacitor determines the value
MOSFET-C integrator, and (c) the tr of the input signal. Another major application of integrating

power consumed by the circuit. We measure dynamic range as the ratio of the largest to the smallest signal level that the **The MOSFET-C Integrator**
circuit can handle. A tradeoff exists between these perfor-
mance criteria: that is the higher the dynamic range re. The MOSFET-C mance criteria; that is, the higher the dynamic range re-

$$
v_O(t) = A \int_0^t v_I(t) \, dt + B \tag{1}
$$

The inverting integrator, also known as the Miller integrator, **The Transconductance-C Integrator** is shown in Fig. 1(a). It is an inverting amplifier, where the
feedback element is the capacitor C. The input voltage, $v_l(t)$,
is converted to a current $i_l(t) = v_l(t)/R$, since a virtual ground
exists at the negative input te *rent* is integrated on the capacitor, forming an output voltage according to the relation,

$$
v_O(t) = -\frac{1}{RC} \int_0^t v_I(t) dt - v_C(0)
$$
 (2)

circuits is in image sensing circuits. Incident light is converted to a photo-current which is integrated on a storage capacitor of the capacitor for a specified length of time. The final voltage on the that even a small

quired, the higher the cost of the integrator. in integrated circuit design, where the amplifier, capacitor, and resistance are fabricated on the same substrate. An MOS **INTEGRATING CIRCUITS** transistor operating in the triode region acts like a voltage-
controlled resistor, where the nominal conductance $G = 1/R$ has units of $1/\Omega$. Using the same analysis as for the Miller There are several means of realizing the mathematical function of integrator, we find that the integrating time constant is
ers, and capacitors. The function we want to synthesize is of
the inverting integrator are: (1) a and (2) the conductance is tunable via the gate voltage V_G . The latter property is particularly important in integrated circuit design, where the tolerance on capacitors is approximately 10 to 50%. **The Inverting Integrator**

$$
i_0 = G(v_+ - v_-) \tag{3}
$$

In Fig. 1(c), we note that $v_+ = v_1(t)$, and $v_- = 0$ V. Thus, the $v_O(t) = -\frac{1}{RC} \int_0^t v_I(t) dt - v_C(0)$ (2) output current is equal to the input voltage times the conductance. The current *i_O*(*t*) is integrated on the capacitor, produc-

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Figure 2. The feedforward Tow–Thomas two-integrator-loop biquadratic circuit.

ing the output voltage, $v₀(t)$. The integrator time constant is function is the same as that for the MOSFET-C integrator, namely, *C*/*G*. The transconductance-C integrator is also used in integrated circuit design. Compared to the MOSFET-C integrator, the transconductance-C integrator has simpler circuits and is generally capable of operating at higher speeds. On the other hand, the MOSFET-C integrator has a higher maximum dynamic range at a given cost than the transcon- By a suitable choice of circuit components, Eq. (4) can be conductance-C integrator. The same state of the second-order low-pass, bandpass, high-pass, h

The switched-capacitor integrator employs a capacitor and at gether. least two MOS transistors operating as switches to emulate **Dual-slope Analog-to-digital Converter** the resistance *^R*. A global clock signal, operating at a frequency much higher than the bandwidth of the input signal, The dual-slope analog-to-digital converter (ADC) is a highturns the switches on and off at a rate which is inversely pro- precision but low speed ADC method. A block diagram is portional to the effective resistance seen by the input. The given in Fig. 3(a). The dual-slope ADC consists of an inverting switched-capacitor integrator is common in integrated circuit integrator, a comparator, a high-speed counter, and control design. Tuning the integrator time constant is straightfor- logic. The charge on the capacitor is initially set to zero. Durward since it depends on the clock frequency and the ratio of ing the integration phase, the input voltage $v_I(t)$ is converted capacitors. In integrated circuit design, the tolerance on the to an input current that is integrated on the capacitor *C* for a ratio of capacitors can be lower than 1%. The cost of this design strategy is increased circuit complexity, power consumption, and noise due to the global clock signal.

If the input signal is a current, integration is easily achieved using a single capacitor. During the reset phase of a capacitor integrator, the capacitor voltage is set to a known initial voltage, typically either 0 V or V_{DD} . During the integration phase, the input current is integrated on the capacitor to produce an output voltage which is proportional to the input current. This output voltage is typically buffered and scaled before it is sent off chip.

MAJOR APPLICATIONS OF INTEGRATOR CIRCUITS

Three major applications of integrator circuits are in filters, dual-slope analog-to-digital converters, and image sensor circuits.

The Biquadratic Filter

The two-integrator-loop biquadratic circuit, or biquad, is used to synthesize an arbitrary second-order filter function in *s*, where $s = j\omega$, and ω is the frequency in radians/s. The feedforward Tow-Thomas biquad is drawn in Fig. 2. It consists of two **Figure 3.** Two applications of integrating circuits: (a) a dual-slope inverting integrators and an inverting amplifier. Its transfer analog-to-digital converter, and (b) a CMOS image sensor circuit.

$$
\frac{V_O(s)}{V_I(s)} = -\frac{s^2 \frac{C_1}{C} + s \frac{1}{C} \left(\frac{1}{R_1} - \frac{r}{RR_3}\right) + \frac{1}{C^2 RR_2}}{s^2 + s \frac{1}{QCR} + \frac{1}{C^2 R^2}}
$$
(4)

notch, or allpass filter. Fourth and higher-order filter func-**Other Integrator Circuits** tions are constructed by cascading two or more biquads to-

fixed length of time. During the discharge phase, current de- maximum dynamic power consumption is rived from a known reference voltage is used to discharge the capacitor. The length of time, as measured in counts, required to discharge the capacitor to 0 V is proportional to the input voltage. The factor 4 takes into account positive charging to *V_{DD}* and

CMOS Image Sensor Circuits sum, $P_s + P_p$.

CMOS image sensor circuits receive as input a photocurrent **Dynamic Range**
which is proportional to the intensity of the incoming light.
The photocurrent is generated at a reverse-biased *nn* junction **Dynamic range (DR)** The photocurrent is generated at a reverse-biased *pn* junction Dynamic range (DR) is defined as the maximum input level in the silicon. A simplified diagram is shown in Fig. 3(b) A the circuit can handle divided by the in the silicon. A simplified diagram is shown in Fig. 3(b). A the circuit can handle divided by the noise level. By level, we description of its operation is as follows. The integrating ca - mean the mean-square value of description of its operation is as follows. The integrating ca- mean the mean-square value of the input or pacitor is initially set to V_{DP} . During the integrating time the Dynamic range is generally expressed in dB. pacitor is initially set to V_{DD} . During the integrating time, the photocurrent discharges the capacitor. The difference between V_{DD} and the final voltage is proportional to the mean **Noise.** Sources of noise in the integrator are found in the value of the photocurrent. Thermal noise associated with conductance and the amplifier. Thermal noise associated with

PERFORMANCE CRITERIA

Two performance criteria that we consider are its cost, as measured in its area and power dissipation, and dynamic where *k* is Boltzmann's constant, *T* is the absolute tempera-
range Other performance criteria may be relevant, such as ture, and ξ the combined noise factors o range. Other performance criteria may be relevant, such as ture, and ξ the combined noise factors of the conductance and ξ is greater than unity. maximum bandwidth or minimum supply voltage.

In integrated circuit design, the cost of an integrator is a non-
dominant at low frequencies.
decreasing function of the area and power consumption. In We now configure the inte decreasing function of the area and power consumption. In We now configure the integrator as a single-pole lowpass this analysis, we assume that the technology is fixed; that is, filter by placing a conductance of value the designer is unable to change all the parameters of the the capacitor. Its transfer function is given by devices, except their size.

Area. The silicon area of an integrator is generally dominated by the area of the capacitor. Define the capacitance per unit area of a capacitor in a given fabrication technology as Considering thermal noise only, the noise level at the output can be written as Eq. (8) and the square magnitude of the lowpass filter in Eq.

$$
A = \zeta \frac{C}{C_{OX}} \tag{5}
$$

where ζ is an area factor that takes into account the portion of silicon area used by the amplifier and conductor. This area The expression Eq. (10) shows that the noise level does not factor is always greater than unity.
depend on the value of the resistor, but primarily on the valu

Power. Static power consumption is the power supply voltage times the quiescent, or bias, current of the amplifier. Let **Distortion.** The sources of distortion in the integrator are:
us denote the total amplifier bias current as I_B , the positive (1) the capacitor (2) the amp us denote the total amplifier bias current as I_B , the positive (1) the capacitor, (2) the amplifier, and (3) the conductance.
supply voltage as V_{DD} , and the negative supply voltage as $-$ Linear capacitors are availa

$$
P_S = 2V_{DD}I_B \tag{6}
$$

charging and discharging of the integrating capacitance. In tance is implemented using an MOS transistor operating in most designs, dynamic power consumption is much larger the triode region, there will be some range of input voltages than static power consumption. The maximum dynamic over which the effective resistance is nearly constant. One power consumption occurs when the capacitor is fully charged measure of distortion that is mathematically tractable is the and discharged with each cycle of the input signal. Let the maximum deviation of the effective resistance, expressed as a input signal have amplitude V_{DD} and frequency f_s . Then, the percent of the nominal value. Then, the linear range is de-

$$
P_D = 4f_S V_{DD}^2 C \tag{7}
$$

negative charging to $-V_{DD}$. Total power consumption is the

each element gives rise to a power spectral density that has a flat frequency power spectrum with one-sided density

$$
S_{TH} = 4kTR\xi \tag{8}
$$

Another major source of noise for integrators is 1/*f*, or flicker, noise. Its power spectrum is proportional to the in- **Cost** verse of the frequency, hence, its name. Flicker noise becomes

filter by placing a conductance of value $1/R$ in parallel with

$$
\frac{V_O(s)}{V_I(s)} = \frac{1}{1 + s/RC}
$$
\n(9)

 C_{OX} with units of F/m². Then, the total area of the integrator is found by integrating the product of the power spectrum in (9) over all positive frequencies. In order to account for the presence of two conductors, the noise level is found to be

$$
\overline{V_N^2} = 2\frac{kT}{C}\xi\tag{10}
$$

of the capacitory.

supply voltage as V_{DD} , and the negative supply voltage as \sim Linear capacitors are available in CMOS fabrication pro-
 V_{DD} . Then the static power consumption is *cesses suitable for analog and mixed-mode circuits. Linear ca*pacitors are needed to obtain a high dynamic range integrator. In addition, an amplifier which operates over the full voltage supply range is necessary to achieve low distortion for Dynamic power consumption results primarily from the large amplitude input signals. If we suppose that the conduc-

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d% of the nominal value, where *d*% is the amount of distor- transconductance-C integrator is at least several dB lower. tion. Other distortion measures are possible, such as meansquare error; however, they can be much more complex to **BIBLIOGRAPHY** compute, as they may require knowledge of the input signal

and the circuit topology.

The highest achievable linear range is limited by the volt-

age supplies. As such, the maximum input and output ampli-

tude range for a sinusoidal signal is V_{DD} . For an input signal

of max

$$
DR = \frac{\overline{V_I^2}}{V_N^2} = \frac{CV_{DD}^2}{4kT\xi}
$$
\n⁽¹¹⁾

Here, we relate the cost of the integrator to its dynamic *Appl.,* **42**: 967–971, 1995. range. If we only consider dynamic power dissipation as found in Eq. (7), we see that **PAUL M. FURTH**

$$
DR = \frac{P_D/f_s}{16kT\xi} \tag{12}
$$

Both the numerator and the denominator in Eq. (12) have the units of energy. Thus, the upper limit on the dynamic range
of the low-pass filter is directly proportional to the amount of
energy dissipated in the integrator. For example, in order to
 \overline{N} **INTEGRATION OF DATABASES.** achieve a dynamic range of 60 dB, we must dissipate at least 16×10^6 kT ξ J per cycle of the input signal.

We can rearrange Eq. (7) to solve for frequency of the input signal, as in

$$
f_S = \frac{P_D}{4V_{DD}^2 C} \tag{13}
$$

Thus, for fixed power supply voltage and power consumption, the input frequency is constrained by the size of the capacitor. The lower the frequency of the input, the larger the area of the integrating capacitor. Values of integrated capacitors range from as low as 10 fF to as high as 1 nF; however, the area penalty of the largest value is not amenable to mixed analog/digital circuits.

Differential Signaling

Differential signaling is a technique used primarily in integrated circuits to increase the maximum amplitude range of the input and output signals by a factor of two. Differential signaling has two other major benefits: even-order distortion in the amplifier, conductor, and capacitor is cancelled, as are common-mode sources of noise. The cost of using differential signaling is increased circuit complexity, area, and static power consumption due to common-mode feedback circuitry. The MOSFET-C integrator is unable to take full advantage of differential signaling since the capacitor must have a virtual ground at one node. Thus, its maximum dynamic range is given by Eq. (11). On the other hand, the transconductance-C integrator can employ a differential signal across the capacitor. Notwithstanding, the transconductance-C integrator cannot operate at the maximum input amplitude. It is con-

fined as the continuous set of input voltages over which the cluded, then, that the MOSFET-C integrator can approach maximum deviation of the effective resistance is less than the dynamic range maximum in Eq. (11), whereas the best

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