FREQUENCY SYNTHESIZERS

Frequency synthesis is the engineering discipline dealing with generation of a single or of multiple tones, all derived from a common time-base, always a crystal oscillator.

Traditionally, frequency synthesis (FS) generated a single tone with variable frequency or amplitude. There are new applications, especially for testing and simulation, that require multitone generation and even arbitrary wave generation, which relate to digital frequency synthesis. In the last two decades, FS has evolved from mainly analog to a mix of analog, radio-frequency (RF), digital, and digital signal processing (DSP) technologies.

There are three major FS techniques:

1. *Phase Lock Loop.* Also known as indirect synthesis, the most popular FS technique, based on a feedback mechanism that enables simplicity and economics via digital division and analog processing.
2. *Direct Analog.* An analog technique using multiplication, division, and mix-filtering, offers excellent signal quality and speed.
3. *Direct Digital.* DSP method that generates and manipulates the signal in the numbers (digital) domain and eventually converts to its analog form via a digital to analog converter.

Table 1. Integrated Circuits Used in Phase Lock Loops

Fujitsu Semiconductors: MB15xx
National Semiconductors: 23xx
Philips: SA7025, SA8025, UMA1014
Motorola: MC145xxx
Plessey: SP55xx, SP56xx, SP88xx
Texas Instruments: TRF2020, 2050, 2052

Frequency synthesis is a mature technology yet evolving rapidly. The traditional analog designs are supplemented with ever-increasing digital and DSP methods and technologies. These allow a high level of integration, lower power, manufacturing uniformity (and thus yield uniformity), and low cost. Though a novel technology only 20 years ago, FS and especially phase lock loop (PLL) are very popular, accessible, and economical. Traditionally, FS started to enter the field of electronics as quite bulky and expensive instruments, using multiple crystals and complex analog processing functions such as mixing, filtering, and division. Better architectures and simpler designs have replaced these. Accelerating integrated circuit (IC) technology and high-level integration silicon now offer complete synthesizers, especially PLL and direct digital synthesizers (DDSs) on a single chip and sometimes more than one on a single dice.

In the engineering realm, all signals generated are *amplified and filtered noise.* There are no deterministic signals in nature. The cardinal issue for FS is therefore how clean these signals are and how close they come to a theoretical $\sin(\omega t)$. Such a theoretical signal will have all of its energy in a single spectral line. In reality, signal spectra have a noise distribution caused by amplitude modulation (AM) noise and phase perturbation, also known in FS as *phase noise.* Phase noise can be described by its spectral properties, usually its noise distribution designated in dBC/Hz, or its time equivalent, also known as jitter. Spectral distribution L(fm) details the exact spectral shape of the signal's noise and is defined by the single side-band energy level of the signal at a specific offset from the carrier relative to the signal's total energy. This detailed technique has become the de facto method to describe and characterize phase noise (see Fig. 1).

For example, a 1000 MHz signal with a spectral noise characteristic of −70 dBC/Hz (dB is used almost exclusively because of the large ratios involved) at an offset of 1 kHz from the carrier means that at 1 kHz from the carrier (either 1000.001 or 999.999 MHz), the single side-band noise power contained in 1 Hz bandwidth is 10^{-7} compared with the signal's total power. The function L(fm) that defines the noise distribution spectrum is always measured in decibel of the noise level. Note that the noise is part of the signal and that the integral energy under the L(fm) curve is the signal total power (Fig. 1).

Table 2. Integrated Circuits Used in Direct Digital Synthesis

Stanford Telecom: STEL-11xx and STEL-21xx
Analog Devices: AD7008, AD9830/9831, AD9720/9721
Sciteq Communications: SEI-432, SEI-631, DCP-1

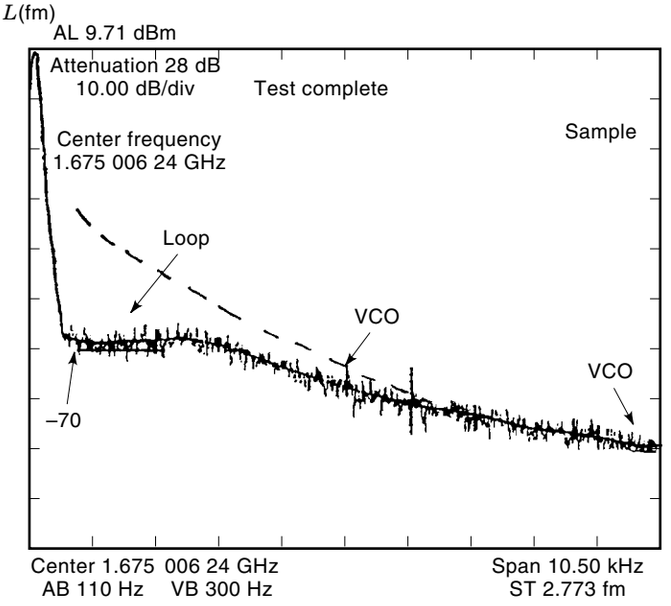

Figure 1. Phase noise of a typical synthesizer.

SYNTHESIZER PARAMETERS

Step Size

This is also known as resolution, and it measures the smallest frequency increment the synthesizer can generate. As an example, an FS used in a North American cellular phone (AMPS—American Mobile Phone Service—standard), or Time Division Multiple Access (TDMA), has 30 kHz resolution. In frequency modulation (FM) broadcasting radio, the step is usually 100 kHz.

Phase Noise

This parameter was already mentioned before. The issue of signal integrity, or otherwise the issue of the signal's "cleanliness," is the major challenge for FS designers. Long-term noise deals mainly with the accuracy, drift, and aging of the crystal, and short-term noise deals with rapid phase fluctuations.

Spurious Responses

These define the level of the discrete interferences, noise sources that are periodic and therefore exhibit spectral lines rather than a spectrum. These noise sources emerge from radiation—for example, line spurious responses at 60 Hz (US)—or from its multiples that always exist in the air and power supplies, as well as from other radiated energy that exists because of the enormous wireless traffic that is emerging and growing. Other sources are mixing products in the radio or synthesizer, nonlinearities, and ground currents.

Switching Speed

This defines the amount of time it takes the synthesizer to hop from a frequency F_1 to another F_2. This parameter is usually measured in two ways: by checking when the new frequency settles to within a frequency tolerance (say within 5

kHz), or (a more strict requirement) by checking the time it takes to settle to within a phase tolerance, in most cases to within 0.1 radian. The phase settling requirement can be as much as three to five times longer than the frequency settling.

Phase Transient

This defines the way the signal's phase behaves in transition from frequency F_1 to frequency F_2. There are mainly three ways to switch:

1. It might be a random parameter, so the phase is unknown after switching.
2. The phase can switch continuously, meaning that when switching from F_1 to F_2, there will be no disturbance in the phase. Such switching requirements are necessary when generating linear FM signals or minimum shift keying (MSK) modulation, or other phase modulation waveforms.
3. In the case of phase memory, if switched from F_1 to F_2 and then back to F_1, the signal's phase will be as if the switching did not occur. This is useful in coherent detection radars and frequency hop communications.

Frequency Range

This defines the frequency band the FS covers.

Other Parameters

Other parameters are not unique to FS; among them are output impedance, power flatness, size, power consumption, environment, and the like.

The main tools used in FS are as follows: multiplication by comb generation; addition and subtraction by mix and filtering; and division (digital) and feedback for PLL. Another cardinal principle in FS is as follows: Multiplication by N corrupts phase noise and spurious by N^2 or 20 log(N) dB. Division improves by the same ratio.

SYNTHESIS TECHNIQUES

Direct Analog Synthesis

This method, the first to be used in FS, derives the signals directly from the reference—as compared to PLL, which it does indirectly. Direct analog uses building blocks such as comb generators, mix and filter, and dividers as the main tools. Many direct analog synthesizers use similar repeating blocks for resolution. These blocks usually generate a 10 MHz band in the ultrahigh frequency (UHF) range, in 1 MHz steps, and after division (mostly by 10) they are used as an input to the next similar stage. Every stage divides by 10, thereby increasing the resolution arbitrarily by as many stages as the designer chooses to use. Most direct analog synthesizers are instruments and traditionally use binary coded decimal (BCD) for control. This is losing importance because a computer controls all modern applications.

Signals are therefore very clean because they are derived directly from the crystal; however, complexity is high and resolution comes at a high price. Direct analog synthesizers also achieve fast switching speed, limited mainly by filters propagation delay. Speed ranges from <1 μs to 50 μs. Because there are no mechanisms to clean the signals at high offset frequencies from carrier, their noise floor—where the phase noise levels—is comparatively (to PLL) high.

Direct analog synthesizers are available from dc to 26 GHz, are usually quite bulky and expensive, exhibit excellent phase noise and switching speed, and found applications in communications, radar, imaging, magnetic resonance imaging, simulators, and ATE.

Direct Digital Synthesis (DDS)

DDS is a DSP technology based on the sampling theorem. The principle of its operation is based on storing the digital values of sine wave amplitude in memory, then flushing these samples out by addressing the memory with an indexer. The indexer is always a digital accumulator, allowing the phase ramp (memory address) to change its slope to any value (compared with a counter that can index the RAM or ROM memory only by increments of 1).

As a consequence, the accumulator output can be interpreted as a signal phase, ωt (actually ωnT, where T is clock time, since it is sample data), with a variable slope given by the accumulator control. For example, if a 32 bit binary accumulator, which performs the function

$$S_n = S_{n-1} + W \quad (S_n \text{ is the output of sample } n, W \text{ is the input}) \tag{1}$$

is addressed with $W = 0$, the output will not change, signifying direct current (dc) signal. However, if $W = 1$, the accumulator will take 2^{32} clock ticks to come back to its original state. So a complete cycle of the phase from $\phi = 0$ (accumulator is 0) to 2π (accumulator is full) takes 2^{32} ticks. Generally, a DDS output frequency is given by

$$F_o = F_{ck} W/\text{ACM} \tag{2}$$

where F_{ck} is the clock frequency, W is the input control, ACM is the accumulator size, and $W < \text{ACM}/2$.

For ACM $= 2^{32}$, $F_{ck} = 20$ MHz, and $W = 1$, output frequency is given by 0.00465 . . . Hz, which is also the synthesizer resolution, its smallest step.

The read-only memory (ROM) output is connected to a digital-to-analog converter (DAC) which generates the analog signal smoothed by the output filter (see Fig. 2). According to the sampling theorem, the maximum output frequency is $F_{ck}/2$, also known as Nyquist frequency.

The various waveforms and modulation points are shown. Because the accumulator output is the signal phase, phase modulation can be applied; amplitude modulation can be applied at the output of the ROM, the amplitude point.

DDS is thus a numbers technology, related to frequency only by the clock. The artifacts caused by sampling generate many (mirror) frequencies as shown in the sampling theorem; these are usually referred to as aliasing frequencies.

DDS offers simplicity, economy, integration, and very fast switching speed. The digital nature of the technology offers design flexibility and simplicity, low-cost manufacturing, and very high density (small dice).

As sampled data, DDS suffers the common problems of quantization. The level of accuracy determines the dynamic range of the design, in most cases 10 to 12 bits. The most

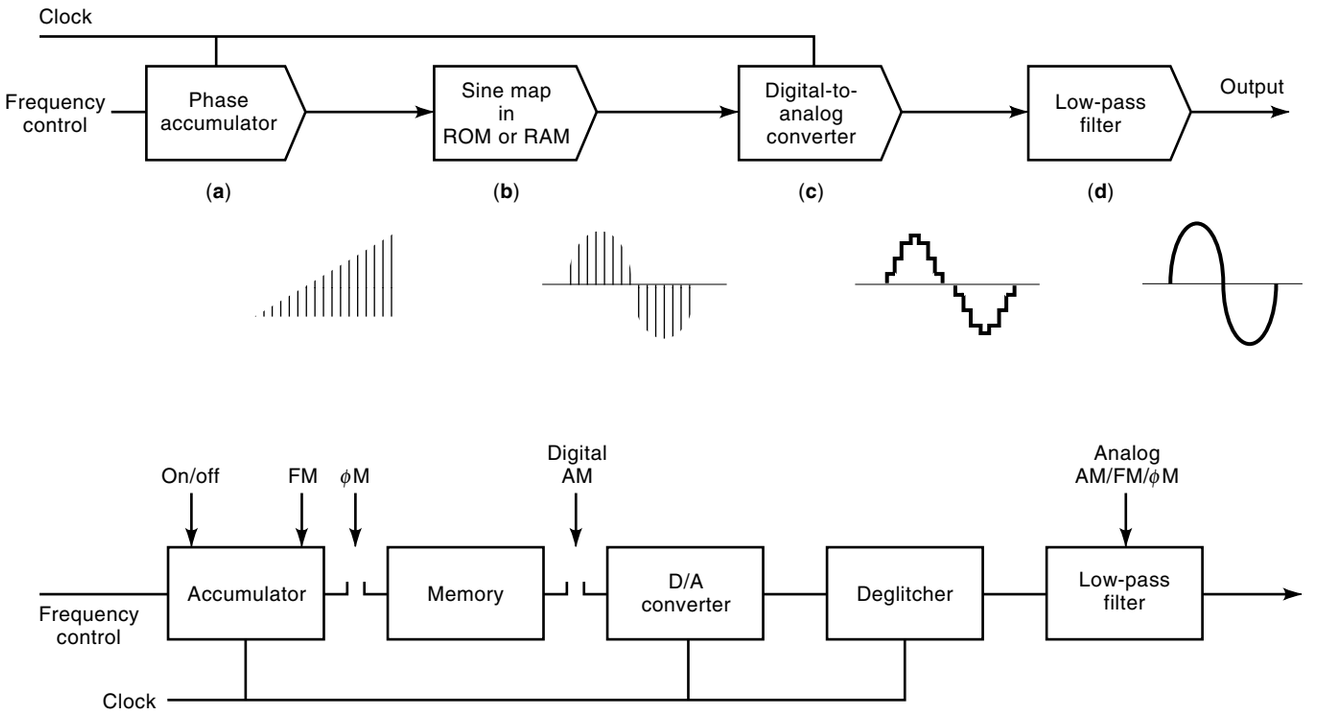

Figure 2. Direct digital synthesizer block diagram and functionality.

significant weakness of DDS are limited bandwidth (clock frequencies are in the 400 MHz for CMOS devices and 1500 MHz for GaAs) and spurious response. Spurious responses are generally limited to $-6D$, where D is the number of bits used in the DAC. Thus a 10 bit DDS (using a 10 bit DAC) usually be limited to -60 dBC spurious responses. These spurious responses are either periodicities generated in the quantization process or intermodulation products generated by the DAC, the only analog part. As a rule of thumb, spurious performance deteriorates with increased output frequency or otherwise with decrease in samples per cycle. Arbitrary waveform generators (AWGs) are a superset of DDS. These enable the memory to be loaded with arbitrary wave samples, and then they sequentially flush the wave samples out. AWGs found use in simulation and testing.

Phase Lock Loop

PLL is the technology of choice for generating radio frequencies and microwave frequencies for radio applications. PLL, also known as indirect synthesis, is a negative feedback loop structure that locks the phase of the output signal after division to the reference. Synthesis is simple because the variable counter (divider) N allows the generation of many frequencies F_o

$$F_o = N\mathrm{Fr} \quad (F_o = \text{output frequency}, F_r = \text{reference}) \qquad (3)$$

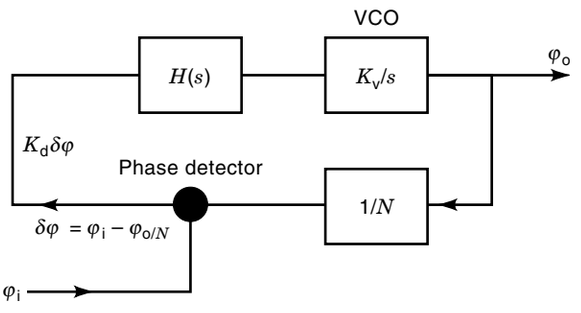

Figure 3. Phase lock loop block diagram.

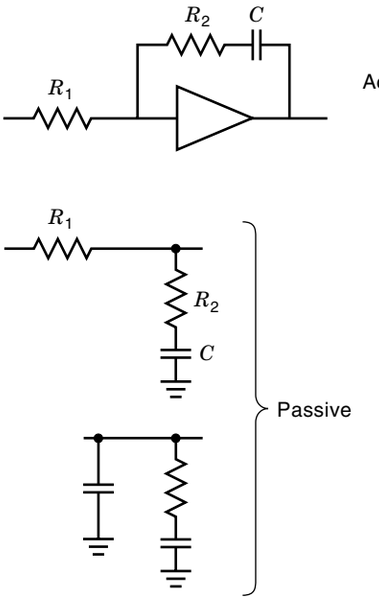

Figure 4. Second-order loop circuits.

by changing the division ratio N. Changing N is made easy by the use of dual modulus devices, capable of dividing by two (and sometimes more) ratios. For example, 64/65 or 128/129 are very common.

PLL chips are available in a great variety, in low power and very low cost, and include all the functionality necessary with the exception of an external crystal, voltage controlled oscillator (VCO) and loop filter (mainly resistors and capacitors). Convenience, economy, simplicity, and ease of use made PLL a household name used in television, radio, consumer electronics, cellular phones, and Satcom terminals, practically in almost any conceivable electronics radio (see Fig. 3).

When locked, PLL can be assumed to be a linear system, and classical feedback theory can be applied for analysis. The most common PLL structure is of second order, and there are two poles in the transfer function denominator: one from the VCO, with a Laplace domain transfer function given by K_v/s (K_v is the VCO constant, phase is the integral of frequency) and one from the loop filter having a memory device (capacitor). The loop transfer function is given by

$$\varphi_o/\varphi_i(s) = \frac{2\xi\omega_n s + \omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2} \tag{4}$$

ω_n is the natural frequency and ξ is the damping, both borrowed from classical control theory. ω_n and ξ are given by (for the active loop structure shown, Fig. 4)

$$\omega_n = (K/T_1 N)^{0.5} \quad \text{and} \quad \xi = \omega_n T_2/2 \tag{5}$$

$T_1 = R_1C$, $T_2 = R_2C$, $K = K_vK_p/N$, K_v (Hz/V), and K_p (V/radian) are VCO and phase detector constants.

Overall performance is controlled by noise sources from phase detector, divider, and other active components within the loop bandwidth and by the VCO outside. Within the loop bandwidth, VCO noise is suppressed by the loop. PLL noise sources within the loop are multiplied by 20 log(N), which can be very significant when N is large. Typical phase detector noise is in the −150 dBC/Hz range for well-designed circuits. An advanced PLL technology known as fractional-n allows lowering N and generating step size smaller than Fr (hence fractional), thereby gaining phase noise performance. The fractional principle requires dynamic changes in division ratio N, thereby causing spurious signals, which are compensated by either extra filtering, analog feed forward correction (open loop), or digital waveshaping techniques.

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