DIODE-TRANSISTOR LOGIC

The first transistor logic family was developed in the 1950s and was named resistor transistor [bipolar junction transistor (BJT)] logic (RTL). To improve upon RTL circuits of the past, *diode-transistor logic* (DTL), was introduced based upon the design of preexisting circuits. As the name implies, circuits of the DTL logic family utilize diodes and transistors in their design.

In 1964, a version of DTL was introduced in integrated circuit (IC) form that became the standard digital IC family of that time. This line of DTL, marketed as the 930 series, is easy to fabricate in IC form and was the standard digital IC for approximately 10 years after introduction in 1964. This family was still in use in some military applications in the late 1980s.

In this article we describe the evolution of the DTL logic family, describing in detail the operation and design of these circuits. Several numerical examples are also included as an aid to understanding. We begin with the basic inverter gate.

BASIC DTL INVERTER

Figure 1 shows the basic DTL inverter and its voltage transfer characteristic. It should be mentioned that the primary reason that DTL logic circuits were introduced was to overcome the low fan-out of RTL for $V_{OUT} = V_{OH}$. From Fig. 1, note that when V_{OH} is the input voltage to a load gate, the input diode D_I' is reverse-biased and sinks only the reverse saturation current, and this current is extremely small.

Output High Voltage (V_{OH})

For V_{IN} low, the input diode D_I is forward-biased as can be seen by following dashed path 1 in Fig. 1. The voltage between the diodes is given by

$$V_X = V_{IN} + V_{D,I}(\text{ON}) < V_{D,L}(\text{ON}) + V_{BE,O}(\text{FA})$$

and is thus not large enough to turn on D_L and Q_O. Hence, Q_O is cutoff and $I_{RC} = I_C = 0$. The output voltage can be found by following dashed path 2 to obtain

$$V_{OUT} = V_{CC} - I_{RC}R_C = V_{CC} = V_{OH}$$

Input Low Voltage (V_{IL})

Increasing V_{IN} to the point where Q_O just turns on is achieved when

$$V_{IN} = V_{BE}(\text{FA}) = V_{IL}$$

where V_{BE}(FA) is the B–E base-emitter forward active turn-on voltage. The corresponding increase in V_X is

$$\begin{aligned} V_X &= V_{IN} + V_{D,I}(\text{ON}) = V_{BE}(\text{FA}) + V_D(\text{ON}) \\ &= V_{BE,O}(\text{FA}) + V_{D,L}(\text{ON}) \end{aligned}$$

where V_D(ON) is the diode turn-on voltage and both D_L and Q_O turn on (conduct) when Q_O is forward active. With Q_O forward active, $V_{OUT} = V_{CC} - I_C R_C$ and begins to reduce from V_{CC} for increases in V_{IN} as $I_{C,O}$ increases.

Output Low Voltage (V_{OL})

Increasing V_{IN} (and therefore V_X) further will eventually drive Q_O into saturation, giving

$$V_{OUT} = V_{CE,O}(\text{SAT}) = V_{OL}$$

where $V_{CE,O}$(SAT) is the B–E saturation voltage.

Input High Voltage (V_{IH})

Transistor Q_O enters saturation at $V_{IN} = V_{BE}(\text{SAT}) = V_{IH}$ where V_{BE}(SAT) is the B–E saturation voltage, which is slightly larger than V_{BE}(FA).

Since V_X cannot increase any further, subsequent increasing of V_{IN} opens D_1. Resistor R_B must be chosen small enough such that Q_O is in saturation when V_X increases to

$$V_X = V_{BE}(\text{SAT}) + V_D(\text{ON})$$

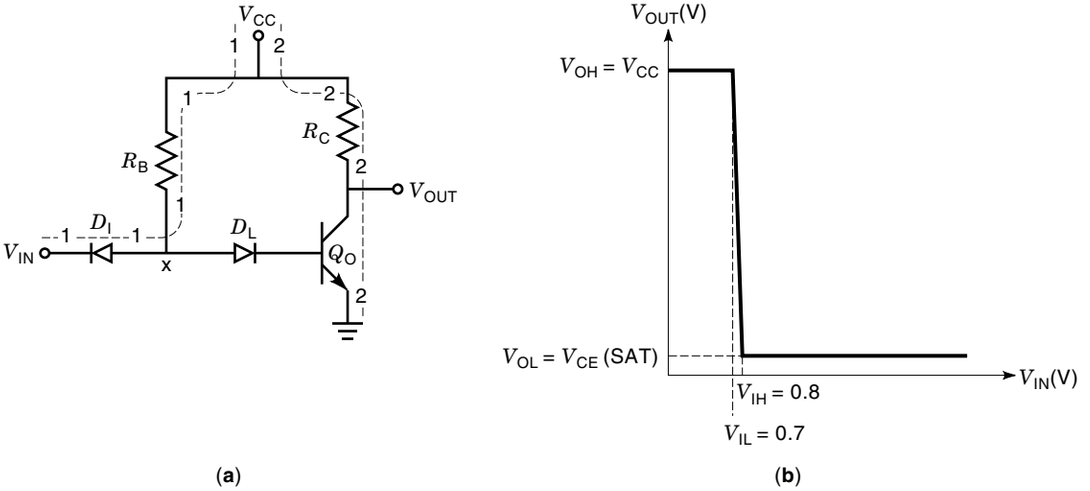

Figure 1. Basic DTL inverter. (a) Circuit. (b) Voltage transfer characteristic.

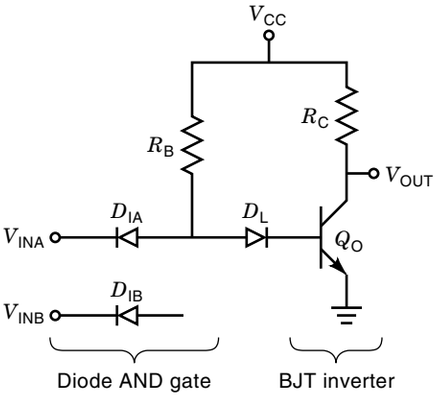

Figure 2. Basic DTL NAND gate.

The logical NOT function is verified by examination of the resulting voltage transfer characteristic of Fig. 1(b). Since V_{IL} and V_{IH} differ only by $V_{BE}(SAT) - V_{BE}(FA)$, the transition width between output high and low logic states is quite abrupt. The actual width can be obtained experimentally or by circuit simulation with results quite close to these.

Basic DTL NAND Gate

Notice that addition of another input diode, as shown in Fig. 2, resembles a diode AND gate connected to a BJT inverter. Indeed, the NAND function is inherently provided by the DTL logic family by adding diodes in parallel at the input pointing outward (OUT).

MODIFIED DTL

Additional Level-Shifting

Figure 3 shows a modified DTL inverter with an additional level-shifting diode D_{L2} added in series with D_L to shift the logic level high-to-low transition by $V_D(ON)$ on the VTC input voltage axis. This improves the low noise margin NM_L, while still exhibiting an acceptable high noise margin NM_H. The additional-level shifting diode also avoids the problem of Q_O turning on before V_{IN} reaches $V_{BE}(FA)$. The addition of D_{L2} increases V_{IL} and V_{IH} by $V_D(ON) = 0.7$ V.

Discharge Path

The inclusion of R_D and $-V_{EE}$ at the base of Q_O provides a path for discharge of the stored base charge of Q_O, when switched from saturation to cutoff. This decreases the transition period and propagation delay time. The need for an additional source voltage (and corresponding pin on the IC) can be avoided by simply taking $-V_{EE}$ to be ground and using a smaller-valued resistance for R_D.

TRANSISTOR MODIFIED DTL

The fan-out of DTL circuits can be further improved by replacing the level-shifting diode D_{L2} with a BJT Q_L and splitting R_B into two resistors, ρR_B and $(1 - \rho)R_B$, whose sum is R_B, as in Fig. 4. When Q_L is on, it is self-biased to operate in the forward-active region and is used in an emitter–follower configuration. This circuit improves fan-out by Q_L, providing more base-driving current to Q_O, allowing Q_O to sink more current from an output load. If $\rho = 1$, the base-collector junction of Q_L is shorted, causing Q_L to become a diode. The circuit then reduces to the one in Fig. 3. The role of each element of the DTL gate in Fig. 4 is summarized in Table 1. The state of each diode and BJT is tabulated in Table 2.

Example 1. Voltage Transfer Characteristic of Transistor Modified DTL. Determine the voltage transfer characteristic (VTC) of the transistor modified DTL inverter in Fig. 4. Use $V_D(ON) = 0.7$ V for the diodes and $V_{BE}(FA) = 0.7$ V, $V_{BE}(SAT) = 0.8$ V, $V_{CE}(SAT) = 0.2$ V for the BJTs, and $V_{CC} = 5$ V.

SOLUTION. The VTC for this improved DTL inverter is found in a manner analogous to the method in the section

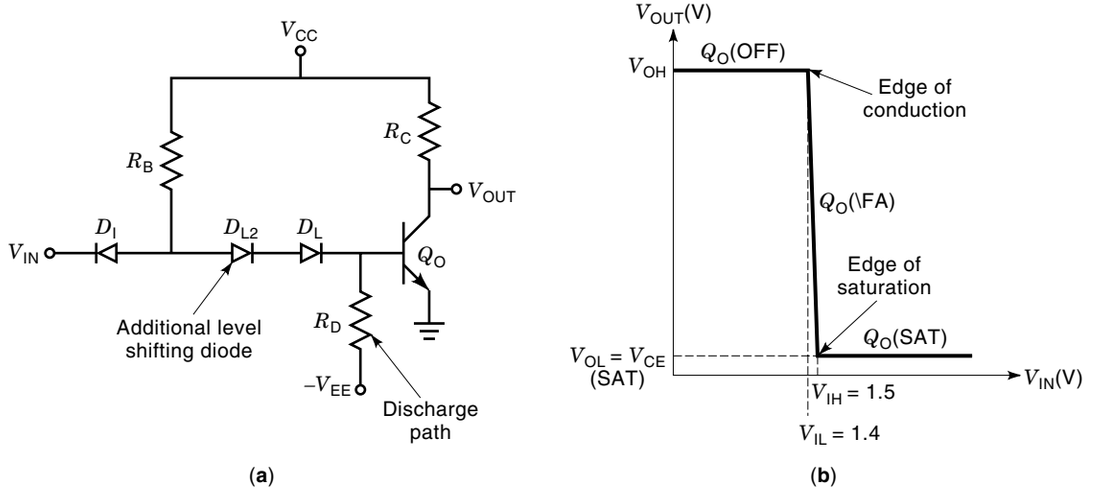

Figure 3. Modified DTL with diode DL2 and discharge path.

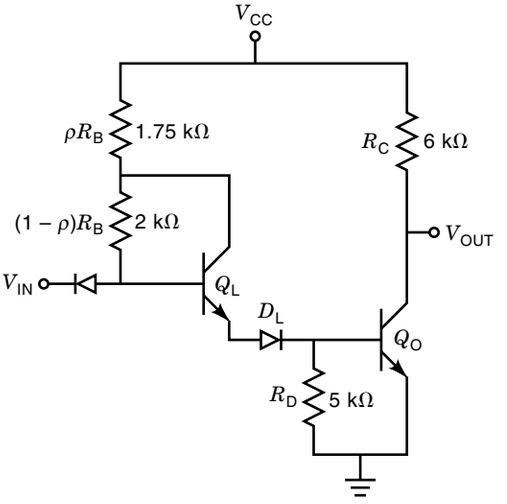

Figure 4. Transistor modified DTL (930 series).

entitled "Basic DTL Inverter." For V_{IN} low, Q_O is cutoff and for V_{IN} high, Q_O is saturated. Thus,

$$V_{OH} = V_{CC} = 5V$$

and

$$V_{OL} = V_{CE,O}(SAT) = 0.2\,V$$

Furthermore, Q_O turns on at

$$\begin{aligned} V_{IL} &= V_{BE,O}(FA) + V_{D,L}(ON) \\ &\quad + V_{BE,L}(FA) - V_{D,I}(ON) \\ &= 2V_{BE}(FA) = 2(0.7) = 1.4V \end{aligned}$$

and just enters saturation when

$$\begin{aligned} V_{IH} &= V_{BE,O}(SAT) + V_{D,L}(ON) \\ &\quad + V_{BE,L}(FA) - V_{D,I}(ON) \\ &= V_{BE}(SAT) + V_{BE}(FA) \\ &= (0.8) + (0.7) = 1.5\,V \end{aligned}$$

Note that Q_L can never saturate because the voltage polarity for the resistor $(1 - \rho)R_B$ maintains a negative $V_{BC,L}$ for Q_L.

Table 1. Purpose of DTL Elements

Element	Purpose
D_I	Input diode, limits I_{IH}, and provides ANDing
ρR_B	Limits I_{IL}
$(1 - \rho)R_B$	Self-biases Q_L
Q_L	Base-emitter level shifting for shift of transition width and provides base driving current to Q_O
D_L	Level shifting diode for shift of transition width
R_D	Provides discharge path for saturation stored charge removal from base of Q_O
Q_O	Output inverting BJT and output low driver for current sinking pull-down
R_C	Passive current sourcing pull-up

Table 2. State of Diodes and BJTs for Output High and Low Levels

Element	V_{OH}	V_{OL}
D_I	On	Cutoff
Q_L	Cutoff	Forward active
D_L	Cutoff	On
Q_O	Cutoff	Saturated

DTL NAND GATE

Adding additional inputs to a DTL inverter, as in Fig. 5, provides a circuit that performs the NAND function. This can be seen by observing when any or all inputs are low,

$$\begin{aligned} V_X &= V_{IN}(\text{low}) + V_{D,I}(ON) \\ &< V_{BE,L}(FA) + V_{D,L}(ON) + V_{BE,O}(FA) \end{aligned}$$

and Q_O is cutoff with

$$V_{OUT} = V_{OH} = V_{CC}$$

When all inputs are high, V_X is high, allowing Q_O to saturate (provided that ρR_B is chosen properly) and

$$V_{OUT} = V_{CE,O}(SAT) = V_{OL}$$

Thus, this basic DTL logic family provides the logical NAND operation.

DTL FAN-OUT

In determining the maximum fan-out for DTL logic gates, we consider the case where $V_{OUT} = V_{OL}$ for the driving gate. The opposite case, where $V_{OUT} = V_{OH}$ for the driving gate, reverse-biases the input diodes of all load gates. Such gates sink very little current and hence do not impose a current limitation on fan-out. On the other hand, a low driving gate output voltage is established with all driving gate inputs high, and fan-out is limited for this situation.

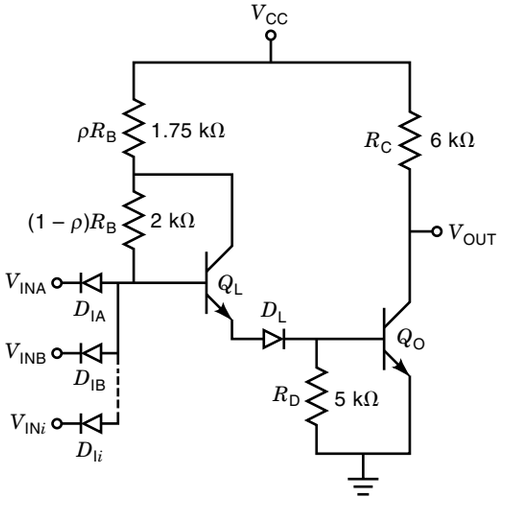

Figure 5. 930 Series DTL NAND gate.

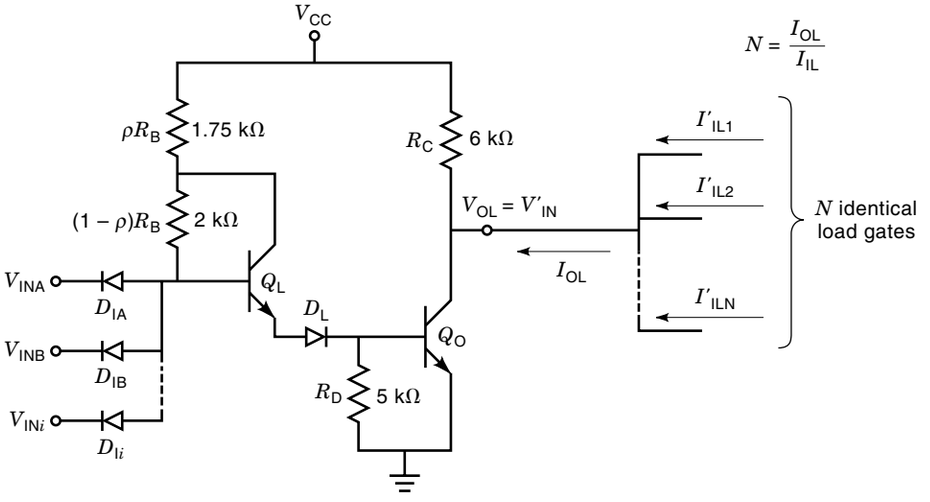

Figure 6. DTL NAND gate in output low state driving N gates.

The maximum fan-out is obtained by determining how much output current I_{OL} the driving gate can sink from multiple, identical output gates as depicted in Fig. 6. Since each load gate will have the same input current I_{IL}, from Kirchhoff's current law we obtain

$$NI_{IL} = I_{OL}$$

or

$$N = \frac{I_{OL}}{I_{IL}}$$

To determine N, we use Fig. 7, which shows one of the load gates explicitly with $V_{OUT} = V'_{IN} = V_{OL}$. Note that the individual device and components in the output load gate have a prime to distinguish the load gate components from the driving gate components.

Input Low Current (I_{IL})

I_{IL} is found by following dashed path 1 of Fig. 7, and then writing this current as the difference in voltage across the resistors in series divided by the sum of the resistors. Hence,

$$I'_{\rho RB} = I_{IL} = \frac{V'_{CC} - V'_{D,I}(ON) - V_{CE,O}(SAT)}{\rho R'_B + (1-\rho)R'_B}$$
$$= \frac{V_{CC} - V_D(ON) - V_{CE}(SAT)}{R_B} = I_{RB}$$

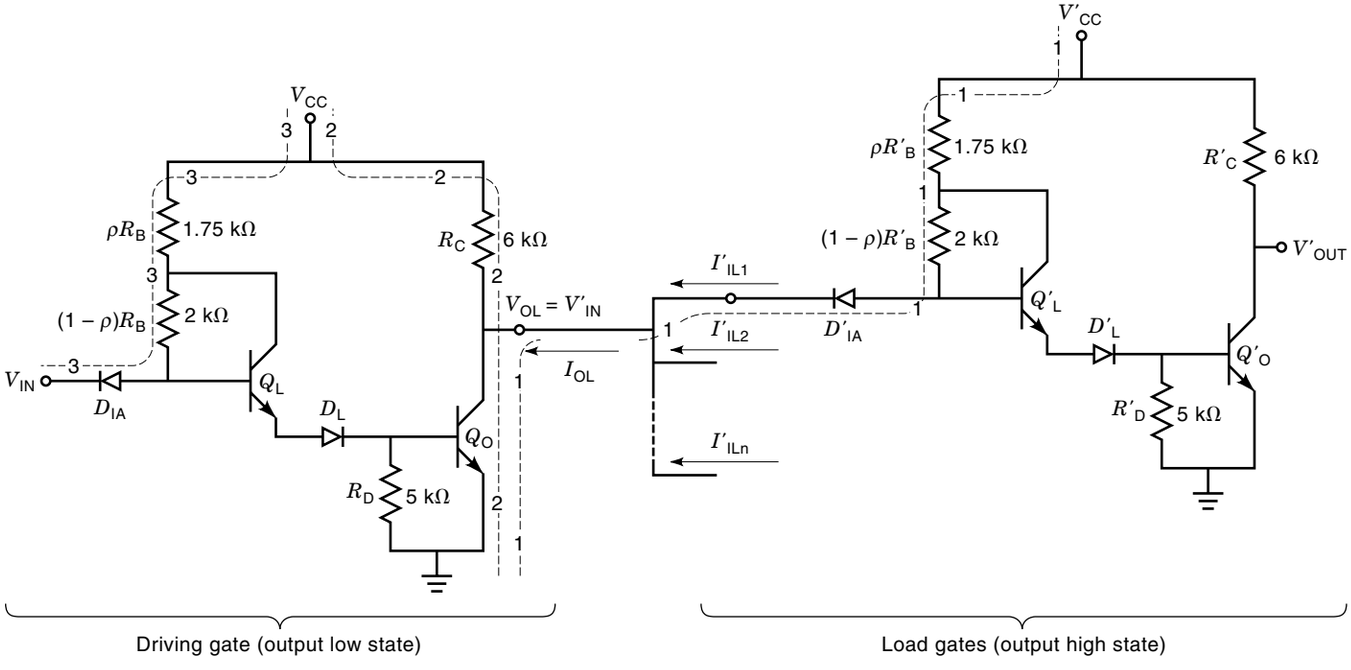

Figure 7. Cascaded DTL gates for fan-out and power calculations.

Output Low Current (I_{OL})

I_{OL} is found by writing Kirchoff's current law (KCL) at the collector of Q_O where

$$I_{OL} = I_{C,O}(\text{SAT}) - I_{RC}$$

The current through R_C is found by following dashed path 2 of Fig. 7, yielding

$$I_{RC} = \frac{V_{CC} - V_{CE,O}(\text{SAT})}{R_C}$$

The collector current of Q_O(SAT) is obtained from

$$I_{C,O}(\text{SAT}) = \sigma_{OL}\beta_F I_{B,O}(\text{SAT})$$

where σ_{OL} is the saturation parameter, smaller for deeper saturation (larger $I_{B,O}$). However, for maximum fan-out, we consider operation at the edge of saturation where $\sigma = 1$ and

$$I_{C,O}(\text{SAT}) = I_{C,O}(EOS) = \beta_F I_{B,O}(\text{EOS})$$

To determine this quantitatively, we write KCL at the base of Q_O to obtain

$$I_{B,O} = I_{E,L} - I_{RD}$$

where

$$I_{RD} = \frac{V_{BE,O}(\text{SAT})}{R_D}$$

The emitter current of Q_L is found by analyzing the portion of the driver gate including V_{CC}, ρR_B, $(1-\rho)R_B$, Q_L, D_L, and Q_O as redrawn in Fig. 8. Considering the base current of Q_L to be zero, the current through ρR_B is equal to the emitter current of Q_L and the emitter current of Q_L is

$$I_{E,L} = \frac{V_{CC} - V_{BE,L}(\text{FA}) - V_{D,L}(\text{ON}) - V_{BE,O}(\text{SAT})}{\rho R_B}$$

The following example indicates the use of these equations.

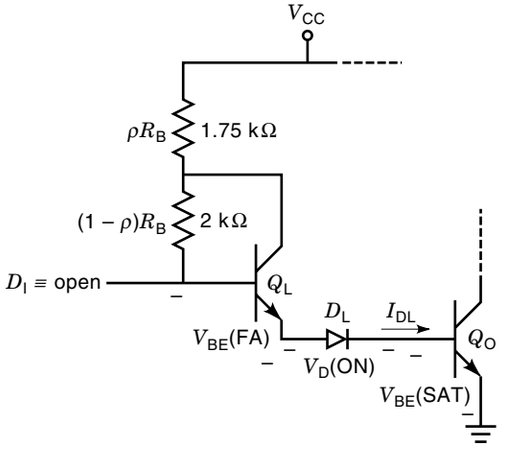

Figure 8. Portion of DTL driving gate.

Example 2. DTL Fan-Out. Calculate the fan-out for the DTL inverter of Fig. 6 considering the circuit in Fig. 7 and the subcircuit in Fig. 8. Let $\beta_F = 49$, V_{BE}(FA) = 0.7 V, V_{BE}(SAT) = 0.8 V, and V_{CE}(SAT) = 0.2 V for the BJTs and let V_D(ON) = 0.7 V for the diodes. Also, use $\sigma_{OL} = 0.85$ for the output low state and $V_{CC} = 5$ V.

SOLUTION. Substituting these values directly into the derived equations yields

$$I_{IL} = I_{\rho RB} = \frac{(5) - (0.7) - (0.2)}{(3.75\ \text{k}\Omega)} = 1.09\,\text{mA}$$

$$I_{RC} = \frac{(5) - (0.2)}{(6\ \text{k}\Omega)} = 800\,\mu\text{A}$$

$$I_{E,L} = \frac{(5) - 2(0.7) - (0.8)}{(0.467)(3.75\ \text{k}\Omega)} = 1.60\,\text{mA}$$

$$I_{RD} = \frac{(0.8)}{(5\ \text{k}\Omega)} = 160\ \mu\text{A}$$

$$I_{B,O} = (1.60\ \text{mA}) - (160\ \mu\text{A}) = 1.44\,\text{mA}$$

$$I_{C,O} = (0.85)(49)(1.44\ \text{mA}) = 60\,\text{mA}$$

$$I_{OL} = (60\ \text{mA}) - (800\ \mu\text{A}) = 59.2\,\text{mA}$$

$$N = \frac{(59.2\ \text{mA})}{(1.09\ \text{mA})} = 54.3$$

Hence, the fan-out of this DTL gate is 54. Note that $I_{B,O}$ = 1.40 mA is indeed large enough to saturate Q_O.

DTL POWER DISSIPATION

To determine the average power dissipation of a DTL gate, we first determine the currents being supplied by V_{CC} for both the high and the low output states. Notice that these currents have already been obtained in the fan-out analysis of the previous section.

Output High Current Supplied [I_{CC}(OH)]

For the output high state the input is low [i.e., V_{CE}(SAT)], and considering dashed path 3 in Fig. 7, we have

$$I_{\rho RB}(\text{OH}) = I_{IL} = \frac{V_{CC} - V_D(\text{ON}) - V_{CE}(\text{SAT})}{R_B}$$

Since Q_O is cutoff, I_{RC}(OH) = 0, and

$$I_{CC}(OH) = I_{\rho RB}(OH)$$

Output Low Current Supplied [I_{CC}(OL)]

For the low output state, the input is high, then

$$I_{\rho RB}(\text{OL}) = I_{E,L} = \frac{V_{CC} - V_{BE}(\text{FA}) - V_D(\text{ON}) - V_{BE}(\text{SAT})}{\rho R_B}$$

Additionally, the current through R_C for this output low state is simply

$$I_{RC}(\text{OL}) = \frac{V_{CC} - V_{CE}(\text{SAT})}{R_C}$$

Thus,

$$I_{CC}(\text{OL}) = I_{\rho RB}(\text{OL}) + I_{RC}(\text{OL})$$

Average Power Dissipation [P_D(avg)]

The average power dissipated is now found by substituting into

$$\begin{aligned} P_D(\text{avg}) &= \frac{I_{CC}(\text{OH}) + I_{CC}(\text{OL})}{2} V_{CC} \\ &= \frac{I_{\rho RB}(\text{OH}) + I_{\rho RB}(\text{OL}) + I_{RC}(\text{OL})}{2} V_{CC} \end{aligned}$$

Example 3. DTL Power Dissipation. Calculate the average power dissipation for the DTL gate in Example 2.

SOLUTION. Direct substitution of the values calculated in Example 2 yields

$$\begin{aligned} P_D(\text{avg}) &= \frac{(1.09\text{ mA}) + (1.60\text{ mA}) + (800\ \mu\text{A})}{2} \\ &= 8.73\,\text{mW} \end{aligned}$$

Compared to metal–oxide–semiconductor (MOS) logic families, this amount of power dissipation is quite large.

CONCLUSIONS

Although DTL logic circuitry can be fabricated quite conveniently in IC form, this family has many disadvantages and was only used extensively prior to the introduction of TTL. In the 1990s, there are numerous other logic families that offer improvement in all aspects of operation.

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THOMAS A. DEMASSA
Arizona State University

JOHN CICCONE
VLSI Technology, Inc.