DIFFERENTIAL AMPLIFIERS

AMPLIFICATION OF DIFFERENCE AND DC SIGNALS

Differential amplifiers represent a class of amplifiers, which amplify the difference between two signals, including dc. To obtain their desired characteristics, differential amplifiers critically depend on component matching. Therefore, discrete realizations, based on vacuum tubes or transistors, necessitate careful component pairing, which is not just painstaking for the design engineer, but also significantly raises the amplifier's cost. In contrast, integrated circuit technology with its inherent small relative component tolerances is particularly suited for this application.

It is a well-known fact that the active elements used for amplification are far from linear devices. To circumvent the problems associated with the nonlinear input–output relationship, the amplifier circuit in a typical application is linearized through the selection of a suitable operating point. An example of an elementary single-stage amplifier is shown in Fig. 1. While the circuit includes a bipolar transistor, it can readily be adapted to MOS technology, or even vacuum tubes. In Fig. 1, the input bias and dc level at the output are separated from the desired input–output signals by means of coupling capacitors C_{ci} and C_{co}. The role of the emitter degeneration resistor R_O is to reduce the drift of the operating point. Further, the decoupling capacitor C_O counteracts the gain reduction associated with the insertion of R_O. Obviously, the presence of coupling and decoupling capacitors makes the circuit in Fig. 1 unsuitable for dc amplification. But, even at low frequencies this amplifier is impractical, due to the large capacitor values required, which, in turn, give rise to large RC time constants and, consequently, slow recovery times from any transient disturbances.

The requirement to avoid capacitors in low-frequency or dc amplifiers leads to a mixing of the concepts of bias and signal.

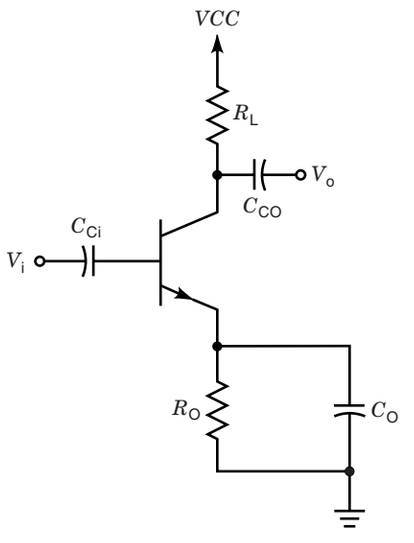

Figure 1. Single-transistor amplifier.

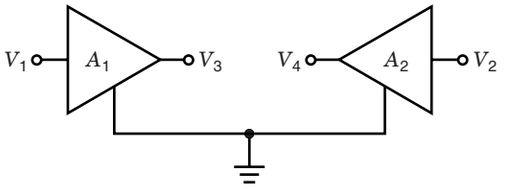

Figure 2. Conceptual drawing of a differential amplifier.

A second characteristic of such amplifiers is the application of symmetry to compensate for the drift of the active components. An intuitive solution appears to lie in the use of two amplifiers, connected in a difference configuration, as illustrated in Fig. 2. For this circuit one can write the following equations:

$$V_3 = A_1 V_1 \tag{1}$$

$$V_4 = A_2 V_2 \tag{2}$$

Assuming A_1 approximately equal to A_2, that is, $A_1 = A + \Delta/2$ and $A_2 = A - \Delta/2$, yields

$$V_3 - V_4 = A(V_1 - V_2) + \frac{\Delta}{2}(V_1 + V_2) \tag{3}$$

$$V_3 + V_4 = A(V_1 + V_2) + \frac{\Delta}{2}(V_1 - V_2) \tag{4}$$

Clearly, when both amplifiers are perfectly matched or $\Delta = 0$, the difference mode is completely separated from the sum mode. Upon further reflection, though, the difference amplifier of Fig. 2 is not really the solution to the amplification problem under consideration. Indeed, in many instances, small signals, which sit on top of large pedestal voltages, need to be amplified. For example, assume $A = 100$, a difference signal of 10 mV and a bias voltage equal to 10 V. The amplifier scheme of Fig. 2 would result in a 1 V difference signal, in addition to a 1000 V output voltage common to both amplifiers. It is clearly unrealistic to assume that both amplifiers will remain linear and matched over such extended voltage range. Instead, the real solution is obtained by coupling the amplifiers. The resulting arrangement is known as the differential pair amplifier.

In the mathematical description of the differential pair, four amplification factors are generally defined to express the relationship between the differential or difference (subscript D) and common or sum mode (subscript C) input and output signals. Applied to the circuit in Fig. 2, one can write

$$V_3 - V_4 = V_{oD} = A_{DD} V_{iD} + A_{DC} V_{iC} \tag{5}$$

$$V_3 + V_4 = 2V_{oC} = 2A_{CC} V_{iC} + 2A_{CD} V_{iD} \tag{6}$$

where $V_{iD} = V_1 - V_2$ and $V_{iC} = (V_1 + V_2)/2$. The ratio A_{DD}/A_{CC} is commonly referred to as the amplifier's common-mode rejection ratio or CMRR. While an amplifier's CMRR is an important characteristic, maximizing its value is not a designer's goal, in itself. Rather, the real purpose is to suppress large sum signals, so that the two amplifiers exhibit a small output swing and, thereby, operate indeed as a matched pair.

Furthermore, the ultimate goal is to avoid that the application of a common-mode input signal results in a differential signal at the output. This objective can only be accomplished through a combination of careful device matching, precise selection of the amplifier's bias and operating point, as well as by a high common-mode rejection. While we have only considered differential output signals up to this point, in some instances a single-ended output is desired. Equations (5) and (6) can be rearranged as

$$V_3 = V_{oC} + \frac{1}{2}V_{oD} = \left(A_{CD} + \frac{1}{2}A_{DD}\right)V_{iD} + \left(A_{CC} + \frac{1}{2}A_{DC}\right)V_{iC} \tag{7}$$

$$V_4 = V_{oC} - \frac{1}{2}V_{oD} = \left(A_{CD} - \frac{1}{2}A_{DD}\right)V_{iD} + \left(A_{CC} - \frac{1}{2}A_{DC}\right)V_{iC} \tag{8}$$

One concludes that in the single-ended case all three ratios A_{DD}/A_{CC}, A_{DD}/A_{CD}, and A_{DD}/A_{DC} must be high, to yield the desired result.

Vacuum-tube-based differential circuits are not discussed in this article, which is devoted solely to mainstream integrated circuit technology, more specifically, bipolar junction and MOS field effect transistors. The next section provides an in-depth analysis of the bipolar version of the differential pair, also known as the emitter-coupled pair. The subsequent treatment of the MOS source-coupled pair adheres to a similar outline, with an emphasis on similarities, as well as important differences.

BIPOLAR DIFFERENTIAL PAIRS (EMITTER-COUPLED PAIRS)

Figure 3 depicts the basic circuit diagram of a bipolar differential pair. A differential signal V_{iD} is applied between the bases of two transistors, which, unless otherwise noted, are assumed to be identical. The dc bias voltage V_{bias} and a common-mode signal V_{iC} are also present. The transistors' common emitter node is connected to ground through a biasing

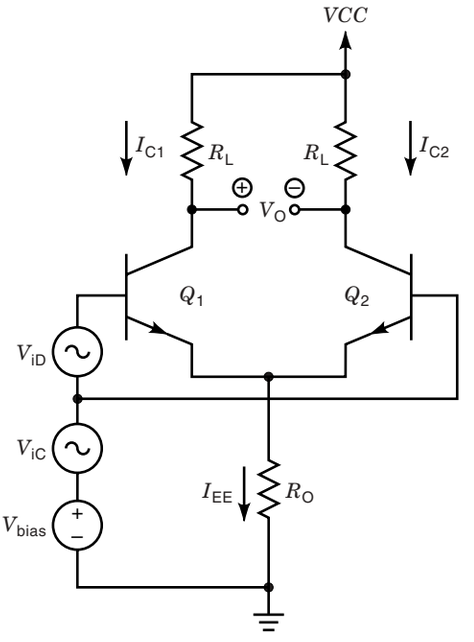

Figure 3. Bipolar differential pair (emitter-coupled pair).

network, which, for simplicity, is represented by a single resistor R_O. The amplifier output is taken differentially across the two collectors, which are tied to the power supply VCC, by means of a matched pair of load resistors R_L.

Low-Frequency Large-Signal Analysis

Applying the bipolar transistor's Ebers–Moll relationship with $V_{be} \gg V_T$ (where $V_T = kT/q$ is the thermal voltage) and assuming that both transistors are matched (i.e., the saturation currents $I_{S1} = I_{S2}$), the difference voltage V_{iD} can be expressed as follows:

$$V_{iD} = V_{be1} - V_{be2} = V_T \ln\left(\frac{I_{C1}}{I_{C2}}\right) \tag{9}$$

After some manipulation and substituting $I_{C1} + I_{C2} = \alpha I_{EE}$ (the total current flowing through R_O), one gets

$$I_{C1} = \frac{\alpha I_{EE}}{1 + \exp\left(\dfrac{-V_{iD}}{V_T}\right)} \tag{10}$$

$$I_{C2} = \frac{\alpha I_{EE}}{1 + \exp\left(\dfrac{V_{iD}}{V_T}\right)} \tag{11}$$

where α is defined as $\beta/(\beta + 1)$.

Since $V_{oD} = -R_L(I_{C1} - I_{C2})$, the expression for the differential output voltage V_{oD} becomes

$$\begin{aligned} V_{oD} &= -\alpha R_L I_{EE} \frac{\exp\left(\dfrac{V_{iD}}{2V_T}\right) - \exp\left(\dfrac{-V_{iD}}{2V_T}\right)}{\exp\left(\dfrac{V_{iD}}{2V_T}\right) + \exp\left(\dfrac{-V_{iD}}{2V_T}\right)} \\ &= -\alpha R_L I_{EE} \tanh\left(\frac{V_{iD}}{2V_T}\right) = -\alpha R_L I_{EE} \tanh x \end{aligned} \tag{12}$$

From Eq. (12) one observes that the transfer function is quite non-linear. When $V_{iD} > 2V_T$, the current through one of the two transistors is almost completely cut off and for further increases in V_{iD} the differential output signal eventually clips at $-\alpha R_L I_{EE}$. On the other hand, for small values of x, $\tanh x \approx x$. Under this small-signal assumption,

$$A_{DD} = \frac{V_{oD}}{V_{iD}} = -\frac{\alpha I_{EE}}{2V_T} R_L = -g_m R_L \tag{13}$$

While the next subsection contains a more rigorous small-signal analysis, a noteworthy observation here is that, under conditions of equal power dissipation, the differential amplifier of Fig. 3 has only one-half the transconductance value and, hence, only one-half the gain of a single transistor amplifier. From Eq. (13) one furthermore concludes that, when the tail current I_{EE} is derived from a voltage source, which is proportional to absolute temperature (PTAT), and a resistor of the same type as R_L, the transistor pair's differential gain is determined solely by a resistor ratio. As such, the gain is well controlled and insensitive to absolute process variations.

An intuitive analysis of the common-mode gain can be carried out under the assumption that R_O is large (for example, assume R_O represents the output resistance of a current source). Then, a common-mode input signal V_{iC} results only in a small current change i_C through R_O and, therefore, V_{be} remains approximately constant. With $i_C \approx V_{iC}/R_O$ and $V_{oC} = -R_L i_C/2$, the common-mode gain can be expressed as

$$A_{CC} = \frac{V_{oC}}{V_{iC}} \approx -\frac{R_L}{2R_O} \tag{14}$$

Combining Eqs. (13) and (14) yields

$$\mathrm{CMRR} = \frac{A_{DD}}{A_{CC}} \approx 2g_m R_O \tag{15}$$

Half Circuit Equivalents

Figure 4 illustrates the derivation of the common-emitter circuit's differential mode half circuit equivalent representation.

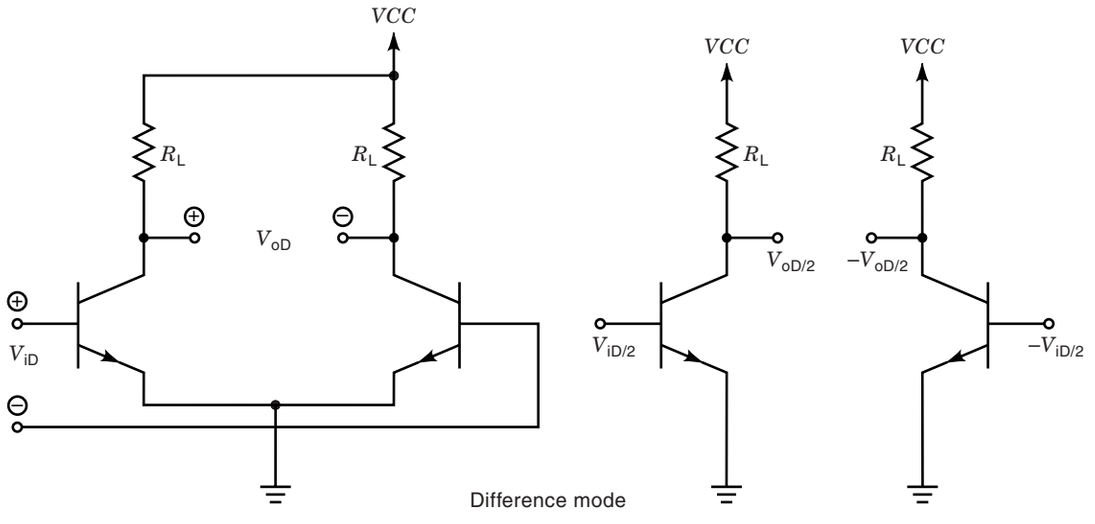

Figure 4. Derivation of the emitter-coupled pair's half circuit equivalent for difference signals.

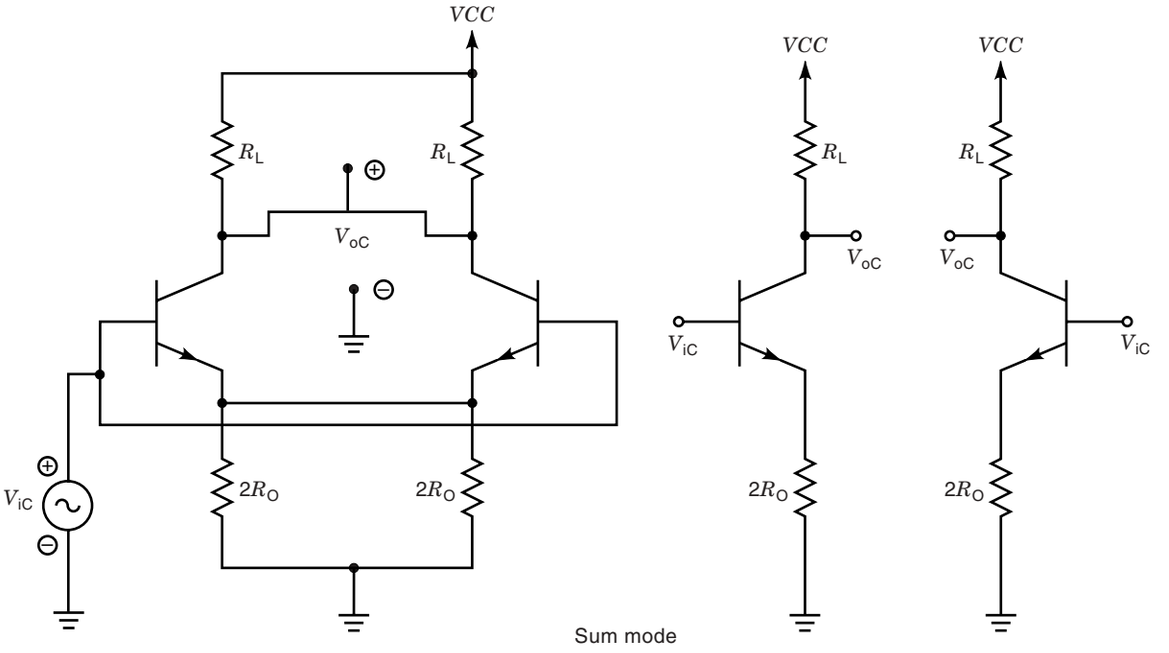

Figure 5. Derivation of the emitter-coupled pair's half circuit equivalent for common-mode signals.

For a small differential signal, the sum of the currents through both transistors remains constant and the current through R_O is unchanged. Therefore, the voltage at the emitters remains constant. The transistors operate as if no degeneration resistor were present, resulting in a high gain. In sum mode, on the other hand, the common resistor R_o provides negative feedback, which significantly lowers the common-mode gain. In fact, with identical signals at both inputs, the symmetrical circuit can be split into two halves, each with a degeneration resistor $2R_O$, as depicted in Fig. 5.

Low-Frequency Small-Signal Analysis

Figure 6 represents the low-frequency small-signal differential mode equivalent circuit wherein R_{SD} models the corresponding source impedance. Under the presumption of matched devices,

$$A_{DD} = \frac{V_{oD}}{V_{iD}} = -g_m R_L \frac{r_\pi}{r_\pi + r_b + \frac{1}{2} R_{SD}} \tag{16}$$

With $r_b \ll r_\pi$ and assuming a low-impedance voltage source, Eq. (14) can be simplified to $-g_m R_L$ as was previously derived in Eq. (13). The low-frequency common-mode equivalent circuit is shown in Fig. 7. Under similar assumptions as in Eq. (16) and with R_{SC} representing the common-mode source impedance, one finds

$$A_{CC} = \frac{V_{oC}}{V_{iC}} = -g_m R_L \frac{r_\pi}{r_\pi + r_b + 2R_{SC} + 2(\beta + 1)R_O} \tag{17}$$

Upon substitution of $\beta = g_m r_\pi \gg 1$, Eq. (17) reduces to $-R_L/2R_O$, the intuitive result obtained earlier in Eq. (14).

The combination of Eqs. (16) and (17) leads to

$$\text{CMRR} = \frac{A_{DD}}{A_{CC}} = \frac{r_\pi + r_b + 2R_{SC} + 2(\beta + 1)R_O}{r_\pi + r_b + \frac{1}{2} R_{SD}} \approx 2g_m R_O \tag{18}$$

Consider the special case where R_O models the output resistance of a current source, implemented by a single bipolar transistor. Then, $R_O = V_A/I_{EE}$, where V_A is the transistor's Early voltage. With $g_m = \alpha I_{EE}/2V_T$,

$$\text{CMRR} = \frac{\alpha V_A}{V_T} \tag{19}$$

which is independent of the amplifier's bias conditions, but only depends on the process technology and temperature. At room temperature, with $\alpha \approx 1$ and $V_A \approx 25$ V, the amplifier's CMRR is approximately 60 dB. The use of an improved current source, for example, a bipolar transistor in series with an emitter degeneration resistor R_D, can significantly increase the CMRR. More specifically,

$$\text{CMRR} = \frac{\alpha V_A}{V_T} \left(1 + \frac{I_{EE} R_D}{V_T}\right) \tag{20}$$

For $I_{EE}R_D = 250$ mV, the CMRR in Eq. (20) is eleven times higher than in Eq. (19).

In addition to expressions for the gain, the emitter-coupled pair's differential and common-mode input resistances can readily be derived from the small-signal circuits in Figs. 6 and 7.

$$R_{inD} = 2r_\pi \tag{21}$$

$$R_{inC} = \frac{1}{2} r_\pi + R_O(\beta + 1) \tag{22}$$

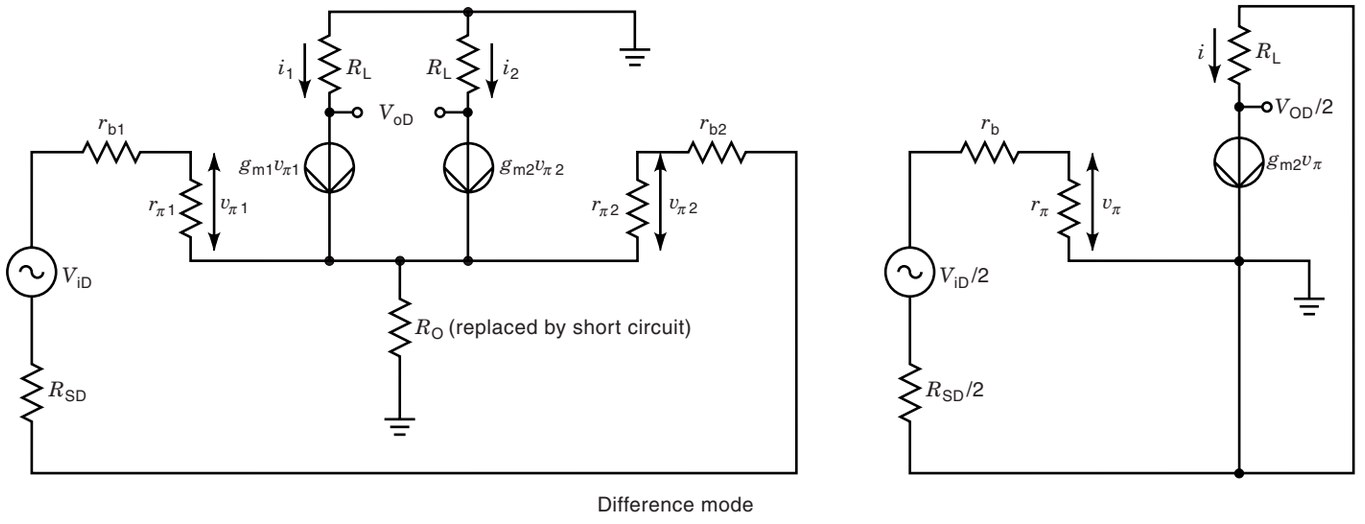

Figure 6. Differential mode small-signal equivalent circuit for the emitter-coupled pair. The complete circuit is on the left and the half circuit equivalent is on the right.

Taking into account the thermal noise of the transistors' base resistances and the load resistors R_L, as well as the shot noise caused by the collector currents, the emitter-coupled pair's total input referred squared noise voltage per hertz is given by

$$\frac{V_{iN}^2}{\Delta f} = 8kT\left(r_b + \frac{1}{2g_m} + \frac{1}{g_m^2 R_L}\right) \tag{23}$$

Due to the presence of base currents, there is also a small input noise current, which, however, will be ignored here and in further discussions.

Small-Signal Frequency Response

When the emitter-base capacitance C_π, the collector-base capacitance C_μ, the collector-substrate capacitance C_{cs}, and the transistor's output resistance r_o are added to the transistor's hybrid-π small-signal model in Fig. 6, the differential gain transfer function becomes frequency dependent. With R_i representing the parallel combination of $(R_{sD}/2 + r_b)$ with r_π, and R_C similarly designating the parallel combination of R_L with r_o, Eq. (16) must be rewritten as

$$A_{DD} = -\frac{g_m R_i R_C}{\frac{1}{2}R_{sD} + r_b}\frac{N(s)}{D(s)} \tag{24}$$

where

$$\frac{N(s)}{D(s)} = \frac{1 - \dfrac{sC_\mu}{g_m}}{1 + s(C_\pi R_i + C_\mu R_i + C_\mu R_C + C_\mu R_i R_C g_m + C_{cs}R_C) + s^2(C_\pi C_{cs} R_i R_C + C_\pi C_\mu R_i R_C + C_\mu C_{cs} R_i R_C)} \tag{25}$$

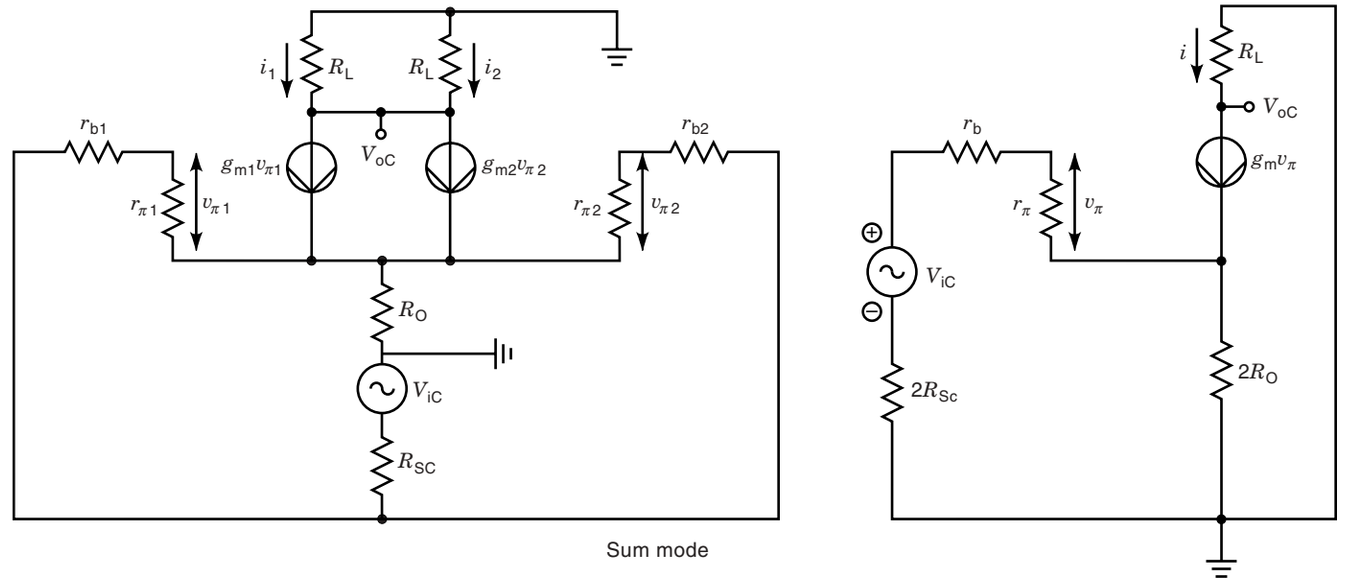

Figure 7. Common-mode small-signal equivalent circuit for the emitter-coupled pair. The complete circuit is on the left and the half circuit equivalent is on the right.

One observes that Eq. (25) contains a right half-plane zero located at $s_z = g_m/C_\mu$, resulting from the capacitive feedthrough from input to output. However, this right half-plane zero is usually at a frequency sufficiently high for it to be ignored in most applications. Furthermore, in many cases, one can assume that $D(s)$ contains a dominant pole p_1 and a second pole p_2 at a substantially higher frequency. If the dominant pole assumption is valid, $D(s)$ can be factored in the following manner:

$$D(s) = \left(1 - \frac{s}{p_1}\right)\left(1 - \frac{s}{p_2}\right) \approx 1 - \frac{s}{p_1} + \frac{s^2}{p_1 p_2} \tag{26}$$

Equating Eqs. (25) and (26) yields

$$p_1 = -\frac{1}{R_i}\frac{1}{C_\pi + C_{cs}\dfrac{R_C}{R_i} + C_\mu\left(1 + g_m R_C + \dfrac{R_C}{R_i}\right)} \tag{27}$$

$$p_2 = -\frac{1}{R_C(C_\mu + C_{cs})}\frac{C_\pi + C_{cs}\dfrac{R_C}{R_i} + C_\mu\left(1 + g_m R_C + \dfrac{R_C}{R_i}\right)}{C_\pi + \dfrac{C_\mu C_{cs}}{C_\mu + C_{cs}}} \tag{28}$$

The collector-base capacitance C_μ in Eqs. (27) and (28) appears with a multiplication factor, which is essentially equal to the amplifier's gain. This phenomenon is widely referred to as the Miller effect.

Rather than getting into a likewise detailed analysis, the discussion of the emitter-coupled pair's common-mode frequency response is limited here to the effect of the unavoidable capacitor C_0 (representing, for instance, the collector-base and collector-substrate parasitic capacitances of the BJT), which shunts R_0. The parallel combination of R_0 and C_0 yields a zero in the common-mode transfer function. Correspondingly, a pole appears in the expression for the amplifier's CMRR. Specifically,

$$\text{CMRR} = 2g_m\frac{R_O}{1 + sC_O R_O} \tag{29}$$

The important conclusion from Eq. (29) is that at higher frequencies the amplifier's CMRR rolls off by 20 dB per decade.

Dc Offset

Input Offset Voltage. Until now, perfect matching between like components has been assumed. While ratio tolerances in integrated circuit technology can be very tightly controlled, minor random variations between "equal" components are unavoidable. These minor mismatches result in a differential output voltage, even if no differential input signal is applied. When the two bases in Fig. 3 are tied together, but the transistors and load resistors are slightly mismatched, the resulting differential output offset voltage can be expressed as

$$\begin{aligned} V_{oO} &= -(R_L + \Delta R_L)(I_C + \Delta I_C) + R_L I_C \\ &= -(R_L + \Delta R_L)(I_S + \Delta I_S)\exp\left(\frac{V_{be}}{V_T}\right) + R_L I_S \exp\left(\frac{V_{be}}{V_T}\right) \end{aligned} \tag{30}$$

or

$$\begin{aligned} V_{oO} &\approx -\left(\frac{\Delta R_L}{R_L} + \frac{\Delta I_S}{I_S}\right) R_L I_S \exp\left(\frac{V_{be}}{V_T}\right) \\ &= -\left(\frac{\Delta R_L}{R_L} + \frac{\Delta I_S}{I_S}\right) R_L I_C \end{aligned} \tag{31}$$

Conversely, the output offset can be referred back to the input through a division by the amplifier's differential gain.

$$V_{iO} = \frac{V_{oO}}{-g_m R_L} = V_T\left(\frac{\Delta R_L}{R_L} + \frac{\Delta I_S}{I_S}\right) \tag{32}$$

The input referred offset voltage V_{iO} represents the voltage, which must be applied between the input terminals, in order to nullify the differential output voltage. In many instances, the absolute value of the offset voltage is not important, because it can easily be measured and canceled, either by an auto-zero technique or by trimming. Rather, when offset compensation is applied, the offset stability under varying environmental conditions becomes the primary concern. The drift in offset voltage over temperature can be calculated by differentiating Eq. (32).

$$\frac{dV_{iO}}{dT} = \frac{V_{iO}}{T} \tag{33}$$

From Eq. (33) one concludes that the drift is proportional to the magnitude of the offset voltage, and inversely related to the change in temperature.

Input Offset Current. Since, in most applications, the differential pair is driven by a low-impedance voltage source, its input offset voltage is an important parameter. Alternatively, the amplifier can be controlled by high-impedance current sources. Under this condition, the input offset current I_{iO}, which originates from a mismatch in the base currents, is the offset parameter of primary concern. Parallel to the definition of V_{iO}, I_{iO} is the value of the current source, which must be placed between the amplifier's open-circuited input terminals to reduce the differential output voltage to zero.

$$I_{iO} = \frac{I_C + \Delta I_C}{\beta + \Delta\beta} - \frac{I_C}{\beta} \approx \frac{I_C}{\beta}\left(\frac{\Delta I_C}{I_C} - \frac{\Delta\beta}{\beta}\right) \tag{34}$$

The requirement of zero voltage difference across the output terminals can be expressed as

$$(R_L + \Delta R_L)(I_C + \Delta I_C) = R_L I_C \tag{35}$$

Eq. (35) can be rearranged as

$$\frac{\Delta I_C}{I_C} \approx -\frac{\Delta R_L}{R_L} \tag{36}$$

Substituting Eq. (36) into Eq. (34) yields

$$I_{iO} = -\frac{I_{EE}}{2\beta}\left(\frac{\Delta R_L}{R_L} + \frac{\Delta\beta}{\beta}\right) \tag{37}$$

I_{iO}'s linear dependence on the bias current and its inverse relationship to the transistors' current gain β, as expressed by Eq. (37), intuitively make sense.

Gain Enhancement Techniques

From Eq. (13) one concludes that there are two ways to increase the emitter-coupled pair's gain, namely, an increase in the bias current or the use of a larger valued load resistor. However, practical limitations of the available supply voltage and the corresponding limit on the allowable $I * R$ voltage drop across the load resistors, in order to avoid saturating either of the two transistors, limit the maximum gain that can be achieved by a single stage. This section introduces two methods, which generally allow the realization of higher gain without the dc bias limitations.

Negative Resistance Load. In the circuit of Fig. 8 a gain boosting positive feedback circuit is connected between the output terminals. The output dc bias voltage is simply determined by *VCC*, together with the product of R_L and the current flowing through it, which is now equal to $(I_E + I_R)/2$. However, for ac signals the added circuit, consisting of two transistors with cross-coupled base-collector connections and the resistors R_C between the emitters, represents a negative resistance of value $-(R_C + 1/g_{mc})$ where $g_{mc} =$

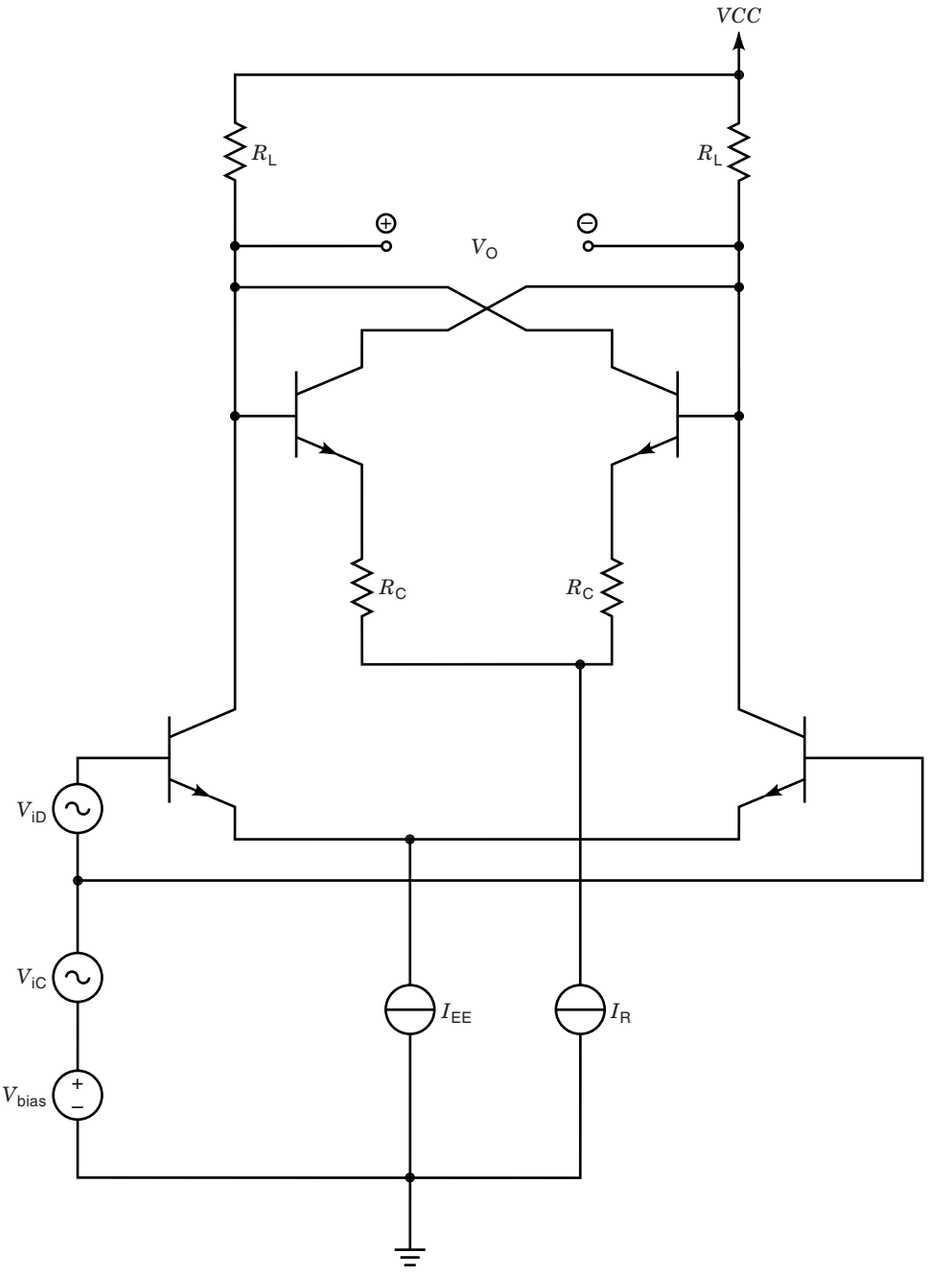

Figure 8. Emitter-coupled pair with negative resistance load circuit, used to increase the amplifier's gain.

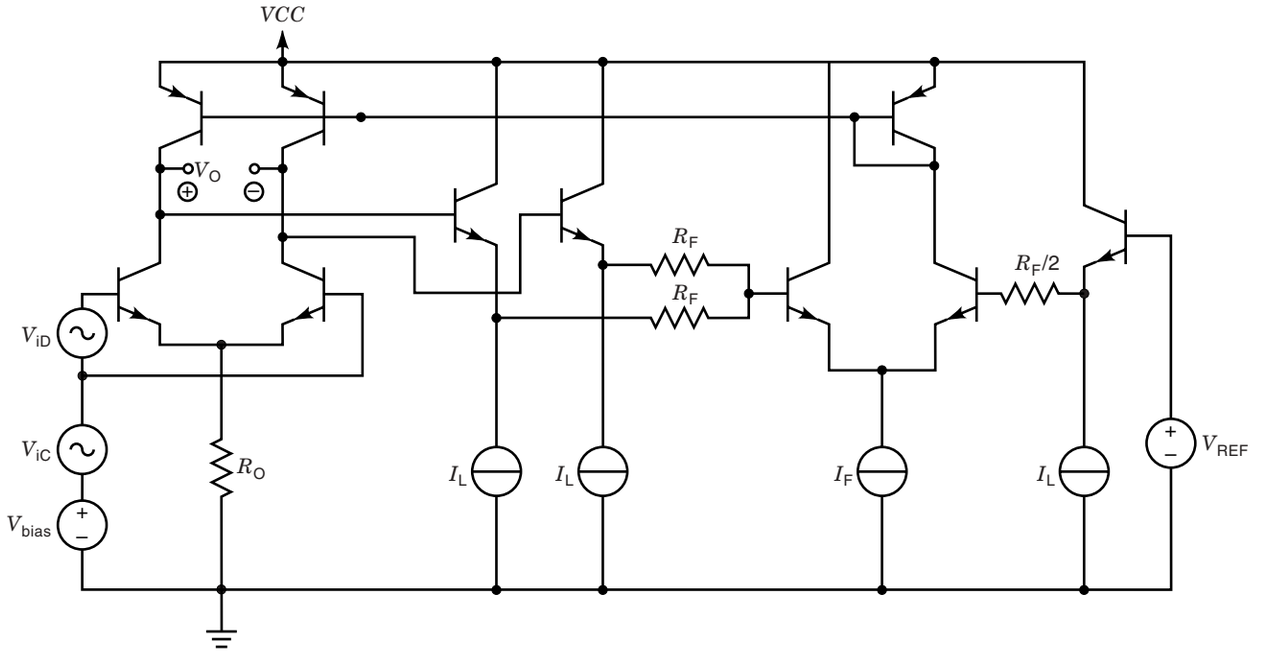

Figure 9. Fully differential emitter-coupled pair with active current source loads and common-mode feedback circuit.

$\alpha I_R/2V_T$. The amplifier's differential gain can now be expressed as

$$A_{DD} \approx -g_m R_L \frac{1}{1 - \dfrac{g_{mc} R_L}{1 + g_{mc} R_C}} \tag{38}$$

Active Load. Another approach to increase the gain consists of replacing the load resistors by active elements, such as *pnp* transistors. Figure 9 shows a fully differential realization of an emitter-coupled pair with active loads. The differential gain is determined by the product of the transconductance of the input devices and the parallel combination of the output resistances of the *npn* and *pnp* transistors. Since $g_m = I_C/V_T$, $r_{on} = V_{An}/I_C$ and $r_{op} = V_{Ap}/I_C$, the gain becomes

$$A_{DD} = -g_m \frac{V_{An} V_{Ap}}{(V_{An} + V_{Ap}) I_C} = -\frac{1}{V_T} \frac{V_{An} V_{Ap}}{V_{An} + V_{Ap}} \tag{39}$$

Consequently, the gain is independent of the bias conditions. The disadvantage of the fully differential realization with active loads is that the output common-mode voltage is not well defined. If one were to use a fixed biasing scheme for both types of transistors in Fig. 9, minor, but unavoidable mismatches between the currents in the *npn* and *pnp* transistors will result in a significant shift of the operating point. The solution lies in a common-mode feedback circuit (CMFB), which controls the bases of the active loads and forces a predetermined voltage at the output nodes. The CMFB circuit has high gain for common-mode signals, but does not respond to differential signals present at its inputs. A possible realization of such CMFB circuit is seen in the right portion of Fig. 9. Via emitter followers and resistors R_F, the output nodes are connected to one input of a differential pair, whose other input terminal is similarly tied to a reference voltage V_{REF}. The negative feedback provided to the *pnp* load transistors forces an equilibrium state in which the dc voltage at the output terminals of the differential pair gain stage are equal to V_{REF}. The need for CMFB can be avoided in a single-ended implementation as shown in Fig. 10. Contrary to the low

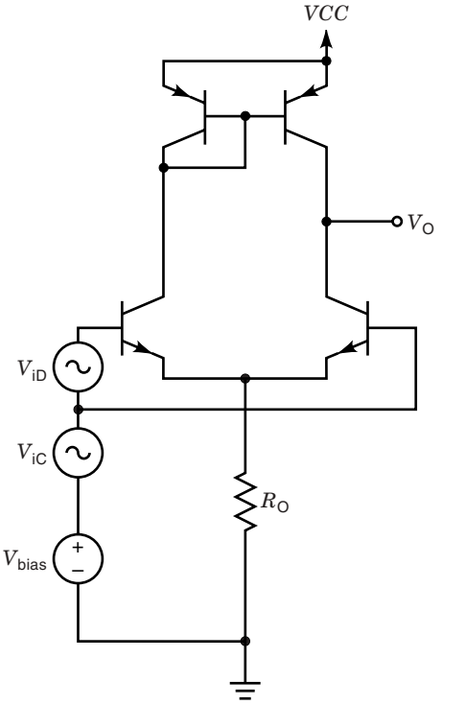

Figure 10. Single-ended output realization of an emitter-coupled pair with active loads.

CMRR of a single-ended realization with resistive loads, the circuit in Fig. 10 inherently possesses the same CMRR as a differential realization since the output voltage depends on a current differencing as a result of the *pnp* mirror configuration. The drawback of the single-ended circuit is a lower frequency response, particularly when low-bandwidth lateral *pnp* transistors are used.

Linearization Techniques

As derived previously, the linear range of operation of the emitter-coupled pair is limited to approximately $V_{\text{iD}} \approx 2V_{\text{T}}$. This section describes two techniques, which can be used to extend the linear range of operation.

Emitter Degeneration

The most common technique to increase the linear range of the emitter-coupled pair relies on the inclusion of emitter degeneration resistors, as shown in Fig. 11. The analysis of the differential gain transfer function proceeds as before, however, no closed-form expression can be derived. Intuitively, the inclusion of R_{E} introduces negative feedback, which lowers the gain and extends the amplifier's linear operating region to a voltage range approximately equal to the product of $R_{\text{E}}I_{\text{E}}$. The small-signal differential gain can be expressed as

$$A_{\text{DD}} \approx -G_{\text{M}}R_{\text{L}} \tag{40}$$

where G_{M} is the effective transconductance of the degenerated input stage. Therefore,

$$G_{\text{M}} = \frac{g_{\text{m}}}{1+g_{\text{m}}R_{\text{E}}} \approx \frac{1}{R_{\text{E}}} \tag{41}$$

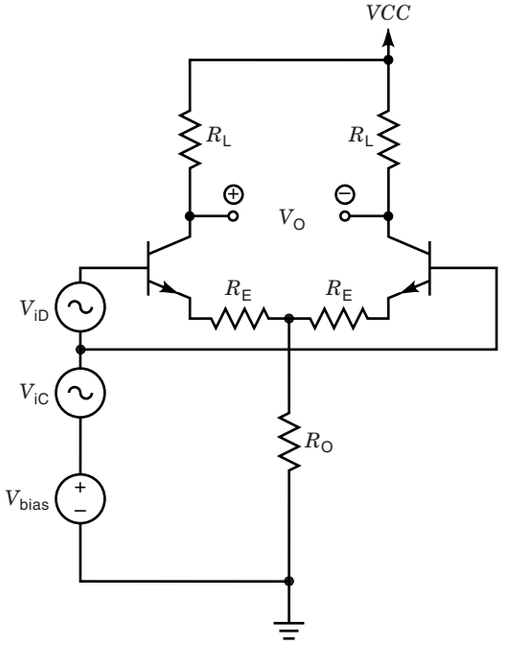

Figure 11. Bipolar differential pair with emitter degeneration resistors used to extend the linear input range.

Consequently,

$$A_{\text{DD}} \approx -\frac{g_{\text{m}}R_{\text{L}}}{1+g_{\text{m}}R_{\text{E}}} \tag{42}$$

In case $g_{\text{m}}R_{\text{E}} \gg 1$,

$$A_{\text{DD}} \approx -\frac{R_{\text{L}}}{R_{\text{E}}} \tag{43}$$

In comparison with the undegenerated differential pair, the gain is reduced by an amount $g_{\text{m}}R_{\text{E}}$, which is proportional to the increase in linear input range. The common-mode gain transfer function for the circuit in Fig. 11 is

$$A_{\text{CC}} \approx -\frac{R_{\text{L}}}{2R_{\text{O}}+R_{\text{E}}} \tag{44}$$

For practical values of R_{E}, A_{CC} remains relatively unchanged compared to the undegenerated prototype. As a result, the amplifier's CMRR is reduced approximately by the amount $g_{\text{m}}R_{\text{E}}$. Also, the input referred squared noise voltage per Hertz can be derived as

$$\frac{V_{\text{iN}}^2}{\Delta f} = 8kT\left[r_{\text{b}} + \frac{1}{2g_{\text{m}}}(g_{\text{m}}^2R_{\text{E}}^2) + \frac{1}{g_{\text{m}}^2R_{\text{L}}}(g_{\text{m}}^2R_{\text{E}}^2) + R_{\text{E}}\right] \tag{45}$$

This means that, to a first order, the noise too increases by the factor $g_{\text{m}}R_{\text{E}}$. Consequently, even though the amplifier's linear input range is increased, its signal-to-noise ratio (SNR) remains unchanged. To complete the discussion of the emitter degenerated differential pair, the positive effect emitter degeneration has on the differential input resistance R_{inD} and, to a lesser extent, on R_{inC} should be mentioned. For the circuit in Fig. 11,

$$R_{\text{inD}} = 2[r_\pi + (\beta+1)R_{\text{E}}] \tag{46}$$

$$R_{\text{inC}} = \frac{1}{2}r_\pi + \frac{(\beta+1)R_{\text{E}}}{2} + R_{\text{O}}(\beta+1) \tag{47}$$

Parallel Combination of Asymmetrical Differential Pairs. A second linearization technique consists of adding the output currents of two parallel asymmetrical differential pairs with respective transistor ratios $1:r$ and $r:1$, as shown in Fig. 12. The reader will observe that each differential pair in Fig. 12 is biased by a current source of magnitude $I_{\text{EE}}/2$, so that the power dissipation, as well as the output common-mode voltage, remain the same as for the prototype circuit in Fig. 3. Assuming, as before, an ideal exponential input voltage–output current relationship for the bipolar transistors, the following voltage transfer function can be derived:

$$V_{\text{oD}} = -\frac{\alpha}{2}I_{\text{EE}}R_{\text{L}}\left[\tanh\left(\frac{V_{\text{iD}}}{2V_{\text{T}}} - \frac{\ln r}{2}\right) + \tanh\left(\frac{V_{\text{iD}}}{2V_{\text{T}}} + \frac{\ln r}{2}\right)\right] \tag{48}$$

After Taylor series expansion and some manipulation, Eq. (48) can be rewritten as

$$V_{\text{oD}} = -\alpha I_{\text{EE}}R_{\text{L}}(1-d)\left[\frac{V_{\text{iD}}}{2V_{\text{T}}} + \left(d-\frac{1}{3}\right)\left(\frac{V_{\text{iD}}}{2V_{\text{T}}}\right)^3 + \cdots\right] \tag{49}$$

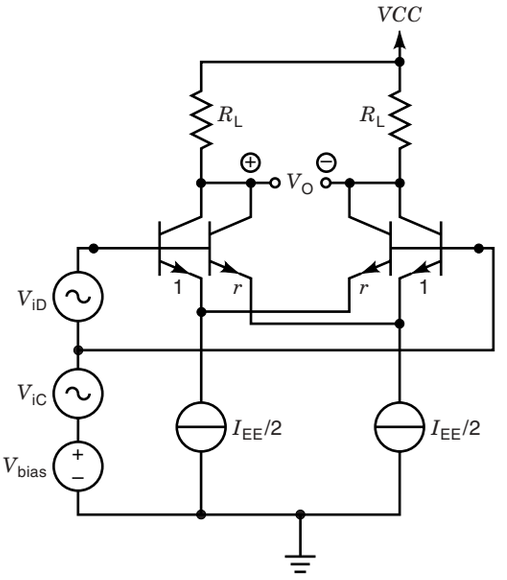

Figure 12. Two asymmetrical emitter-coupled pairs with respective transistor ratios $r:1$ and $1:r$. The collector currents are summed. If r is selected appropriately, the linear input range and SNR are increased.

where

$$d = \left(\frac{r-1}{r+1}\right)^2 \tag{50}$$

Equation (49) indicates that the dominant third harmonic distortion component can be canceled by setting $d = 1/3$ or $r = 2 + \sqrt{3} = 3.732$. The presence of parasitic resistances within the transistors tends to require a somewhat higher ratio r for optimum linearization. In practice, the more easily realizable ratio $r = 4$ (or $d = 9/25$) is frequently used. When the linear input ranges at a 1% total harmonic distortion (THD) level of the single symmetrical emitter-coupled pair in Fig. 3 and the dual circuit with $r = 4$ in Fig. 12 are compared, a nearly threefold increase is noted. For $r = 4$ and neglecting higher-order terms, Eq. (49) becomes

$$A_{DD} \approx -0.64 g_m R_L \tag{51}$$

where $g_m = \alpha I_{EE}/2V_T$ as before. Equation (51) means that the trade-off for the linearization is a reduction in the differential gain to 64 percent of the value obtained by a single symmetrical emitter-coupled pair with equal power dissipation. The squared input referred noise voltage per hertz for the two parallel asymmetrical pairs can be expressed as

$$\frac{V_{iN}^2}{\Delta f} = \frac{8kT}{(0.64)^2}\left(\frac{r_b}{5} + \frac{1}{2g_m} + \frac{1}{g_m^2 R_L}\right) \tag{52}$$

The factor $r_b/5$ appears because of an effective reduction in the base resistance by a factor $(r + 1)$, due to the presence of five transistors versus one in the derivation of Eq. (23). If the unit transistor size in Fig. 12 is scaled down accordingly, a subsequent comparison of Eqs. (23) and (52) reveals that the input referred noise for the linearized circuit of Fig. 12 is 1/0.64 or 1.56 times higher than for the circuit in Fig. 3. Combined with the nearly threefold increase in linear input range, this means that the SNR nearly doubles. The increase in SNR is a distinct advantage over the emitter degeneration linearization technique. Moreover, the linearization approach introduced in this section can be extended to a summation of the output currents of three, four, or more parallel asymmetrical pairs. However, there is a diminished return in the improvement. Also, for more than two pairs the required device ratios become quite large, and the sensitivity of the linear input range to small mismatches in the actual ratios versus their theoretical values increases as well.

Rail-to-Rail Common-Mode Inputs and Minimum Supply Voltage Requirement

With the consistent trend toward lower power supplies, the usable input common-mode range as a percentage of the supply voltage is an important characteristic of differential amplifiers. Full rail-to-rail input compliance is a highly desirable property. Particularly for low power applications, the ability to operate from a minimal supply voltage is equally important. For the basic emitter-coupled pair in Fig. 3, the input is limited on the positive side when the *npn* transistors saturate. Therefore,

$$V_{iC,pos} = V_{CC} - \frac{1}{2}R_L I_{EE} + V_{b_c,forward} \tag{53}$$

If one limits $R_L I_{EE}/2 < V_{bc,forward}$, $V_{iC,pos}$ can be as high as V_{CC} or even slightly higher. On the negative side, the common-mode input voltage is limited to that level, where the tail current source starts saturating. Assuming a single bipolar transistor is used as the current source,

$$V_{iC,neg} > V_{be} + V_{ce,sat} \approx 1\,\text{V} \tag{54}$$

The opposite relationships hold for the equivalent *pnp* transistor based circuit. As a result, the rail-to-rail common-mode input requirement can be resolved by putting two complementary stages in parallel. In general, as the input common-mode traverses between V_{CC} and ground, three distinct operating conditions can occur: at high voltage levels only the *npn* stage is active; at intermediate voltage levels both the *npn* and *pnp* differential pairs are enabled; finally, for very low input voltages only the *pnp* stage is operating. If care is not taken, three distinct gain ranges can occur: based on g_{mn} only; resulting from $g_{mn} + g_{mp}$; and, contributed by g_{mp} only. Nonconstant g_m and gain, which depends on the input common-mode, is usually not desirable for several reasons, not in the least in case of phase compensation if the differential pair is used as the first stage in an operational amplifier. Fortunately, the solution to this problem is straightforward if one recognizes that the transconductance of the bipolar transistor is proportional to its bias current. Therefore, the only requirement for a bipolar constant g_m complementary circuit with full rail-to-rail input compliance is that under all operating conditions the sum of the bias currents of the *npn* and *pnp* subcircuits remains

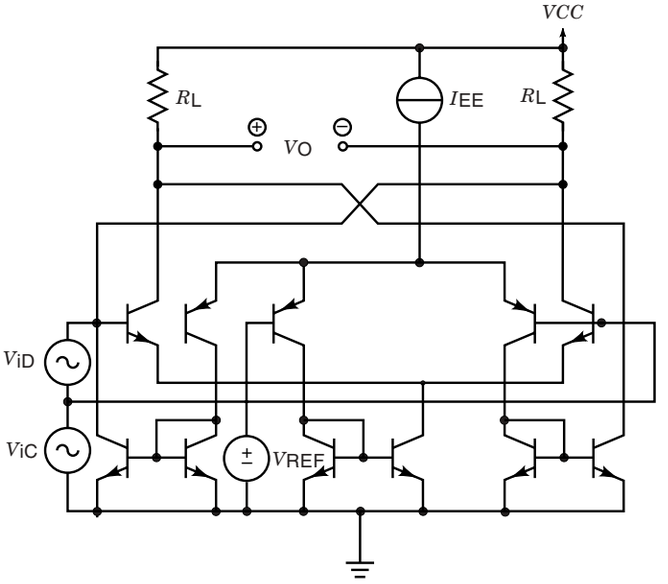

Figure 13. Complementary bipolar differential amplifier with rail-to-rail input common-mode compliance.

constant. A possible implementation is shown in Fig. 13. If $V_{iC} < VREF$, the *pnp* input stage is enabled and the *npn* input transistors are off. When $V_{iC} > VREF$, the bias current is switched to the *npn* pair and the *pnp* input devices turn off. For $R_L I_{EE}/2 < V_{cb,forward,n}$ the minimum required power supply voltage is $V_{be,n} + V_{be,p} + V_{ce,sat,n} + V_{ce,sat,p}$, which is lower than 2 V.

MOS DIFFERENTIAL PAIRS (SOURCE-COUPLED PAIRS)

The MOS equivalent of the emitter-coupled pair is the source-coupled pair. Since the analysis of both circuits is generally quite similar, the discussion of the source-coupled pair will be more concise with an emphasis on important differences.

Low-Frequency Large-Signal Analysis

Figure 14 depicts the source-coupled pair with a resistive load. When the MOS transistors are in the saturation region, their current–voltage relationship can be described by the square law characteristic.

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{gs} - V_t)^2 = K_p(V_{gs} - V_t)^2 \tag{55}$$

Using Eq. (55) and assuming perfect matching, the differential input voltage can be expressed as

$$V_{iD} = V_{gs1} - V_{gs2} = \sqrt{\frac{2I_{D1}}{\mu C_{ox}\dfrac{W}{L}}} - \sqrt{\frac{2I_{D2}}{\mu C_{ox}\dfrac{W}{L}}} = \sqrt{\frac{I_{D1}}{K_p}} - \sqrt{\frac{I_{D2}}{K_p}} \tag{56}$$

Equation (56) can be rearranged as

$$I_{D1} - I_{D2} = \frac{1}{2}\mu C_{ox}\frac{W}{L}V_{iD}\sqrt{\frac{4I_{DD}}{\mu C_{ox}\dfrac{W}{L}} - V_{iD}^2} = K_p V_{iD}\sqrt{\frac{2I_{DD}}{K_p} - V_{iD}^2} \tag{57}$$

where

$$I_{DD} = I_{D1} + I_{D2} \tag{58}$$

Hence, the relationship between the differential output and input voltages is

$$V_{oD} = -R_L(I_{D1} - I_{D2}) = -\frac{1}{2}\mu C_{ox}\frac{W}{L}R_L V_{iD}\sqrt{\frac{4I_{DD}}{\mu C_{ox}\dfrac{W}{L}} - V_{iD}^2}$$
$$= -K_p R_L V_{iD}\sqrt{\frac{2I_{DD}}{K_p} - V_{iD}^2} \tag{59}$$

As mentioned above, Eq. (59) is only valid as long as both transistors are in saturation or

$$V_{iD} \le \sqrt{\frac{2I_{DD}}{K_p}} \tag{60}$$

Similar to the bipolar case, Eq. (59) is quite nonlinear and the output voltage eventually clips when one of the input transistors is completely starved of current. However, unlike the emitter-coupled pair, the linear operating range of the source-coupled pair also depends on the bias current and device sizes. Equation (60) indicates that the linear range of operation can be expanded by increasing I_{DD} and/or reducing the W/L ratio of the MOS devices.

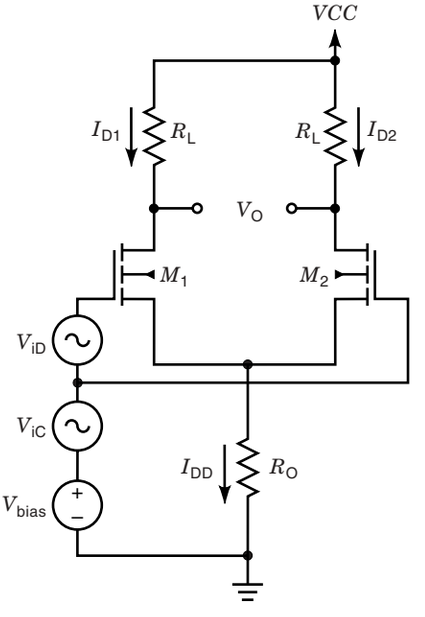

Figure 14. MOS differential pair (source-coupled pair) with resistive loads.

Low-Frequency Small-Signal Analysis

An expression for the small-signal transconductance of the source-coupled pair can be derived by taking the derivative of Eq. (57) with respect to the input voltage.

$$g_m = \frac{d(I_{D1} - I_{D2})}{dV_{iD}} \tag{61}$$

$$g_m = \sqrt{\mu C_{ox} \frac{W}{L} I_{DD}} = \sqrt{2K_p I_{DD}} = 2\sqrt{K_p I_D} = 2K_p(V_{gs} - V_t) \tag{62}$$

As was noted for the bipolar differential pair, the transconductance of the source-coupled pair is only equal to the transconductance of one of the input devices. However, in contrast to the bipolar transistor, g_m in Eq. (62) is only proportional to the square root of the bias current. Due to g_m's dependence on the mobility μ and the threshold voltage V_t, stabilization of g_m over temperature is not as straightforward as is the case for bipolar. Furthermore, g_m of the source-coupled pair is a function of the device size and the oxide capacitance.

Dc Offset

As pointed out previously, small device mismatches are unavoidable and they give rise to an offset voltage. Assuming such small differences in the circuit of Fig. 14 where the inputs are tied together, one can derive an expression for the output offset voltage as follows:

$$V_{oO} = -(R_L + \Delta R_L)(I_D + \Delta I_D) + R_L I_D \approx -R_L \Delta I_D - \Delta R_L I_D \tag{63}$$

The current mismatch ΔI_D can be expanded as

$$\begin{aligned} \Delta I_D &= (K_p + \Delta K_p)(V_{gs} - V_t - \Delta V_t)^2 - K_p(V_{gs} - V_t)^2 \\ &\approx -2K_p \Delta V_t (V_{gs} - V_t) + \Delta K_p (V_{gs} - V_t)^2 \\ &= -g_m \Delta V_t + \frac{\Delta K_p}{K_p} I_D \end{aligned} \tag{64}$$

Substituting Eqs. (62) and (64) into (63) yields

$$\begin{aligned} V_{oO} &= -g_m R_L \left[-\Delta V_t + \left(\frac{\Delta K_p}{K_p} + \frac{\Delta R_L}{R_L} \right) \frac{I_D}{g_m} \right] \\ &= -g_m R_L \left[-\Delta V_t + \left(\frac{\Delta K_p}{K_p} + \frac{\Delta R_L}{R_L} \right) \frac{(V_{gs} - V_t)}{2} \right] \end{aligned} \tag{65}$$

This output offset voltage can be referred to the input by dividing Eq. (65) by the amplifier's gain.

$$V_{iO} = \frac{V_{oO}}{-g_m R_L} = -\Delta V_t + \frac{(V_{gs} - V_t)}{2} \left(\frac{\Delta K_p}{K_p} + \frac{\Delta R_L}{R_L} \right) \tag{66}$$

The input referred offset voltage V_{io} is the voltage, which must be applied between the open-circuited gate terminals to cancel the differential voltage across the output nodes. Equation (66) indicates that V_{iO} is directly related to the mismatch of the threshold voltages. The second term in Eq. (66) is reminiscent of Eq. (32) for the bipolar differential pair. However, since the multiplicative term $(V_{gs} - V_t)/2$ in Eq. (66) is usually much larger than its counterpart V_T in

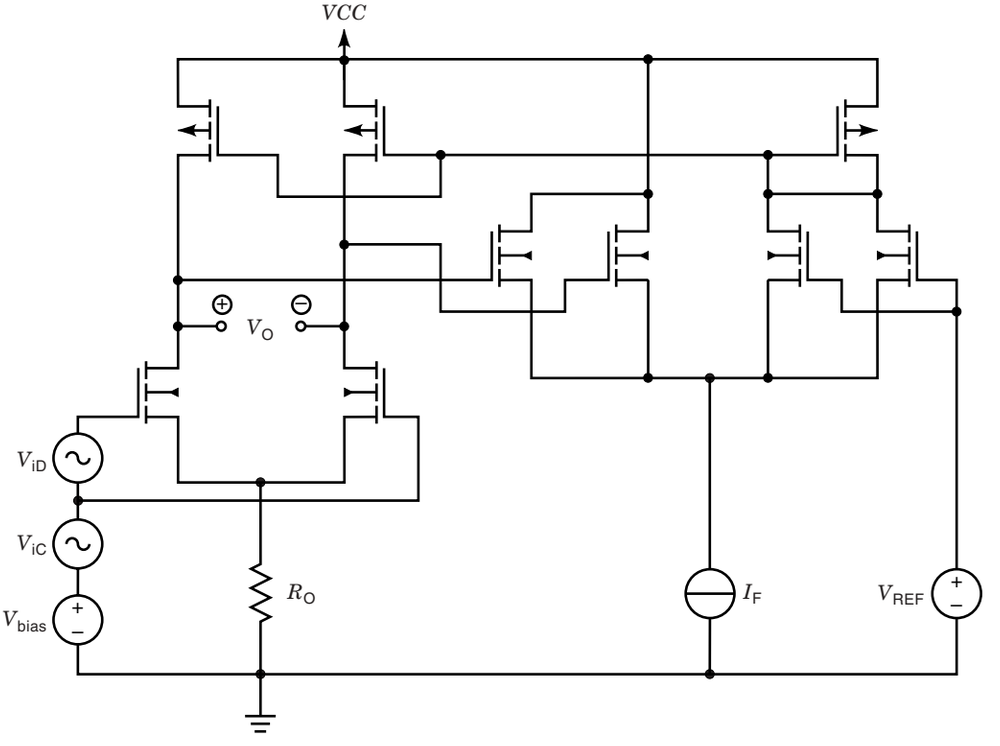

Figure 15. Fully differential source-coupled pair with active current source loads and common-mode feedback circuit.

Eq. (32), one concludes that the source-coupled pair is inherently subject to a larger offset voltage. On the other hand, the source-coupled pair has no input offset current since there is no gate current.

Active Load

Source-coupled pairs are almost exclusively used in conjunction with active loads. Figure 15 illustrates a fully differential realization, including a possible implementation of the required common-mode feedback circuit. Its operation is similar to the bipolar version in Fig. 9. A single-ended circuit is shown in Fig. 16.

Linearization

In addition to controlling the linear range of operation by proper selection of bias current and device sizes, the techniques discussed for the emitter-coupled pair can also be applied to the source-coupled pair. Figure 17 illustrates the application of source degeneration. However, the degeneration resistor is implemented by a MOS transistor, which operates in the linear region by connecting its gate to an appropriate control voltage V_C. The differential pair's gain can be adjusted by varying V_C. Similarly, the technique of multiple asymmetrical pairs in parallel can also be extended to the MOS domain.

Rail-to-Rail Common-Mode Input Signals

As for the bipolar case, the highly desirable rail-to-rail input voltage compliance can be obtained by a parallel combination of NMOS and PMOS differential pairs. However, the realization of a constant g_m over the whole range of operation is not as straightforward. One possible solution is to operate the MOS differential pairs in the subthreshold region, where the exponential current–voltage relationship holds and, as in the bipolar case, g_m is only a function of the bias current. Many circuits using MOS transistors in saturation require some kind of matching between the NMOS and PMOS devices, which is extremely difficult to achieve in mass production. Research into new circuit techniques to circumvent this problem continues and, judging by the numbers of recent papers on the subject, constitutes an area of significant contemporary academic interest.

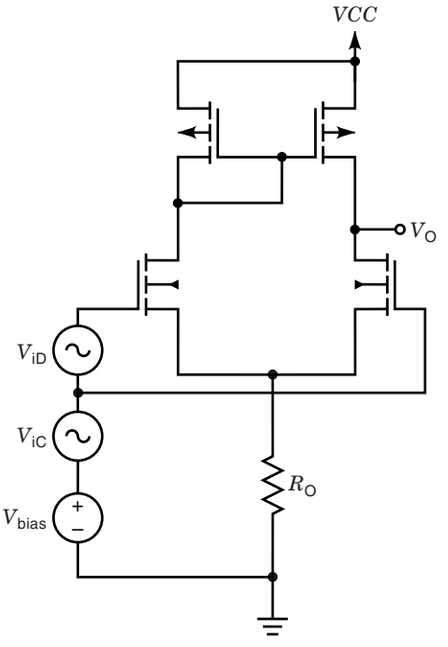

Figure 16. Single-ended output implementation of a source-coupled pair with active current source loads.

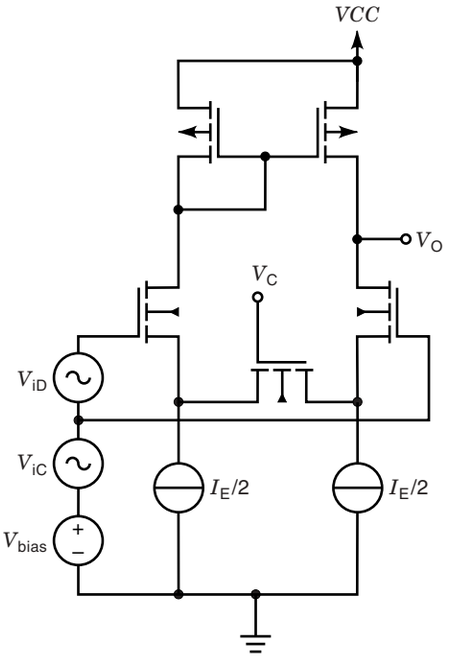

Figure 17. MOS differential pair with degeneration implemented by a MOS transistor in the linear region.

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DIFFERENTIAL EQUATIONS, ORDINARY. See ORDINARY DIFFERENTIAL EQUATIONS.

DIFFERENTIAL PAIRS. See DIFFERENTIAL AMPLIFIERS.

DIFFERENTIAL RESISTANCE, NEGATIVE. See NEGATIVE RESISTANCE.