## DATA ACQUISITION AND CONVERSION

Data acquisition and conversion pertain to the generation of signals from sensors, their conditioning, and their conversion into a digital format. In this article we describe typical sensors that generate signals and examples of data converter topologies suitable for sensor interfaces. We restrict ourselves to integrated implementations of sensors and sensor interface circuits. In particular, we target sensors and sensor interfaces that are compatible with CMOS fabrication technologies.

This article is organized as follows. First, we describe some examples of sensors and sensor interfaces; then we describe some sample data converter topologies. After that, we provide two complete design examples.

### SENSORS

Sensors are devices that respond to a physical or chemical stimulus and generate an output that can be used as a measure of the stimulus. The sensed inputs can be of many types: chemical, mechanical, electrical, magnetic, thermal, and so on. The input signal sensed by the sensor is then processed (amplified, converted from analog to digital, etc.) by some signal conditioning electronics, and the output transducer converts this processed signal into the appropriate output form. The primary purpose of interface electronics is to convert the sensor's signal into a format that is more compatible with the electronic system that controls the sensing system. The electric signals generated by sensors are usually small in amplitude. In addition to this, sensors often exhibit errors, such as offsets, drift, and nonlinearities, that can be compensated for with the correct interface circuitry. Analog elements have been improved substantially to achieve high speed and high accuracy; however, for many applications digital is still the preferred format. The sensors yield a wide variety of electric output signals: voltages, currents, resistances, and capacitances. The signal conditioning circuitry modifies the input signal into a format suitable for the follow-on data converter.

Figure 1 shows the system architecture for a sensor–actuator-based control system. The sensor(s) senses the external physical and chemical parameters and converts them into an electrical format. The sensed data are processed and digitized using integrated circuitry and transmitted to the host controller. The host uses this information to make the appropriate decisions, and information is fed back to the external environment through a set of actuators (1). These microprocessor-based controllers have revolutionized the design and use of instrumentation systems by allowing system operation to be defined in software, thus permitting a substantial increase in signal-processing and user-interface features. In general, a power supply is also connected to these blocks but is not explicitly shown in Fig. 1. If a sensor can provide a signal without a power supply, it is referred to as a self-generating sensor.

Integrated sensors are used in many applications, including automotive, manufacturing, environmental monitoring, avionics, and defense. In the past few years, integrated sensors that monolithically combine the sensor structure and some signal-processing interface electronics on the same substrate have begun to emerge. By combining microsensors and circuits, integrated smart sensors increase accuracy, dynamic range, and reliability and at the same time reduce size and cost. Some examples of semiconductor sensors are pressure sensors used in pneumatic systems, magnetic sensors used in position control, temperature sensors used in automotive systems, chemical sensors used in biological diagnostic systems, and acoustic emission sensors used in structural diagnostics.

In the next two sections we illustrate the use of sensors and sensor interfaces with the two most common types of sensors: resistive and capacitive sensors. We then describe two complete sensor systems that include an acoustic emission sensor and a temperature sensor.

#### Resistive Sensors

Sensors based on the variation of electric resistance are called *resistive* sensors. They can be further classified according to the physical quantity that they measure: thermal, magnetic, optical, and so on.

A *potentiometer* is a simple resistance measurement device in which the resistance is proportional to its length. However, the linearity of a potentiometer is limited because its resistance is not perfectly uniform. The resistance value also drifts with temperature. Applications of potentiometers are in the measurement of linear or rotary displacements.

Another simple and commonly used resistive sensor is the *strain gauge,* which is based on the variation of the resistance of a conductor or semiconductor when subjected to a mechanical stress. The variation in the resistance of a metal is given (2) by

$$R = R_0(1 + G\epsilon) \tag{1}$$

where $R_0$ is the resistance when there is no applied stress, $G$ is the *gauge factor,* and $\epsilon$ is the strain. There are a number of limitations on strain gauges, such as temperature dependence, light dependence, and inaccuracies in the measurement of a nonuniform surface; but in spite of these limitations, they are among the most popular sensors because of their small size and linearity.

Some of the applications of the strain gauge are in measuring force, torque, flow, acceleration, and pressure. Figure 2 shows a micromachined piezoresistive cantilever beam used as a strain gauge sensor. Strain gauges are capable of detecting deformations as small as 10 $\mu$m or lower.

A resistance temperature detector (RTD) is a temperature detector based on the variation in electric resistance. An increase in temperature increases the vibrations of atoms around their equilibrium positions, and this increases the resistance in a metal: Thus there is a positive temperature coefficient of resistance. The complete temperature dependence



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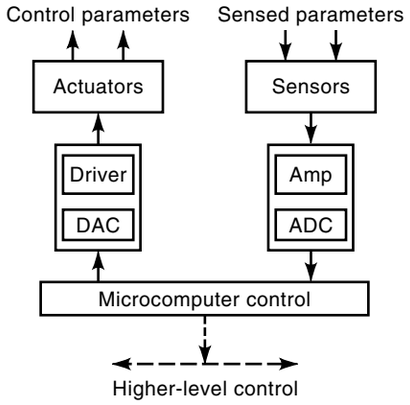


**Figure 1.** Overall system architecture of a sensor–actuator control system.

can be expressed (2) as

$$R = R_0(1 + \alpha_1 T + \alpha_2 T^2 + \cdots + \alpha_n T^n) \tag{2}$$

where $T$ is the temperature difference from the reference and $R_0$ is the resistance at the reference temperature.

The main advantages of these sensors are their high sensitivity, repeatability, and low cost. There are some limitations too. Firstly, to avoid destruction through self-heating, the RTD cannot measure temperatures near the melting point of the metal. Secondly, the change in temperature may cause physical deformations in the sensor. Additionally, for each metal there is only a small range over which the RTD is linear. The most common metals used for RTDs are platinum, nickel, and copper.

*Thermistors* are also temperature-dependent resistors but are made of semiconductors rather than metals. The temperature dependence of the resistance of a semiconductor is due to the variation in the available charge carriers. Semiconductors have a negative temperature coefficient, as the resistance is inversely proportional to the number of charge carriers. The temperature dependence of thermistors is given (2) by

$$R_T = R_0 \exp\left[B\left(\frac{1}{T} - \frac{1}{T_0}\right)\right] \tag{3}$$

where $T_0$ is the reference temperature, $R_0$ is the resistance at $T_0$, and $B$ is the characteristic temperature of the material, which itself is temperature-dependent. The limitations and advantages of a thermistor are similar to those of a RTD, except that the thermistor is less stable. There are many types of thermistors available, and each type has its own applications. The foil and bead types are suitable for temperature measurement, whereas the disk and rod types are suitable for temperature control. Some of the applications of thermistors are in the measurement of temperature, flow, level, and time delay. Two simple applications of thermistors are discussed below.

*Light-dependent resistors,* or LDRs, are devices whose resistance varies as a function of the illumination. LDRs are also known as photoconductors. The conductivity is primarily dependent on the number of carriers in the conduction band of the semiconductor material used. The basic working of the photoconductor is as follows. The valence and conduction bands in a semiconductor are quite close to each other. With increased illumination, electrons are excited from the valence to the conduction band, which increases the conductivity (reduces the resistance). The relation between resistance and optical radiation or illumination is given (2) by

$$R = AE^{-\alpha} \tag{4}$$

where $A$ and $\alpha$ are process constants, $R$ is the resistance, and $E$ is the illumination.

An important limitation of LDRs is their nonlinearity. Also, their sensitivity is limited by fluctuations caused by changes in temperature. Finally, the spectral response of LDRs is very narrow and primarily depends on the type of material used.

Some of the most common LDRs are made of PbS, CdS, and PbSe. Some applications of LDRs are shutter control in cameras and contrast and brightness control in television receivers.

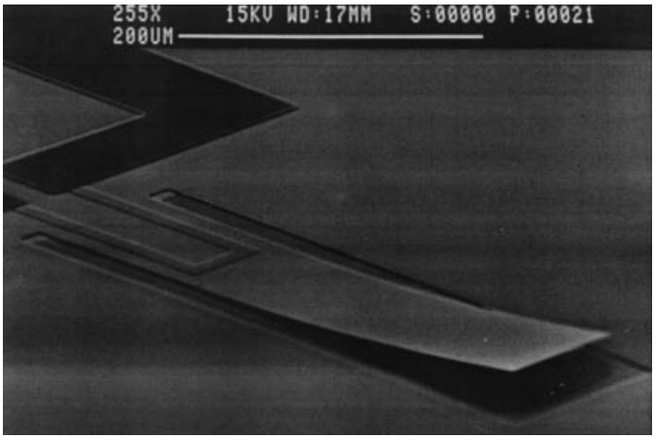


**Figure 2.** Micromachined piezoresistive cantilever beam used as a strain gauge sensor.

**Measurement Techniques for Resistive Sensors.** Various measurement techniques can be used with resistive sensors. The basic requirement for any measurement circuitry is a power supply to convert the change in resistance into a measurable output signal. In addition, it is often necessary to custom-build interface circuits for some sensors. For example, we may be required to add a linearization circuit for thermistors.

Resistance measurements can be made by either the deflection method or the nulling method. In the deflection method the actual current through the resistance or the voltage across the resistance is measured. In the nulling method a bridge is used.

The two-readings method is a fundamental approach to resistance measurement. A known resistance is placed in series with the unknown resistance as shown in Fig. 3. The voltage is then measured across each of them. The two voltages can

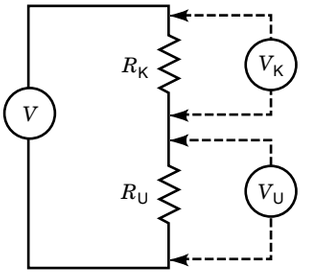


**Figure 3.** Two-readings method for resistance measurement.

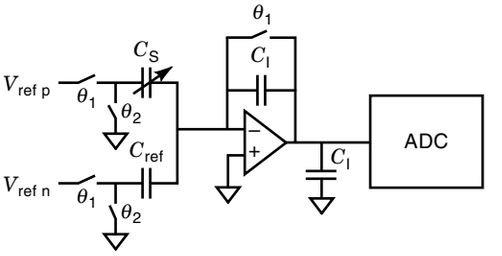


**Figure 5.** Capacitive sensor interface.

be written as

$$V_K = \frac{V}{R_K + R_U} R_K \tag{5}$$

$$V_U = \frac{V}{R_K + R_U} R_U \tag{6}$$

where $V$ is the supply voltage, $V_K$ and $R_K$ are the known voltage and resistance, and $V_U$ and $R_U$ are the unknown voltage and resistance. Thus from the above equations $R_U$ can be written as follows:

$$R_U = R_K \frac{V_U}{V_K} \tag{7}$$

A similar method is the *voltage divider,* in which the unknown resistance is once again calculated from known voltages and resistances. It is easier to resolve small voltage changes for low voltages than it is for high voltages. Thus to measure small changes in resistance, another voltage divider is placed in parallel to the one with the sensor. The parallel voltage dividers are designed to give the same voltage for no input. Thus the signal obtained by taking the difference between their output signals is totally dependent on the measured signal. This method of measuring small changes using parallel voltage dividers is called the *Wheatstone bridge method* (2–5). A simple Wheatstone bridge measurement method is shown in Fig. 4.

The Wheatstone bridge is balanced with the help of a feedback system, which adjusts the value of the standard resistor until the current through the galvanometer is zero. Once this is done, the value for $R_3$ is given by

$$R_3 = R_4 \frac{R_2}{R_1} \tag{8}$$

Thus the resistance $R_3$ is directly proportional to the change required in $R_4$ in order to balance the circuit.

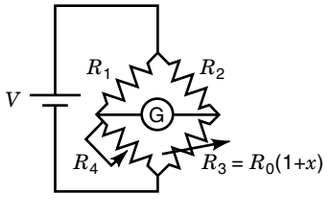


**Figure 4.** Simple Wheatstone bridge measurement method.

The Wheatstone bridge can also be used for deflection measurement. In this case, instead of measuring the change needed to balance the bridge, the voltage difference between the bridge outputs is measured or the current through the center arm is measured. This method is shown in Fig. 4. When the bridge is completely balanced (i.e., $x = 0$), $k$ is defined as follows:

$$k = \frac{R_1}{R_4} = \frac{R_2}{R_0} \tag{9}$$

Thus the voltage difference between the outputs can be written as follows.

$$V_0 = V\left(\frac{R_3}{R_2 + R_3} - \frac{R_4}{R_1 + R_4}\right) = V\frac{kx}{(k+1)(k+1+x)} \tag{10}$$

The maximum sensitivity for very small changes in $x$ is obtained when $k = 1$.

### Capacitive Sensors

Recently capacitive sensor have gained popularity. They generally exhibit lower temperature sensitivity, consume less power, and provide an overall higher sensor sensitivity with higher resolution than resistive sensors. For these reasons they have begun to show up in areas where resistive sensors were the norm. They are used in many applications such as pressure sensors and accelerometers. Capacitive sensors typically have one fixed plate and one moving plate that responds to the applied measurand. The capacitance between two plates separated by a distance $d$ is given by $C = \epsilon A/d$, where $\epsilon$ is the dielectric constant and $A$ is the area of the plate. It is easily seen that the capacitance is inversely proportional to the distance $d$.

For capacitive sensors there are several possible interface schemes. Figure 5 shows one of the most common capacitive sensor interfaces. The circuit is simply a charge amplifier, which transfers the difference of the charges on the sensor capacitor $C_S$ and the reference capacitor $C_{ref}$ to the integration capacitor $C_I$. If this interface is used in a pressure sensor, the sensing capacitor $C_S$ can be written as the sum of the sensor capacitor value $C_{S0}$ at zero pressure and the sensor capacitor variation $\Delta C_S(p)$ with applied pressure: $C_S = C_{S0} + \Delta C_S(p)$. In many applications $C_{S0}$ can be 5 to 10 times larger than the full-scale sensor capacitance variation $\Delta C_S(p)_{max}$; the reference capacitor $C_{ref}$ is used to subtract the nominal value of the sensor capacitor at half the pressure range, which is $C_{ref} = C_{S0} + \Delta C_S(p)_{max}/2$. This ensures that the transferred charge is

the charge that results from the change in the capacitance. This results in a smaller integration capacitor and increased sensitivity.

This type of capacitive interface is insensitive to the parasitic capacitance between the positive and negative terminals of the opamp, since the opamp maintains a virtual ground across the two terminals of the parasitic capacitor. This type of interface is also much faster than most other capacitive interfaces; its speed of operation is determined by the opamp's settling time. This technique also allows for the amplifier's offset and flicker noise to be removed very easily by using correlated double sampling or chopper stabilization. The resolution of this interface is in most cases limited by $kT/C$ noise and charge injection due to the switches.

There are a number of other sensor types, and two more will be discussed later in this article. However, we first describe the most common data converters that are used as part of sensor interfaces.

## DATA CONVERTERS

The analog signals generated and then conditioned by the signal conditioning circuit are usually converted into digital form via an analog-to-digital converter (ADC). In general, most of the signals generated by these sensors are in the low frequency region. For this reason, certain data converter topologies are particularly well suited as sensor interface subblocks. These include the charge redistribution implementation of the successive approximation converter, along with incremental and sigma–delta converters (6). In the following subsections we shall briefly describe successive approximation (incremental) and sigma–delta converters. Incremental and sigma–delta converters are very similar and the details of the former are later described extensively as part of a sample system design.

### Successive-Approximation Converter

A block diagram for the successive approximation converter is shown in Fig. 6. The successive approximation topology requires $N$ clock cycles to perform an $N$ bit conversion. For this reason, a sample-and-held (S/H) version of the input signal is provided to the negative input of the comparator. The comparator controls the digital logic circuit that performs the binary search. This logic circuit is called the successive approximation register (SAR). The output of the SAR is used to drive the digital-to-analog converter (DAC) that is connected to the positive input of the comparator.

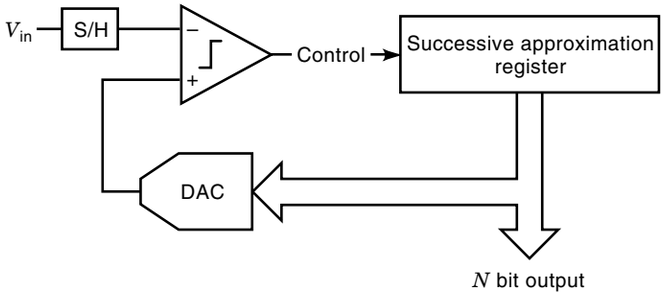


**Figure 6.** Successive approximation converter: block diagram.

During the first clock period the input is compared with the most significant bit (MSB). For this, the MSB is temporarily raised high. If the output of the comparator remains high, then the input lies somewhere between zero and $V_{ref}/2$ and the MSB is reset to zero. However, if the comparator output is low, then the input signal is somewhere between $V_{ref}/2$ and $V_{ref}$ and the MSB is set high. During the next clock period the MSB-1 bit is evaluated in the same manner. This procedure is repeated so that at the end of $N$ clock periods all $N$ bits have been resolved.

The charge-redistribution implementation of the successive approximation methodology is the most common topology in metal–oxide–semiconductor (MOS) technologies (7). The circuit diagram for a 4 bit charge redistribution converter is shown in Fig. 7. In this circuit the binary weighted capacitors $\{C, C/2, \ldots, C/8\}$ and the switches $\{S_1, S_2, \ldots, S_5\}$ form the 4 bit scaling DAC. For each conversion the circuit operates as a sequence of three phases. During the first phase (sample), switch $S_0$ is closed and all the other switches $S_1, S_2, \ldots, S_6$ are connected so that the input voltage $V_{in}$ is sampled onto all the capacitors. During the next phase (hold), $S_0$ is open and the bottom plates of all the capacitors are connected to ground, i.e., switches $S_1, S_2, \ldots, S_5$ are switched to ground. The voltage $V_x$ at the top plate of the capacitors at this time is equal to $-V_{in}$, and the total charge in all the capacitors is equal to $-2CV_{in}$. The final phase (redistribution) begins by testing the input voltage against the MSB. This is accomplished by keeping the switches $S_2, S_3, \ldots, S_5$ connected to ground and switching $S_1$ and $S_6$ so that the bottom plate of the largest capacitor is connected to $V_{ref}$. The voltage at the top plate of the capacitor is equal to

$$V_x = \frac{V_{ref}}{2} - V_{in} \tag{11}$$

If $V_x > 0$, then the comparator output goes high, signifying that $V_{in} < V_{ref}/2$, and switch $S_1$ is switched back to ground. If the comparator output is low, then $V_{in} > V_{ref}/2$, and $S_1$ is left connected to $V_{ref}$ and the MSB is set high. In a similar fashion the next bit, MSB-1, is evaluated. This procedure is continued until all $N$ bits have been resolved. After the conversion process the voltage at the top plate is such that

$$V_x = -V_{in} + \left( b_3 \frac{V_{ref}}{2^1} + b_2 \frac{V_{ref}}{2^2} + b_1 \frac{V_{ref}}{2^3} + b_0 \frac{V_{ref}}{2^4} \right) \tag{12a}$$

$$-\frac{V_{ref}}{2^4} < V_x < 0 \tag{12b}$$

where $b_i$ is 0 or 1 depending on whether bit $i$ was set to zero or one, and LSB is the least significant bit.

One of the advantages of the charge-redistribution topology is that the parasitic capacitance from the switches has little effect on its accuracy. Additionally, the clock feedthrough from switch $S_0$ only causes an offset, and those from switches $S_1, S_2, \ldots, S_5$ are independent of the input signal because the switches are always connected to either ground or $V_{ref}$. However, any mismatch in the binary ratios of the capacitors in the array causes nonlinearity, which limits the accuracy to 10 or 12 bits. Self-calibrating (8) techniques have been introduced that correct for errors in the binary ratios of the capacitors in charge redistribution topologies. However, these techniques are fairly complex, and for higher resolu-

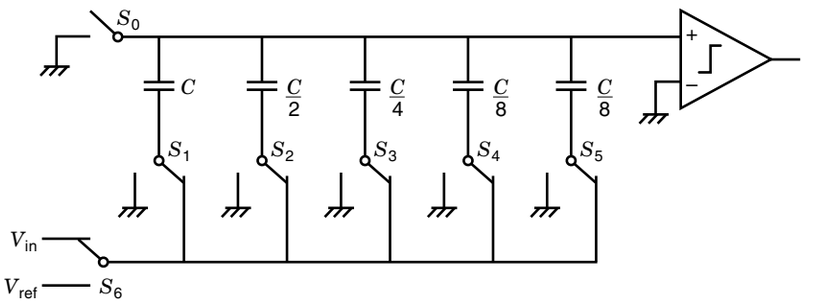


**Figure 7.** Charge-redistribution implementation of the successive approximation architecture.

tions sigma–delta converters are the preferred topology. We now briefly describe sigma–delta converters.

### Sigma–Delta Data Converters

Oversampling converters sample the input at a rate larger than the Nyquist frequency. If $f_S$ is the sampling rate, then $f_S/2f_0$ = OSR is called the *oversampling ratio.* Oversampling converters have the advantage over Nyquist rate converters that they do not require very tight tolerances from the analog components and that they simplify the design of the antialias filter. Sigma–delta converters (9) are oversampling single-bit converters that use frequency shaping of the quantization noise to increase resolution without increasing the matching requirements for the analog components.

Figure 8 shows a block diagram for a general noise-shaping oversampled converter. In a sigma–delta converter both the ADC and DAC shown in Fig. 8 are single-bit versions and as such provide perfect linearity. The ADC, a comparator in the case of a sigma–delta converter, quantizes the output of the loop filter, $H_1$. The quantization process approximates an analog value by a finite-resolution digital value. This step introduces a quantization error $Q_n$. Further, if we assume that the quantization noise is not correlated to the input, then the system can be modeled as a linear system. The output voltage for this system can now be written as

$$V_0 = \frac{Q_n}{1+H_1} + \frac{V_{in}H_1}{1+H_1} \tag{13}$$

For most sigma–delta converters $H_1$ has the characteristics of a low-pass filter and is usually implemented as a switched-capacitor integrator. For a first-order sigma–delta converter $H_1$ is realized as a simple switched-capacitor integrator, $H_1 = z^{-1}/(1 - z^{-1})$. Making this substitution in Eq. (13), we can write the transfer function for the first-order sigma–delta converter as

$$V_0 = V_{in}z^{-1} + Q_n(1 - z^{-1}) \tag{14}$$

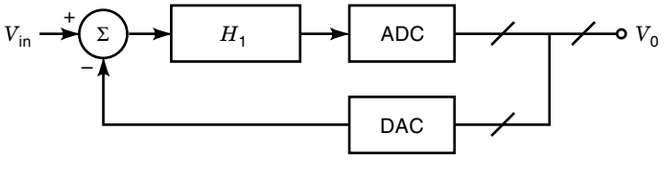


**Figure 8.** Figure for a general noise-shaping oversampled converter.

As can be seen from Eq. (16) below, the output is a delayed version of the input plus the quantization noise multiplied by the factor $1 - z^{-1}$. This function has a high-pass characteristic with the result that the quantization noise is reduced substantially at lower frequencies and increases slightly at higher frequencies. The analog modulator shown in Fig. 8 is followed by a low-pass filter in the digital domain that removes the out-of-band quantization noise. Thus we are left with only the in-band ($0 < f < f_0$) quantization noise. For simplicity the quantization noise is usually assumed to be white with a spectral density equal to $e_{rms}\sqrt{2/f_s}$. Further, if the OSR is sufficiently large, then we can approximate the root-mean-square (rms) noise in the signal band by

$$N_{f_0} \approx e_{rms}\frac{\pi}{3}\left(\frac{2f_0}{f_s}\right)^{3/2} \tag{15}$$

As the oversampling ratio increases, the quantization noise in the signal band decreases; for a doubling of the oversampling ratio the quantization noise drops by $20(\log 2)^{3/2} \approx 9$ dB. Therefore, for each doubling of the oversampling ratio we effectively increase the resolution of the converter by an additional 1.5 bits.

Clearly, $H_1$ can be replaced by other, higher-order functions that have low-pass characteristics. For example, in Fig. 9 we show a second-order modulator. This modulator uses one forward delay integrator and one feedback delay integrator to avoid stability problems. The output voltage for this figure can be written as

$$V_0 = V_{in}z^{-1} + Q_n(1 - z^{-1})^2 \tag{16}$$

The quantization noise is shaped by a second-order difference equation. This serves to further reduce the quantization noise at low frequencies, with the result that the noise power in the signal bandwidth falls by 15 dB for every doubling of the oversampling ratio. Alternatively, the resolution increases by 2.5 bits for every doubling of the oversampling ratio. In general, increasing the order of the filter will reduce the necessary oversampling ratio for a given resolution. However, for stability reasons, topologies other than the simple Candy-style (10) modulator discussed above are required for filter orders greater than two. Topologies that avoid this stability problem include the MASH and interpolative topologies (6).

For low-frequency inputs, the white noise assumption for the quantization noise breaks down. This results in *tones* which reduce the effective resolution of lower-order sigma–delta converters. Incremental converters utilize this observa-

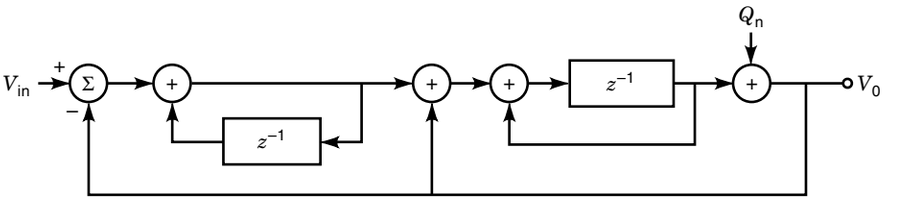


**Figure 9.** Modulator for second-order oversampled converter.

tion to simplify the low-pass filter that follows the sigma–delta converter. Details for the incremental converter are discussed below.

We now consider two system design examples. The first is an acoustic emission sensor system and the second is a temperature measurement system.

## SYSTEM DESIGNS EXAMPLES

We illustrate the sensor and sensor interface scenario with two examples. The first uses a piezoelectric acoustic emission sensor interfaced with a charge amplifier and a data converter. The second describes an integrated temperature sensor.

### Acoustic Emission Sensing System

Acoustic emission sensors are microsensors that are used for the detection of acoustic signals. These devices use elastic acoustic waves at high frequencies to measure physical, chemical, and biological quantities. Typically, integrated acoustic sensors can be made to be extremely sensitive and also to have a large dynamic range. The output of these sensors is usually a frequency, a charge, or a voltage.

The piezoelectric effect is one of the most convenient ways to couple elastic waves to electrical circuits. Piezoelectricity is caused by the electric polarization produced by mechanical strain in certain crystals. Conversely, an electric polarization will induce a mechanical strain in piezoelectric crystals. As a consequence, when a voltage is applied to the electrodes of a piezoelectric film, it elongates or contracts depending on the polarity of the field. Conversely, when a mechanical force is applied to the film, a voltage develops across the film. Some properties of a good piezoelectric film are wide frequency range, high elastic compliance, high output voltage, high stability in wet and chemical environments, high dielectric strength, low acoustic impedance, and low fabrication costs. Piezoelectric materials are anisotropic, and hence their electrical and mechanical properties depend on the axis of the applied electric force. The choice of the piezoelectric material depends on the application.

Crystalline quartz ($SiO_2$) is a natural piezoelectric substance. Some other commonly used piezoelectric materials are ferroelectric single-crystal lithium niobate ($LiNbO_3$) and thin films of ZnO and lead zirconium titanate (PZT). Recently, advances have been made in sensor technology with ultrasonic sensor configurations such as the surface acoustic wave (SAW) and acoustic plate mode (APM). In SAW devices the acoustic waves travel on the solid surface, and in an APM arrangement they bounce off at an acute angle between the bounding planes of a plate. The main types of acoustic wave sensors are shown in Fig. 10 (11).

Piezoelectric thin films are particularly well suited for microsensor applications that require high reliability and superior performance. When prepared under optimal conditions piezoelectric thin films have a dense microstructure without cracks and holes, good adherence, and good electrical properties. The three most popular materials used for thin films include ZnO (zinc oxide), AlN (Aluminum nitride), and PZT (lead zirconium titalate). Deposition, sputtering, and sol–gel are some of the methods used for preparing piezo films; the choice depends on the material and substrate used. ZnO thin films are prepared using laser-assisted evaporation and are often doped with lithium. Such films have excellent orientation. AlN thin films maintain a high acoustic velocity and are able to withstand extremely high temperatures. PZT thin films have a much higher piezoelectric coefficient than ZnO and AlN.

Recently, it has become possible to generate piezoelectric thin films with extremely good properties through the sol–gel process. This process consists of the following steps: synthesis of a metal–organic solution, deposition of this solution by spin coating, and a final heating that helps to crystallize the ceramic film. A cross-sectional view of a thin film PZT sensor is shown in Fig. 11. The advantages of thin film PZT sensors include their small size, which allows them to be positioned virtually anywhere, and their ability to operate at high frequencies.

**Measurement Techniques.** The different modes of use for an acoustic sensor are summarized in Fig. 12. Using either a resonator-transducer or a delay line, measurements can be made

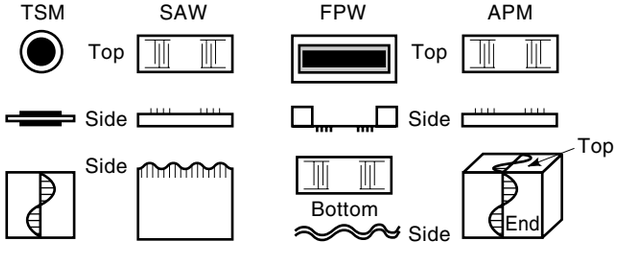


**Figure 10.** Types of acoustic wave sensors.

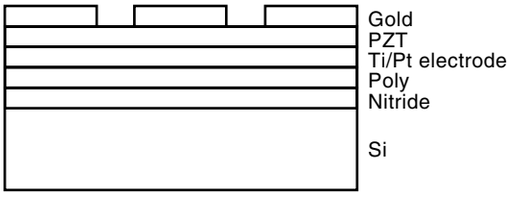


**Figure 11.** Cross-sectional view of a thin film PZT sensor.

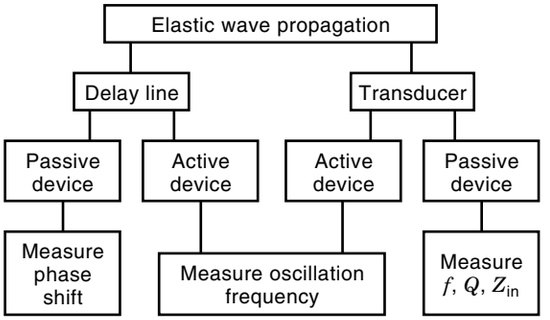


**Figure 12.** Different measurement techniques for acoustic sensors.

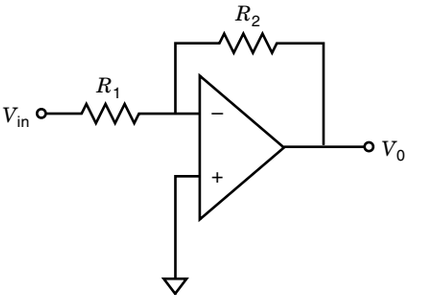


**Figure 14.** Voltage amplifier.

on the device itself or incorporated into an oscillator circuit. There are basically two ways to implement this measurement technique: active or passive. In the case of passive bulk-wave resonators, we measure the resonant frequency to infer the wavelength and hence the velocity. Likewise, for passive delay lines the phase shift between the input and the output of the transducer, which are separated by a known distance, yields the velocity. On the other hand, for active resonators or delay-line oscillators, the frequency can be directly measured with the help of a digital counter.

As an example, let us consider the complete design and implementation of an integrated acoustic emission sensor with low-power signal-conditioning circuitry for the detection of cracks and unusual wear in aircraft and submarines. Within a health and usage monitoring system, it is necessary by some means, either directly or indirectly, to monitor the condition of critical components, e.g., airframe, gearboxes, and turbine blades. The overall aim is to replace the current practice of planned maintenance with a regime of required maintenance. Typical parameters used include stress (or strain), pressure, torque, temperature, vibration, and crack detection. In this example, acoustic emission sensors are used for crack detection. The thin film piezoelectric sensor, coupled to an aircraft component, senses the outgoing ultrasonic waves from any acoustic emission event as shown in Fig. 13. The magnitude of the output signal is proportional to the magnitude of the acoustic emission event. For our example design, the acoustic emission signal bandwidth varies from 50 kHz to approximately 1 MHz. Mixed in with the desired acoustic emission signal is vibration noise due to fretting of the mechanical parts. However, this noise is limited to about 100 kHz and is easily filtered out.

Due to the acoustic emission event, the piezoelectric sensor generates a charge on the top and bottom plates of the sensor. There are two basic methods of interfacing to this sensor. We can use either a voltage amplifier (Fig. 14) or a charge amplifier (Fig. 15).

In general, the charge amplifier interface provides a number of advantages. First, it is not affected by parasitic capacitances at the input of the amplifier. Second, the output voltage at the piezoelectric sensor is very small. This is because the piezoelectric material, PZT, that is used for its high piezoelectric coefficient also has a very high dielectric constant. As shown below, the output voltage is proportional to the charge and inversely proportional to the dielectric constant:

$$V = \frac{Q}{C} = \frac{Q}{\epsilon A/d} = \frac{eSA}{\epsilon A/d} = \frac{eSd}{\epsilon} \tag{17}$$

[The output voltage can also be written in terms of the strain $S$, the distance $d$, the electron charge $e$, and the dielectric constant $\epsilon$ as shown in Eq. (19) below.] For these and other reasons the charge amplifier interface was selected for our design example.

The charge amplifier circuit shown in Fig. 15 is in its simplest form. The charge $Q$ and capacitance $C_S$ are used to model the sensor charge and sensor capacitance. The inverting terminal of the operational amplifier is a virtual ground, and no charge flows into the operational amplifier inputs. Therefore, any charge that is generated across the sensor has to flow into the feedback capacitance $C_f$. The output voltage developed across the feedback capacitor is inversely proportional to the value of this capacitance. The voltage gain of the circuit is given by the ratio of $C_S$ to $C_f$, and hence, to obtain high gain, $C_f$ can be made much smaller than $C_S$. This basic topology has a number of limitations, including low-frequency flicker noise of the amplifier, operational amplifier offset, and long-term drift. Traditionally, correlated double sam-

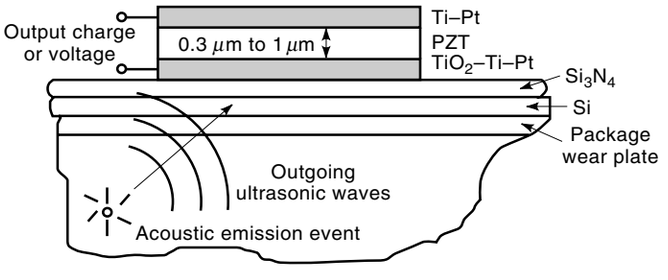


**Figure 13.** Acoustic emission sensor.

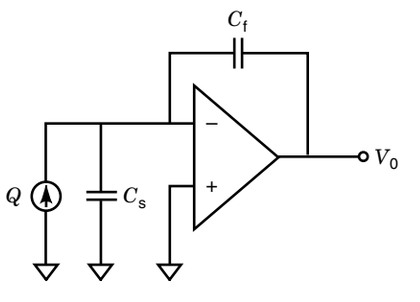


**Figure 15.** Charge amplifier.

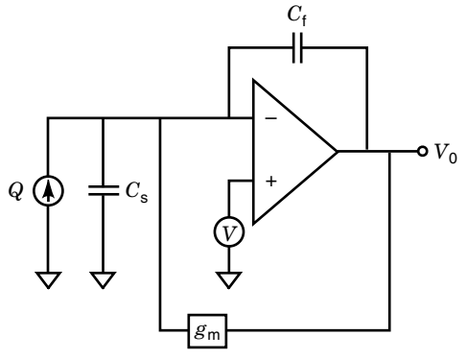


**Figure 16.** Modified charge amplifier circuit.

pling and chopper stabilization are used to remove low-frequency noise and offset. However, as noted earlier, our signal band does not include the frequencies from dc to 50 kHz, and our maximum signal frequencies are fairly high. Therefore, an alternative design topology shown in Fig. 16 was selected to circumvent the problem.

Here, low-frequency feedback is provided to reduce the effects of offset, long-term drift, and low-frequency noise. In the modified circuit, a transconductor is connected in negative feedback. The transfer function of the modified circuit is given by

$$\frac{V_0(s)}{Q_{\text{in}}(s)} = -\frac{s \cdot (g_{m_a} - g_m - C_f \cdot s)}{C_s \cdot C_f \cdot s^2 + s(C_s \cdot g_m + g_{m_a} \cdot C_f) + g_{m_a} \cdot g_m} \tag{18}$$

In this equation, $C_s$ is the sensor capacitance, $C_f$ is the feedback capacitance of the operational amplifier, $g_{m_a}$ and $g_m$ are the transconductances of the operational amplifier and the transconductor. If the higher-order terms are neglected, then Eq. (18) can be simplified to

$$\frac{V_0(s)}{Q_{\text{in}}(s)} = -\frac{s}{g_m} \cdot \frac{1}{\left(1 + \dfrac{C_s \cdot s}{g_{m_a}}\right)} \tag{19}$$

From Eq. (19) it is clear that the circuit has the characteristics of a high-pass filter, that is, none of the low-frequency noise or offsets affect the circuit performance.

Next, we perform a power analysis to analyze the effects of different design tradeoffs. Both MOS and bipolar transistor technologies are considered, and power and noise analysis and design tradeoffs for both technologies are presented.

**Power Analysis.** If MOS transistors in strong inversion (SI) are used to implement the operational amplifier, then the minimum power requirement is given by

$$P = VI = \frac{V(2\pi\,\text{BW}C)^2}{2K \cdot W/L} \tag{20}$$

where BW is the signal bandwidth, $C$ is the sensor capacitance, $K$ is the transconductance factor, $V$ is the output voltage, $I$ is the supply current, and $W/L$ is the aspect ratio of the transistor. From this equation it is clear that the power is proportional to the square of the signal bandwidth and sensor capacitance.

If, however, bipolar transistors are used to implement the operational amplifier, the minimum power requirements is given by

$$P = VI = V \cdot 2\pi\,\text{BW}U_T C \tag{21}$$

Here, $U_T$ is the thermal voltage, which is equal to 26 mV at room temperature. From this equation it is clear that in the case of bipolar transistors, the power is linearly proportional to the signal bandwidth and sensor capacitance. This difference in the power consumption between bipolar and MOS implementations for a signal frequency of 1 MHz is shown in Fig. 17. Here we note that the power consumption for both MOS and bipolar implementations increases with increased sensor capacitance. However, for very low frequencies, the MOS devices can be operated in weak inversion (WI). In WI, MOS devices behave very similarly to bipolar devices, and hence the slopes for weak inversion and bipolar devices are initially very similar. However, at higher frequencies MOS devices are forced to operate in strong inversion and hence consume more power for the same performance.

Next, we consider the design tradeoffs in connection with device noise.

**Noise Analysis.** The power spectral density for the wide-band gate-referred noise voltage for MOS transistors is given by

$$V_{nT}^2 = \frac{8}{3}\frac{kT}{g_m} \tag{22}$$

Here, $k$ is Boltzmann's constant, $T$ is the temperature, $g_m$ is the transconductance. Likewise, for bipolar transistors the power spectral density for the wide band input-referred noise voltage is given by

$$V_{nT}^2 = 2qI_C \tag{23}$$

For both MOS and bipolar implementations the total rms input referred noise is independent of frequency and inversely

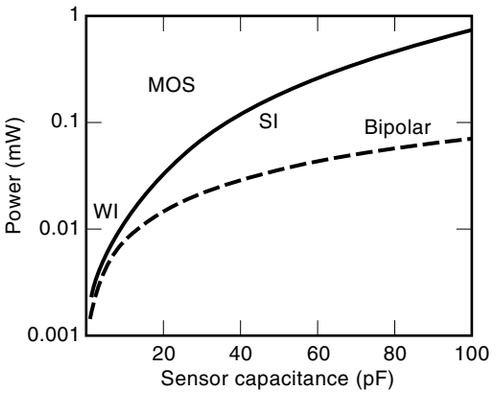


**Figure 17.** Minimum power requirements versus sensor capacitance for a MOS or bipolar design.

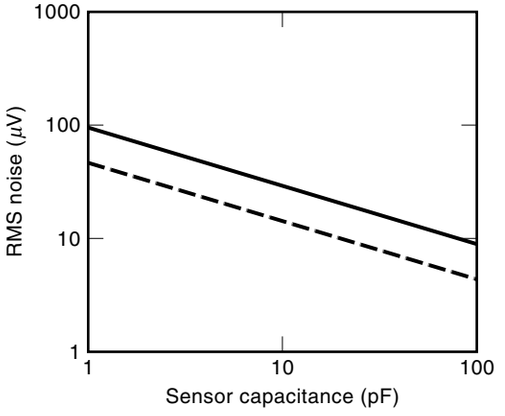


**Figure 18.** Noise power spectral density versus capacitance.

proportional to the sensor capacitance as shown in Fig. 18. Here, we note that the ratio of the noise spectral density for the MOS and the bipolar implementations is a constant equal to four.

In summary we note that: For a MOS implementation the power consumption is proportional to the square of the sensor capacitance, whereas for a bipolar implementation it is linearly proportional to the sensor capacitance. On the other hand, the input-referred noise for both the MOS and bipolar implementations is inversely proportional to the sensor capacitance. Thus, there is a clear tradeoff between the minimum power consumption and the maximum input-referred noise. If the sensor capacitance is increased, then the input-referred noise decreases, but the power increases, and vice versa. Using the equation above, we can calculate the minimum bound on the power requirements for our application. For 10 bits of accuracy and a signal bandwidth of 1 MHz, the minimum sensor capacitance size is 5 pF and the minimum power consumption is around 500 $\mu$W.

Next, we provide some simulation and measurement results for our acoustic emission sensor system.

**Results.** Simulation and measurement results for the charge amplifier with a sensor capacitance of 100 pF and a feedback capacitance of 10 pF are shown in Fig. 19. For this measurement, discrete versions of the sensor and feedback capacitors were used. As expected, the signal band gain is given by the ratio of the sensor to the feedback capacitance, which is equal to 20 dB. Both measurement and simulation results agree fairly well with this value. The primary difference between the measurement and simulation results is in the low-frequency and high-frequency poles. It is expected that this is largely a result of parasitic capacitances and possibly a lower realized transconductance in comparison with the simulated value.

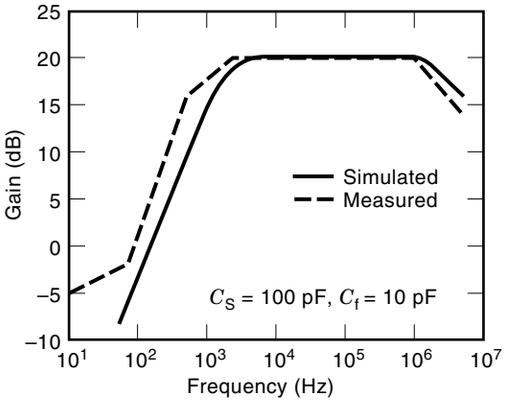


**Figure 19.** Small-signal frequency response of the charge amplifier.

The charge amplifier circuit design just described converts the sensor charge into a voltage. This amplified signal voltage is then converted to digital form using an ADC. For our implementation a 10-bit fourth-order sigma–delta implemented as a MASH topology was used. The fourth-order topology was used to keep the oversampling ratio low, as the signal frequency is fairly high. Details of this implementation are not included here; interested readers are referred to Ref. 6 for more information.

Next, we describe a complete temperature sensor system.

### Temperature Sensing System

In many control systems, temperature sensors are used as the primary sensor. Additionally, as most electronic components and circuits are affected by temperature fluctuations, temperature sensors are often needed in microsensor systems to compensate for the temperature variations of the primary sensor or sensors.

Because integrated sensors can be manufactured on the same substrate as the signal-processing circuitry, most recent temperature measurement schemes concentrate on integrated silicon temperature sensors. The resulting smart sensor is extremely small and is also able to provide extremely high performance, as all the signal processing is done on chip before the data is transmitted. This avoids the usual signal corruption that results from data transmission. The disadvantage of the smart sensor is that since all the processing is done on chip, it is no longer possible to maintain the signal preprocessing circuits in an isothermal environment. The on-chip sensor interface electronics must therefore be temperature-insensitive or be compensated to provide a temperature-insensitive output.

A *smart* temperature sensor is a system that combines on the same chip all the functions needed for measurement and conversion into a digital output signal. A smart temperature sensor includes a temperature sensor, a voltage reference, an ADC, control circuitry, and calibration capabilities. A block diagram for a smart temperature sensor is shown in Fig. 20. The use of $p$–$n$ junctions as temperature sensors and for the generation of the reference voltage signals has been reported extensively (12,13). A bandgap voltage reference can be gener-

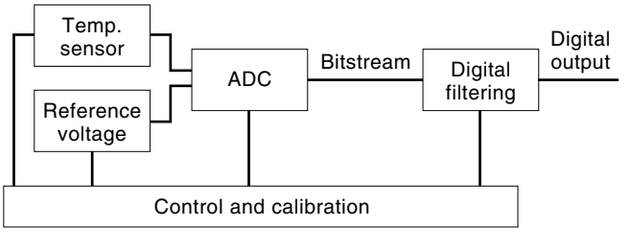


**Figure 20.** Smart temperature sensor.

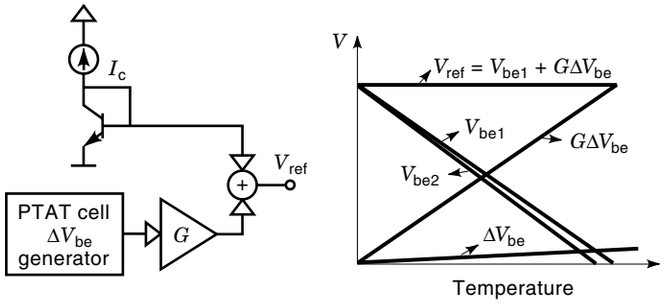


**Figure 21.** Principle of bandgap reference.

ated with the help of a few $p$–$n$ junctions. The basic principle for the operation of a bandgap voltage reference is illustrated in Fig. 21.

The base–emitter voltage $V_{be}$ of a bipolar transistor decreases almost linearly with increasing temperature. The temperature coefficient varies with the applied current, but is approximately $-2$ mV/°C. It is also well known that the difference between the base–emitter voltages of two transistors, $\Delta V_{be}$, operated at a constant ratio of their emitter current densities, possesses a positive temperature coefficient. At an emitter current density ratio of 8, the temperature coefficient of this PTAT (proportional to absolute temperature) source is approximately 0.2 mV/°C. Amplifying this voltage ($G\Delta V_{be}$) and adding it to a base-emitter voltage $V_{be}$ produces a voltage reference that is independent of temperature. Many circuits have been developed to realize bandgap voltage references using this principle (14,15). A circuit diagram for one of the early bandgap reference implementations is shown in Fig. 22 (16).

For an ideal operational amplifier, the differential input voltage is equal to zero, so that resistors $R_1$ and $R_2$ have equal voltages across them. Since the voltage across the resistors is the same, the two currents $I_1$ and $I_2$ must have a ratio that is determined solely by the ratio of the resistances $R_1$ and $R_2$. The base–emitter voltage of a diode-connected bipolar transistor is given by Eq. (24) below, where $T$ is the absolute temperature of the junction, $I_s$ is the reverse saturation current, $I_d$ is the current through the junction, $k$ is Boltzmann's constant, $q$ is the electronic charge, and $n$ is a constant that depends on the junction material and fabrication technique. To see this, we write

$$V_{be} = \frac{nkT}{q} \ln \frac{I_d + I_s}{I_s} \approx \frac{nkT}{q} \ln \frac{I_d}{I_s} \tag{24}$$

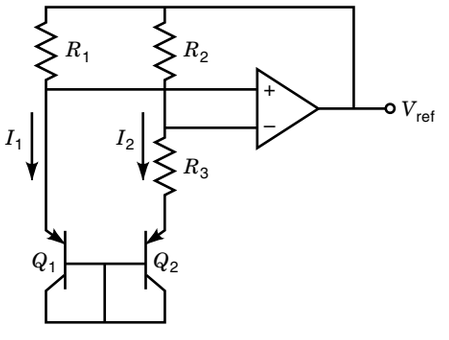


**Figure 22.** Example bandgap voltage reference circuit.

Therefore, the difference between the two base–emitter voltages ($\Delta V_{be}$) is given by

$$\Delta V_{be} = V_{be1} - V_{be2} = \frac{nkT}{q} \ln \frac{I_1 I_{s2}}{I_2 I_{s1}} = \frac{nkT}{q} \ln \frac{R_2 I_{s2}}{R_1 I_{s1}} \tag{25}$$

This voltage appears across $R_3$. Since the same current that flows through $R_3$ also flows through $R_2$, the voltage across $R_2$ is given by

$$V_{R_2} = \frac{R_2}{R_3} \Delta V_{be} = \frac{R_2}{R_3} \frac{nkT}{q} \ln \frac{R_2 I_{s2}}{R_1 I_{s1}} \tag{26}$$

as desired.

The output voltage is the sum of the voltage across $R_1$ and the voltage across $Q_1$. Since the voltage across $R_1$ is equal to the voltage across $R_2$, the output voltage is equal to

$$V_{out} = V_{be1} + \frac{R_2}{R_3} \frac{nkT}{q} \ln \frac{R_2 I_{s2}}{R_1 I_{s1}} = V_{be1} + G\,\Delta V_{be} \tag{27}$$

Therefore, this circuit behaves as a bandgap reference, where the gain factor $G$ is set by the ratios $R_2/R_3$, $R_2/R_1$, and $I_{s2}/I_{s1}$. In many designs $R_2 = R_1$ and $I_{s2} = 8I_{s1}$. Since the reverse saturation current $I_s$ is proportional to the emitter area, to make $I_{s2} = 8I_{s1}$ we let the emitter area of $Q_2$ be 8 times as large as the emitter area of $Q_1$.

The operational amplifier's input-referred voltage offset is the largest error source in this type of voltage reference. This voltage offset is highly temperature-dependent and nonlinear, making an accurate calibration of such a reference virtually impossible. It is therefore necessary to use some type of offset cancellation technique such as autozero or chopper stabilization (17).

Another source of error is the nonzero temperature coefficient of the resistors. Usually on-chip resistors are used, in the form of polysilicon resistors or well resistors. Both of these resistor implementations tend to occupy very large amounts of chip area if low power is desired. Low-power implementations demand the use of large-value resistors, which unfortunately require large areas. Though well resistors have a much larger resistivity than polysilicon resistors, they also have a very nonlinear temperature coefficient, which makes for difficult calibration.

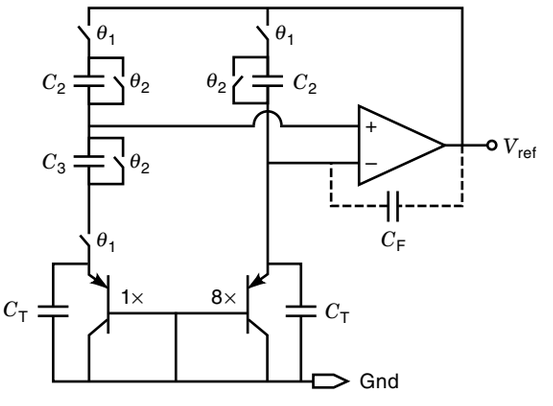


**Figure 23.** A switched-capacitor implementation of the bandgap reference.

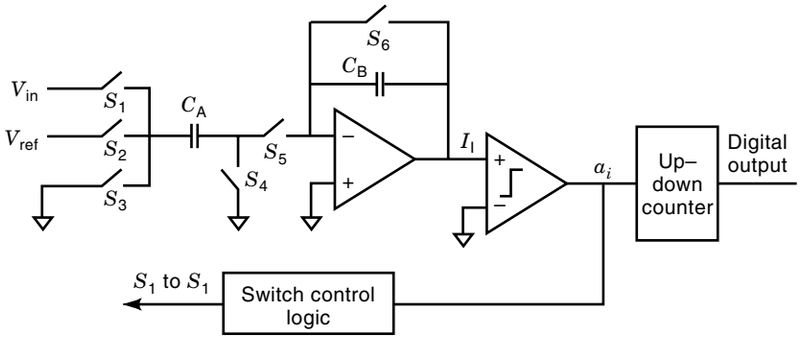


**Figure 24.** Incremental ADC.

A solution to these problems is to use switched-capacitor circuits to implement the resistors in the voltage reference circuit. A switched-capacitor implementation makes offset removal simple and also reduces the power consumption, as the area occupied by large-value switched-capacitor resistors is significantly smaller than the area occupied by continuous-time resistors. In fact, the area occupied by switched-capacitor resistors is inversely proportional to the value of the resistance desired. Another advantage is that the temperature coefficient of on-chip poly–poly capacitors is much smaller than that of on-chip resistors, making design and calibration easier. A switched-capacitor implementation of the bandgap voltage reference is shown in Fig. 23.

The structure of this voltage reference is similar to the one shown in Fig. 22, except that the continuous time resistors have been replaced by switched-capacitor resistors, and capacitors $C_T$ and $C_F$ have been added. The switched capacitors emulate resistors with an effective resistance value given by

$$R_{eff} = \frac{1}{f_C C} \tag{28}$$

where $f_C$ is the clock frequency of the switch. The feedback capacitor $C_F$ is designed to be very small and is added to ensure the operational amplifier is never in an open-loop mode of operation. The capacitors located in parallel with the diodes act as tank capacitors to ensure that current is constantly supplied to the diodes. The output of this voltage reference can similarly be calculated and is given by

$$V_{ref} = V_{be1} + \frac{C_3}{C_2}\frac{nkT}{q}\ln\frac{C_1 I_{s2}}{C_2 I_{s1}} = V_{be1} + G\,\Delta V_{be} \tag{29}$$

which is the desired bandgap voltage reference.

Most temperature-sensing devices also use the difference between two diodes ($\Delta V_{be}$) as the sensing element of the system. Since the temperature coefficient of $\Delta V_{be}$ is small (≈0.2 mV/°C), it is almost always amplified to a much larger value (≈10 mV/°C) for increased sensitivity. Since we already have an amplified value of $\Delta V_{be}$ in the voltage reference ($G\Delta V_{be}$), all that needs to be done is to subtract $V_{be1}$ from the voltage reference to obtain an amplified value of $\Delta V_{be}$. If more sensitivity is needed, the additional amplification can be incorporated in the ADC by simply adjusting the capacitor ratio of $C_A$ and $C_B$ as shown in Fig. 24. Additionally, the subtraction of $V_{be1}$ from the voltage reference can be easily accomplished with the circuit shown in Fig. 25, where $V_{in1}$ is the output of the voltage reference, $V_{in2}$ is equal to $V_{be1}$, and $V_G$ is the negative input of the operational amplifier in the follow-on data converter. During clock cycle $\theta_1$ the capacitor $C$ is charged to the input voltage $V_{in2}$. During clock cycle $\theta_2$, the charge $(V_{in1} - V_{in2})/C$ is transferred. This circuit effectively does the voltage subtraction that is needed to obtain the amplified temperature-dependent output voltage ($G\Delta V_{be}$).

Incorporating the voltage reference and temperature-sensing circuitry shown in Figs. 23 and 25 into a smart temperature sensor system involves some additional circuitry. Since switched capacitors are already being used for the voltage reference and the sensing circuitry, it makes sense to use switched-capacitor technology for the ADC. A simple ADC that utilizes oversampling techniques is the incremental converter (18). The advantage of this data converter topology, shown in Fig. 24, is its low power consumption, small area, and insensitivity to component mismatch. Additionally, in comparison with sigma–delta converters the postquantization digital low-pass filter is much simpler. It consists of just an up–down counter instead of a more complicated decimation filter. Unfortunately, the first-order incremental ADC has a relatively long conversion time, making this converter suitable only for very slow signals such as temperature.

The first-order incremental ADC shown in Fig. 24 is composed of a stray-insensitive switched-capacitor integrator, a comparator, switch control logic, and an up-down counter. A four phase nonoverlapping clock as shown in Fig. 26 consti-

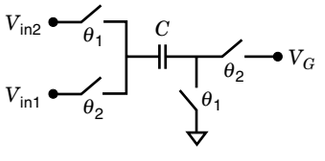


**Figure 25.** Switched-capacitor subtraction circuit.

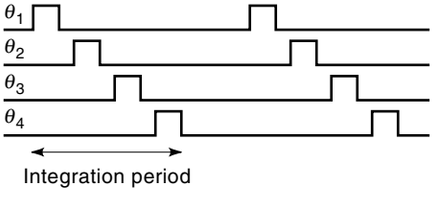


**Figure 26.** Four-phase nonoverlapping clock.

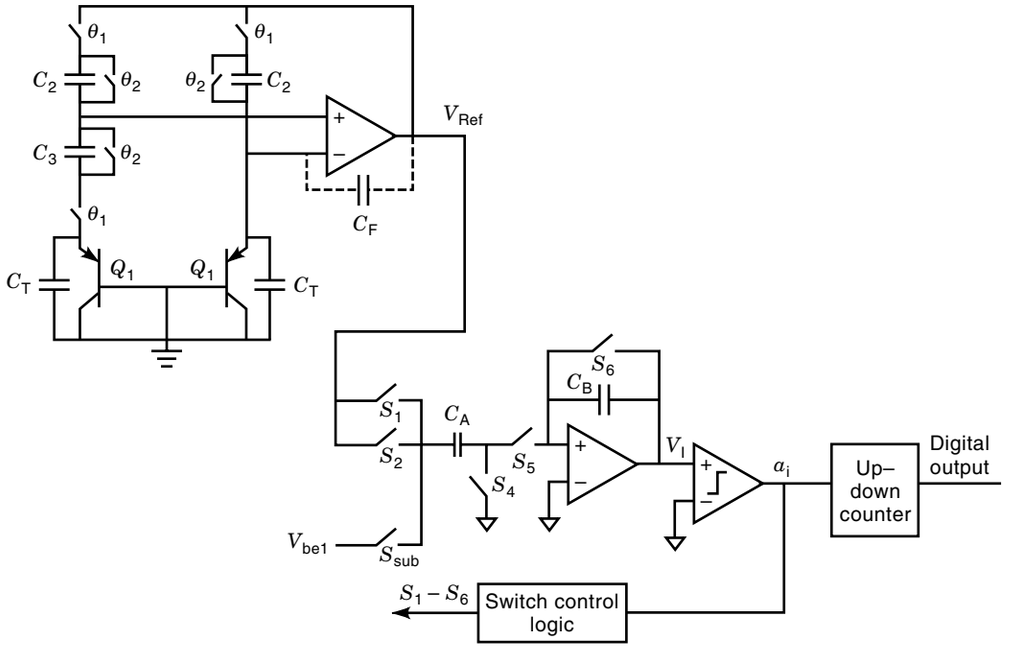


**Figure 27.** Smart temperature sensor circuit.

tutes an integration period. The integrator output voltage is designated by $V_I[i, j]$, where $i$ corresponds to the current integration period and $j$ to the clock cycle (1, 2, 3, or 4).

During clock cycle $\theta_1$, $S_1$ and $S_4$ are closed, charging $C_A$ to the input voltage $V_{in}$. During $\theta_2$, $S_3$ and $S_5$ are closed, transferring the charge that was stored on $C_A$ to $C_B$. At the end of the charge transfer from $C_A$ to $C_B$ the comparator output is denoted by

$$a_i = \begin{cases} 1 & \text{if} \quad V_I[i, 2] > 0 \\ -1 & \text{if} \quad V_I[i, 2] < 0 \end{cases}$$

During $\theta_3$, $S_4$ is closed, and if:

$$a_i = 1, \qquad S_3 \text{ is closed}$$
$$a_i = -1, \qquad S_2 \text{ is closed}$$

During $\theta_4$, $S_5$ is closed, and if:

$$a_i = 1, \qquad S_2 \text{ is closed}$$
$$a_i = -1, \qquad S_3 \text{ is closed}$$

Also during $\theta_4$, the integrator output voltage $V_I[i, 4]$ is given by

$$V_I[i, 4] = V_I[i, 1] + \frac{C_A}{C_B}(V_{in} - a_i V_{ref}) \tag{30}$$

The final $N$ bit output code, denoted by $D_{out}$, that results from the up–down counter is obtained by evaluating the quantity

$$D_{out} = \frac{1}{n}\sum_{i=1}^{n} a_i \tag{31}$$

Here $n$ is the number of integration periods, and is a function of the resolution that is required of the ADC.

The complete smart temperature sensor is shown in Fig. 27. The subtraction circuit of Fig. 25 is incorporated into the ADC by simply adding switch $S_{sub}$. The only difference in the operation of the incremental converter shown in Fig. 27 from the one shown in Fig. 24 is that now during $\theta_2$, $S_3$ is not closed but instead $S_{sub}$ is closed.

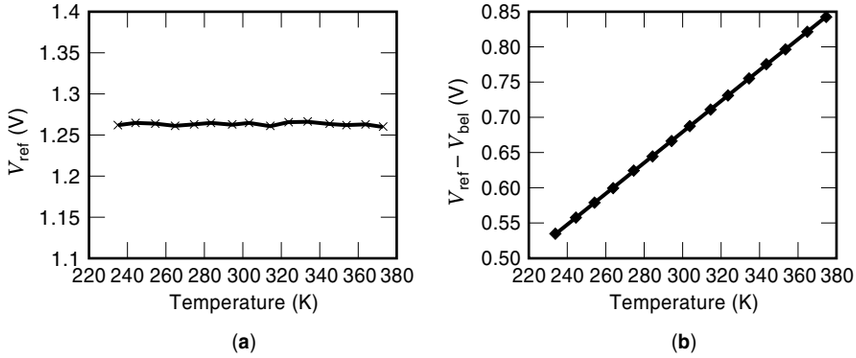


**Figure 28.** Measurement results for the (a) voltage reference, (b) the temperature sensor.

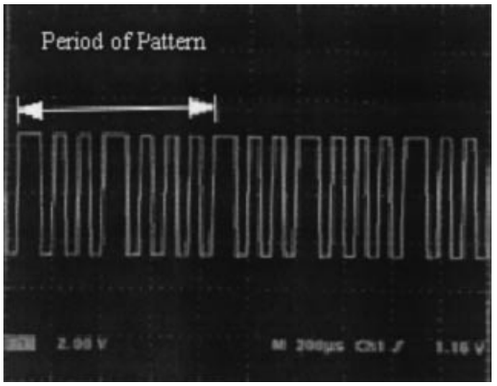


**Figure 29.** Measurement results for the analog-to-digital converter.

The calibration of this system is done in two steps. First the voltage reference is calibrated by adjusting the ratio of $C_3$ and $C_2$; next the amplified sensor voltage is calibrated by adjusting the ratio of $C_A$ and $C_B$. Adjusting the ratios of the capacitors is done with the use of a capacitor array that is controlled digitally. The output is an $N$ bit digital word.

In Fig. 28 we show measurement results for the voltage reference and final temperature output. For these results a first-pass design of the circuit in Fig. 27 was used. This design was not completely integrated and included external resistors to obtain gain. We expect final integrated results to behave similarly. Figure 28(a) shows the reference voltage obtained as a sum of a $V_{be}$ and an amplified $\Delta V_{be}$ as described in Eq. (29). The $x$ axis shows the temperature in kelvin and the $y$ axis shows the measured output reference voltage in volts. The measured value is fairly close to the expected value except for some small experimental variations. We suspect these variations are a result of the length of time used to stabilize the temperature between temperature output measurements. The graph in Fig. 28(b) shows the output voltage, which is $V_{ref} - V_{be}$. As expected, this voltage varies linearly with temperature. Figure 29 shows the expected 1 bit output stream ($a_i$ shown in Fig. 24) of the sigma–delta converter before the digital low-pass filter. This output corresponds to an input voltage equal to one-eighth of the reference voltage.

We have provided detailed designs for two complete data acquisition systems, namely an acoustic emission sensor system and a smart temperature sensor system. We provide both measurement and simulation results to show their performance.

## CONCLUSION

In this article we have provided brief descriptions of data acquisition and data conversion systems. In particular, we provided some general descriptions of integrated capacitive and resistive sensors. This was followed by descriptions of two of the most common data converter topologies used in sensor interface systems, namely successive approximation and sigma–delta. Finally, these were followed by detailed descriptions of two complete acquisition systems. The first system was based on a piezoelectric acoustic emission sensor interfaced to a charge amplifier and data converter. The second system was a smart temperature sensor. As feature sizes continue to decrease and integrated sensor technologies progress, it is likely that extremely smart and high-performance systems will be integrated on single chips. Additionally, significant reduction in power and area as a result of smaller feature sizes will make such systems ubiquitous.

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