DC AMPLIFIERS

The term *direct coupled amplifier,* or *dc amplifier,* means direct coupling between the amplifier and the input signal to be amplified. Basically, a directly coupled amplifier has no capacitive or inductive coupling between the input source and the amplifier. Consequently, the dc amplifier, as opposed to capacitively coupled or ac amplifiers, allows amplification of continuous and low-frequency signals (1,2). Direct coupled amplifiers appeared at the same time as amplifiers. But they have performed better ever since, and with the introduction of integrated circuits (ICs), it was possible to use a truly differential input stage implemented from a pair of matched transistors (2,3). Figure 1 illustrates the direct and capacitive coupling amplifications with alternating current (ac) and direct current (dc) input voltage sources. For proper operation, it is necessary to have the same reference voltage level for the amplifier and the input signal. In most cases the ground is used as the reference.

A large number of applications require dc amplifiers to amplify low-frequency signals down to dc. They are, for example, used in dc–dc voltage down converters in which it is necessary to amplify a dc voltage reference (4). Directly coupled amplifiers are also used in linear feedback loops to control speed or position of dc motors. There are many measurement transducers, such as temperature sensors, or load transducers used to measure weights. These exhibit a very low dc output voltage and are often directly coupled to a high-gain dc amplifier (2). Direct coupled amplifiers are predominantly used in monolithic integrated circuits where using coupling capacitors would necessitate a large and expensive silicon area (1). In addition, at very low frequencies, dc feedback amplifiers are also preferred to ac coupled feedback amplifiers, which can induce 'motorboating' or stability problems due to the phase shift caused by several capacitive coupled stages (2). Other high-speed applications, such as optical communications, necessitate high-performance dc amplifiers with a wide bandwidth (5).

The amplifier gain and the dc operating point depend on multiple parameters, such as transconductance, load resistor values, bias currents, and power supplies. Inherent fabrication process variation, thermal drifts, and component sensitivity inevitably introduce amplification and biasing errors. The predominant errors result from voltage and current offsets corresponding to the input voltage and input current which must be applied to force the output voltage of the amplifier to zero.

Considering the high process sensitivity of transistor parameters, offsets, and thermal drifts, the use of a single transistor input stage to build a dc amplifier is unreasonable. In contrast, an input stage built from a differential pair of matched transistors allows considerable reduction of these effects. This is the case, for example, of voltage-feedback operational amplifiers (VFOA), usually called op-amps. So, a high-gain voltage-feedback amplifier allows designing an accurate dc amplifier. In this case, with a very low common mode rejection ratio (CMRR), the gain of the dc amplifier depends only on the feedback ratio that can be easily kept invariable.

GENERAL SCHEMA FOR DC AMPLIFIERS

Basic dc Amplifiers

Figure 2 shows the building blocks of a classical dc amplifier. It is composed of three main stages. The first block corresponds to a differential input stage and is followed by a second which consists of a high-gain voltage amplifier. The last stage is a voltage follower. Usually, the dc amplifier is biased between positive (V_{cc}) and negative voltages ($V_{ee} = V_{cc}$).

Considering the various gain stages, the output voltage V_O in the case of Fig. 2 is given by

$$V_O = AG_V V_{id} \tag{1}$$

This expression clearly shows the dependence of the amplifier gain on the parameters A and G_V. Because these parameters are sensitive to process variation and thermal drift, amplifier gain varies from one component to the other. The differential

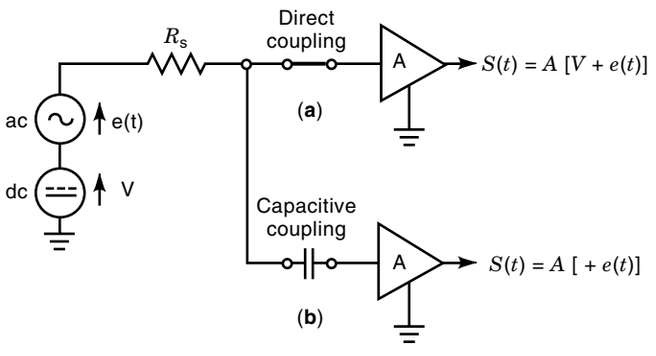

Figure 1. Different kinds of coupled amplifiers: (a) dc amplifier; (b) ac amplifier using coupling capacitor.

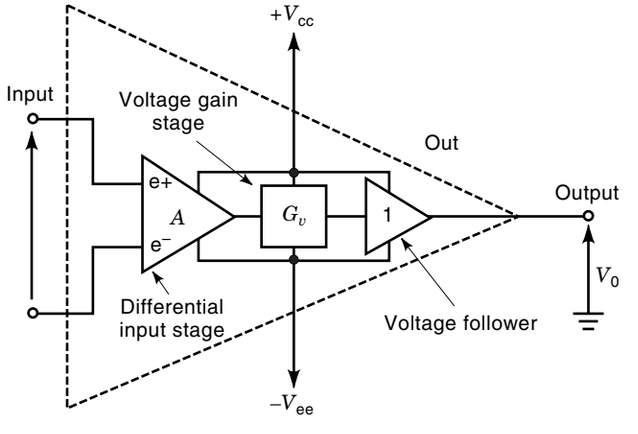

Figure 2. Schema block for a dc amplifier showing the various stages.

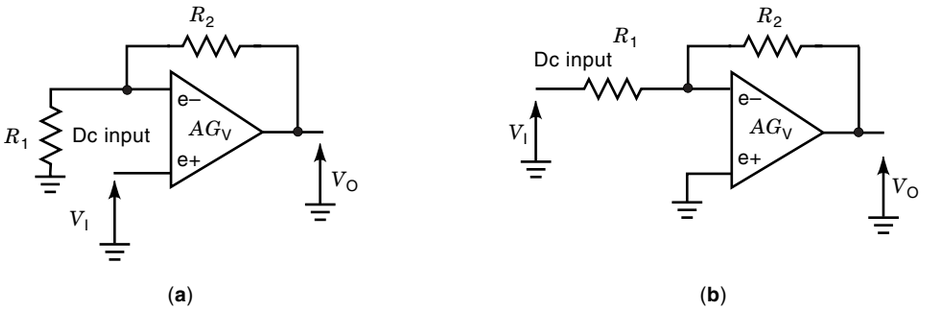

Figure 3. The two configurations for dc feedback amplifiers: (a) noninverting amplifier; (b) inverting amplifier.

input stage behaves as a preamplifier, and it amplifies offset and drift voltages and currents. Consequently, the characteristics of this preamplifying stage define the performance and limits of the dc amplifier. Another important parameter is the input noise that also limits the minimum detectable signal. In the next section describing the characteristics of the differential input stage, we show that its components have to be well matched to obtain the smallest error signal possible.

Main Effects of Feedback Loop

The feedback loop is used mainly to prevent amplification from the variation of the dc amplifier gain (AG_V). Figures 3(a) and 3(b) describe the feedback loop technique in both noninverting and inverting amplifiers. In these cases, considering a dc amplifier with infinite gain ($AG_V \to \infty$) and infinite input resistance gain, the transfer functions V_O/V_i is given as follows:

$$\text{Noninverting amplifier} \quad \frac{V_O}{V_i} = \left(1 + \frac{R_2}{R_1}\right) \tag{2a}$$

$$\text{Inverting amplifier} \quad \frac{V_O}{V_i} = -\frac{R_2}{R_1} \tag{2b}$$

When resistors R_1 and R_2 are accurate, this system constitutes an excellent directly coupled amplifier. Thus, this technique is a good solution for removing some of the shortcomings of the dc amplifier.

ANALYSIS OF THE BIPOLAR DIFFERENTIAL INPUT STAGE

In this section, the relationship between input and output voltages is determined for an ideal stage implemented from bipolar transistors. Then, the mismatch effects (offsets and drift sensitivities) are analyzed for a real dc amplifier.

Ideal Differential Stage

Figure 4 shows the schema of an ideal differential input stage (or emitter-coupled pair), implemented from bipolar transistors. $V_{id} = V_{i1} - V_{i2}$ is the differential input voltage, and $V_{od} = V_{o1} - V_{o2}$ is the differential output voltage of the circuit. For an ideal amplifier, i.e., including perfectly matched elements, transistors Q_1 and Q_2 are assumed identical, and resistors R_{C1} and R_{C2} have the same value of R_C.

For forward-biased transistors Q_1 and Q_2 (i.e., $V_{be} \gg V_T$; $V_T = kT/q$ is the thermal voltage), the reverse saturation currents of the collector–base junctions can be ignored. Neglecting the Early effect and assuming very low values for currents I_{b1} and I_{b2}, so that their effects are negligible, then the collector currents are given by (6–9)

$$I_{C1} = (\alpha_F I_0)/[1 + \exp(-V_{id}/V_T)] \tag{3}$$

$$I_{C2} = (\alpha_F I_0)/[1 + \exp(+V_{id}/V_T)] \tag{4}$$

In these equations $\alpha_F = -(I_c/I_e)_{VBC=0}$ is the common-base forward, short-circuit current gain. Thus the expression of the differential output voltage of this stage can directly be deduced from Eqs. (3) and (4):

$$V_{od} = R_C(I_{C2} - I_{C1}) = -\alpha_F R_C I_0 \tanh(V_{id}/2V_T) \tag{5}$$

As a result, for $|V_{id}| \ll 2V_T$, the differential output voltage has a 180° phase difference with respect to V_{id}, and the amplifier gain is given by $A = R_c \times I_0$ (as $\alpha_F \approx 1$). In this way, A is increased by increasing either the value of load resistors R_C or the bias current I_0. Nevertheless, increasing I_0 leads to a rise in power consumption. However, the value of R_C is artificially enlarged by using active loads (current mirrors), which are easier to fabricate in IC form than high-value resistors.

Figure 5, which shows the variation of output voltage as a function of V_{id}, illustrates the nonlinear effects that appear as soon as $|V_{id}|$ approaches $2V_T$. For an ideal differential stage, this reveals that the output voltage V_{od} is zero for $V_{i1} = V_{i2}$.

Real Differential Stage

For a real differential stage implemented in IC form, the base currents of Q_1 and Q_2, the component mismatches (amplifier dissymmetry), the equivalent input noise, and the thermal

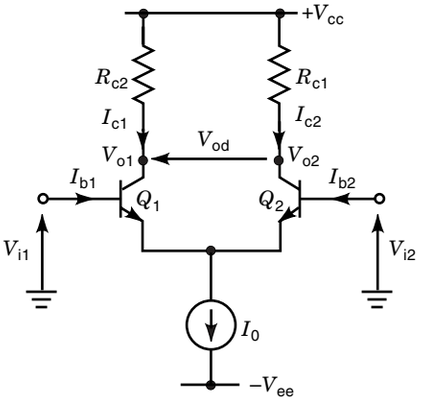

Figure 4. Bipolar differential input stage using matched devices.

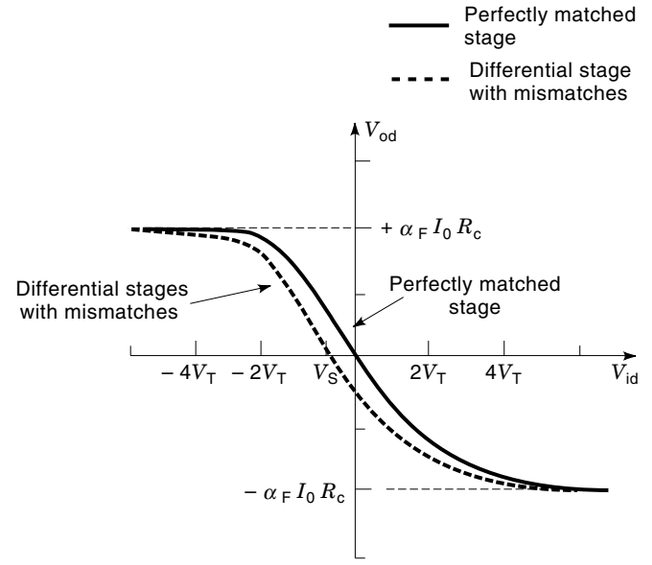

Figure 5. Differential output voltage as a function of input voltage showing the curves for matched and mismatched stages.

drifts must be taken into account to determine the minimum differential dc voltage detectable (amplifier sensitivity).

Base Input Bias Currents. The dc input bias currents ($I_{b1} \approx I_{b2}$ in Fig. 4, for $V_{od} = 0$) required for biasing the transistors are taken from the driving generators connected to the inputs. Their value, $I_{bias} = (I_{b1} + I_{b2})/2$, is directly related to the design of the differential stage. A very low base current value requires high current gain (β). This can be obtained, for example, by using Darlington or super $-\beta$ transistors. It can also be noted that the influence of the base currents is reduced to the minimum, if both inputs are driven by generators with the same equivalent output resistance.

Component Mismatch Effects. All of the effects due to amplifier dissymmetry can be characterized with only two continuous generators: a voltage generator (V_{os}) and a current generator (I_{os}). These two generators are discussed in the next paragraphs. Thus, as indicated in Fig. 6, the real amplifier is

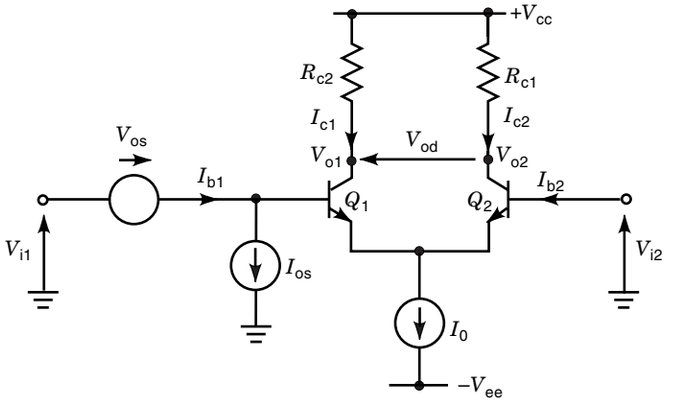

Figure 6. Mismatched differential stage. Equivalent circuit with a perfectly matched amplifier and offset voltage and current sources.

equivalent to the ideal differential stage previously discussed, with V_{os} and I_{os} connected on input.

Input Offset Voltage. This voltage results principally from the dissymmetries between transistors Q_1 and Q_2: mismatches in the base widths, in the base and collector doping levels, and in emitter areas. It is also caused by mismatch in collector resistors R_{C1} and R_{C2}. By definition V_{os} is the ideal equivalent generator voltage, which applied to the input, drives the output voltage (V_{od}) to zero. Then $V_{os} = V_{be1} - V_{be2}$ (Fig. 6).

Assuming that the relationship between the base-emitter voltage and collector current for a forward biased transistor is $V_{BE} = V_T \ln(I_C/I_S)$,

$$V_{os} = V_T \ln[(I_{C1}/I_{C2})(I_{S2}/I_{S1})] \tag{6}$$

Now the saturation and collector currents can be written as $I_{S1} = I_S = I_{S2} - \Delta I_S$ and $I_{C2} = I_C = I_{C1} - \Delta I_C$. In addition, with $R_{C1} = R_C = R_{C2} - \Delta R_C$, which represents the resistor dissymmetry,

$$R_{C2} I_{C2} = R_{C1} I_{C1}$$

Finally, assuming that $\Delta I_S/I_S \ll 1$ and $\Delta R_C/R_C \ll 1$, V_{os} can be described by

$$V_{os} = V_T \left[\frac{\Delta R_C}{R_C} + \frac{\Delta I_S}{I_S} \right] \tag{7}$$

Input Offset Current. This current results principally from the mismatched values of the current gains β of Q_1 and Q_2. When V_{od} is zero, I_{os} is defined by $I_{os} = I_{b1} - I_{b2}$. Assuming that $\beta_1 = \beta = \beta_2 - \Delta\beta$, from the previous equations this gives

$$I_{os} = \frac{I_C}{\beta} \left[\frac{\Delta R_C}{R_C} + \frac{\Delta\beta}{\beta} \right] \tag{8}$$

Now we can deduce that the offset current is directly proportional to the base input bias current. Then a low value for I_{os} necessitates either a low I_0 or a high β. High R_C values also reduce this unwanted current I_{os}.

Thermal Drift. We define thermal drift as the variation of component electrical parameters with temperature. So, for a given differential amplifier design, the drift of I_b, V_{os}, and I_{os} characterizes the influence of temperature on the output voltage V_{od}. Thus, the drift of the bias current I_b determines the output stability for different values of the driving generator resistance. The thermal drift of V_{os} can be directly calculated from Eq. (7). Assuming that R_C and I_S are temperature-independent,

$$\frac{dV_{os}}{dT} = \frac{V_{os}}{T} \tag{9}$$

Equation (9) shows a direct proportionality to V_{os}. Moreover, a low drift for I_{os} is necessary to obtain low output variation when the internal resistances of the driving generators have high values.

Long-Term Drift Variation. All of the previous values of drift given by manufacturers are rigorously valid for fresh components, but drift changes as components age.

Voltage Input Noise. Low-frequency input noise is an important limitation in precision dc application, as, for example, instrumentation measurements.

ANALYSIS OF MOS DIFFERENTIAL PAIR

Now we analyze a differential stage implemented from MOS transistors to compare their performance to bipolar ones.

Ideal Input Stage

An NMOS source-coupled pair is shown in Fig. 7. We assume that both M_1 and M_2 are matched transistors with equal W/L ratios (W is the channel width and L is the channel length) and equal threshold voltage V_{th}. We neglect the body effect and the channel modulation length. The load resistors R_d are assumed identical. As usual we suppose that the drain current is related to the gate-source voltage V_{gs} and the threshold voltage V_{th} by the well-known approximate square-law relationship $I_d = K(V_{gs} - V_{th})^2$, where the gain factor $K = 1/2\mu C_{ox}\ W/L$ (μ is the electron-mobility and C_{ox} is the gate capacitance per unit). From Kirchhoff's laws it follows that the differential input voltage is given by $V_{id} = V_{i1} - V_{i2} = \sqrt{I_{d1}/K} - \sqrt{I_{d2}/K}$, and at the source node, $I_{d1} + I_{d2} = I_0$. Combining these expressions yields (8)

$$I_{d1} = \frac{I_0}{2}\left[1 + KV_{id}\sqrt{\frac{2}{KI_0} - \left(\frac{V_{id}}{I_0}\right)^2}\right] \tag{10}$$

$$I_{d2} = \frac{I_0}{2}\left[1 - KV_{id}\sqrt{\frac{2}{KI_0} - \left(\frac{V_{id}}{I_0}\right)^2}\right] \tag{11}$$

Consequently the differential output voltage V_{od} is expressed by

$$V_{od} = R_d(I_{d2} - I_{d1}) = -R_d KV_{id}\sqrt{\frac{2I_0}{K} - (V_{id})^2} \tag{12}$$

This expression is valid as long as both transistors M_1 and M_2 are in the saturated mode which is proved by $|V_{id}| \ll \sqrt{I_0/K}$. When this condition is satisfied, the gain A of the differential amplifier is given by $V_{od}/V_{id} = R_d\sqrt{2I_0K}$.

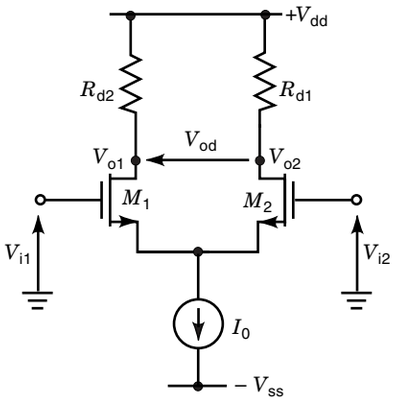

Figure 7. The NMOS source-coupled pair using matched devices.

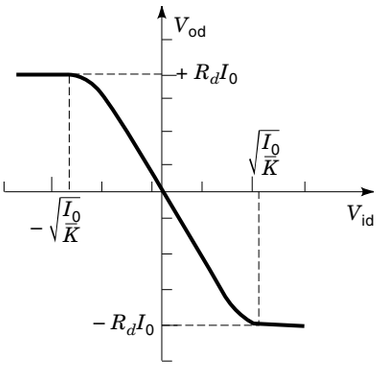

Figure 8. The dc transfer characteristic of the ideal source-coupled pair.

Note that for the MOS differential pair, the V_{id} range for linear operation depends on the biasing current I_0 and the W/L ratio of the transistors. In contrast, for the bipolar differential pair this range is about $2V_T$ and is independent of transistor size and bias current. The gain of the source-coupled pair depends on bias current I_0, load resistance R_d, and transistor dimensions (W/L). In contrast, the gain for the bipolar differential pair depends only on the biasing current I_0 and load resistance R_c.

The dc transfer characteristic of the source-coupled pair is shown in Fig. 8. When $|V_{id}| > \sqrt{I_0/K}$, either M_1 or M_2 is completely turned off, and V_{od} is equal to R_dI_0. An increase in I_0 increases the linear operating region, whereas an increase in the W/L ratio causes the opposite effect (8).

Real Input Stage

Technological Constraints. Until now we have studied the behavior of the ideal MOS amplifier. A real differential pair presents some dc errors that produce basic limitations for many analog systems.

In dc and low frequencies, the threshold voltage V_{th} and the gain factor K represent the predominant sources of static errors in a source-coupled pair (3). The deviations in the threshold voltage and the gain factor are due to technological parameters. The difference in V_{th} between two matched transistors results mainly from differences in oxide thickness and bulk doping. Actually the oxide thickness in VLSI MOS processing is so reproducible that it has only a negligible effect on V_{th}. Consequently, changes in substrate doping are the principal source of threshold voltage mismatch V_{th} which is typically 10 mV to 25 mV. The gain factor includes two parameters, the factor $K' = 1/2\mu C_{ox}$ and the gate dimensions W and L. The changes in mobility in K' depend on deviations in bulk doping. Deviations in W and L result from photolithography variations. The latter variations represent the main source of deviations in the gain factor. The differences between the load resistances, whose typical values depend on size, also contribute to the dc errors in the source-coupled pair (3).

The effects of mismatches on dc performance in MOS amplifiers are represented only by the input offset voltage due to high impedance of the gate of MOS transistors (6).

Input Offset Voltage. As mentioned earlier, the input offset voltage V_{os} is the input voltage required to force the differential output voltage to zero. Summing voltages around the source loop in Fig. 9 gives

$$V_{os} = V_{th1} - V_{th2} + \sqrt{\frac{I_{d1}}{K_1}} - \sqrt{\frac{I_{d2}}{K_2}}$$

To make the differential output V_{od} exactly zero requires that $R_{d1}I_{d1} = R_{d2}I_{d2}$. Using the last expression, we find that (3)

$$V_{os} = \Delta V_{th} + \frac{V_{gs} - V_{th}}{2}\left[-\frac{\Delta R_d}{R_d} - \frac{\Delta K}{K}\right] \tag{13}$$

where the difference quantities are given by $\Delta V_{th} = V_{th1} - V_{th2}$, $\Delta R_d = R_{d1} - R_{d2}$, and $\Delta K = K_1 - K_2$, and the average quantities are given by

$$V_{th} = \frac{V_{th1} + V_{th2}}{2}, R_d = \frac{R_{d1} + R_{d2}}{2}, \quad \text{and} \quad K = \frac{K_1 + K_2}{2}$$

The offset voltage in Eq. (13) consists of two parts. One equals the threshold voltage mismatch and the other contains mismatches in load resistances and gate dimensions. Note that V_{os} mismatch depends on differences and also on biasing points. When the transistors are biased at small values of $(V_{gs} - V_{th})$, the influence of ΔR_d and ΔK becomes smaller. Consequently, at weak inversion the main factor influencing the input offset voltage is ΔV_{th}.

The main difference between bipolar and MOS differential stages is the mismatch in the threshold voltage. For a MOS stage, this results in a constant offset component that is independent of bias current. Consequently the MOS differential stage displays a higher offset voltage than the bipolar pair.

Offset Voltage Drift. The drift of the input offset voltage of a MOS differential pair is given by $\Delta V_{os}/\Delta T$ (8). Contrary to the bipolar case, the offset voltage drift in MOS stages is not directly correlated with the offset voltage.

The temperature drift of the offset value depends on variations of V_{th} and K. The variation of V_{th} is as high as some mV/°C. But the changes in K are considerably larger because K includes mobility.

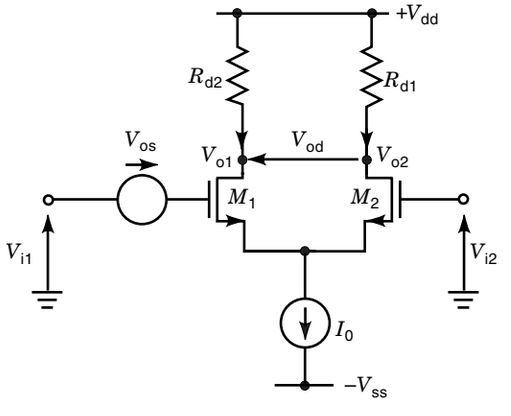

Figure 9. The NMOS source-coupled pair with the dc offset voltage source.

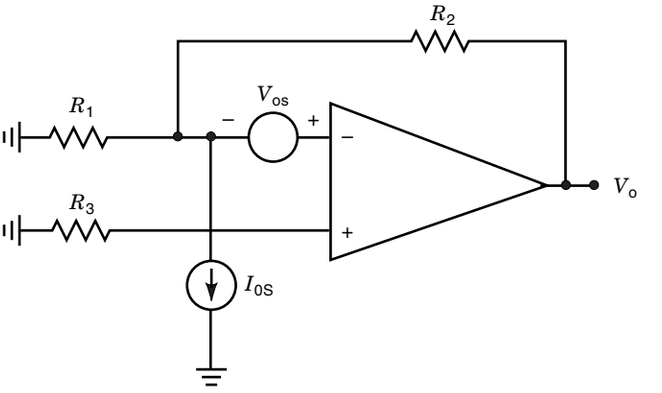

Figure 10. Schematic form of the feedback implementation including offset generators.

GENERAL CRITERION FOR IMPLEMENTING DC AMPLIFIERS

Comparison Between Bipolar and MOS Stages

Generally bipolar input stage amplifiers have much better long-term stability than MOS devices can offer. Very good matching between the input transistors is obtained with bipolar differential pairs. Indeed for bipolar transistors the transconductance parameters do not depend on both the area of the transistor and the technology. In contrast, for MOS differential stages the transconductance is strongly dependent on the W/L ratio and the fabrication processes. As a result bipolar stages exhibit lower offset voltage and temperature drift. In addition for the same value of the bias current, they will be smaller than MOS to have the same value for the transconductance. Nevertheless bipolar stages exhibit large input bias currents. In contrast, MOS input stages take advantage of a high input impedance resulting in low offset current and low bias current. This makes them ideal for portable systems and micropower applications.

Feedback Loop Effects

Figure 10 shows the circuit that can be used to calculate the output offset voltage of an amplifier in its usual feedback configuration. This is valid for both the inverting and noninverting amplifier configurations, shown in Fig. 3. The value of R_3 is assumed to be $(R_1//R_2)$ and to cancel the effects of the bias current I_b.

Calculation gives

$$V_o = -\left(1 + \frac{R_2}{R_1}\right)V_{os} + R_2 I_{os} \tag{14}$$

This reveals that the coefficient of V_{os} can be expressed directly in terms of the closed loop gain. Consequently the input offset voltage becomes preponderant for low values of R_2.

GENERAL TECHNIQUES USED TO REDUCE DC ERRORS IN AMPLIFIERS

As shown previously, dc offset limits numerous applications in linear IC. For example, offset voltage is a particularly important parameter for precision instrumentation amplifiers

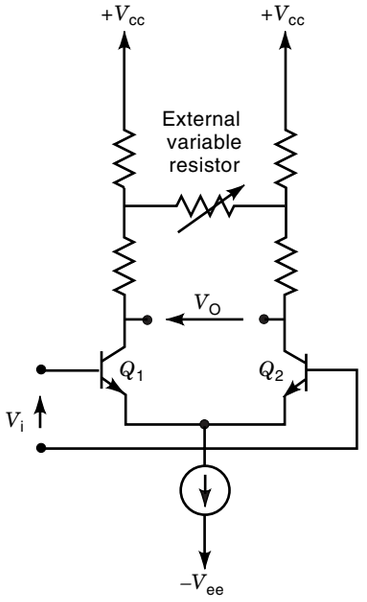

Figure 11. Conventional method for canceling dc offset voltage using a variable resistor to adjust the collector resistors ratio.

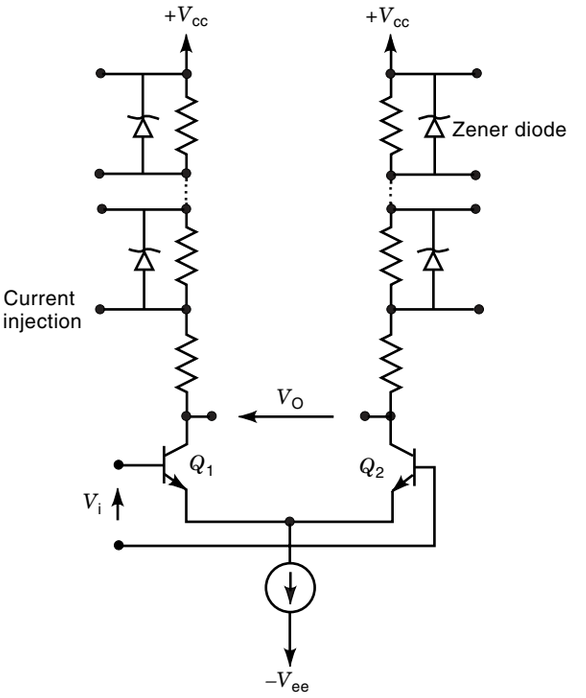

Figure 12. Zener-zap trimming technique. Zener diodes are placed in parallel with load resistors, and must be shorted with a current injection to adjust the offset voltage to zero.

and for applications where rail-to-rail output signal swing is required. In these latter cases, the *dc* offset reduces the dynamic range, which is, in turn, very restrictive when designing in low-voltage technology (CMOS). Several techniques, however, can be used to compensate for this nonideal effect. Two ways to proceed are addressed in this section. We have, on the one hand, what we call "offset trimming techniques" and, on the other, improved circuit designs tending to eliminate the dc offset.

Various Adjustment Possibilities

Because the input differential stage generates the dc offset, it is exclusively on this stage that any corrections need to be performed. The emitter-coupled pair (or source-coupled pair) analyzed previously, is the most commonly used input stage. One solution for canceling the offset is to adjust the collector resistor ratio (which should be equal to one) with an external (out of chip) variable resistor, as shown in Fig. 11. This variable resistor is controlled by a potentiometer which adjusts its value for canceling the dc offset voltage. Thus $V_{od} = 0$ when $V_{id} = 0$. The well-known operational amplifier 741 uses this technique to eliminate the dc offset which is typically about 2 mV without correction. The offset drift is about 70 μV/°C. Moreover, this resistor adjustment can also be realized with a laser beam. This automated process is performed directly on the wafer, and the laser adjusts the resistor size on the chip. This has the possible disadvantage of being an irreversible process. The precision operational amplifier OPA177 from Burr–Brown combines both of these methods: laser-trimming offset and an optional connection to an external potentiometer. Then the offset achieved is about 10 μV, and the drift is only 0.3 μV/°C.

Another nulling technique consists of replacing each of the two load resistors R_c with several resistors in series. Then each resistor is in parallel with Zener diodes, as shown in Fig. 12. Injecting a current pulse into the diode permanently shorts its parallel resistor. In practice the series resistors have different values for refining the adjustment. In the OP-07A from Precision Monolithic Inc., this "Zener-zap trimming" technique reduces the offset voltage to 10 μV and the drift to 0.2 μV/°C (9).

We demonstrated previously that in the bipolar, emitter-coupled pair, the dc offset voltage and drift are given by Eqs. (7) and (9). Thus in theory, if we null V_{os}, then the drift is also nulled. In practice, however, introducing the potentiometer creates a new drift factor, which cannot be eliminated simultaneously (10).

In conclusion it is important to see in these offset trimming techniques that adjusting the resistors is performed at a single fixed temperature. In consequence, for applications over a wide range of temperature, the drift will be important (11). In the next part we see more ways to improve the performance when designing specific circuits to correct dc errors.

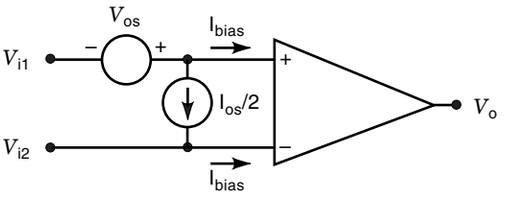

Figure 13. An amplifier with dc offset sources; input offset voltage (V_{os}), and input offset current (I_{os}).

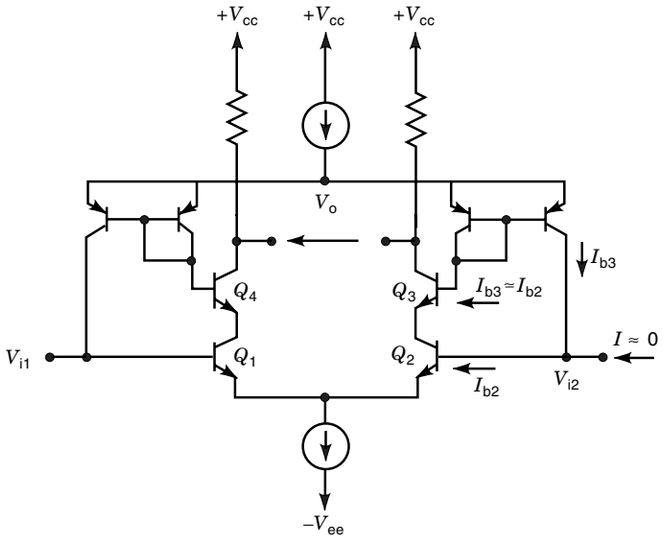

Figure 14. A method for canceling the input bias current in a bipolar differential pair. The base current of Q_3 is mirrored to the base of Q_2. It reduces considerably I_{bias} current and I_{os} current.

Circuits with Improved Design

Correcting the dc Offset Current and Input Bias Current. We can represent an amplifier with different offset sources as shown in Fig. 13. The advantage of the MOS differential pair, compared with the similar bipolar input stage, is the very low (about 100 pA) input bias current (I_{bias}). In addition, the MOS differential pair results in very low input offset current (I_{os}), about 10 pA. The isolated gate of the MOS allows this characteristic. Nevertheless, this advantage practically disappears when diodes are included to protect the gates from electrostatic discharges. In the case of the bipolar differential pair, the values of I_{bias} and I_{os} are directly proportional to the base currents of the transistors, as explained previously.

A method for canceling the input bias current is shown in Fig. 14. The base currents of Q_2 and Q_3 are practically identical because the same current flows through their collectors. Then the base current of Q_3 is mirrored to the base of Q_2. The same applies for Q_4 and Q_1. As a result, the I_{bias} current is nulled, and I_{as} is considerably reduced. For example, using this method, the precision operational amplifier OPA177 from Burr–Brown provides 0.5 nA for I_{bias} and 0.1 nA for I_{os}.

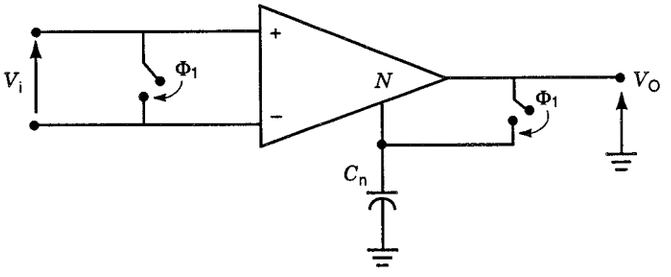

Figure 15. A basic autozero amplifier. The offset voltage is sampled, held in capacitor C_n, and injected at a nulling input (N). This correction is controlled by a clock (Φ).

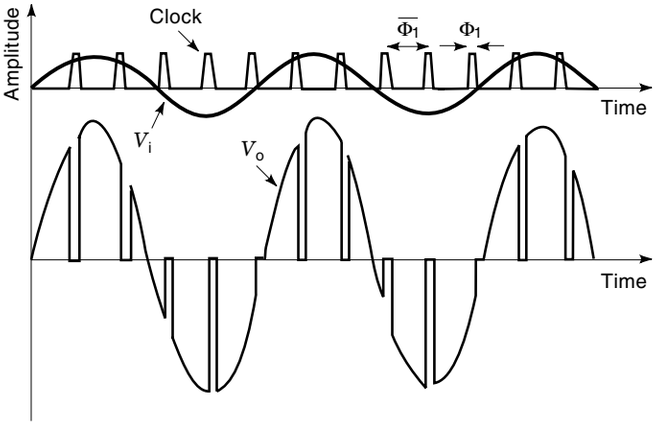

Figure 16. Input, output, and clock signals in a basic autozero amplifier. The discontinuities in output signal must be eliminated with a low-pass filter.

Correcting the dc Offset Voltage. In this section we address a widely used method for designing low-offset voltage and low-drift amplifiers. This technique, based on the "autozero" concept (AZ) (12), in addition, allows canceling low-frequency noise (12,13). An AZ amplifier is shown in Fig. 15. This technique consists of sampling the dc offset of the amplifier and subtracting it from the signal. The sample operations, moreover, are performed with switched-capacitor circuits. This brings us to the functioning of such a configuration. Two phases are needed. In a first stage (Φ_1), the switch shorts the input, and the dc offset appears at the output. Then this quantity is sampled, held by capacitor C_n, and applied at an auxiliary nulling input (N), to eliminate it. In the second stage ($\overline{\Phi_1}$), the amplifier is ridded of the offset and is connected back to the input signal for amplification. Figure 16 shows the input and output signals and the clock which drives the nulling operations. It is easy to see that the output

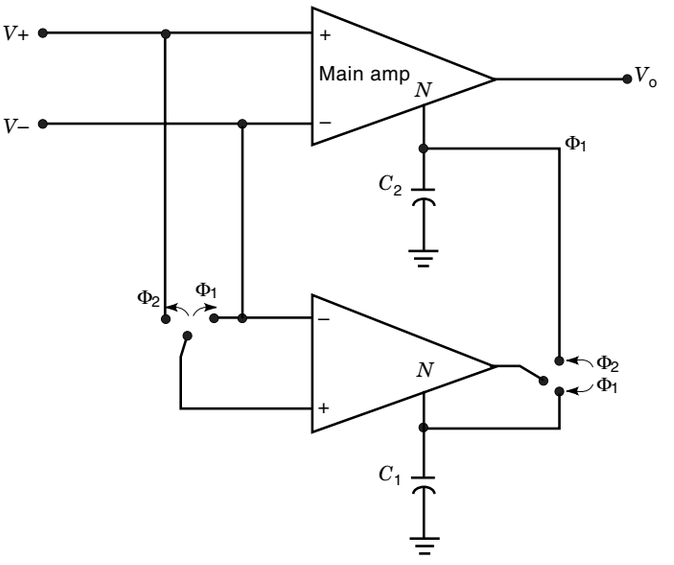

Figure 17. Continuous time autozero amplifier using a main amplifier and a basic auto-zero amplifier.

Table 1. Integrated Circuits Used for dc Applications and Main Characteristics at 25°C

Designation	Manufacturer	Function	Input Offset Voltage	Voltage Drift	Input Bias Current	Input Offset Current
LM741C	National Semiconductor	op amp	2 mV		80 nA	20 nA
OP07A	PMI	ultra low offset op amp	10 μV	0.2 μV/°C	0.7 nA	0.3 nA
AD708S	Analog Devices	ultra low offset op amp	5 μV	0.1 μV/°C	0.5 nA	0.1 nA
OPA177F	Burr–Brown	Precision op amp	10 μV	0.3 μV/°C	0.5 nA	0.1 nA
ICL7650	Maxim	Chopper	0.7 μV	10 nV/°C	1.5 pA	0.5 pA
LTC1100ACN	Linear Technology	Chopper op amp	1 μV	5 nV/°C	2.5 pA	10 pA
TLC2652AM	Texas Instrument	Chopper op-amp	0.5 μV	3 nV/°C	4 pA	2 pA

signal displays discontinuities due to phase Φ_1. Hence it must be low-pass filtered to reduce continuity of the signal. Note that the clock frequency must have at least twice the signal frequency to fulfill the Shannon criterion. Consequently this reduces the application of autozero amplifiers to the low-frequency domain.

Nevertheless, some applications require continuous time amplification. In these cases the amplifier should not be disconnected from the input signal. An improved schema is proposed in Fig. 17: the "continuous time AZ amplifier" or "chopper amplifier." Generally designed with MOS transistors, such amplifiers incorporate two amplifiers internally, a main amplifier and an AZ amplifier. Two phases are needed to describe the operation. During the first phase (Φ_1), the AZ amp corrects its own offset, as addressed previously. Then, during the second phase (Φ_2), the offset-free AZ amplifier senses the main amplifier's offset, stores this value in capacitor C_2, and applies it at the nulling input of the main amplifier. Because the offset is constantly corrected even during temperature variations, chopper amplifiers feature very good performance. For instance, the LTC110 precision chopper instrumentation amplifier from Linear Technology reduces the offset voltage to typically 1 μV and the drift to 5 nV/°C. Therefore such amplifiers are very useful for precision applications. Table 1 lists the main dc characteristics at 300 K of different amplifiers used for dc operation (9,14–16).

OTHER AVAILABLE IMPLEMENTATIONS

Dc amplifiers can also be designed from basic building blocks other than operational amplifiers. Various possible implementations and their particularities are addressed in this section. Their typical dc input errors are listed in Fig. 18. This figure also displays the errors of classical IC amplifiers.

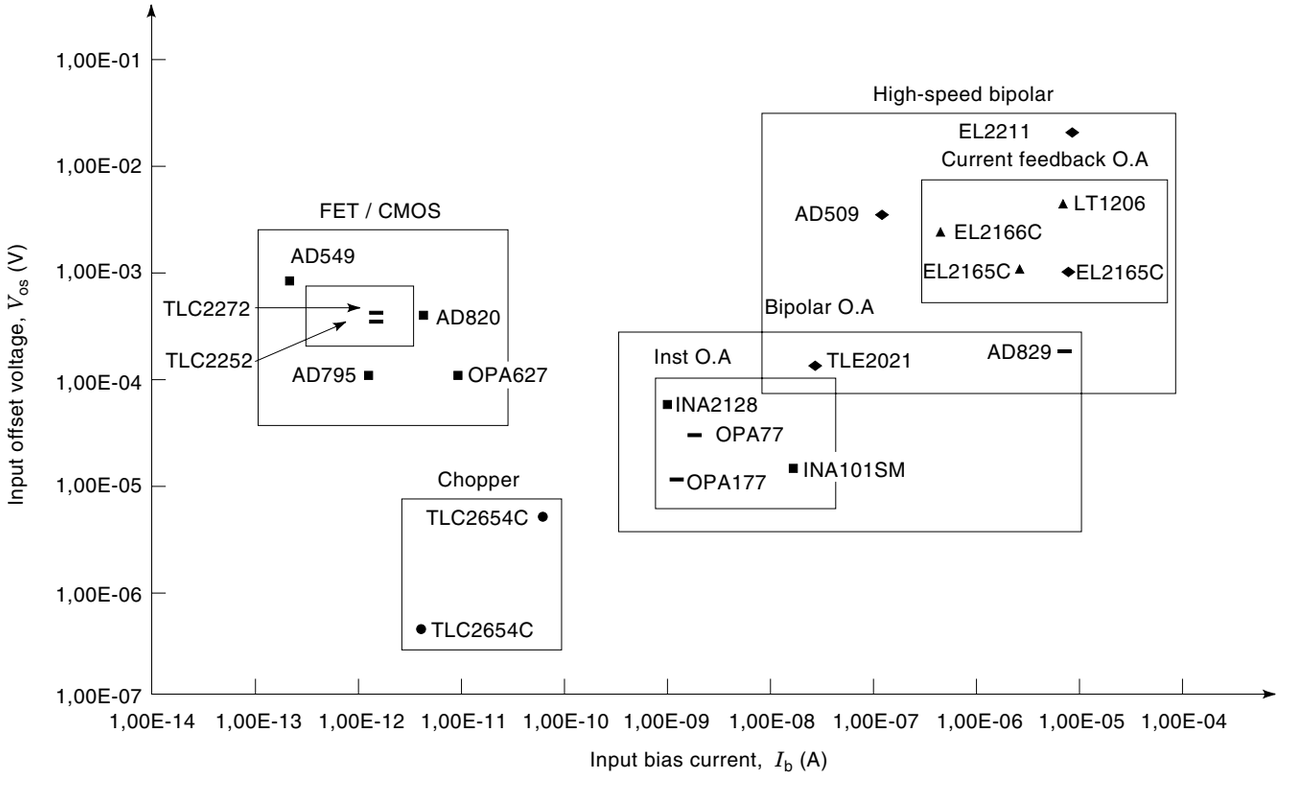

Figure 18. Typical voltage and current offsets for various IC amplifier families.

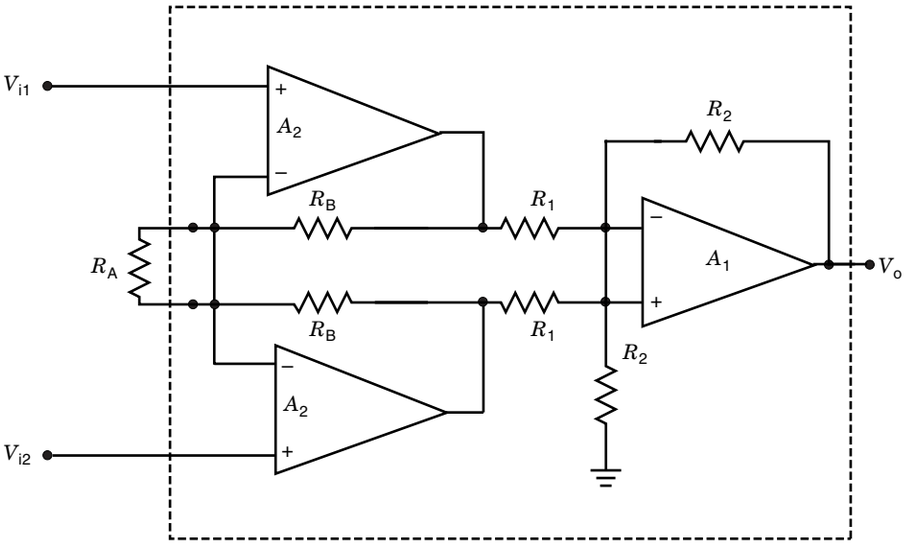

Figure 19. Instrumentation amplifier.

Instrumentation Amplifiers

Such integrated amplifiers incorporate three operational amplifiers in a single chip (1,7). Matched resistors obtained with laser trimming are also included to cancel typical dc errors. The resulting circuit is shown in Fig. 19. A_1 is connected as a difference amplifier. A_2 and A_2' are in a noninverting configuration. Thus the output voltage is given by

$$V_o = (V_{i1} - V_{i2})\frac{R_2}{R_1}\left(1 + \frac{2R_B}{R_A}\right) \tag{15}$$

So, the amplifier gain can be easily adjusted with R_A connected out of chip.

Current Feedback Operational Amplifiers

In current feedback operational amplifiers (CFOA) also called transimpedance op-amps, the input cell is different from that used in voltage-feedback op-amps (VFOA) (see Figs. 4 and 7) (17). This cell is basically a second-generation current conveyor (CCII) as shown in Fig. 20, which is commonly described by the following matrix relation:

$$\begin{pmatrix} iy \\ vx \\ iz \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{pmatrix} \times \begin{pmatrix} vy \\ ix \\ vz \end{pmatrix} \tag{16}$$

Figure 21 represents the equivalent electrical circuit for a CFOA (17–21). The inverting and noninverting configurations are realized as shown in Fig. 3. But in that case the output voltage is given by

$$V_o = -Z_T \times i^- \tag{17}$$

with $Z_T = R_T \| C_T$ which is the output impedance at port Z of the CCII. The CFOA exhibits higher bandwidths than classical operational amplifiers. Indeed the bandwidths are proportional to $1/R_2C_T$ (R_2 is the feedback resistor in Fig. 3). The slew rate is also greatly increased (about 1000 V/μs). Nevertheless, dc errors are particularly prevalent in CFOA designs. The dissymmetries between the inputs imply that their bias currents do not match or cancel.

High-Speed Operational Amplifiers

The input stage of high-speed operational amplifiers is generally identical to the one of classical op-amps. Their output is nevertheless constituted from the difference between two output currents. This improves the speed and bandwidth to the detriment of input errors.

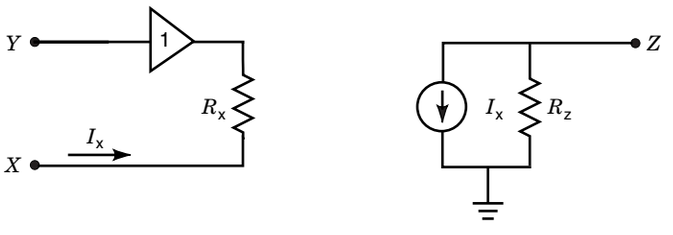

Figure 20. Equivalent macromodel of the second generation current conveyor.

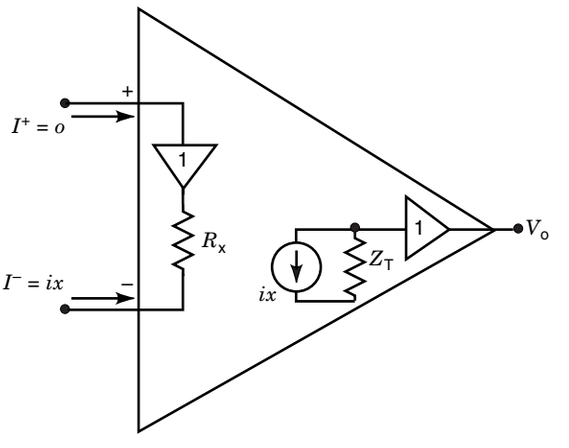

Figure 21. Current feedback operational amplifier obtained from a second generation current conveyor and a voltage follower.

CONCLUDING REMARKS AND PROSPECTIVE DEVELOPMENTS

In this article we have inspected the mismatches and drift effects on the performance of dc amplifiers implemented from op-amps. Bipolar and MOS differential inputs stages have successively been analyzed. NPN and NMOS transistors have only been considered above. Nevertheless differential amplifiers can also be implemented from PNP or PMOS elements. In these cases note that PNP transistors exhibit lower β values and the mobility of PMOS transistors is about three times smaller.

The general criterion to consider for implementing dc amplifiers and the most commonly used techniques to reduce dc errors have been investigated.

As indicated, dc amplifiers can also be designed from other available building blocks: Traditionally all these dc amplifier implementations use voltage input signals. Rushing into the opening created by the introduction of the CFOA, another design approach could consist in using current input signals in place of voltages.

Second-generation current conveyors can be driven from current signals and these could certainly be used advantageously in designing dc amplifiers.

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DC CONVERTERS. See HVDC POWER CONVERTERS.