$$\begin{pmatrix} i_Y \\ v_X \\ i_Z \end{pmatrix} \begin{pmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & -1 & 0 \end{pmatrix} \begin{pmatrix} v_Y \\ i_X \\ v_Z \end{pmatrix}$$

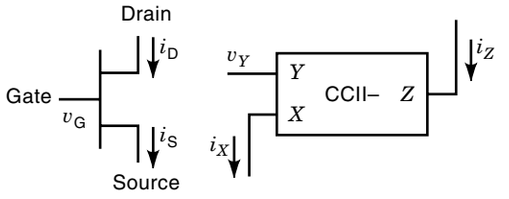


Figure 2. Comparison of a CCII− and an ideal field effect transistor.

CURRENT CONVEYORS

A current conveyor is an active circuit used to carry out analog signal processing functions for many different types of applications. In general, this device has two inputs and n outputs; however, most applications involve a current conveyor with two inputs and one output port, as illustrated in Fig. 1 (1). The current conveyor can be thought of as a basic design building block much like an operational amplifier. During work on his master's thesis in 1966, Adel Sedra was developing a voltage-controlled waveform generator to be used as part of a design of a programmable instrument for incorporation in a system for computer controlled experiments, when he happened upon a novel circuit (2). He generalized the concept and developed the *current conveyor,* a circuit that conveys current from one port to another. His original design, now called a *first-generation current conveyor* (CCI) is a three-port device (with ports defined as X, Y, and Z) described by the following hybrid matrix:

$$\begin{pmatrix} i_Y \\ v_X \\ i_Z \end{pmatrix} = \begin{pmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{pmatrix} \begin{pmatrix} v_Y \\ i_X \\ v_Z \end{pmatrix} \tag{1}$$

This circuit exhibited a virtual short circuit at node X, a virtual open circuit at node Y, and the current supplied at X was conveyed to Z. Node Z had a very high impedance. Applications of the CCI included current meters and negative impedance converters (NICs). To increase the versatility of the current conveyor, a second-generation current conveyor (CCII) was introduced (2). This design was the same as the previous except that no current flowed through node Y. This design was introduced in 1968 and is described by the following hybrid matrix:

$$\begin{pmatrix} i_Y \\ v_X \\ i_Z \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{pmatrix} \begin{pmatrix} v_Y \\ i_X \\ v_Z \end{pmatrix} \tag{2}$$

The current supplied to node X has either a positive or negative polarity resulting in the CCII+ or CCII−, respectively. The CCII− can be thought of as an *ideal* field effect transistor (FET) where the gate = node Y, drain = node Z, and source = node X. This relationship is illustrated in Fig. 2. Traditionally, the current conveyor has been implemented using low-frequency bipolar transistors, FETs, or operational amplifiers (3–5). Two particular applications of the current conveyor are active network synthesis and analog signal processing. Table 1 (6) illustrates several networks useful in active network synthesis. These circuit topologies are by no means the only way to implement these functions.

An important application is analog signal processing. Table 2 (6) illustrates the use of current conveyors to carry out five different signal-processing functions. For purposes of analysis, it is much easier to relate the current conveyor to two ideal one-port networks known as norators and nullators.

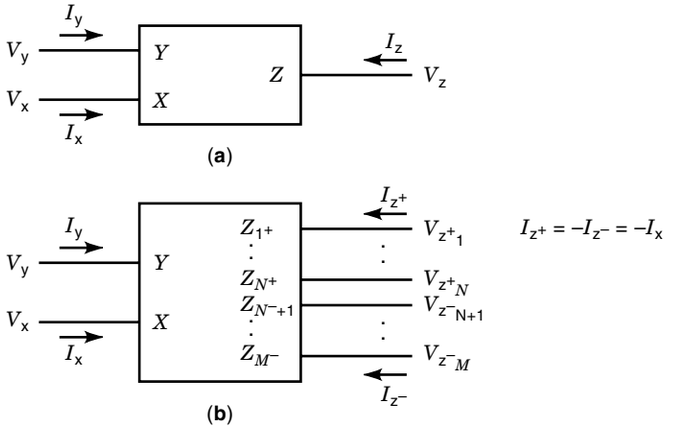
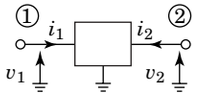
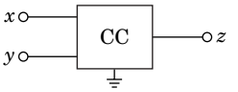
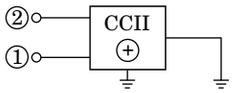
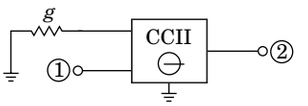
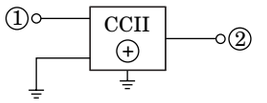
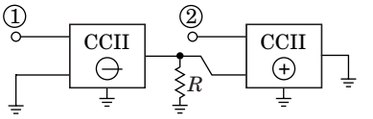
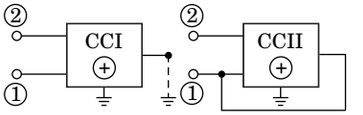
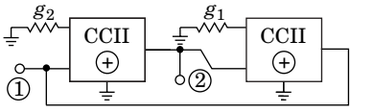
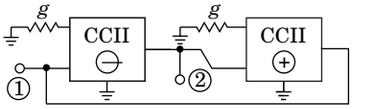


Figure 1. Current conveyor schematic definitions: (a) basic current conveyor and (b) multiple output current conveyor. © 1996 IEEE.

NULLATOR–NORATOR CIRCUIT ANALYSIS AND ITS APPLICATION TO CURRENT CONVEYOR DESIGN

There is good reason to discuss the design of current conveyor circuits using nullator–norator design techniques. One of the strongest motivations is that numerous papers and texts have been written that address circuit synthesis using these ideal circuit elements (7–11). As a result, the use of this technique provides the designer with a wealth of information on designing many types of active networks including negative impedance converters, negative impedance inverters, positive impedance inverters, and a myriad of other useful active networks. All that is required to use this information is a basic understanding of circuit analysis using the norator–nullator approach and an understanding of how to convert norator–nullator topologies into current conveyor topologies.

Table 1. Application of Current Conveyors to Active Network Synthesis

	2-Port Realized	Characterization	Realization Using Current Conveyors
			
1	Voltage—controlled Voltage—source	$\mathbf{G} = \begin{bmatrix} 0 & 0 \\ 1 & 0 \end{bmatrix}$	
2	Voltage—controlled Voltage—source	$\mathbf{Y} = \begin{bmatrix} 0 & 0 \\ g & 0 \end{bmatrix}$	
3	Current—controlled Current—source	$\mathbf{H} = \begin{bmatrix} 0 & 0 \\ 1 & 0 \end{bmatrix}$	
4	Current—controlled Voltage—source	$\mathbf{Z} = \begin{bmatrix} 0 & 0 \\ R & 0 \end{bmatrix}$	
5	INIC	$\mathbf{G} = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix}$	
6	NIV	$\mathbf{Y} = \begin{bmatrix} 0 & -g_1 \\ -g_2 & 0 \end{bmatrix}$	
7	Gyrator	$\mathbf{Y} = \begin{bmatrix} 0 & -g \\ g & 0 \end{bmatrix}$	

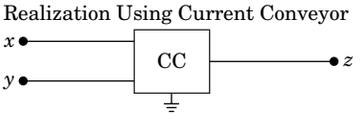
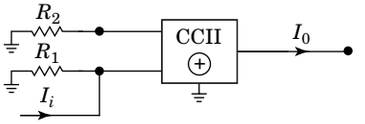
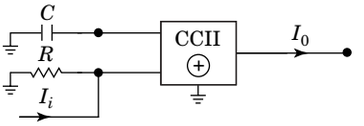
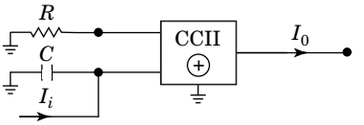
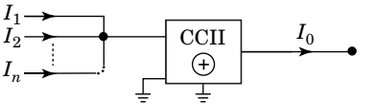
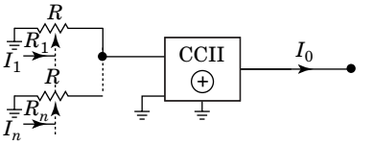
When analyzing active linear networks, several distinct types of circuit elements are used. These include resistors, capacitors, inductors, transmission lines, independent voltage sources, independent current sources, dependent voltage sources, and dependent voltage sources. The dependent voltage and current sources tend to be two-port networks that associate a voltage or current from one port to a voltage or current to the second port. Although analyzing circuits containing these two-port networks is relatively straightforward, the simultaneous solution of equations that usually results from such analysis serves to reduce the designer's intuition about the circuit. The use of two ideal one-port network representations known as *nullators* and *norators* can help to restore some of this lost intuition. Nullators and norators can replace all dependent voltage and current sources in a network so as to reduce the primitive elements in a linear network to only one-port networks. This is a very powerful technique that can be used to gain insight into active network synthesis (7–9). The properties of the nullator and norator will now be introduced.

Definition 1. A nullator is a one port network with $v_1(t) = i_1(t) = 0$ defining the the voltage and current on its one port (9).

Definition 2. A norator is a one port network with $v_1(t) = A_1(t)$ and $i_1(t) = A_2(t)$ defining the voltage and current on its one port. The functions $A_1(t)$ and $A_2(t)$ are arbitrary, and thus $v_1(t)$ and $i_1(t)$ are unconstrained resulting in a degree of freedom not found in any other one port network (9).

The schematic symbol used to describe the nullator and norator are shown in Fig. 3. When carrying out nodal circuit analysis of a circuit that has nullators and norators, Defini-

Table 2. Application of Current Conveyors to Analog Signal Processing

Functional Element	Function	Realization Using Current Conveyor
		
Current—amplifier	$I_0 = (R_1/R_2)I_I$	
Current—differentiator	$I_0 = CR\,\frac{dI_1}{dt}$	
Current—integrator	$I_0 = \frac{1}{CR}\int I_1\,dt$	
Current—summer	$I_0 = \overset{n}{\underset{i}{\bullet}} I_d$	
Weighted current summer	$I_0 = \overset{n}{\underset{i}{\bullet}} I_d \frac{R_j}{R}$	

tions 1 and 2 can be easily applied when the node being analyzed has a norator or nullator connected to it. When a node has a nullator connected to it, the voltage at that node is assumed to be equal to the voltage at the other node of the nullator; however, it is assumed that no current can flow through the nullator. When a node has a norator connected to it, it is assumed that current flows through the norator, but the voltages on either node of the norator are determined by the rest of the circuit. Similarly, the current through the norator is determined by the rest of the circuit.

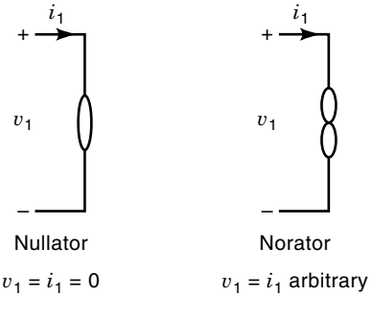


Figure 3. Norator and nullator schematic representations.

Several equivalence properties of norators and nullators that allow for network simplification will be described presently (9):

1. A series or parallel connection of $\pm R$s, $\pm L$s, $\pm C$s, and at least one nullator is equivalent to a single nullator.
2. A series or parallel connection of $\pm R$s, $\pm L$s, $\pm C$s, and at least one norator is equivalent to a single norator.
3. A series or parallel connection of $\pm R$s, $\pm L$s, $\pm C$s, and at least one norator and at least one nullator is equivalent to an open circuit or a short circuit, respectively.
4. A four-terminal circuit composed of two nullators and two norators all of which have a single terminal tied to one node is equivalent to a four-terminal network composed of an uncoupled single nullator and a single norator.

Another circuit element that is worth mentioning is the nullor. The nullor is a two-port network, which is simply composed of a nullator at one port and a norator at the second port. Effectively, it is two uncoupled one-port networks. The schematic symbol for this network is illustrated in Fig. 4. The reason for its use is that many dependent current and voltage sources can be expressed in terms of this unit. It is important

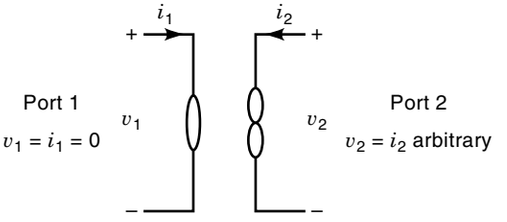


Figure 4. Nullor schematic representation.

to note that the nullor can always be thought of as simply a nullator and a norator and, therefore, provides no additional insight into the analysis of a network. It is mentioned here merely so that the reader will be familiar with the terminology.

Given the matrix definition of the negative second-generation current conveyor (CCII−) from Eq. (2), an equivalent representation for the CCII− can be expressed in terms of a single nullator and norator as illustrated in Fig. 5. The hybrid matrices for these two circuits are equivalent. In summary, any active network composed of nullators and norators in pairs, as illustrated in Fig. 5, can be fabricated using CCII− networks. This fact will prove to be a useful property for synthesizing many types of active circuits.

As an example, two useful illustrations of the nullator–norator design technique types will be discussed. First, the impedance inverter is presented. Table 3 (10) illustrates five different methods for carrying out voltage and current inversion. It is important to note that these realizations do not require a specific hardware realization. By looking for pairs of norators and nullators, we can convert these circuits into current conveyor circuits. Each topology will have its own specific performance benefit as explained in Ref. 10.

Another useful topology is shown in Fig. 6 and can be used as a general impedance converter (GIC). Each of the branches of the circuit can be a complex impedance. The relationship that will hold between impedances is

$$Z_1 Z_3 Z_5 = Z_2 Z_4 Z_6 \tag{3}$$

The way the network is used is to remove one of the complex load impedances illustrated in Fig. 6 and solve for its value in terms of the remaining five impedances. The relationship in Eq. (3) will define the effective impedance at the circuit port where the complex impedance was removed. This process allows for the transformation of one of the five remaining load impedances to an effective output impedance whose properties depend on the circuit elements used in the network, thus the name general impedance converter (GIC). This type of circuit can be used as a positive impedance converter (PIC) or a positive impedance inverter (PII). Another useful application of this circuit is realization of a frequency-dependent negative resistance (FDNR), sometimes called a D element or an E element (9). These are very useful in active filter synthesis as explained by Bruton (9). Filters can be synthesized using only FDNRs and resistor elements. The D element has an impedance $Z = k/s^2$ where k is real and s is the complex frequency variable of the Laplace transform. Similarly, the E element has the form $Z = ks^2$ where again k is real.

Note that pairs of norators and nullators from Fig. 6 can be replaced with second-generation current conveyors. The way in which these current conveyors can be realized in hardware is the subject of the next section.

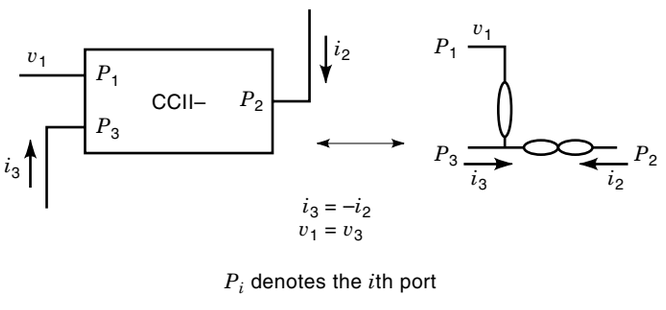


Figure 5. Nullator–norator representation of a CCII−.

CURRENT CONVEYOR CIRCUIT ARCHITECTURE

Current conveyors can be built using either bipolar or metal oxide semiconductor (MOS)–type transistors. Because the majority of applications to date have focused on the second-generation current conveyor, this type of current conveyor will be addressed here. Another motivation for focusing on the implementation of second-generation current conveyors is that first- and third-generation current conveyors can be realized using multiple output second-generation current conveyors (1,12). As mentioned earlier, a CCII− can be thought of as an ideal FET. Similarly, it can also be thought of as an ideal bipolar transistor. In reality, FETs and bipolar devices do not behave ideally, and thus more complex circuit implementations result in order to compensate for the imperfections of real devices. In the process of obtaining more ideal performance, many devices may need to be combined in order to model more closely the ideal behavior exhibited by an ideal device. Implementation of CCIIs with bidirectional current capabilities require the use of complementary devices (i.e., p–n–p and n–p–n bipolars or nMOS and pMOS FETs) (13). It is difficult to fabricate an integrated circuit (IC) with identically performing p–n–p and n–p–n devices. It is much easier to support complementary structures using MOS devices, and thus many IC current conveyor designs are based on MOS implementation. Figures 7 and 8 (13) illustrate CMOS implementation of CCII+ and CCII− current conveyors, respectively. In Fig. 7 current is transferred to the output using complementary current mirrors. To fabricate a CCII− (Fig. 8), two additional current mirrors are required.

A new approach to designing current conveyors at microwave frequencies has been proposed by Sinsky and Westgate (14). This approach uses a GaAs monolithic microwave integrated circuit (MMIC) to closely approximate the required hybrid matrix parameters of Eq. (2) over a specified band of microwave frequencies. This technique was developed to support the design of tunable synthetic microwave circuit elements using negative impedance converters (NICs) and positive impedance converters (PICs). Such circuits can be used to design tunable microwave filters and matching networks.

NOISE CONSIDERATIONS

In many applications, it is necessary to have a current conveyor that has good noise performance. Current mode circuits

Table 3. Voltage and Current Inversion Using Nullators and Norators

Type	Voltage Inversion	Current Inversion
I	$V_2 = -V_1$ $I_2 = I_1$	$-I_2 = -I_1$ $V_2 = V_1$
II	$V_2 = -(R_2/R_1)V_1$ $-I_2 = I_1$	$-I_2 = -(G_2/G_1)I_1$ $V_2 = V_1$
III	$V_2 = -(R_2/R_1)V_1$ $-I_2 = I_1$	$-I_2 = -(G_2/G_1)I_1$ $V_2 = V_1$
IV	$V_2 = -(R_2/R_1)V_1$ $-I_2 = I_1$	$-I_2 = (G_2/G_1)I_1$ $V_2 = V_1$
V	$V_2 = [1 - (R_2/R_1)]V_1$ $I_2 = I_1$	$-I_2 = [1 - (G_2/G_1)]I_1 V_2 = V_1$

(such as the current conveyor) are candidates for use in low-voltage analog signal processing because large current swings can be obtained even with small voltage excursions. Unfortunately, for low-noise performance in such circuits, low-noise bias circuitry, which tends to require higher voltages for the required low-transconductance devices, is required. This presents a design challenge when trying to obtain low-noise, low-

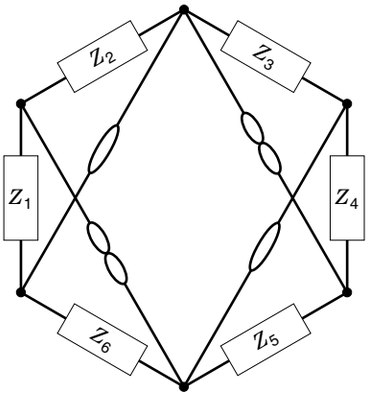


Figure 6. Norator–nullator immitance converter/inverter topology.

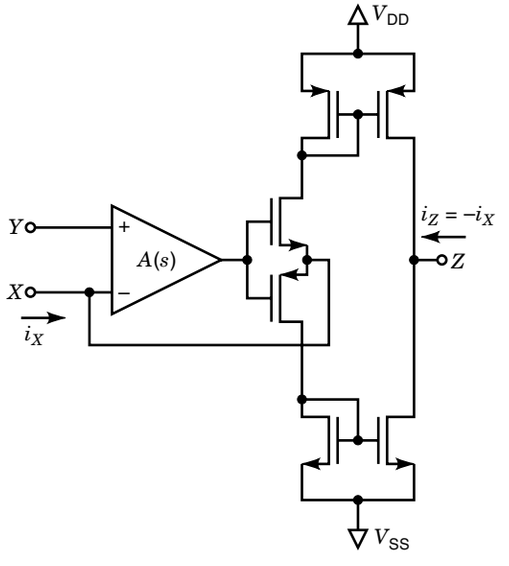


Figure 7. Positive second-generation current conveyor using MOS devices and OP amp. © IEE 1990.

voltage current conveyors. The problem of designing low-noise current conveyors is best addressed by Bruun (1,12) who has developed a way to look at the problem and drawn some important conclusions.

Ideal Current Conveyor Noise Analysis

To address noise issues in the CCI, CCII, and CCIII type current conveyors, it is sufficient to analyze the multi-output CCII current conveyor as shown by Bruun (1,12). The general noise analysis requires addressing the multi-output current conveyor illustrated in Fig. 1. Because this device has multiple outputs, noise contributions cannot be modeled using only an equivalent noise input voltage and current as done on conventional amplifiers. The multiple outputs may have correlated and uncorrelated noise contributions, and thus noise sources must be assumed at each of the output ports as well as the input ports. For more details on the mathematical formulation of the noise for the multioutput second-generation current conveyor, see Refs. 1 and 12. Because most applications simply require single output CCII+ or CCII− current conveyors, the noise modeling for this type of device will be emphasized here. For an ideal two-input single-output second-generation current conveyor whose input X terminal is terminated in an impedance R_X and whose Y input is terminated in an impedance R_Y where $R_{SX} \gg R_{SY}$, Bruun (1,12) has shown that

$$\overline{di_z^2} = \overline{di_{\text{xeq}}^2} + \overline{di_{z_{\text{eq}}}^2} + \frac{\overline{dv_{\text{yeq}}^2}}{R_{SX}^2} + \frac{4kT}{R_{SX}}\,df \tag{4}$$

where k is Boltzmann's constant, T is the absolute temperature, and df is the frequency bandwidth considered (see Fig. 9). The dominant source of error in this formulation is the finite input and output impedances to the current conveyor.

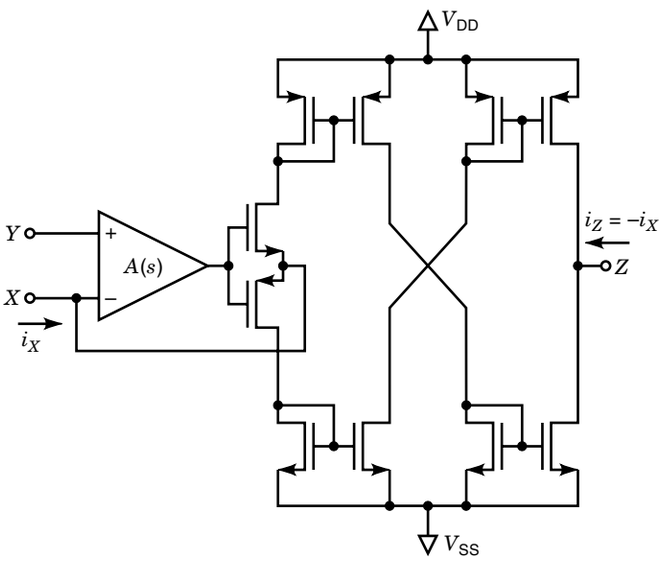


Figure 8. Negative second-generation current conveyor using MOS devices and OP amp. © IEE 1990.

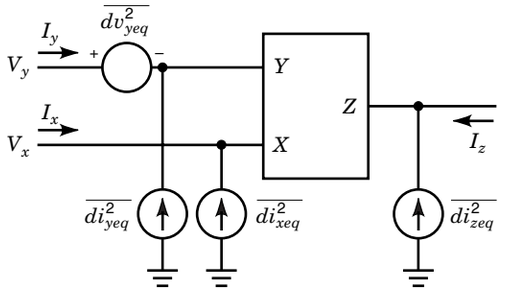


Figure 9. Second-generation current conveyor with equivalent noise sources.

CMOS Current Conveyor Noise Considerations

A detailed analysis of noise optimization for CMOS current conveyors has been carried out by Bruun (1,12). For class A designs, it was found that the optimal signal-to-noise ratio is proportional to the maximum output terminal current (the Z terminal of Fig. 1 is the output terminal). This is because the output noise power of the current conveyor is proportional to the bias current and the output signal power is proportional to the square of the output terminal current. Interestingly, the class *AB*-biased current conveyor can provide better performance than the class *A* circuit because the output signal swing is not limited by the bias current. In summary, the use of low-noise bias circuitry and current mirrors are essential in the design of low-noise CMOS current conveyors.

CONCLUSION

The current conveyor is a very powerful building block that can be used in a myriad of applications ranging from power supply control circuits to the design of high-frequency active filters. Despite the many different applications and implementations of this circuit, there is one important point to remember: the current conveyor is a fundamental building block that can be used in circuit synthesis in much the same way as the operational amplifier. It allows the circuit designer to concentrate on a higher level of circuit functionality. The current conveyor has the capability to revolutionize the circuit design industry in much the same way as the operational amplifier has. With much interest in current mode circuits, it is inevitable that the current conveyors time has finally come.

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CURRENT-FEEDBACK AMPLIFIERS. See ANALOG INTEGRATED CIRCUITS.

CURRENT MEASUREMENT. See AMMETERS; ELECTRIC CURRENT MEASUREMENT.

CURRENT-MODE CIRCUITS. See TRANSLINEAR CIRCUITS.