COMPARATOR CIRCUITS

Comparators are used to *detect* the sign of the difference between two *analog* signals $x_+(t)$ and $x_-(t)$, and to *codify* the outcome of the detection through a *digital* signal y. This operation can be formulated as follows:

$$y = \begin{cases} > E_{\mathrm{OH}} & \text{for} \quad x_+(t) > x_-(t) \\ < -E_{\mathrm{OL}} & \text{for} \quad x_+(t) < x_-(t) \end{cases} \tag{1}$$

where E_{OH} and $-E_{\mathrm{OL}}$ are *levels* that guarantee correct logic interpretation of the output signal, that is, $y > E_{\mathrm{OH}}$ guarantees that the output is unambiguously interpreted as a true logic one (1_{D}) by any digital circuit connected to the output node, whereas $y < -E_{\mathrm{OL}}$ guarantees that the output is interpreted as a true logic zero (0_{D}). The definition of these levels is related to the concepts of logic restoration and digital noise

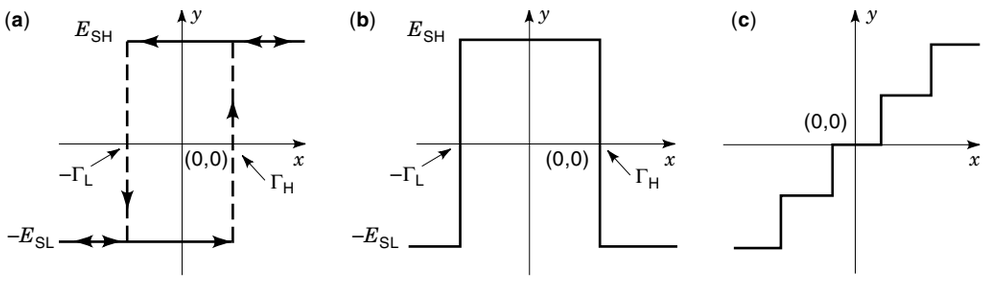

Figure 1. Some useful extensions of the binary comparator concept.

margins that the interested readers will find in Ref. 1. In many applications one of the inputs is a reference value, say $x_-(t) = E$, and the comparator function is to detect whether the signal applied to the other input, say $x_+(t) = x(t)$, is larger or smaller than such reference.

Comparators are classified according to the physical nature of their inputs and output. The most significant structures for practical applications have voltage input and voltage output and are called *voltage comparators.* Most of this article is devoted to them. Others that are also of interest for the newest class of current-mode circuits that have current-input and voltage-output—*current comparators*—are also covered in this article.

Another criterion for classifying comparators is their operation in the time domain. *Continuous time* (CT) comparators operate *asynchronously.* They respond to input changes at any time instant. The speed of change is limited only by the intrinsic comparator response. On the other hand, *discrete-time* (DT) comparators operate in *synchronization* with a clock signal. They respond only at some prescribed time intervals (called *compare,* or active, intervals), whereas others (called *reset,* or strobe, intervals) are used to establish initial conditions. In many applications synchronization is imposed by system-level timing considerations. But, even when synchronization is not mandatory, DT operation can be used for error correction. On the other hand, although DT comparator speed is limited by clock frequency, proper architectures enable operation in the video range and above. Overall responses faster than with CT comparators might even be achieved through proper design.

Comparators are the basic building blocks of analog-to-digital converters. Hence they are crucial components for realizing the front-ends of the newest generations of *mixed-signal* electronic systems (2). Mixed-signal systems are those which combine analog and digital signals. Most modern electronic systems are mixed-signal. They handle analog signals at the input and output interfaces and perform most of the processing, control, and memory tasks by using digital techniques. Other comparator applications include such diverse areas as signal and function generation (3), digital communications (4), or artificial neural networks (5), among others. Because in these applications the prevalent trend is towards microelectronic realizations, this article emphasizes those issues related to the realization of comparators as integrated circuit components. There are also a few extensions of the basic comparator concept of Eq. (1) which further increase the scope of comparator application. Figure 1 shows transfer characteristics for some typical extensions, namely: the *hysteresis* comparator [Fig. 1(a)] (This device has memory. Once the output is in the high state, it remains there whenever the input remains larger than $-\Gamma_L$. On the other hand, once the output is in the low state, it remains there whenever the input remains smaller than Γ_H.), the *window* comparator [Fig. 1(b)], and the *M-ary* (multilevel) comparator [Fig. 1(c)] not covered in this article.

COMPARATOR BEHAVIOR

Ideal Comparator Behavior

Figure 2(a) illustrates the *ideal* comparator operation, where $-E_{SL}$ and E_{SH} are *saturation* levels for the output signal. The interval defined by these levels is usually wider than that defined by the restoring logic level's logic. According to Eq. (1) the output is at the high logic state whenever the differential input $x(t) \equiv x_+(t) - x_-(t)$ is positive, and at the low logic state otherwise. Thus, the ideal *transfer characteristic* exhibits a step transition at $x = 0$, as Fig. 2(a) illustrates. On the other hand, ideally the transitions between the two output states should happen *instantaneously* following any change of the sign of $x(t)$, also illustrated in Fig. 2(a).

Let us focus on voltage comparators. Ideal voltage comparators have the following features:

- infinitely large voltage *gain* [equivalently, infinitely small transition region between the output states, or the capability of detecting infinitely small values of $x(t)$]
- zero input *offset* voltage (meaning that the transitions occurs at $x = 0$)
- zero *delay* (meaning that changes in the sign of the analog input voltage $x(t)$ are transmitted instantaneously to the output)
- infinitely large variation range for the *common-mode* input voltage (meaning that the operation should depend only on the input voltage difference, not on the value of the positive and negative components despite how small or large these components are)
- infinitely large input *impedance* and unlimited driving capability at the output node

Correspondingly, ideal current comparators must have infinitely large *transimpedance* gain, zero input offset current, zero delay, infinitely large range for the common-mode input current, zero input impedance, and unlimited driving capability at the output node.

There is no practical voltage or current comparator circuit capable of realizing all of these ideal features. Actual com-

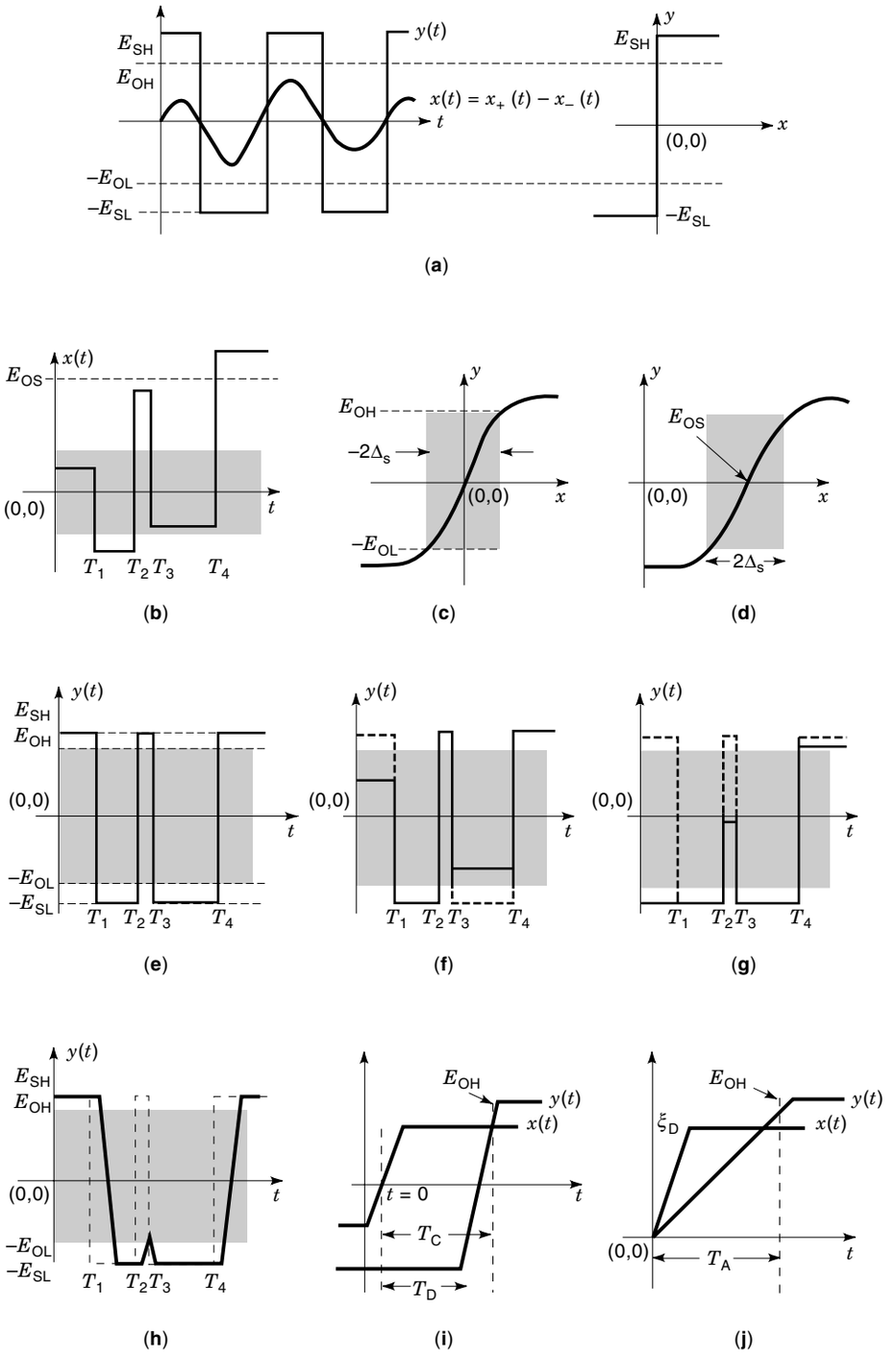

Figure 2. (a) Ideal comparator operation. (b)–(j) Illustrating static and dynamic errors in the comparator response.

parator behavior deviates from the ideal comparator illustrated in Fig. 2(a). Depending on how large the deviations are, comparator circuits may qualify for some applications and not for others. Thus, comparator users should quantify the maximum allowed deviations through a proper set of *specification* parameters, and comparator designers should try to fulfill these specifications when implementing a comparator circuit.

Nonideal Comparator Behavior and Comparator Specification

Consider the input waveform shown in Fig. 2(b) whose sign changes at the time instants T_1, T_2, T_3, and T_4. Figure 2(e) shows the corresponding ideal output waveform. On the other hand, Figs. 2(f)–(h) show erroneous waveforms. To understand the causes and meaning of these errors, first let us assume that the instantaneous transient response feature is retained. Then the error sources are comparator *finite gain* and

offset. First consider the effect of finite gain. It results in the transfer characteristic of Fig. 2(c), whose transition region (shaded in the figure) is not abrupt. Because the input values inside this transition region are not large enough to drive the output voltage to a logical state, their sign is not correctly coded, as Fig. 2(f) shows. For simplicity, it has been assumed that this transition region is symmetrical around the origin (equivalently, the central piece of the transfer characteristic is linear and $E_{OH} = E_{OL}$). However, in the more general case, this symmetry constraint should be removed for proper analysis.

Now consider the added influence of input offset voltage. Figure 2(d) shows the transfer characteristics where the zero crossing is shifted to E_{OS}. Consequently, sign codification is incorrect for all positive levels smaller than $E_{OS} + \Delta_S$, as illustrated in Fig. 2(g). Now assume that the gain is infinite and the input offset is zero. Then errors may appear because the intrinsic transient comparator response. Because the comparator takes a finite time to react to the input changes, the comparator output may be unable to follow the fastest input transitions, as illustrated in Fig. 2(h) for the input change at T_2.

The errors due to nonideal comparator behavior can be anticipated through proper specification of the comparator *resolution* and *transient response* (6). Resolution of the comparator under static excitation is characterized by the following specification parameters,

- Δ_S (*incremental static sensitivity*) defined as the input increase (decrease) needed to drive the output voltage to E_{OH} ($-E_{OL}$) from the central point of the transfer characteristics. This is closely related to the *static gain* $k_S \approx (E_{OH} + E_{OL})/(2\Delta_S)$. The larger this gain, the smaller Δ_S, and hence the more sensitive the comparator. Rigorously speaking and because $E_{OH} \neq E_{OL}$, two different incremental sensitivities should be defined, one for positive excursions Δ_{S+} and other for negative excursions Δ_{S-}. However, for simplicity both are considered equal.
- E_{OS} (*input offset*) defined as the input level required to set the output voltage at the central point of the transfer characteristics.

From these parameters, the comparator *static resolution* is calculated as

$$\xi_S = |E_{OS}| + \Delta_S \tag{2}$$

where the modulus is used because the offset is essentially a random variable. For any input level inside the interval $[-\xi_S, \xi_S]$ the comparator digital output state is uncertain. On the other hand, any input level outside this interval is called an *overdrive.* The overdrive variable measures how far from this interval the actual input is: $|x_{ovd}| = |x| - \xi_S$.

Parameters used to characterize the comparator transient operation include the following:

- T_D (*delay time*) defined as the time required for the comparator output voltage to emerge from a saturated state, either at E_{SH} or at $-E_{SL}$, and to start evolving to the other after a falling/rising input edge among two overdrive levels [see Fig. 2(i)]. A closely related figure is the T_C (*response, or comparison time*), which measures the time interval between the falling/rising input edge and the instant where the output reaches the corresponding restoring logic level [see Fig. 2(i)]. For completeness, the rise T_R and fall T_F times might also be considered. As is conventional in digital circuits, they are defined as the time between 10% and 90% of the total output swing.
- T_A (*amplification time*) defined as the time needed for the output to reach a restoring logic level, starting from steady state at the central point of the characteristics and following the application of an overdrive with amplitude $\xi_D = |E_{OS}| + \Delta_D$ [see Fig. 2(j)]. Generally this time differs for positive and negative excursions. For simplicity we assume full symmetry and calculate T_A from the following expression:

$$E_{OH} = y(t)|_{t=T_A} = \frac{y(t)|_{t=T_A}}{\Delta_D}\,\Delta_D \equiv k_D \Delta_D \tag{3}$$

It shows that the output value at $t = T_A$ is obtained by multiplying the incremental input Δ_D by a number k_D that represents the equivalent *dynamic gain* featured after a time T_A. On the other hand, parameter Δ_D defines the *incremental dynamic sensitivity,* and ξ_D defines the *dynamic resolution,* both functions of T_A. When the output waveform is monotonic and bounded and assuming $\Delta_D = \Delta_S$, Eq. (3) shows that $k_D < k_S$ $\forall T_A$ finite, and that $k_D \to k_S$, for $T_A \to \infty$. It means that the dynamic resolution parameter ξ_D is larger than the static one, that is ξ_D poses a stronger constraint on resolution than ξ_S. On the other hand, Eq. (3) highlights a tradeoff between resolution and speed, that is, the smaller T_A, the smaller the dynamic gain, and hence, the less sensitive the comparator.

Because discrete-time comparators are driven to their central point during the reset phase, the amplification time is particularly pertinent for them. It is complemented with the *reset time* T_R, defined as the time needed for the output to evolve from a logic state to reach the steady state at the central point.

Commonly, timing parameters for falling edges differ from those for rising edges. To distinguish between rise and fall parameters, an additional subscript, "r" for rising and "f" for falling, is used with T_D, T_C, T_A, and T_R. Thus, T_{Ar} denotes the amplification time for a rising edge. On the other hand, because the output waveform depends on the input signal level, this level should be indicated when specifying delay, comparison, and amplification times.

ONE-STEP VOLTAGE COMPARATORS

Concept and Circuits

Equation (1) and the transfer characteristics of Figs. 2(a), (c), and (d) show that the voltage comparator function consists of amplifying a voltage difference while it is transmitted from input to output. There are several circuit architectures for achieving this. Each one features different properties for static and dynamic behavior. Figure 3(a) shows the symbol, and Fig. 3(b) shows a first-order behavioral model for the simplest architecture. Such a model is representative of a wide

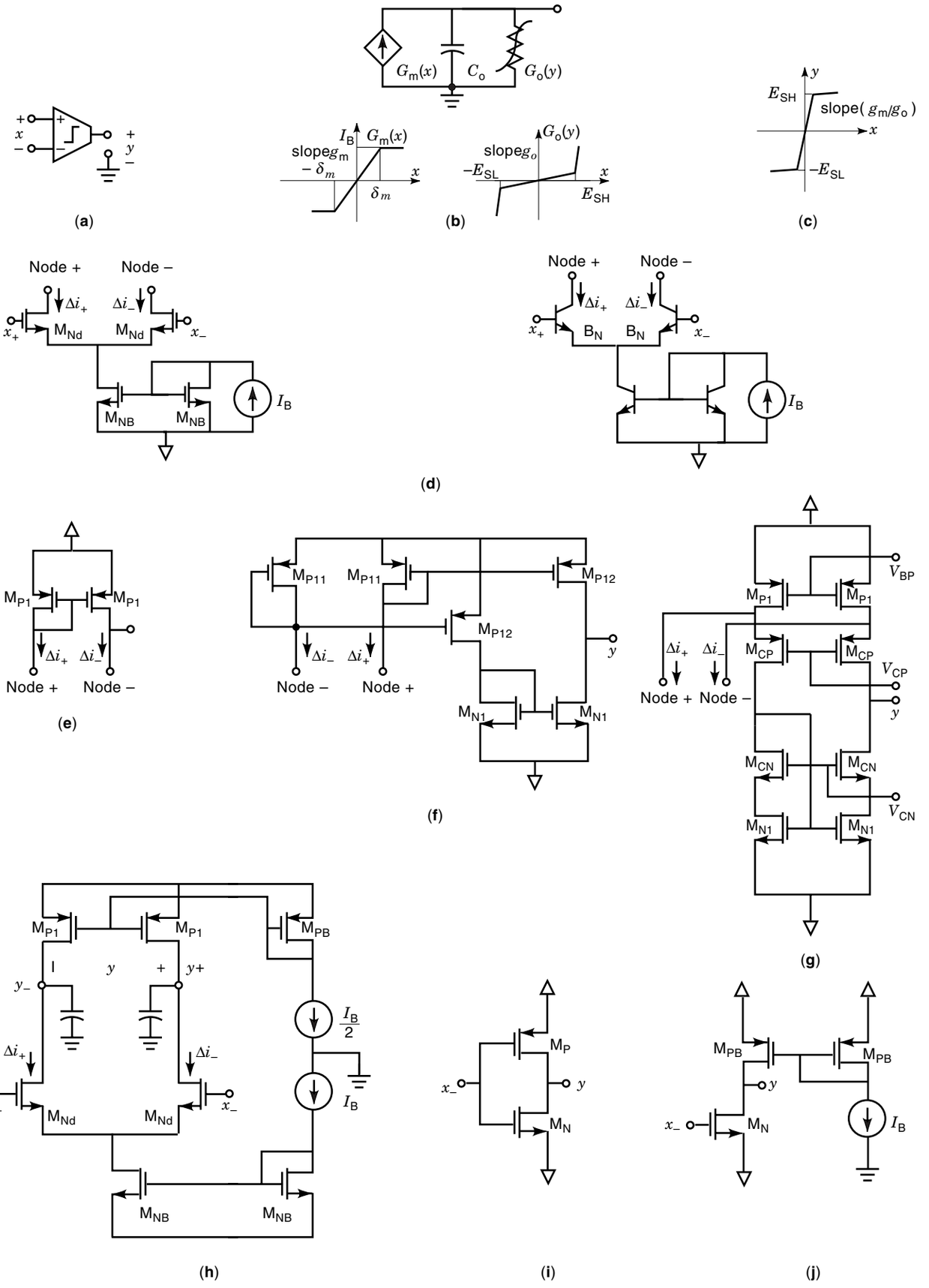

Figure 3. One-step voltage comparators.

Table 1. Model Parameters of One-Step CMOS Comparator Structures

Param. → / Structure ↓	g_m	δ_m	g_o	C_o
AOTAC			$\frac{I_B}{2}\left(\frac{1}{V_{ANd}}+\frac{1}{V_{APl}}\right)$	$C_L + n_{Nd}W_{Nd}C_{GD0Nd} + n_{Pl}W_{Pl}C_{GD0Pl}$
SOTAC			$\frac{I_B}{2}\left(\frac{1}{V_{ANl}}+\frac{1}{V_{APl2}}\right)$	$C_L + n_{Nl}W_{Nl}C_{GD0Nl} + n_{Pl2}W_{Pl2}C_{GD0Pl2}$
FOTAC	$\sqrt{2\frac{\beta_{0Nd}}{n_{Nd}}\left(\frac{W}{L}\right)_{Nd}I_B}$	$\sqrt{\frac{n_{Nd}I_B}{2\beta_{0Nd}\left(\frac{W}{L}\right)_{Nd}}}$	$\frac{1}{4V_{ANl}V_{ACN}}\sqrt{2\frac{\beta_{0CN}}{n_{CN}}\left(\frac{W}{L}\right)_{CN}I_B^3} + \frac{1}{V_{APl}V_{ACP}}\sqrt{2\frac{\beta_{0CP}}{n_{CP}}\left(\frac{W}{L}\right)_{CP}I_B^3}$	$C_L + n_{CN}W_{CN}C_{GD0CN} + n_{CP}W_{CP}C_{GD0CP}$
FDPC			$\frac{I_B}{2}\left(\frac{1}{V_{ANd}}+\frac{1}{V_{APl}}\right)$	$C_L + n_{Nd}W_{Nd}C_{GD0Nd} + n_{Pl}W_{Pl}C_{GD0Pl}$
CInvC	$2\sqrt{\frac{\beta_{0N}}{n_N}\left(\frac{W}{L}\right)_N I_Q} + 2\sqrt{\frac{\beta_{0P}}{n_P}\left(\frac{W}{L}\right)_P I_Q}$	Not applicable	$I_Q\left(\frac{1}{V_{AN}}+\frac{1}{V_{AP}}\right)$	$C_L + n_NW_NC_{GD0N} + n_PW_PC_{GD0P}$
InvC	$2\sqrt{\frac{\beta_{0N}}{n_N}\left(\frac{W}{L}\right)_N I_B}$		$I_B\left(\frac{1}{V_{AN}}+\frac{1}{V_{APB}}\right)$	$C_L + n_NW_NC_{GD0N} + n_{PB}W_{PB}C_{GD0PB}$

catalog of circuit implementations, using either BJTs or MOSTs.

The model of Fig. 3(b) consists of connecting a transconductor and a resistor, plus a capacitor to represent the unavoidable parasitic dynamics, and obtains the voltage gain in a single step, as the product of transconductance g_m and resistance $r_o = g_o^{-1}$, so that $k_S = g_m r_o = g_m/g_o$. It is shown at the transfer characteristic of Fig. 3(c) where it has been assumed that $|\delta_m(g_m/g_o)| \gg (E_{SH}, E_{SL})$ which is fulfilled by all well-behaved practical circuits.

The transconductor of Fig. 3(b) is commonly realized in practice through a differential pair [Fig. 3(d)] shows realizations using MOSTs and BJTs, respectively) (7). With small variations of the differential input voltage $x = x_+ - x_-$ around the quiescent point (defined by $x_+ = x_- = 0$), these pairs produce incremental currents $\Delta i_+ = -\Delta i_- = g_m(x/2)$. On the other hand, large values of x produce saturated transconductor characteristics similar to those in Fig. 3(b). The resistor of Fig. 3(b) is commonly built by using an active-load transistor-based configuration. Figures 3(e)–(g) show three CMOS alternatives (7). By connecting each of these active loads to the CMOS differential pair of Fig. 3(d), three one-step CMOS comparator structures are obtained, called, respectively, AOTAC [Fig. 3(e)], SOTAC [Fig. 3(f)] and FOTAC [Fig. 3(g)]. For purposes of illustration, the first three rows in Table 1 includes expressions for the pertinent model parameters of these one-step comparators as functions of the transistor sizes, the large-signal MOST transconductance density β_0, and the zero-bias threshold voltage V_{T0} (see Appendix I for a simplified MOST model).

Some practical one-step comparators provide a differential output voltage given as the difference between the voltages at the output terminals of symmetrically loaded differential pairs. In such cases the differential-pair bias current (henceforth called tail current) must be controlled through feedback circuitry to stabilize and set the quiescent value of the common-mode output voltage (8). Figure 3(h), where the common-mode regulation circuitry has not been included, shows a CMOS circuit realization called FDPC. The fourth row in Table 1 shows the corresponding model parameter expressions.

In some applications it is also possible to use logic inverters as one-step comparators. Figures 3(i) and (j) show two CMOS examples (9), called CInvC and InvC, respectively. The fifth and sixth rows in Table 1 contain their corresponding model parameter expressions. These structures have only the negative input x_- accessible, whereas the positive input x_+ is set to an internal reference given approximately by

$$x_+ \equiv E \approx \frac{\sqrt{\frac{\beta_P}{n_P}}(V_{DD} - |V_{T0P}|) + \sqrt{\frac{\beta_N}{n_N}}(V_{SS} + V_{T0N})}{\sqrt{\frac{\beta_P}{n_P}} + \sqrt{\frac{\beta_N}{n_N}}} \quad \text{for CInvC}$$

$$x_+ \equiv E \approx V_{SS} + V_{T0N} + \sqrt{\frac{n_N I_B}{\beta_N}} \quad \text{for InvC} \tag{4}$$

This feature constrains the usefulness of these circuits as isolated comparators. They are used mostly as components of multistage comparator architectures.

Static and Dynamic Gain in One-Step Comparators

The static resolution of the one-step comparator is given by

$$\xi_S \approx |E_{OS}| + \frac{E_{OH}}{k_S} = |E_{OS}| + E_{OH}\frac{g_o}{g_m} \tag{5}$$

Hence, it is limited by the input offset voltage and by the amount of voltage gain which can be realistically built into a single step. It depends on technology, circuit structure, and transistor sizes. The FOTAC can obtain up to around 10^5, whereas the others obtain smaller gain values. For such medium-to-large gain values, say $k_S > 10^3$, the static resolution is basically constrained by the offset voltage, whereas the constraint imposed by the gain dominates for lower values of k_S.

Now let us consider the dynamic resolution. Assume that the capacitor in the model of Fig. 3(b) is discharged at $t = 0$ and consider a unit-step excitation of amplitude Δ_D, such that Δ_D is in the linear transconductor region. The output waveform is given by

$$y(t) = \Delta_D \frac{g_m}{g_o}\left(1 - e^{-\frac{t}{\tau_o}}\right) \qquad \text{, where } \tau_o \equiv \frac{C_o}{g_o} \tag{6}$$

Δ_D must be larger than Δ_S for monotonic comparator responses. Here it is assumed that $\Delta_D \gg \Delta_S$, so that $\Delta_D(g_m/g_o) \gg E_{OH}$. This means that the output reaches the restoring level E_{OH} in a small fraction of τ_o and, hence, Eq. (6) can be series-expanded and approximated to obtain the following expressions for the output waveform and the amplification time:

$$y(t) \simeq \Delta_D \frac{g_m}{g_o}\frac{t}{\tau_o}\bigg|_{t \le T_A} \equiv \Delta_D \frac{t}{\tau_u}\bigg|_{t \le T_A} \tag{7}$$

where $\tau_u \equiv C_o/g_m$ is the *unitary time constant* of the amplifier. From here and Eq. (3), the amplification time and dynamic resolution, respectively, are given by

$$T_A = \tau_u \frac{E_{OH}}{\Delta_D}$$

and

$$\xi_D = |E_{OS}| + \frac{E_{OH}}{k_D} \approx |E_{OS}| + E_{OH}\frac{\tau_u}{T_A} \tag{8}$$

which highlights a *tradeoff* between *resolution and speed:*

$$\Delta_D\left(\frac{T_A}{\tau_u}\right) \approx E_{OH} \tag{9}$$

The curve labeled $N = 1$ in Fig. 6(a) illustrates this tradeoff for a typical $E_{OH} = 1$ V. Because practical applications require $\Delta_D \ll E_{OH}$, this curve and Eq. (8) show that $T_A \gg \tau_u$, meaning that the comparator is much slower than the underlying voltage amplifier.

As Δ_D decreases, Eq. (9) shows that T_A increases at the same rate. On the other hand, the comparator becomes increasingly slower as the input approaches the static resolution limit, that is, as $\Delta_D \to \Delta_S = E_{OH}/k_S$. Because then it is not possible to assume $T_A \ll \tau_0$, Eq. (6) cannot be approximated, and the resolution for speed tradeoff is given by

$$\Delta_D\left(\frac{T_A}{\tau_u}\right) = E_{OH}\left[\left(\frac{k_S\Delta_D}{E_{OH}}\right)\ln\frac{1}{1 - \frac{1}{k_S}\frac{E_{OH}}{\Delta_D}}\right] \tag{10}$$

Consider $\Delta_D \approx \Delta_S(1 + \epsilon)$ with $\epsilon \ll 1$. Equation (10) can be simplified to obtain a relationship between the static gain and the amplification time needed to obtain such limiting sensitivity;

$$\left(\frac{T_A}{\tau_u}\right) = A_0 \ln\left(\frac{1}{\epsilon}\right) \tag{11}$$

where for homogeneity with subsequent discussions, the static gain has been renamed as A_0. In the limit, as $\Delta_D \to \Delta_S$ and $\epsilon \to 0$, $T_A \to \infty$.

The time-transient performance of one-step comparators is illustrated through a typical example with $k_S = 2 \times 10^3$, $\tau_u = 10$ ns and $E_{OH} = 1$ V, such that $\Delta_D \times T_A \approx 10^{-8}$ Vs. Thus, $\Delta_D = 10$ mV requires from Eq. (9), that $T_A \approx 1$ μs, and $\Delta_D = 1$ mV requires from Eq. (10) that $T_A \approx 14$ μs. On the other hand, if the static resolution limit has to be approached within 1%, Eq. (11) yields $T_A \approx 92$ μs.

Overdrive Recovery and Comparison Time in One-Step Comparators

In CT applications, where comparators are not reset prior to applying the input, characterization of the comparator transient requires calculating the delay and comparison times. For the purpose consider that the output is saturated because of an overdrive and that an opposite overdrive of amplitude Δ_D is applied at $t = 0$. Let us assume that $y(0) = -E_{SL}$. The model of Fig. 3(b) gives zero delay time T_D and the following comparison time:

$$\frac{T_C}{\tau_u} = k_S \ln\frac{\left(1 + \frac{1}{k_S}\frac{E_{SL}}{\Delta_D}\right)}{1 - \frac{1}{k_S}\frac{E_{OH}}{\Delta_D}} \tag{12}$$

For $k_S\Delta_D \gg E_{OH}$ and E_{SL} and assuming $E_{OH} \approx E_{SL}$, this equation implies a resolution for speed tradeoff similar to that in Eq. (9): $\Delta_D \times (T_C/\tau_u) \approx 2E_{OH}$. On the other hand, in the worst case when the comparator is used close to the static resolution limit so that $\Delta_D \approx \Delta_S(1 + \epsilon)$ with $\epsilon \ll 1$, Eq. (12) can be simplified to give the following fundamental relationship between static gain A_0 and the comparison time required to attain such limiting sensitivity:

$$\left(\frac{T_C}{\tau_u}\right) = A_0 \ln\left(\frac{2}{\epsilon}\right) \tag{13}$$

Assuming that $A_0 = 2 \times 10^3$ and $\tau_u = 10$ ns, $T_C \approx 106$ μs is needed to approach the resolution limit within 1%, slightly larger than $T_A \approx 92$ μs obtained from Eq. (11).

OFFSET CANCELLATION IN ONE-STEP COMPARATORS

The Offset Problem

As already mentioned, the input offset voltage E_{OS} poses an important constraint on one-step comparator performance. This nonideal feature reflects a lack of symmetry and has two different components. *Deterministic offset* is caused by asymmetries of the comparator circuit structure itself. For instance, the FDPC structure of Fig. 3(h) is symmetrical, whereas the AOTAC structure formed by connecting the MOS differential pair of Fig. 3(d) and the active load of Fig. 3(e) is asymmetric. Consequently, the output voltage at the quiescent point Y_Q is typically nonnull, thus making $E_{OS} = Y_Q/k_S$. However, because Y_Q, in the worst case, is of the same order of magnitude as E_{OH}, the deterministic offset component places a similar constraint on comparator resolution as on the static gain, not significant enough to justify further consideration. On the other hand, *random offset* contemplates asymmetries caused by random fluctuations of the transistor technological parameters and is observed in asymmetrical and in symmetrical structures. These fluctuations mismatch nominally identical transistors. The amount of mismatch is inversely proportional to the device area and distance between them. Particularly, it has been observed that the threshold voltage and the large-signal transconductance density of MOSTs fluctuate with standard deviations given by (10),

$$\sigma^2(\Delta V_{T0}) \approx \frac{\alpha_{V_{T0}}^2}{WL}$$

and

$$\sigma^2\left(\frac{\Delta\beta_0}{\beta_0}\right) \approx \frac{\alpha_{\beta_0}^2}{WL} \tag{14}$$

where W and L are the channel width and length, respectively, $\alpha_{V_{T0}}^2$ and $\alpha_{\beta_0}^2$ are technological constants, and $\Delta\beta_0/\beta_0$ denotes percentage variations. There is at least one additional term due to the separation between transistors, but this can be attenuated through proper layout. On the other hand, typical characterization values for the parameters of Eq. (4) in a 0.5 μm technology are $\alpha_{V_{T0}}^2 \approx 10^{-5}$ V$^2\mu$m^2 and $\alpha_{\beta_0}^2 \approx 10^{-4}$ μm^2. In the case of the MOST differential pair of Fig. 3(d), random mismatches between the two transistors labelled M_{N1} render their currents different for $x_+ = x_-$, and a voltage difference given by

$$\begin{aligned} E_{OS}|_{DP} &\approx \Delta V_{T0Nd} + \sqrt{\frac{I_B}{8\beta_{Nd}}}\left(\frac{\Delta\beta_0}{\beta_0}\right)_{Nd} \\ &= \Delta V_{T0Nd} + \frac{I_B}{2}\frac{1}{g_m}\left(\frac{\Delta\beta_0}{\beta_0}\right)_{Nd} \end{aligned} \tag{15}$$

has to be applied to equalize these currents. Another voltage difference $E_{OS}|_{AL}$ has to be added to this to compensate for the asymmetries in the active-load circuitry. In the case of the AOTAC and the FDPC structures, this latter input offset component is calculated as

$$\begin{aligned} E_{OS}|_{AL} &\approx \Delta V_{T0Pl}\sqrt{\frac{\beta_{Pl}}{\beta_{Nd}}} + \sqrt{\frac{I_B}{8\beta_{Nd}}}\left(\frac{\Delta\beta_0}{\beta_0}\right)_{Pl} \\ &= \Delta V_{T0Pl}\sqrt{\frac{\beta_{Pl}}{\beta_{Nd}}} + \frac{I_B}{2}\frac{1}{g_m}\left(\frac{\Delta\beta_0}{\beta_0}\right)_{Pl} \end{aligned} \tag{16}$$

to obtain $|E_{OS}| = |E_{OS}|_{DP} + |E_{OS}|_{AL}$.

Equations (14), (15), and (16) suggest that E_{OS} can be reduced through proper transistor sizing. However, these techniques hardly obtain offsets less than a few millivolts, not low enough for many practical applications. This drawback is overcome by adding offset-cancellation circuitry, by which residual offset values as small as 0.1 mV are obtained (11). There are three basic approaches for offset cancellation; component trimming; control through an auxiliary nulling port; and dynamic correction.

Component trimming commonly refers to modifications of some critical component geometries, for instance, through laser or electron beam cutting, to compensate for the asymmetries and thus minimize offset. Because such trimming is applied only once during the circuit life right after circuit production, the adjustment must be stable to temperature and circuit aging. Recently, techniques for nondestructive trimming have been proposed that exploit the long-term analog storage capabilities of floating-gate MOSTs (12,13).

Another common offset cancellation technique uses additional components controlled through a nulling port. Figure 4(a) illustrates this technique for the SOTAC comparator. Note that a differential pair controlled by the voltages z_{os+} and z_{os-} has been added to the uncompensated structure (drawn with solid black lines). Mismatch-induced current unbalances are compensated for by setting these control voltages and the transconductance of the additional differential pair such that

$$g_{mos}(z_{os+} - z_{os-} - E_{OS}^{os}) = E_{OS}g_m \tag{17}$$

where E_{OS}^{os} is the offset voltage of the offset-nulling differential pair. For increased robustness under environmental changes, the control voltages are generated through a control feedback loop that monitors E_{OS} and updates the control voltages until this error is annulled. Figure 4(b) shows a conceptual block diagram for this technique which implies two different operating modes. During the *calibration mode,* switches labeled S_{cal} are ON and those labeled S_{com} are OFF. Thus the nulling control voltage is generated by the control loop and stored in memory. Then, during the *comparison mode* the circuit features the comparator operation with reduced offset. Alternative implementations of the control loop reported in technical literature use either fully analog control loops or mixed analog/digital control loops and feature offset voltages between 40 μV and 120 μV over a 120°C temperature range (11,14,15). Although this offset cancellation technique involves synchronization, careful design may enlarge the time interval between calibration events to enable quasi-continuous-time operation.

Self-adjusting comparators are not easy to design and are area-intensive. Thus they are especially suitable for large cir-

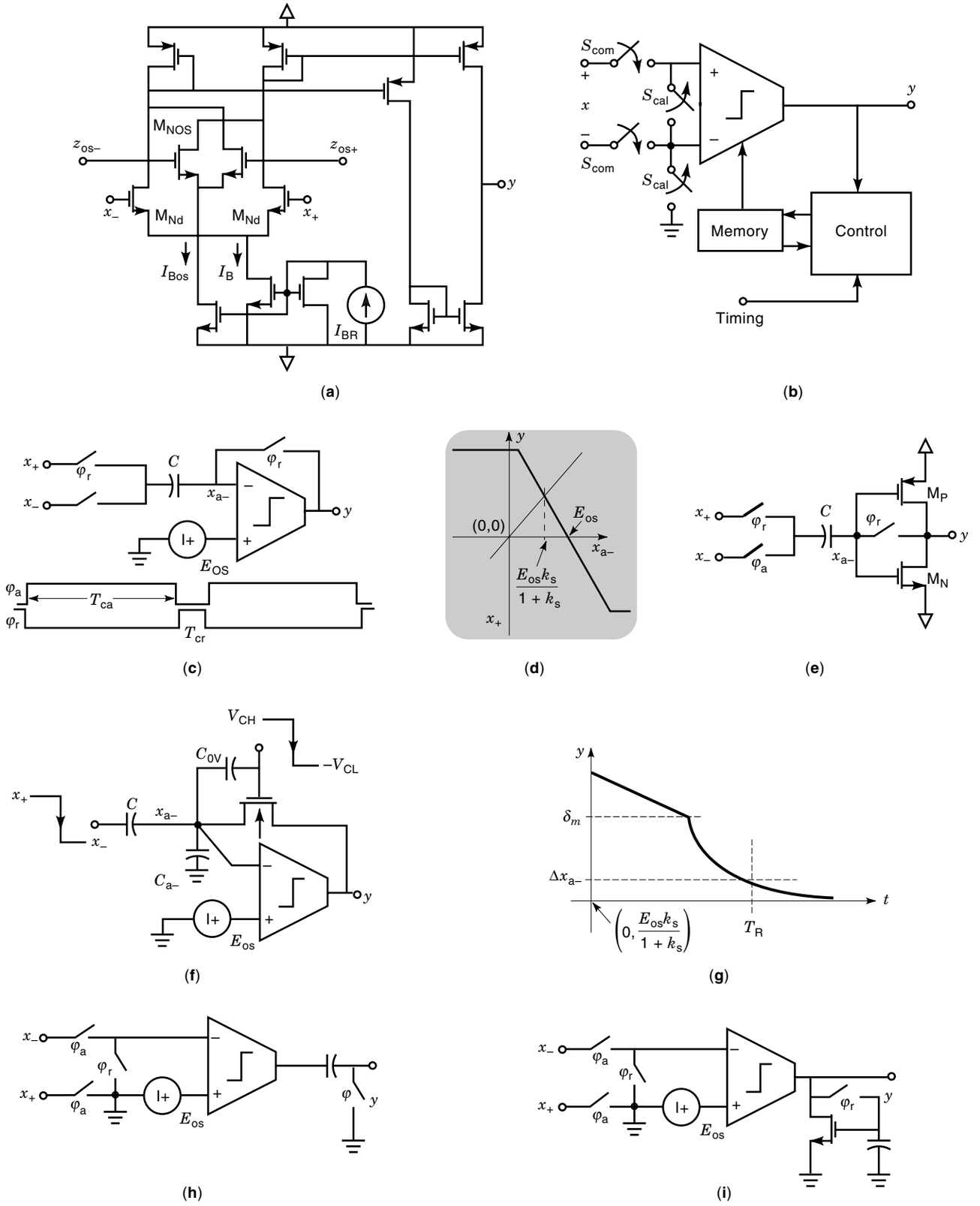

Figure 4. Offset cancellation in one-step voltage comparators.

cuits where the correction circuitry is shared by many comparators.

Offset Compensation Using Dynamic Techniques

The Self-Biased Comparator Circuit. A simple, yet efficient correction technique uses dynamic self-biasing to extract the offset and offset storage to annul their influence (16,17). Figure 4(c) shows the corresponding circuit, consisting of an uncompensated comparator (its offset has been represented through a separate voltage source for enhanced clarity) plus three clocked analog switches and a capacitor. The circuit requires two *nonoverlapping* clocks, as indicated in the figure.

While φ_r is at the high-state and correspondingly φ_a is at the low-state, switches controlled by the latter clock are ON, and the others are OFF. Thus, the amplifier is shorted, and hence its output voltage evolves toward a steady state $x_{a-}|_r = E_{OS}(1 + k_S^{-1})^{-1}$ defined by the intersection of the amplifier transfer characteristics and the bisecting line, as represented in Fig. 4(d). Providing that the *reset* interval is long enough for the transient to vanish, capacitor C is charged at a voltage $v_{Cr} = x_+ - x_{a-}|_r$. Note that for $k_S \gg 1$, $x_{a-}|_r \approx E_{OS}$. Hence, during the reset phase the negative plate of the capacitor samples a voltage very close to the offset.

During the subsequent *active* time interval, φ_r goes low, φ_a goes high, and C keeps its charge because the current flow is blocked. Thus, the comparator input $x_a \equiv x_{a+} - x_{a-}$ evolves to a steady state $x_a = E_{OS} - (x_- - v_{Cr}) = E_{OS} - x_{a-}|_r + (x_+ - x_-)$ where the offset is substracted from its previous sample. The following static resolution expression results:

$$\xi_S \approx \frac{|E_{OS}|}{1+k_S} + \frac{E_{OH}}{k_S} = \frac{|E_{OS}|}{1+g_m/g_o} + E_{OH}\frac{g_o}{g_m} \tag{18}$$

which shows that the offset error is smaller by a factor $1 + k_S$ than for uncompensated comparators, see Eq. (5).

This procedure of dynamically sampling the "central" point of an inverting transfer characteristic during reset intervals and substracting it from the input during active intervals can also be applied to single-ended amplifiers. Figure 4(e) shows the CInvC circuit which yields

$$y \approx k_S\left(x_+ - x_- + \frac{E}{1+k_S}\right) \tag{19}$$

where E is the intrinsic reference voltage of the single-ended amplifier, given by Eq. (4). Although the underlying amplifier is single-ended, dynamic biasing renders it capable of handing a differential input which may be of interest for practical applications.

Residual Offset and Gain Degradation in Self-Biased Comparators. There are several second-order phenomena that modify the voltage stored at node x_{a-} and consequently degrade the static resolution of self-biased comparators. The most important among them take place during the ON → OFF transition of the reset feedback switch, namely feedthrough of the clock signal that controls this switch and injection of its channel charge. They make the voltage stored at note x_{a-} exhibit a step during this transition so that its value in the active phase differs from that stored during the reset phase, that is, $x_{a-}|_a \approx x_{a-}|_r - \Delta x_{a-}$. During the active phase this value also continues degrading due to leakage current. Figure 4(f) is a simplified model for evaluating all of these degradations. In addition to the nominal capacitor C this model includes a parasitic capacitor between node x_{a-} and ground and another parasitic capacitor between node x_{a-} and the feedback switch control. Analysis using this model provides the following expression for static resolution:

$$\begin{aligned}\xi_S &\approx |V_{CH} + V_{CL}|\frac{C_{ov}}{C} + \frac{|q_{ch}|}{C} + \frac{|I_{leak}|}{C}t + \frac{|E_{OS}|}{1+k_S} + \frac{E_{OH}}{\alpha_C k_S} \\ &\equiv |E_{OSd}| + \frac{|E_{OS}|}{1+k_S} + \frac{E_{OH}}{\alpha_C k_S}\end{aligned} \tag{20}$$

where $\alpha_C = C/(C + C_{ov} + C_{a-})$, q_{ch} is the charge built in the switch channel while it is ON during the reset phase, and t is measured from the instant when the ON → OFF transition happens. This expression shows the residual offset $|E_{OSd}|$ that is not attenuated by comparator gain. If capacitance C is chosen very small, this offset may become larger than the original offset. Small values of this capacitance also may result in small values of α_C, thus increasing the incremental sensitivity [last term in Eq. (20)], and hence producing additional resolution degradation.

Transient Behavior and Dynamic Resolution in Self-Biased Comparators. The calculations for amplification time apply to the active phase of self-biased comparators and show the resolution for speed tradeoff in Eq. (10) already discussed. On the other hand, the transients during the reset phase arise from another tradeoff related to the onset of an additional residual offset component. The dynamic behavior within the reset phase can be calculated using the model of Fig. 3(b). Two different transients are observed. First of all there is a very fast charge redistribution transient, dominated by the ON resistances of the switches. The output value $y(0)$ at the end of this transient, in the worst case, is equal to one of the saturation levels. Let us assume that $y(0) = E_{OH}$. From this value, the output evolves toward the steady state at $E_{OS}(1 + k_S^{-1})^{-1}$ through a second transient which is dominated by comparator dynamics. Figure 4(g) provides a global view of this second transient. It consists of a nonlinear part, where the transconductor is in the saturation region and y evolves from $y(0)$ to δ_m with a fixed slew-rate δ_m/τ_u, followed by a linear segment where the evolution is realized with time constant $\tau_{ur} = (C + C_{a-} + C_o)/(g_m + g_o) \approx C/g_m \equiv \tau_u$. Thus, the *reset time* needed to reach a final value larger than the steady state by Δx_{a-} is given by

$$T_R \approx \frac{E_{OH} - \delta_m}{\delta_m}\tau_u + \tau_u \ln\left(\frac{\delta_m}{\Delta x_{a-}}\right) \tag{21}$$

Δx_{a-} remains as a residual offset after cancellation. For the typical values of $k_S = 2 \times 10^3$, $\tau_u = 10$ ns, $E_{OH} = 1$ V and $\delta_m = 250$ mV, Eq. (21) yields $T_R \approx 8.5$ μs for a 1 mV residual offset. This time is smaller than the amplification time ($T_A \approx 14$ μs) required to obtain $\Delta_D = 1$ mV from Eq. (10).

Offset Cancellation Through Storage at the Output Node. Figure 4(c) employs offset storage at the comparator input node. Alternatively, offset can be compensated for by storing it at the output node. Such storage can be realized in either

the voltage or the current domain. Figures 4(h) and (i) show the corresponding circuits.

MULTISTEP VOLTAGE COMPARATORS

Static and Dynamic Gain

The resolution for speed tradeoff of one-step voltage comparators is improved by using a multistep architecture (18,19) similar to the strategy used to enhance the voltage gain of operational voltage amplifiers (20). Such a multistep architecture consists of the cascade connection of several one-step stages. These stages are different in the more general case. A structure typically found in practice is a differential one-step comparator at the front-end and single-ended inverters in the rest of the chain, as shown in Fig. 5(b) (21). However, for improved clarity in presenting the architectural principles, it will be assumed that the cascade is formed of N identical stages [see Fig. 5(a)], each having gain $k_S = g_m/g_o$ and time constant $\tau_o = C_o/g_o$. Hence the static resolution is given by

$$\xi_S \approx |E_{OS}| + E_{OH}\left(\frac{g_o}{g_m}\right)^N \tag{22}$$

where $|E_{OS}|$ is the offset of the front-end stage at the cascade. Equation (22) shows that for a large enough value of N, the static resolution becomes basically constrained by offset voltage, that is, the constraint due to static gain becomes negligible. Such a feature is specially important when the amplifiers are realized through inverters, such as InvC and CInvC, which have inherently low dc gain.

For the dynamic resolution, assume as for the one-step case that offsets are null, that all capacitors are discharged at $t = 0$, and that an input step of amplitude Δ_D is applied at this instant. The output voltage Laplace transform is given by

$$Y(s) = \left(\frac{k_S}{1 + s\tau_o}\right)^N \frac{\Delta_D}{s} \tag{23}$$

Assuming that $\Delta_D(g_m/g_o)^N \gg E_{OH}$, $T_A \ll \tau_o$, and hence Eq. (23) simplifies $Y(s) \simeq \Delta_D/(s^{N+1}\tau_u^N)$. From here the output waveform and T_A, respectively, are given by

$$y(t) \approx \frac{\Delta_D}{\tau_u^N}\frac{1}{N!}t^N$$

and

$$T_A \approx \tau_u\left(\frac{E_{OH}}{\Delta_D}N!\right)^{1/N} \tag{24}$$

and the expressions for the dynamic resolution and the resolution for speed trade-off are

$$\xi_D \approx |E_{OS}| + E_{OH}N!\left(\frac{\tau_u}{T_A}\right)^N$$

and

$$\Delta_D\left(\frac{T_A}{\tau_u}\right)^N \approx N!E_{OH} \tag{25}$$

As for the one-step comparator [see Eq. (9)], Eq. (25) yields $T_A > \tau_u$ for the practical case where $\Delta_D < E_{OH}$. However, because of the potential dependence on N, the multistep architecture yields smaller values of T_A for any Δ_D such that $\Delta_D < (E_{OH}/2)$. For instance, for $\tau_u = 10$ ns, $E_{OH} = 1$ V and $\Delta_D = 10$ mV, Eq. (24) yields $T_A \approx 141$ ns for $N = 2$, $T_A \approx 65$ ns for $N = 5$, and $T_A \approx 67$ ns for $N = 8$, smaller in all cases than for the one-step.

Figure 6(a) depicts T_A/τ_u as a function of Δ_D for different values of N and $E_{OH} = 1$ V. Figure 6(b) is an enlargement of the previous diagram. It shows that for each Δ_D there is an optimum value of N that minimizes T_A. For $\Delta_D > (10^{-3}\,E_{OH})$ this optimum number is given by (19),

$$N_{opt} \approx 1.1\ln\left(\frac{E_{OH}}{\Delta_D}\right) + 0.79 \tag{26}$$

For instance, for $\Delta_D \approx (10^{-2}\,E_{OH})$, maximum speed is achieved by using $N = 6$. Using either less or more stages in the cascade yields slower operation.

Offset Cancellation in Multistep Comparators

Dynamic self-biasing can also be applied to cancel the offset of multistage comparators. However, the high-order dynamics preclude direct feedback connection of the overall output node and the negative input. Unless compensation circuitry is used, such direct feedback connection leads to instabilities, similar to the problem found in two-stage op amps (7,20). Instabilities are avoided by making each stage store its own offset, as shown in Fig. 5(c). Thus, only residual offsets—see Eq. (20)—generated at the different stages remain. However, they are also attenuated through proper timing of the switches used for self-biasing. The inset of Fig. 5(c) shows this timing. Note that the stages are switched ON at different instants, each one after the previous. Consequently, the residual offset of each stage is stored at the input capacitor of the next stage while the latter remains grounded, and hence the output remains unaltered. In this way only the residual offset of the last stage $|E_{OSdN}|$ contributes to the output. Because this offset is amplified only by the last stage itself, whereas the signal is amplified by all of the stages, the following expression results for static resolution:

$$\xi_S \approx \frac{|E_{OSdN}|}{(\alpha_C k_S)^{N-1}} + \frac{E_{OH}}{(\alpha_C k_S)^N} \tag{27}$$

Overdrive Recovery and Delay Time in Multistep Voltage Comparators

Transient characterization of multistep comparators for CT applications requires calculating delay and comparison times. The worst case happens when the initial condition is such that all stages are saturated due to an input overdrive applied and held for some instant $t < 0$ and then an opposite overdrive of amplitude Δ_D very close to the static resolution limit is applied at $t = 0$. Assume, as for the calculation of comparison time in the one-step comparator, that $y(0) = -E_{SL}$. During the transient evolution toward the steady-state, $y(\infty) = k_S^N\Delta_D$, each stage remains saturated and hence latent, while its input is smaller than $-E_{SL}/k_S$. Figures 5(d) and 5(e) show the transient waveforms for comparators with two and three stages, respectively.

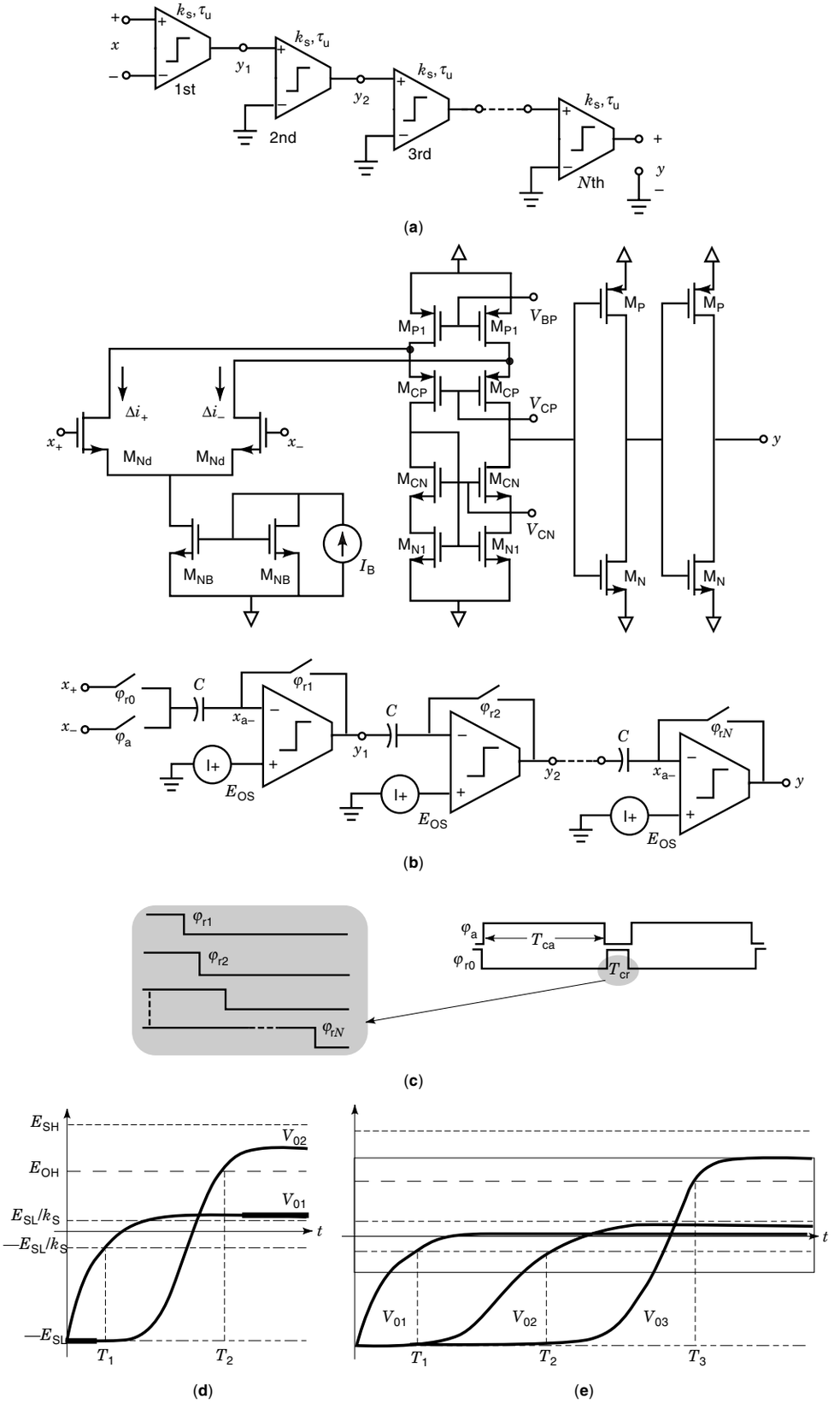

Figure 5. Multistep voltage comparators.

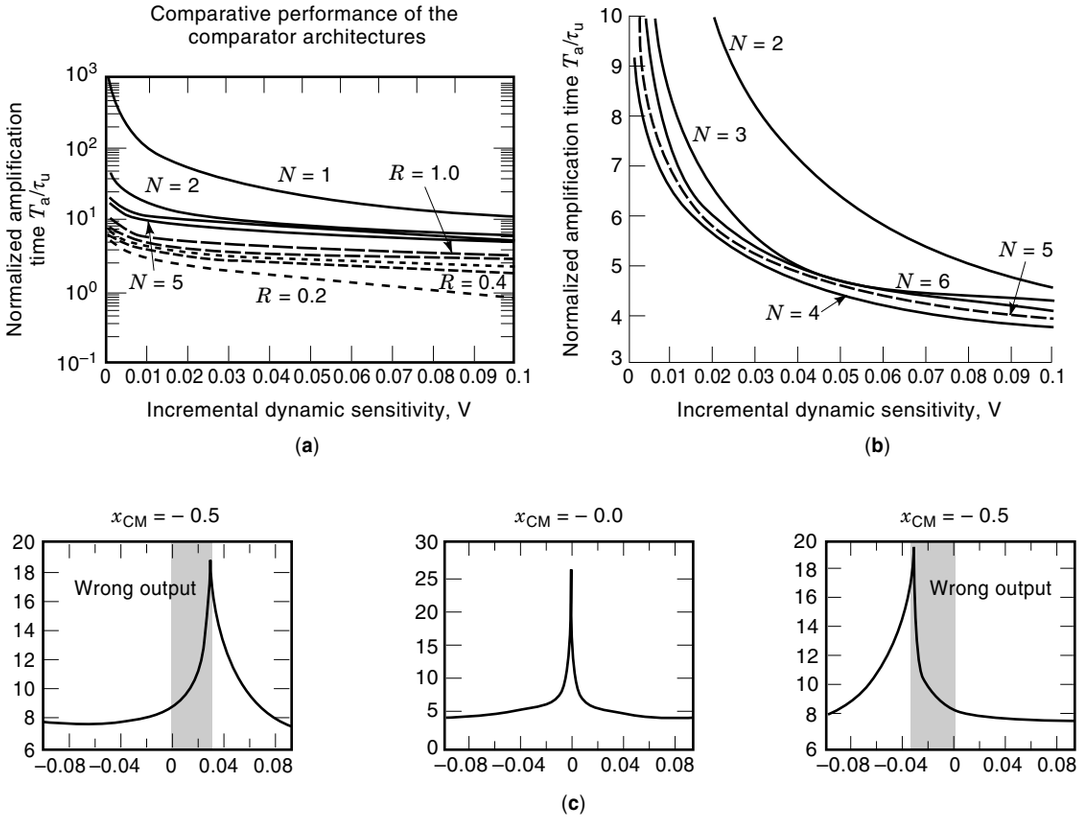

Figure 6. Illustrating the resolution-speed tradeoff for different voltage comparators.

Two-Stage Comparator. First consider the two-stage comparator whose waveforms are depicted in Fig. 5(d). The delay time is that invested by the first stage in delivering the voltage $-E_{SL}/k_S$. Because the transient at node y_1 is the first-order type, T_D is mathematically expressed similarly to Eq. (12):

$$\frac{T_D}{\tau_u} = k_S \ln \frac{1 + \dfrac{E_{SL}}{k_S \Delta_D}}{1 + \dfrac{E_{SL}}{k_S^2 \Delta_D}} \tag{28}$$

From $t = T_D$, the second stage starts contributing to the voltage gain thus giving

$$y(t) = k_S^2 \Delta_D - (E_{SL} + k_S^2 \Delta_D) \left(1 + \frac{1}{k_S} \frac{\zeta}{\tau_u}\right) e^{-\frac{1}{k_S} \frac{\zeta}{\tau_u}} \tag{29}$$

where $\zeta = t - T_D$. This equation is difficult to solve exactly. However, for our purposes it can be approximated by the first two terms of its power expansion:

$$y(t) \approx -E_{SL} + \frac{(E_{SL} + k_S^2 \Delta_D)}{2} \left(\frac{1}{k_S} \frac{\zeta}{\tau_u}\right)^2 \tag{30}$$

The comparison time is the instant at which $y(t) = E_{OH}$:

$$\frac{T_C}{\tau_u} \approx \frac{T_D}{\tau_u} + k_S \sqrt{2 \frac{\dfrac{E_{SL} + E_{OH}}{k_S^2 \Delta_D}}{1 + \dfrac{E_{SL}}{k_S^2 \Delta_D}}} \tag{31}$$

Because $\Delta_D \approx \Delta_S$ and taking into account Eqs. (2) and (22), $k_S^2 \Delta_D \approx E_{OH}$. Thus, by assuming that $E_{OH} \approx E_{SL}$,

$$\frac{T_D}{\tau_u} \approx k_S \ln \frac{k_S}{2}$$

and

$$\frac{T_C}{\tau_u} \approx \frac{T_D}{\tau_u} + k_S \sqrt{2} \approx k_S \left(\ln \frac{k_S}{2} + \sqrt{2}\right) \tag{32}$$

By comparing this T_C with an optimistic estimation of the corresponding value for one-step architecture and assuming the same overall static gain ($A_0 = k_S$ for one-step; $A_0 = k_S^2$ for two-step),

$$\frac{T_C|_{\text{two-step}}}{T_C|_{\text{one-step}}} = \frac{1}{2\sqrt{A_0}} \left[\sqrt{2} + \ln\left(\frac{\sqrt{A_0}}{2}\right)\right] < 1 \tag{33}$$

It shows that the possibility of distributing the gain between the two stages also gives faster operation in overdrive recovery.

Three-Stage Comparator. Now consider Fig. 5(e), corresponding to the three-stage comparator. The delay time now has two components. The first T_{D1} is given by Eq. (28). The second is the time needed for the second-stage output to reach $-E_{SL}/k_S$ and is calculated by using Eqs. (29) and (30):

$$\frac{T_D}{\tau_u} = \frac{T_{D1}}{\tau_u} + \frac{T_{D2}}{\tau_u} \approx k_S \left\{ \ln \frac{1 + \dfrac{E_{SL}}{k_S \Delta_D}}{1 + \dfrac{E_{SL}}{k_S^2 \Delta_D}} + \sqrt{2 \frac{\dfrac{E_{SL}}{k_S^2 \Delta_D} - \dfrac{E_{SL}}{k_S^3 \Delta_D}}{1 + \dfrac{E_{SL}}{k_S^2 \Delta_D}}} \right\} \tag{34}$$

From $t = T_D$ the third stage starts working so that after a power-series expansion,

$$\begin{aligned} y(t) &\approx -E_{SL} + \frac{(E_{SL} + k_S^3 \Delta_D)}{3!} \left(\frac{\zeta}{k_S \tau_u} \right)^3 \Rightarrow \frac{T_C}{\tau_u} \\ &\approx \frac{T_D}{\tau_u} + k_S \sqrt[3]{3! \frac{\dfrac{E_{SL} + E_{OH}}{k_S^3 \Delta_D}}{1 + \dfrac{E_{SL}}{k_S^3 \Delta_D}}} \end{aligned} \tag{35}$$

Under assumptions similar to those for two-stages, namely, $k_S^3 \Delta_D \approx E_{OH}$ and $E_{OH} \approx E_{SL}$, the following expression is obtained for the comparison time as a function of the overall gain $A_0 = k_S^3$:

$$\frac{T_C}{\tau_u} \approx k_S [\ln(k_S) + \sqrt{2} + \sqrt[3]{3!}] = \sqrt[3]{A_0} \left[\frac{\ln(A_0)}{3} + \sqrt{2} + \sqrt[3]{3!} \right] \tag{36}$$

This can be easily generalized to N stages:

$$\frac{T_C}{\tau_u} \approx \sqrt[N]{A_0} \left[\frac{\ln(A_0)}{N} + \sum_{m=2}^{N} \sqrt[m]{m!} \right] \tag{37}$$

It shows that for the same static gain, equivalently, the same static incremental sensitivity $\Delta_S = E_{OH}/A_0$, the comparison time decreases with the number of stages, even in overdrive recovery.

VOLTAGE COMPARATORS WITH POSITIVE FEEDBACK

Using Partial Positive Feedback to Enhance the Voltage Gain

Consider the conceptual circuit of Fig. 7(a). In addition to the conventional transconductor $G_m(x)$ controlled by input voltage, this circuit contains another $G_{mo}(y)$ controlled by output voltage. The former injects a current proportional to x into the output node, whereas the current injected by the latter is a function of the output node voltage. Hence this new transconductor is acting as a resistor. Its current enters the node for positive values of y which means that its incremental resistance is negative and, consequently, induces a positive feedback action on the overall comparator operation.

This is confirmed through analysis of Fig. 7(a). Assuming that both transconductors and the resistor $G_o(y)$ operate inside their linear regions [see Fig. 3(b)] and defining $\alpha_F \equiv 1 - (g_{mo}/g_o)$,

$$k_S = \frac{g_m}{g_o - g_{mo}} = \frac{g_m}{g_o} \alpha_F^{-1} \tag{38}$$

Let us consider that $g_o > g_{mo}$, and hence $\alpha_F > 0$. Equation (38) shows that as g_{mo} increases by approaching the g_o value, the voltage gain also increases, thereby confirming the action of positive feedback. Because the incremental static sensitivity Δ_S is inversely proportional to the static gain, such an effect could be exploited to improve the resolution of one-step comparators, with no additional stages needed. In the limit for $g_{mo} \to g_o$, $k_S \to \infty$, and hence $\Delta_S \to 0$. On the other hand, Eq. (10) shows that for τ_u and Δ_D fixed, the speed of a one-step comparator also increases with increasing k_S. For instance, with $\tau_u = 10$ ns, $E_{OH} = 1$ V and $\Delta_D = 1$ mV, Eq. (10) yields $T_A \approx 47\ \mu s$ for $k_S = 1010$ and $T_A \approx 10\ \mu s$ for $k_S = 11000$.

Figure 7(b) shows a circuit implementation of positive feedback in one-step comparators. Figure 7(f) shows a CMOS schematic for this implementation where

$$g_{mo} = \sqrt{2 \frac{\beta_{0No}}{n_{No}} \left(\frac{W}{L} \right)_{No} I_{Bo}}$$

and

$$g_o = \frac{I_B + I_{Bo}}{2} \left(\frac{1}{V_{ANl}} + \frac{1}{V_{APl}} \right) \tag{39}$$

Because of the positive feedback action, this circuit, as any other including positive feedback, for instance, Fig. 7(g), is very sensitive to random fluctuations of technological parameters, such as β_0 in Eq. 39. Consequently, very small nominal values of α_F should be avoided if this parameter must be kept positive in the presence of such fluctuations. In practice it is hard to guarantee robust operation with $\alpha_F \approx 0.01$. A robust conservative value might be $\alpha_F \approx 0.1$, which reduces Δ_S by a factor of 10 and improves the nominal speed by a factor around 4.7—not too much improvement. Actually, analysis of Eq. (10) taking into account Eq. (38) shows that speed cannot be improved any further despite the value of α_F. The following section shows that much larger speed improvement is achieved by allowing α_F to be negative, the counterpart being degradation of resolution.

One-Step Comparators with Global Positive Feedback: The Onset of Hysteresis

Let us focus again on Fig. 7(a) and define $\beta_F = -\alpha_F = (g_{mo}/g_o) - 1$. Consider $\beta_F > 0$. This implies that $g_{mo} > g_o$ and hence that the amount of negative feedback exercised by g_o is smaller than the positive feedback due to g_{mo}. The global feedback is hence positive. This has two major consequences on comparator behavior:

- The time constant for small-signal variations around $y = 0$ is negative. Consequently, the transient evolution from this point follows an exponentially increasing law. In particular, assuming that $y(0) = 0$ and that an input step

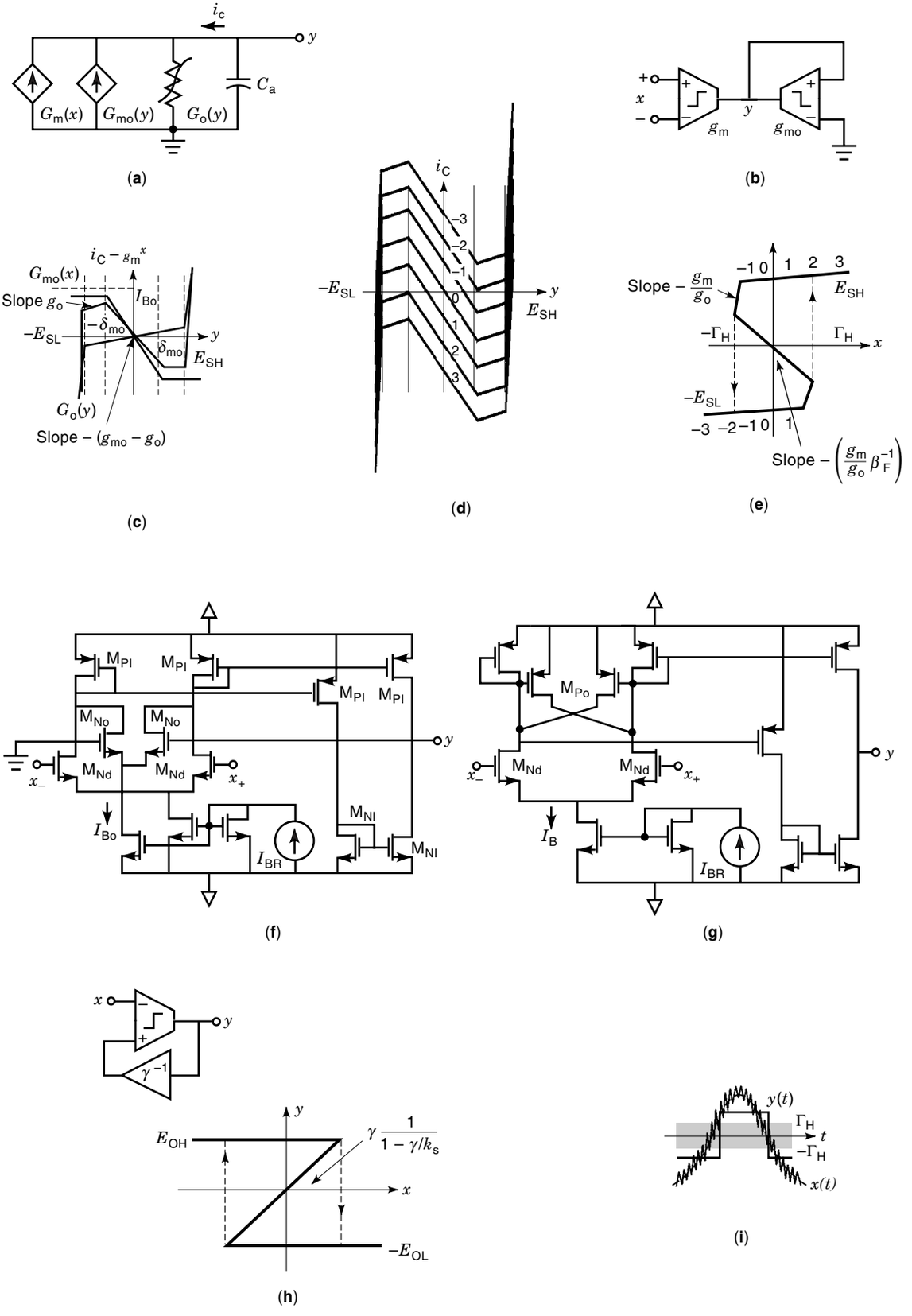

Figure 7. Using positive feedback in one-step comparators.

of amplitude Δ_D is applied at $t = 0$, the output waveform is given by

$$y(t) = \Delta_D \frac{g_m}{g_o} \beta_F^{-1} \left(e^{t\beta_F \frac{g_o}{C_o}} - 1 \right) \tag{40}$$

This exponentially increasing law enables much faster operation than for conventional one-step and multistep comparators.

- The large-signal comparator transfer characteristics are multivalued. Hence, the comparator exhibits hysteresis when operating in the CT mode with large-signal excitations.

Let us focus on the second feature. Graphical analysis of Fig. 7(a) using the models of Fig. 3(b) yields the characteristics drawn in solid black in Fig. 7(c). It displays $i_C + g_m x$ as a function of y, where i_C is the current leaving the capacitor. This figure shows that the capacitor sees a negative resistance around $y = 0$—the reason why the time constant around this point is negative. The figure also shows that the global characteristic seen by the capacitor is multivalued. To better understand why this latter feature leads to hysteresis, let us consider x changing, and draw a family of i_C versus y curves with x as parameter. Figure 7(d) shows such a family and Fig. 7(e) shows the corresponding y versus x comparator transfer characteristic. Assume that x is such that the capacitor sees the curve labeled **3** in Fig. 7(d). This curve intersects the y axis only at $y = E_{SH}$. Hence this is the steady-state output as Fig. 7(e) shows. At the intersection points the current through the capacitor is null and hence $dy/dt = 0$. These points are equilibrium states where $y(t) = cte$ and the circuit may remain static (22). In practice the circuit actually remains static provided that the slope of the i_o versus y curve is positive around the point (stable equilibrium) and is not otherwise (unstable equilibrium). Starting from any arbitrary initial value of y, the circuit trajectory toward steady-state is determined by the attraction exercised by stable equilibrium points and the repulsion exercised by unstable equilibrium points.

Now consider that x decreases such that the curve seen by the capacitor changes sequentially from that labeled **2** to that labeled **−3**. For x corresponding to curve **2**, the circuit operates at the rightmost edge of the multivalued region:

$$\Gamma_H = \delta_{mo} \frac{g_o}{g_m} \beta_F \tag{41}$$

and yields $y \approx E_{SH}$. For smaller x and until the other edge is reached, the circuit operates inside the multivalued region where there are two valid solutions. However, the output voltage remains positive. The reason is that this voltage is stored in the capacitor and the capacitor charge remains unchanged because at steady-state $i_C = 0$. When x reaches the leftmost edge of the hysteresis region, for $x = -\Gamma_H$, the capacitor sees the curve **−2**, whose only valid solution is $y = -E_{SL}$. Consequently, around this x value the output must jump from $y = \delta_{mo}$ to $y = -E_{SL}$. The dynamics of such a jump are dictated by the slopes of the different segments of the characteristic seen by the capacitor. First, the output evolves from $y = \delta_{mo}$ to $y = -\delta_{mo}$ with negative time constant $\tau = -(\beta_F^{-1} C_o)/g_o$. Then, from $y = -\delta_{mo}$ to $y = -E_{SL}$ the evolution is with positive time constant $\tau = C_o/g_o$. Once on the bottom segment of the transfer characteristics, the output remains negative while the edge $x = \Gamma_H$ is not surpassed.

Obviously, the incremental static sensitivity of hysteretic comparators is inherently smaller than Γ_H. Hence the onset of hysteresis implies degradation of resolution. However, small hysteresis is useful to avoid glitches in those applications where signals are embedded in a noisy environment. This is illustrated in Fig. 7(i), which shows that by defining the edges of the hysteretic characteristic equal or slightly greater than the amount of the largest expected noise amplitude, spurious glitches are avoided.

The circuits of Figs. 7(f) and 7(g) can be designed to have hysteresis. Figure 7(h), where we assume $0 < \gamma < 1$, shows another hysteretic circuit that uses a single one-step comparator and exploits the positive input terminal for positive feedback. The figure also shows the cycle featured by the circuit, where the hysteresis region edges are set through proper gain setting of the scaling block in the feedback path.

Discrete-Time Regenerative Comparators

The onset of hysteresis in positive-feedback comparators is a consequence of capacitor memory. If comparators are made to operate in discrete time and the memory is periodically eliminated through resetting, hysteresis disappears (in practice some hysteresis remains because of second-order phenomena). As in any discrete-time (DT) comparator, a clock must be used to control operation. In the clock-reset phase the comparator is disconnected from the inputs and driven to a central point. Then, in the comparison phase, the input is applied and a transient evolution happens toward one of the saturated states. The qualitative issues for this behavior are illustrated in Fig. 8(a) for the circuit of Fig. 7(b). During the reset phase the output is driven to the central point of Fig. 8(a), P_0, where $y = 0$. During the comparison phase, for $x > 0$, the capacitor sees the bottom characteristics of Fig. 8(a) which include three equilibrium points (see previous discussion of intersection points): two stable, Q_L and Q_H, and the other unstable, Q_0 (refer again to the previous discussion). Because the capacitor charge cannot change instantaneously, the initial state is $y = 0$ corresponding to P_+ on the characteristic, which is located on the right-hand side of Q_0. From P_+ the repulsion action exercised by Q_0, precludes reaching the left-hand stable equilibrium at Q_L, and the trajectory is attracted toward the right-hand stable equilibrium at Q_H, where $y = E_{SH}$. On the other hand, for $x < 0$, the central point pushes the trajectory toward the equilibrium at Q_L, where $y = -E_{SL}$. In both cases, dynamic evolution is realized with negative time constants and hence at very high speed.

Except for the influence of second-order effects, the operation described is valid no matter how small the input signal magnitude may be. Only the input sign is significant. It means that DT positive feedback comparators can build infinitely large dynamic gain—a feature not shared by one-step or by multistep comparators whose maximum dynamic gain is smaller than the static gain. This is confirmed by Eq. (40), which shows that the output waveform is not bounded no matter how small Δ_D may be.

DT positive-feedback comparators, usually called *regenerative* comparators, are commonly built by cross-coupling a pair of inverters to form a *latch*—a circuit structure often used as

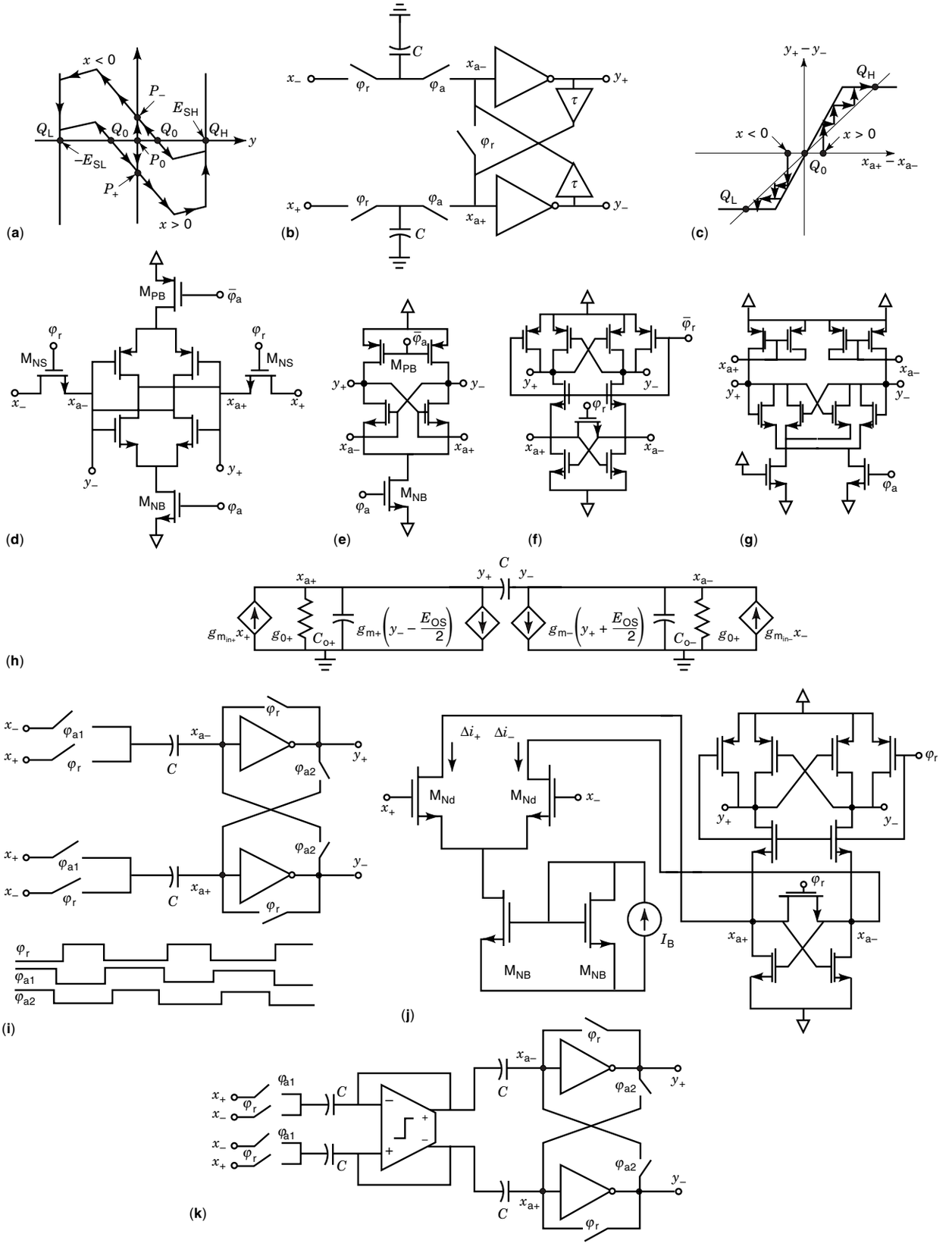

Figure 8. Regenerative comparators.

a sense amplifier in dynamic RAMs (1). Figure 8(b) shows the concept of a regenerative comparator based on a latch, where the triangles in the feedback loop model delays in the transmission of voltages around the loop. [This is a very crude model. Correct modelling requires a nonlinear vectorial differential equation of at least second-order that takes into account impedances at the different nodes. Then the dynamic has to be analyzed in the phase space (22).] The inverters amplify the differential input $x_{a+} - x_{a-}$ to obtain the saturated differential output $y_+ - y_-$ according to the characteristics drawn in solid black in Fig. 8(c). During the reset phase, the circuit is driven to the central state Q_0. During the active phase, the differential input is applied, forcing an initial state either at the right, $x > 0$, or at the left, $x < 0$, of Q_0. From this initial state, the action of positive feedback forces the output to evolve either toward Q_H, for $x > 0$, or toward Q_L, for $x < 0$, as illustrated by the gray line trajectories in Fig. 8(c).

Figures 8(d) to 8(g) show several CMOS latches reported in the literature (23–27). For Figures 8(d) and 8(e) during the reset phase, transistors M_{NB} and M_{PB} are OFF so that the latch is disabled. Hence, nodes x_{a+} and x_{a-} are at a high-impedance state and input voltages can be sampled at these nodes. Transistors M_{NS} in Fig. 8(d) are used for that purpose. Then, the voltage difference is amplified when the latch becomes enabled during the active phase. Alternatively, the nodes x_{a+} and x_{a-} are driven in the active phase with currents obtained from the input voltages by transconductors, as illustrated in Fig. 8(k). This is the only excitation alternative for Figs. 8(f) and 8(g).

The circuit of Fig. 8(h) is a small-signal, first-order model of the latch behavior during the active phase. It corresponds to the case where signals are applied through transconductors and includes asymmetries between the two latch branches and capacitive coupling between the two latch outputs. Such coupling and asymmetries appear in practical circuits and are responsible for significant errors observed in actual latch operation (28). The circuit of Fig. 8(h) captures the latch dynamic in the following state equations:

$$(C_{o+} + C_c)\frac{dy_+}{dt} = -g_{o+}y_+ - g_{m+}y_- + g_{m_{in+}}x_+ + g_{m+}\frac{E_{OS}}{2} + C_c\frac{dy_-}{dt}$$

and

$$(C_{o-} + C_c)\frac{dy_-}{dt} = -g_{m-}y_+ - g_{o-}y_- + g_{m_{in-}}x_- - g_{m-}\frac{E_{OS}}{2} + C_c\frac{dy_+}{dt} \tag{42}$$

First assume full symmetry, equal positive and negative parameters, $E_{OS} = 0$, and negligible capacitive coupling. Then, the previous two equations can be substracted so that dynamics are represented by a single differential equation:

$$C_o\frac{d(y_+ - y_-)}{dt} = g_m(y_+ - y_-) - g_o(y_+ - y_-) + g_{m_{in}}(x_+ - x_-) \tag{43}$$

The first term on the right-hand side of this equation represents positive feedback, the second negative feedback, and the last the input. Assume $(g_m/g_o) \gg 1$. Then, assuming that the circuit is initialized at $t = 0$ such that $y(0) = y_+(0) - y_-(0)$ and that a differential input step of amplitude $\Delta_D \equiv x_+ - x_-$ is applied at this instant, the differential output waveform can be approximated as

$$y(t) \equiv y_+(t) - y_-(t) \approx \Delta_D\frac{g_{m_{in}}}{g_m}e^{t\frac{g_m}{C_o}} \equiv \Delta_D\frac{g_{m_{in}}}{g_m}e^{\frac{t}{\tau_u}} \tag{44}$$

A similar equation is found for those cases where the latch is driven during the reset phase by establishing a voltage unbalance $y(0) = y_+(0) - y_-(0) \equiv \Delta_D$. Then $y(t) \approx \Delta_D e^{t/\tau_u}$. From Eq. (44) the following expression is found for the resolution for speed tradeoff:

$$\Delta_D\left(\frac{T_A}{\tau_u}\right) \simeq E_{OH}\left[\left(\frac{\Delta_D}{E_{OH}}\right)\ln\left(\frac{E_{OH}}{\Delta_D}\frac{g_m}{g_{m_{in}}}\right)\right] \tag{45}$$

Figure 6(a), where $R \equiv g_m/g_{m_{in}}$ compares this tradeoff to that given by Eq. (25) for multistep comparators. It shows that, as already anticipated, regenerative comparators feature faster operating speed despite the value of N.

Asymmetries in DT Regenerative Comparators: Mixed Comparator Architectures

Spurious differential signals, coupling between the two latch branches, and mismatches between their parameters preclude correct amplification of small Δ_D values. Their influence can be assessed by studying the equilibrium points of Eq. (42), their eigenvalues, and their eigenvectors (22) which are out of this article's scope. On the other hand, the influence of spurious random signals is a much harder problem.

Note from Eq. (42) that the influence of offset E_{OS} between two branches is similar to that observed in one-step and multistep comparators, that is, $\xi_D \propto |E_{OS}|$. It can be attenuated through separate self-biasing of the two latch branches. The circuit of Fig. 8(i) employs this strategy (29). Larger offset attenuation is achieved by using capacitors, instead of just wires, in the latch coupling branches of this circuit.

However, dissymmetries between transconductances g_{m+} and g_{m-} and between the capacitors C_{o+} and C_{o-} produce much larger errors for regenerative comparators than for one-step and multistep comparators. The amount of error depends on the input signal common mode x_{CM}, as Fig. 6(c) illustrates. This figure shows the outcome of simulations realized using Eq. (42) with realistic transconductance mismatches of 10% and capacitive coupling of 30%. For zero common mode the figure does not anticipate limitations on Δ_D. On the other hand, as the common mode increases to half of the swing range, $|\Delta_D|$ has to be larger than ≈30 mV for correct codification of the input signal polarity. This value increases up to ≈50 mV if 10% mismatches are considered for transconductances and capacitances. It imposes a strong constraint on comparator resolution, not shared by either one-step or multistep comparators.

This problem of regenerative comparators is overcome by placing a preamplifier in front of the regenerative core. This is actually the role played by transconductances $g_{m_{in}}$ in Fig. 8(h), and resolution improvement is roughly proportional to the ratio $g_{m_{in}}/g_m$. Figure 8(j) shows an actual CMOS circuit implementation of this concept (25). Alternatively, if the latch is driven through voltages, a mixed comparator architecture

consisting of the cascade of a self-biased one-step comparator and a self-biased latch can be used. Larger accuracy is achieved by making the latter a fully differential type, as shown in Fig. 8(k) (18,29).

BASIC CURRENT COMPARATORS

Building Current Comparators from Voltage Comparators

As defined in the first Section, current comparators are used to map the difference between two analog currents $x_+(t)$ and $x_-(t)$ onto a digital voltage y, so that the state of the latter codifies the sign of the former. The larger the *transimpedance gain* k_S, the smaller the incremental static sensitivity parameter Δ_S, and the more sensitive the comparator under dc excitation. Hence, the process of current comparator synthesis consists essentially of finding circuit structures to obtain the largest possible k_S. One obvious architecture uses a large resistor for current-to-voltage conversion and a buffer for output voltage isolation [shown at the conceptual level in Fig. 9(a)]. Thus, the transimpedance gain is contributed only by the resistor. For greater design flexibility, the buffer is replaced by a voltage comparator that also contributes to k_S. The front-end current-sensing device can also be replaced by a more general reactive impedance $Z_a(s)$ (30), thus leading to the conceptual architecture of Fig. 9(b).

For design purposes it is worth considering two extreme cases for the architecture of Fig. 9(b), one where the sensing device is dominated by the resistive component and one where the capacitive component is dominant. Figure 9(c) shows an example of a practical current comparator belonging to the former class (31), and Fig. 9(d) shows a corresponding example for the latter (32). These two classes display quite different properties for dynamic resolution ξ_D.

About the Resolution of Resistive-Input and Capacitive-Input Current Comparators

Obviously, the resolution of Fig. 9(b) depends on the sensing device and on the voltage comparator structure. For comparison, consider the simplest case where the latter is realized through a one-step architecture with dc gain $g_m R_b$ and unitary time constant $\tau_u = C_b/g_m$ as shown at the conceptual level in Fig. 9(e). Assume, as shown in Fig. 9(e), that an overdrive current step of magnitude Δ_D is applied at $t = 0$ and that the circuit is at its central point before applying the step. Routine analysis obtains the following expression for the output voltage waveform:

$$y(t) = g_m R_a R_b \Delta_D \left(1 - \frac{\delta_0}{\delta_a - \delta_b} e^{-t/\delta_a} - \frac{\delta_b}{\delta_b - \delta_a} e^{-t/\delta_b}\right), \quad t > 0 \tag{46}$$

where $\tau_a = R_a C_a$ and $\tau_b = R_b C_b$. From here the amplification time T_A and the incremental dynamic sensitivity Δ_D are calculated by using Eq. (3).

Consider the resistive-input case first. It yields $R_a \ll R_b$ and $C_a \approx C_b$. The resistance R_a and capacitance C_a in the input stage of Fig. 9(e) model the parallel combination of the nominal sensing elements and the parasitics from the driving and amplifying stages. This means that in an optimum de-

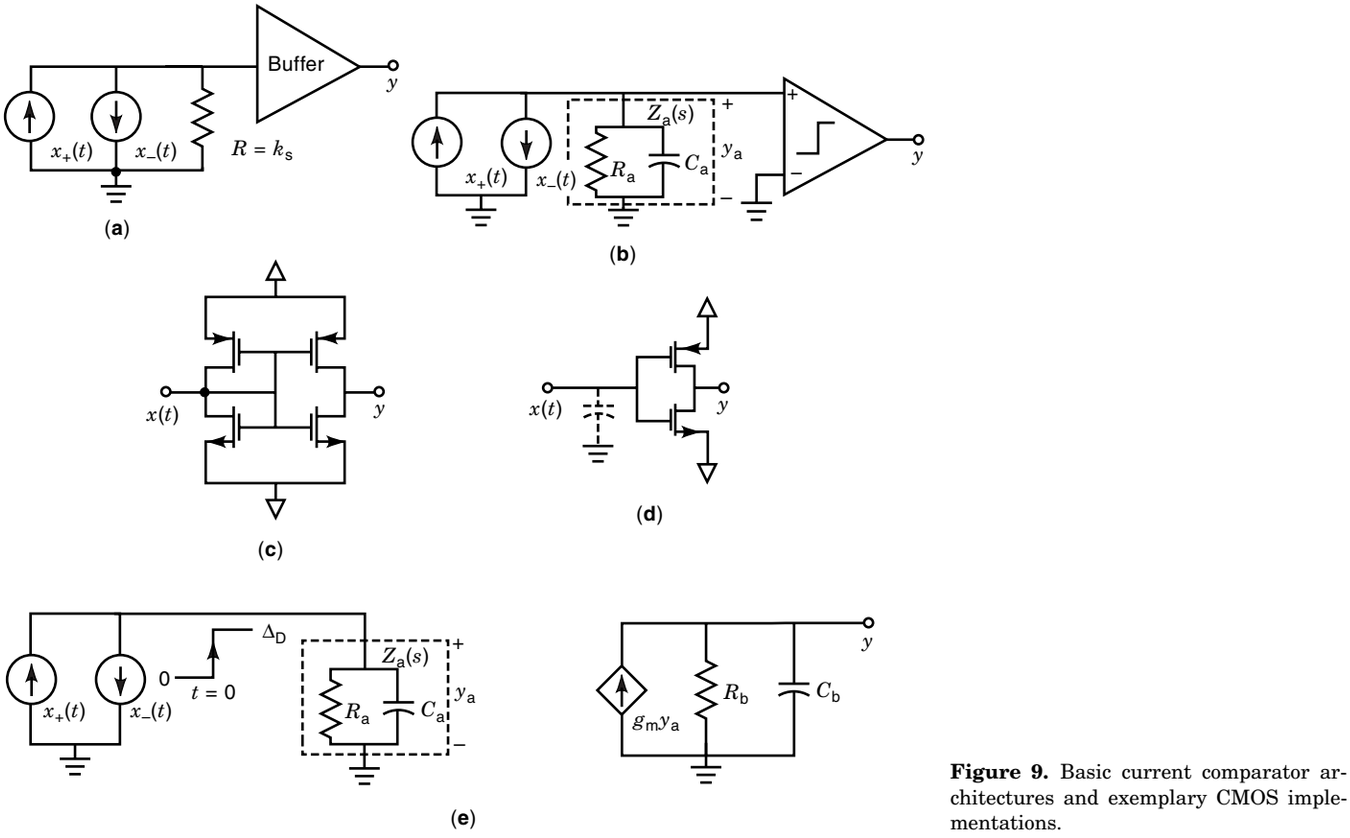

Figure 9. Basic current comparator architectures and exemplary CMOS implementations.

sign C_a is of the same order of magnitude as C_b and that the maximum attainable R_a value is limited by the device's early voltage, similar to what occurs for R_b. Therefore the time constant of the input stage is much lower than that of the output stage. Taking this into account and assuming $t \ll \tau_b$, Eq. (46) is simplified to obtain

$$\Delta_{D_{RI}} \approx \frac{1}{T_A}\frac{C_b}{g_m}\frac{E_{OH}}{R_{a_{RI}}} = \frac{\tau_u}{T_A}\frac{E_{OH}}{R_{a_{RI}}} \tag{47}$$

which shows a direct dependence with the unitary time constant of the voltage comparator and an inverse dependence with T_A, similar to that observed for one-step voltage comparators.

Now consider the capacitive-input case. The input node of this structure is the high-impedance type and hence, τ_a and τ_b are of the same order of magnitude. Taking this into account and assuming $t \ll \tau_b$, the dynamic resolution is calculated by making a Taylor expansion of Eq. (46) and keeping the linear and the quadratic terms:

$$\Delta_{D_{CI}} \cong 2\frac{1}{T_A^2}\frac{C_b}{g_m}(C_a R_{a_{CI}})\frac{E_{OH}}{R_{a_{CI}}} \approx 2\frac{\tau_u \tau_{a_{CI}}}{T_A^2}\frac{E_{OH}}{R_{a_{CI}}} \tag{48}$$

where $\Delta_{D_{CI}}$ is directly proportional to the unitary time constants of the voltage comparator and the current sensing front-end and inversely proportional to the square of the amplification time.

Comparative analysis of Eqs. (47) and (48) shows a different accuracy for speed tradeoff for each current comparator architecture. The two architectures feature the same speed (i.e., the same amplification time) for the following value of the dynamic resolution parameter:

$$\Delta_D^* \approx \frac{1}{2}\frac{\tau_u}{\tau_{a_{CI}}}\frac{E_{OH}}{R_{a_{RI}}}\frac{R_{a_{CI}}}{R_{a_{RI}}} \tag{49}$$

Analysis of Eq. (49) using a feasible set of parameter values, namely $\tau_u = 10^{-8}$ s, $\tau_{a_{CI}} = 10^{-7}$ s, $E_{OH} = 1$ *V*, $R_{a_{RI}} = 10^5\ \Omega$, and $R_{a_{CI}} = 10^6\ \Omega$, yields $\Delta_D^* \approx 5\ \mu A$. For $\Delta_D < \Delta_D^*$ and because $\Delta_{D_{CI}} \propto T_A^{-2}$, capacitive-input architecture yields smaller T_A than resistive-input, where $\Delta_{D_{RI}} \propto T_A^{-1}$. This means that capacitive-input architecture is faster for applications involving small input currents.

The advantages of capacitive-input for small currents are confirmed by calculating the static sensitivity Δ_S and the offset $|E_{OS}|$. The former is inversely proportional to the dc transimpedance, given as the product of R_a and the dc voltage comparator gain. Thus,

$$\Delta_S = \frac{1}{2}\frac{E_{OH} + E_{OL}}{g_m R_a R_b} \tag{50}$$

On the other hand, the offset has two components: the input current offset of the sensing device and the input offset of the voltage comparator attenuated by R_a. Thus,

$$|E_{OS}| = |E_{OSa}| + \frac{|E_{OSb}|}{R_a} \tag{51}$$

Hence, the static resolution parameter is given by

$$\zeta_S \equiv |E_{OS}| + \Delta_S = |E_{OSa}| + \frac{1}{R_c}\left(|E_{OSb}| + \frac{E_{OH} + E_{OL}}{2g_m R_b}\right) \tag{52}$$

where the larger R_a, the smaller ξ_S. Actually, for ideal capacitive input, where $R_{a_{CI}} \to \infty$, Eq. (52) yields $\xi_S \to |E_{OSa}|$. Then, any input current $x(t)$ such that $|x(t)| > |E_{OSa}|$, no matter how small $|x(t)| - |E_{OSa}|$ may be, is integrated by the input capacitor forcing the input of the voltage comparator to evolve so that the sign of the input current is correctly coded.

Now consider applications involving large currents. Analysis of Eq. (47)–(49) shows that the resistive-input architecture is faster whenever $\Delta_D > \Delta_D^*$. Also, because the voltage variations at the input node $y_a = x \cdot R_a$ are smaller for resistive-input comparators, this structure can be expected to exhibit smaller interstage loading errors and to perform better under overdrive excitations.

Multistep Current Comparators

Multistep current comparators are implemented by cascading a current-sensing device to perform current-to-voltage conversion, followed by a multistep voltage comparator. Analysis of such a structure yields the following expressions for amplification time:

$$T_A \simeq \delta_u \left(\frac{E_{OH}}{\Delta_{D_{RI}} R_{a_{RI}}} N!\right)^{1/N}, \quad \text{for resistive input}$$

and

$$T_A \approx \tau_u \left(\frac{\tau_{a_{CI}} E_{OH}}{\Delta_{D_{CI}} \tau_u}\frac{(N+1)!}{R_{a_{CI}}}\right)^{1/(N+1)} \quad \text{for capacitive input} \tag{53}$$

Both architectures feature the same speed (i.e., the same amplification time) for the following value of the dynamic resolution parameter:

$$\Delta_D^* \approx \left[\frac{N!}{(N+1)^N}\right]\frac{E_{OH}}{R_{a_{RI}}}\left(\frac{R_{a_{CI}}}{R_{a_{RI}}}\frac{\tau_u}{\tau_{a_{CI}}}\right)^N \tag{54}$$

Analysis of Eq. (54) using a feasible set of parameter values, namely, $\tau_u = 10^{-8}$ s, $\tau_{a_{CI}} = 10^{-7}$ s, $E_{OH} = 1$ *V*, $R_{a_{RI}} = 10^5\ \Omega$, $R_{a_{CI}} = 10^6\ \Omega$, and $N = 2$ results in $\Delta_D^* \approx 2.2\ \mu A$ which is lower than the dynamic resolution term obtained for the one-step current comparator for the same parameters.

ADVANCED CURRENT COMPARATORS

The previous section shows that resistive-input and capacitive-input comparators are complementary architectures. This section presents improved architectures that combine the advantages of these two basic schemes, namely, large sensitivity and reduced amplification time for low-current levels and reduced input voltage excursion for large current levels.

Current Comparators with Nonlinear Current Sensing

Figure 10(a) shows the conceptual block diagram of a current comparator where the linear resistor R_a of Fig. 9(b) is re-

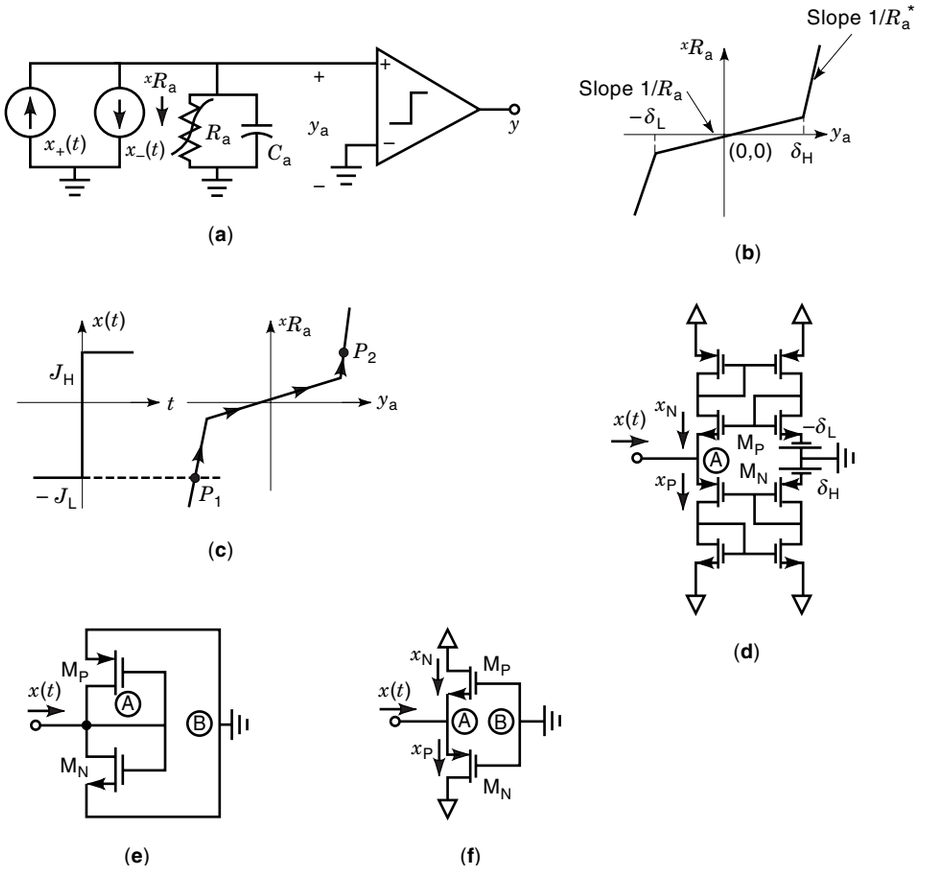

Figure 10. Current comparator with nonlinear current sensing.

placed by a nonlinear resistor $\Re_a$ with the driving-point characteristics of Fig. 10(b). This characteristic has three segments. In the inner one, for low currents, the equivalent resistance R_a is very large, and the circuit behaves as a capacitive-input architecture. On the other hand, for large currents, the equivalent resistance R_a^* is much smaller and the circuit behaves as a resistive-input one.

To calculate the incremental dynamic sensitivity, consider that the voltage comparator has one-step architecture, similar to Fig. 9(e). Following the application of a current step of amplitude Δ_D, the input voltage evolves quasi-linearly with time while in the inner segment of the nonlinear resistor and remains quasi-constant otherwise. Correspondingly, the output voltage evolves quadratically with time during the first part of the transient and linearly afterward. To keep the speed advantages of capacitive-input architecture, the restoring logic level E_{OH} should be reached during the first part of the transient, that is, such that,

$$y_a(T_A) \approx \frac{T_A}{\tau_a} \Delta_D R_a < \delta_H$$

and

$$y(T_A) = E_{OH} \approx \frac{1}{2} \frac{T_A^2}{\tau_u \tau_a} \Delta_D R_a \tag{55}$$

where it is assumed that $\tau_a \equiv R_a C_a \approx \tau_b \equiv R_b C_b$ and $\tau_a^* \equiv R_a^* C_a \ll \tau_b \equiv R_b C_b$. This results in the following design constraint:

$$\frac{\delta_H^2}{R_a} \frac{\tau_a}{\tau_u} > 2\Delta_D E_{OH} \tag{56}$$

where the incremental dynamic sensitivity is given by Eq. (48). On the other hand, the formula for the static resolution parameter [Eq. (52)] remains valid.

In the more general case of an excitation between two overdrive levels $-J_L$ and J_H, the dynamic evolution of the input node also includes points in the outer segments of the nonlinear resistor [see the dynamic route of Fig. 10(c)], and calculating the output waveform is not direct. However, neglecting delays in the devices used to realize the nonlinear resistor, the response time will be a monotonic function of the time invested for the input voltage to change from $-\delta_L$ to δ_H. Hence,

$$T_C = f\left[\frac{C_a}{J_H}(\delta_H + \delta_L)\right] \tag{57}$$

where the exact functional relationship depends on the actual voltage comparator used.

Figures 10(d) and 10(e) show simple CMOS nonlinear resistor realizations. Both yield $\delta_L = |V_{TP}|$ and $\delta_H = V_{TN}$. This results in a rather large dead zone around 2V, and hence Eq.

(57) anticipates rather poor response time. In the case of Fig. 10(e), the dead zone length can be reduced by biasing the gates of M_N and M_P with different voltages, namely, $V_{GN} = V_{TN} - \delta_L$ and $V_{GP} = |V_{TP}| + \delta_H$. This can be done with the circuit of Fig. 10(f), which consists of two stacked complementary, first-generation current conveyors as originally proposed by Smith and Sedra (33). The circuit is similar to the class AB current amplifier proposed in Ref. (34) (see also Ref. 35 for an improved version). In any case, δ_H and δ_L should be large enough to guarantee that the central region of the driving-point characteristics matches that of the voltage comparator under global and local statistical variations of the technological parameters. Such a large central region length may induce significant loading errors in operating the stage used to drive the comparator (30). Besides, the aspect ratios of M_N and M_P must be large enough to reduce R_a^*.

Current Comparators with Nonlinear Feedback

Figure 11(a) shows an improved architecture that reduces the central region length. Contrary to Fig. 10(a), the voltage-mode comparator of Fig. 11(a) does not operate in open loop but uses the nonlinear resistor for negative feedback. There are three different operating regions that correspond to the three segments of the nonlinear resistor characteristic depicted in Fig. 10(b). For small changes around the quiescent point ($x_+ = x_- = 0$), the equivalent resistance of the feedback resistor is large, the voltage amplifier operates practically in open

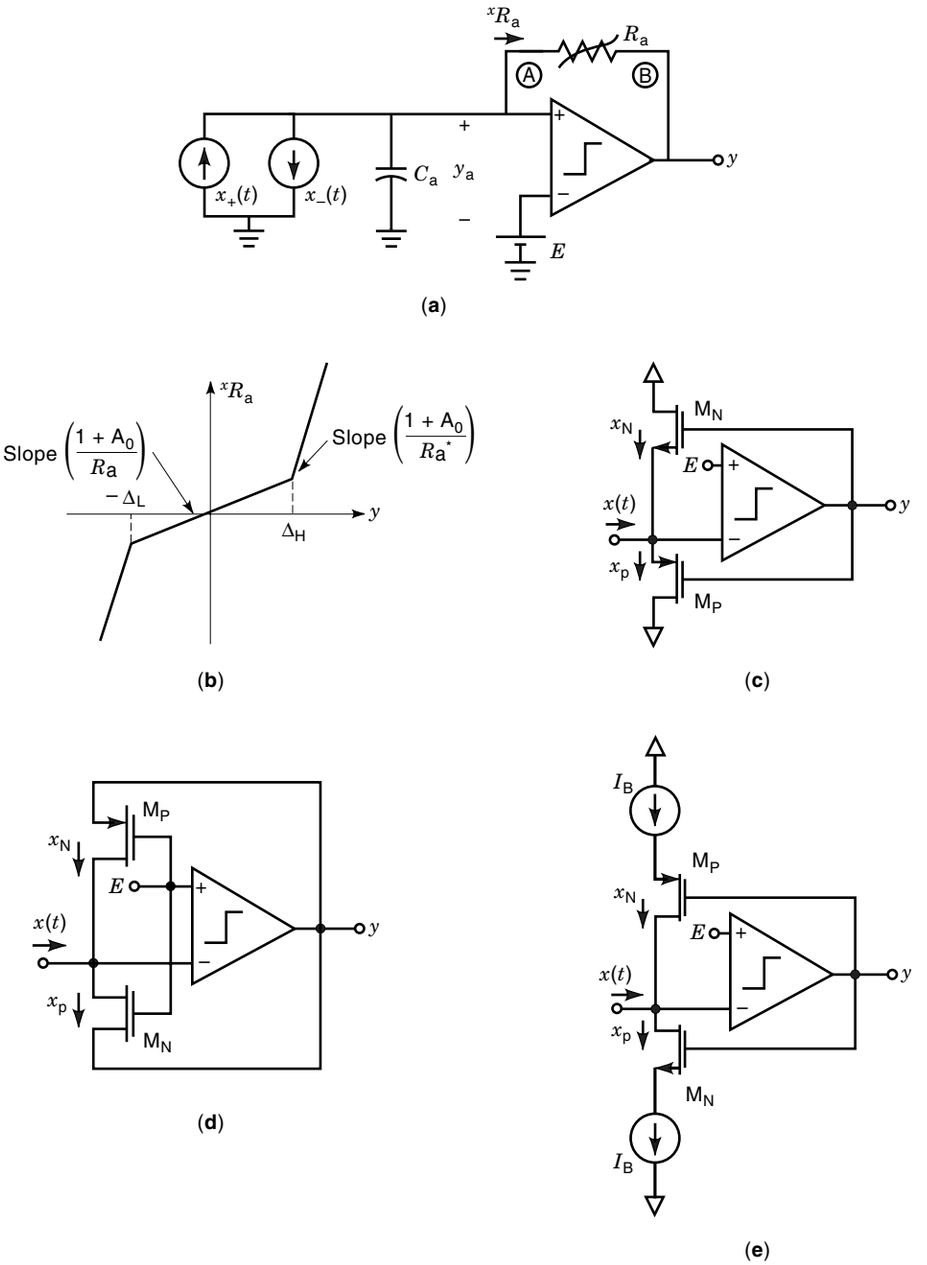

Figure 11. Current-mode comparator using nonlinear feedback.

loop, and the circuit preserves the capacitive-input feature (the comparator input is the high-impedance type). For $x_+ > x_-$, voltage y_a is pulled up and the amplifier decreases y. Thus, the resistor enters in the rightmost segment of the characteristic, allowing the input voltage to reach a bounded steady-state (the input of the comparator is a low-impedance node). A dual situation occurs for $x_+ < x_-$, where y_a is pulled down and y is high. Consequently, the comparator sees the characteristics of Fig. 11(b), where, when $E = 0$,

$$\Delta_L = \frac{\delta_L}{1+A_0}$$

and

$$\Delta_H = \frac{\delta_H}{1+A_0} \tag{58}$$

where A_0 denotes the amplifier gain and $-\delta_L$ and δ_H are the nonlinear resistor breakpoints. Note that the central region length reduces as the amplifier gain increases. A negative consequence of feedback is that the output signal becomes clamped at $-\delta_L$ and δ_H, respectively. Hence, it may be necessary to cascade an additional voltage comparator to restore the logic level.

Figures 11(c) and 11(d) show practical CMOS realizations of the nonlinear feedback current comparator. A common feature of these circuits is that the transition region of the nonlinear resistor tracks by construction that of the voltage amplifier, which means that the operation is insensitive to mismatches and hence permits using minimum size transistors. This is important because minimum transistors mean minimum parasitic capacitances and hence reduced response times.

In the case in Fig. 11(c), simple CInvC or InvC structures can be used for the voltage comparator, thus leading to very compact realizations. However, this structure has the drawback that the transient behavior is largely dominated by the overlapping capacitance C_f which connects input and output terminals of the voltage amplifier. Analysis obtains the following expression for comparison time (30):

$$T_C \approx \frac{A_0}{1+A_0}(V_{TN} + |V_{TP}|)\frac{C_f}{J_H} \tag{59}$$

which implies that, although the high-resolution properties of the capacitive-input architecture remain, the quadratic response feature is lost due to the Miller effect created around C_f, significant even for minimum size feedback transistors.

The circuit of Fig. 11(d), called a current steering comparator, circumvents this problem by decoupling the amplifier input and output nodes. Its static operation follows principles similar to those used in the circuit of Fig. 11(c). When $x(t) = 0$, transistors M_P and M_N are OFF and the circuit realizes capacitive-input behavior. Positive currents integrate in the input capacitor increasing the node voltage and consequently decreasing y until the transistor M_N becomes conductive, absorbing the input current and stabilizing the output. The same occurs for negative currents, where M_P is the conductive transistor. For transient behavior, analysis shows, that under the same assumptions as for the circuit of Fig. 11(a), the response time is given by (36),

$$T_C \approx \sqrt{\frac{2\tau_u C_s}{J_H}(V_{TN} + |V_{TP}|)} \tag{60}$$

where τ_u is the unitary time constant of the voltage comparator and C_s is the input capacitance.

To conclude this section, Fig. 11(e) shows a circuit similar to Fig. 11(c) where transistors M_P and M_N are swapped and the feedback is positive, instead of negative. It operates as a CMOS current Schmitt trigger where the positive and negative threshold values of the hysteretic characteristic are defined by the lower and upper current sources, respectively.

APPENDIX I. SIMPLIFIED MOST MODEL

MOS transistors exhibit different operation depending on the current and voltage levels. Throughout this article we considered only the MOST model under *strong* channel inversion, and described its first-order behavior using a model with four parameters, namely, zero-bias *threshold voltage* V_{T0}, the *slope factor* n, the *intrinsic transconductance density* β_0, and the *equivalent Early voltage* V_A (37). Two subregions are considered within strong inversion:

- *Triode* (or *ohmic*) region. In this regime, the source and drain voltages V_S and V_D remain below $V_p = (V_G - V_{T0})/n$, where V_G is the gate voltage (all voltages are referred to the local substrate). The drain current takes the form

$$I_D = 2\beta_0 \frac{W}{L}\left[V_G - V_{T0} - \frac{n}{2}(V_D + V_S)\right](V_D - V_S) \tag{61}$$

  where W/L is the aspect ratio of the transistor.
- *Saturation* region. Assuming forward operation, this regime is reached when $V_S < V_p < V_D$ and the drain current is given by

$$I_D = \beta_N(V_G - V_{T0} - nV_S)^2\left(1 + \frac{V_D - V_p}{V_A}\right) \tag{62}$$

  where

$$\beta \equiv \frac{\beta_0}{n}\frac{W}{L}$$

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