BOOTSTRAP CIRCUITS

The word *bootstrapping* is defined in *Webster's New World College Dictionary* (1) as "to lift (or raise) oneself by the (or one's own) bootstraps to achieve success by one's own unaided efforts." A similar phenomenon may occur in some electrical and electronic circuits. A circuit can sense a voltage change at one terminal of a two-terminal element and cause an equal change in the voltage of the other terminal (2). Thus the voltage drop across that element remains almost unchanged. For example, while terminal a of the device shown in Fig. 1 may have higher potential than terminal b (by V volts), if the voltage or potential at b is somehow raised, a potential change at a follows that at node b. This is referred to as bootstrapping since it is similar to a person trying to lift himself or herself off the ground by pulling his or her bootstraps. In actual circuits where bootstrapping is used, the voltage across the element may change.

The bootstrapping technique has been used for both digital and analog circuits. Some examples of each are presented next.

BOOTSTRAPPING IN DIGITAL CIRCUITS

Bootstrapping has been used in digital circuits (CMOS and BiCMOS) mainly to increase the voltage swing of the logic gates. In such circuits, bootstrapping is achieved by using capacitive coupling (3), as in the NMOS bootstrapped inverter shown in Fig. 2 (4).

In Fig. 2, M_1 maintains the voltage of node a at $V_{dd} - V_T$ (where V_T is the threshold voltage of the NMOS transistor). If the input is grounded, M_3 is turned off, whereas M_2 is turned on and thus provides current to charge C_{out}. This causes the output voltage V_o to rise toward V_{dd}. If C_{boot} is ignored temporarily, M_2 should turn off as soon as $V_o = V_{dd} - 2V_T$. However, due to the capacitor coupling provided by C_{boot}, the voltage of the gate of M_2 will follow the rising output. In other words, node a is bootstrapped. Notice that M_1 cuts off once V_a exceeds $V_{dd} - V_T$; thus node a can be assumed floating (isolated from V_{dd}). This allows the voltage V_a to rise above V_{dd} until it reaches $V_{dd} + V_T$, and as a result V_o can be pulled up to V_{dd}. This is the main advantage of using bootstrapping in the case of the NMOS inverter. To achieve proper bootstrapping, C_{boot} must satisfy the following condition (4):

$$C_{boot} \geq \frac{2V_T}{V_{dd} - 2V_T - V_{OL}} C_{par}$$

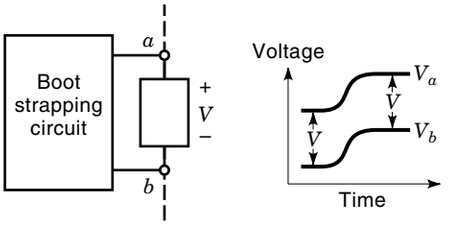

Figure 1. Bootstrapping in electronic circuits: The bootstrapping circuit forces the voltage at node a to track any voltage changes occurring at node b.

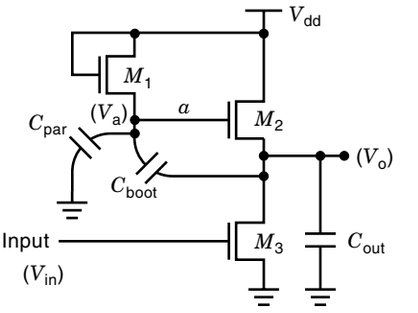

Figure 2. Bootstrapped NMOS inverter (4). The bootstrapping is achieved by C_{boot}.

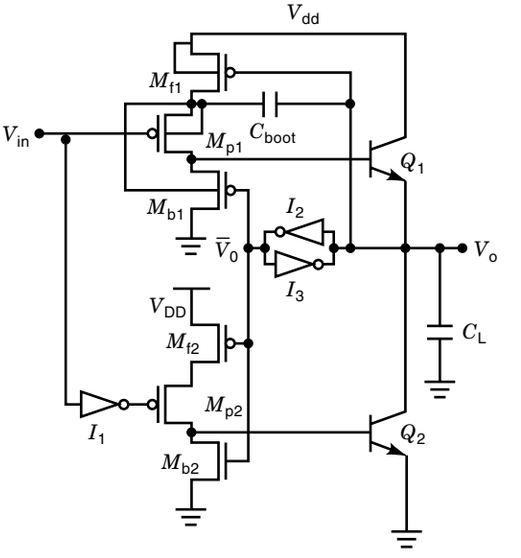

Figure 3. A bootstrapped BiCOMOS inverter (5).

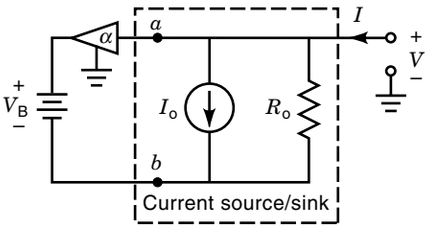

Figure 4. Bootstrapping to increase the output resistance of a current source.

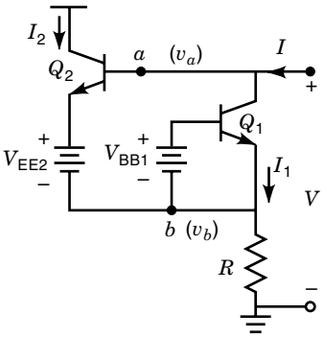

Figure 5. A bipolar bootstrapped current source. Any change in v_a will cause a similar change in v_b, such that the voltage across Q_1 remains constant.

where C_{par} is the parasitic capacitor at node a and V_{OL} is the low logical level of the NMOS inverter. It is important to notice that the bootstrapping due to capacative coupling is valid for a finite period of time. The charge stored on the boot node (node a) will leak off as time passes, and the voltage at node a will drift back to its nominal value $V_{dd} - V_T$; V_o will consequently drift to $V_{dd} - 2V_T$.

Bootstrapping has also been used for BiCMOS digital inverters to force the output logic high levels to approach V_{dd} (similar to NMOS). One example of such circuits is shown in Fig. 3 (5).

BOOTSTRAPPING FOR ANALOG CIRCUITS

Bootstrapping techniques can be effective in analog circuits, for instance, to increase the output resistance of a current source (2,6). This can be explained conceptually using Fig. 4. The bootstrapping circuit senses any change in V (the voltage of node a) and generates an equal change at node b so that the voltage across the current source is almost constant. This implies that the output resistance of the current source remains high. It can be shown that output resistance R_0 increases by a factor $1/1 - \alpha$, where α is the small signal voltage gain (2) where v_a is the small signal voltage at node a and V_b is the small signal voltage at node b. The gain α should ideally be unity so that the output resistance of the current source is infinite. But in practice it will have a finite value ($\alpha < 1$).

Figure 5 shows how the current source, consisting of Q_1 and V_{BB1}, is bootstrapped using Q_2, V_{EE2}, and R. The voltage gain from the base of Q_2 (node a) to the emitter of Q_1 (node b) is less than but very close to unity. Therefore, node b tracks node a. Thus the collector–emitter voltage and the collector current of Q_1 remains almost unchanged even though the voltage at node a may vary. This implies that the output resistance is increased.

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