VOLTAGE-TO-FREQUENCY CONVERTERS

INTRODUCTION

The *Voltage-to-Frequency Converters* (VFCs) belong to the category of the *oscillator* circuits. The function of an oscillator is to produce periodic time-varying signals with only dc excitations [1]. These signals may have quite diverse waveform shapes such as triangular, square, impulsive, exponential, sinusoidal, etc. For some oscillator applications, the shape of the generated signal is an important design criteria. For instance, in the production of periodic sweep voltages for display systems; or in the generation of quasi-sinusoidal signals for testing and instrumentation purposes. In other applications, the important design criteria is the signal *frequency,* while the spectral purity of the signal remains secondary. This is for instance the case of the oscillators used to generate clock signals for timing purposes. And this is also the case of VFCs.

The function of VFCs is to convert the value of an analog *input* voltage or current into an *output* frequency; *i.e.* they must generate signals of any shape whose frequency is a faithful representation of the analog input data. Thus, they also belong to the category of the *data converter* circuits, whose function is to convert the information among different domains with minimum degradation of the information itself. From this point of view, the VFCs have some similarities with the Analog-to-Digital Converters (ADCs), whose function is to convert an analog data into a digital word with the minimum error possible. In the case of VFCs the domain of the transformed information is the frequency of a signal, instead of a digital word, and the aim is to obtain the smallest possible error in the voltage-to-frequency mapping. The design criteria for VFCs include the following (14):

- *Dynamic Range,* i.e. the range of input voltage values where the transformation takes place. A related magnitude is *the frequency range* – the range of output frequencies which corresponds to the input voltage range. 60dB and larger dynamic ranges [2]are commonplace.
- *Linearity* of the voltage-to-frequency map, $f_0 = F(v_{in})$. This map is required to be highly linear,

$$F(v_{in}) = k \cdot v_{in} + E(v_{in}) \tag{1}$$

  with error $E(v_{\rm in})$ much smaller than 1% of full scale.
- *Scale Factor Accuracy* and *Stability.* The parameter k in Eq. (1) must be externally set for given voltage-to-frequency gain. After its setting, the gain must remain stable with temperature $- \leq 100$ppm/$^\circ$C $-$, aging, and changes of the power supply $- \leq 0.1\%/V$.

Such requirements are related to the main application area of the VFCs, namely the encoding of information for telemetry or remote control. In these applications, the analog data is converted into frequency at the emitter front-end by using a VFC. The generated signal is then transmitted through an optical or radio link – a process in which the signal frequency remains essentially unchanged. Then, at the receiver front-end, the analog data is recovered from the signal frequency by using a *Frequency-to-Voltage Converter* (FVC).

From the construction point of view, the VFCs are in the same category as the so-called Volt-age-Controlled-Oscillators (VCOs), in the sense that the circuit structures employed to realize VFCs and VCOs are actually quite similar. However, the typical applications of VCOs usually demand low precision in the voltage-to-frequency map and, in some cases, high spectral purity. In this chapter, we will start by presenting a broad overview of the different circuit structures that qualify to generate periodic signals with voltage-controlled frequency. Then, in the remaining of the chapter we will focus on those which are better suited to achieve accuracy in the volt-age-to-frequency mapping.

BASIC CONCEPTS AND MODELS FOR OSCILLATOR DESIGN

Circuit synthesis is the process of interconnecting circuit components so as to realize some targeted behavior. The first step for systematic circuit synthesis is to identify mathematical descriptions for the targeted behavior. In the case of oscillators, the target is to obtain a steady-state cyclic solution with only dc excitations. For VCOs and VFCs, the timing of these cyclic solutions must also be electronically controllable.

"The simpler the better"; this is a basic motto for electronic circuit design. In the case of oscillators, two ineludible ingredients are dynamics and nonlinearity. Thus, oscillator circuits must contain capacitors and/or inductors together with nonlinear elements. Strictly speaking, the dynamics must be at least of second-order type–meaning that the corresponding circuit requires at least two energy-storage elements. With regards to the nonlinearity, the simplest one is the N-like shape of Figure 1(a), which can be approximated by a series expansion,

$$\xi(x) = -\eta_{\rm NI} \cdot x + \eta_{\rm NE} \cdot x^3 \tag{2}$$

where $\eta_{\rm NI}$ and $\eta_{\rm NE}$ are real parameters which can be used to fit the required function shape. Alternatively, Figure 1(a) can be approximated by the *piecewise-linear* curve depicted in Figure 1(b), where the fitting is realized through the real parameters $\gamma_{\rm NI}$ and $\gamma_{\rm NE}$.

Basic Oscillator Model

The basic oscillator model is built by combining the ingredients above into

$$\begin{aligned} \tau_x \frac{dx}{dt} &= -y - \xi(x) \\ \tau_y \frac{dy}{dt} &= x \end{aligned} \tag{3}$$

Figure 2(a) shows a conceptual realization of this equation using two integrators, one adder and one block with nonlinear transfer function $\xi(x)$ – all realizable in electronic form. Figure 2(b) and (c) show realizations using capacitors, inductors and nonlinear resistors; it is easy to confirm that Figure 2(b) maps onto Eq. (3) for $x = v, \quad y = Ri_L, \quad \tau_x = RC, \quad \tau_y = L/R$ and assuming

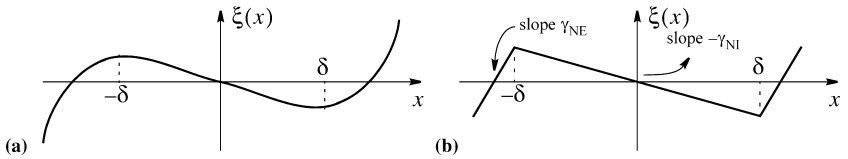

Figure 1. N-like shaped characteristics necessary to implement oscillator circuits and associated piecewise-linear approximation.

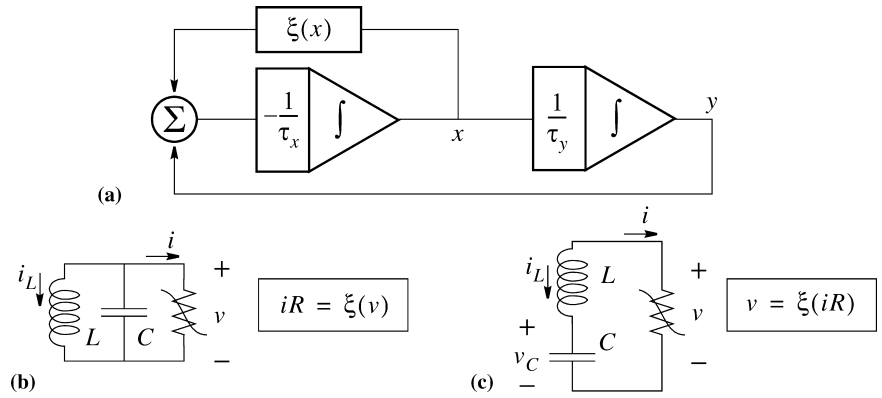

Figure 2. Conceptual realization of the basic oscillator model in Eq. (3) (a) and LC realizations for $x = v$, $y = Ri_L$, $\tau_y = L/R$ (b) and for $x = Ri_L$, $y = v_C$, $\tau_x = L/R$, $\tau_y = CR$ (c).

that the resistor has a voltage-controlled characteristic $iR = \xi(v)$; similarly, Figure 2(c) maps onto Eq. (3) for $x = Ri_L, \quad y = v_c, \quad \tau_x = L/R, \quad \tau_y = CR$ and assuming that the resistor has a current-controlled characteristic $v = \xi(iR)$.

The model of Eq. (3) generates stable oscillations–called *limit cycles*–due to the dynamic *equilibrium* between two opposite forces, one *expansive,* the other *contractive.* The expansive force happens for $|x|<\delta$ due to the negative slope of the nonlinearity in this region–see Figure 1(b) [3]. This negative slope can only be realized through an active element which injects energy into the system thereby making $|x|$ increase with time. On the other hand, the contractive force occurs for $|x|>\delta$ due to the positive slope of the nonlinearity in this region. Because of this positive slope, the system dissipates energy and, consequently, $|x|$ decreases with time.

The actual trajectories in the transient evolution towards the limit cycle depend on the values of the parameters τ_x, τ_y, γ_{NI}, γ_{NE} and δ. The shape of the limit cycle orbit and the frequency of the motion are also dependent on these values. Finding closed relationships among the shape and frequency, on the one side, and the parameter values, on the other, is not even possible in the more general case. However, for our purposes here it suffices to study the approximated solutions in two particular cases. First of all, we find convenient rewriting Eq. (3) in terms of a normalized time variable $\tau = t/\tau_o$ with $\tau_o = \sqrt{\tau_x \tau_y}$. It yields

$$\begin{aligned} \frac{dx}{d\tau} &= \alpha[-y - \xi(x)] \\ \frac{dy}{d\tau} &= \frac{1}{\alpha}\, x \end{aligned} \tag{4}$$

where $\alpha = \sqrt{\tau_y/\tau_x}$.The two particular cases of interest occur for extreme values of the parameter α; they are respectively caalled the harmonic oscillator case–which corresponds to $\alpha \ll 1$, and the relaxation oscillator case–which corresponds to $\alpha \gg 1$.

Harmonic Oscillator Case

This corresponds to $\alpha \gg 1$, i.e. to $\tau_y \ll \tau_x$. For a better understanding of what happens in this case, it is convenient to recast Eq. (4) into the following scalar form,

$$\frac{d^2x}{d\tau^2} + \alpha \frac{d\xi dx}{dx d\tau} + x = 0 \tag{5}$$

obtained after differentiating the top expression in Eq. (4) and using the bottom expression to substitute $dy/d\tau$.

Assume first that the nonlinearity is null. Then $d\xi/dx = 0$ and the solution of Eq. (5) for initial conditions $x(0) = x_0$ and $dx/d\tau|_{\tau=0} = 0$ is $x(\tau) = x_0 \cos(\tau)$, and hence,

$$x(t) = x_0 \cos(\omega_0 t) \tag{6}$$

where $\omega_o \equiv 1/\tau_0$. Obviously, such a solution could not be kept in practice due to the unavoidable energy dissipation–which is why nonlinearity is needed for practical oscillator design. However, because $\alpha \ll 1$, the second term in Eq. (5) is negligible and at the limit cycle $x(t)$ is quasi-sinusoidal; $x(t) \approx \rho \cos(\omega_0 t)$ with amplitude for fixed α and τ_0 depending on γ_{NI},γ_{NE} and δ .

The set of drawings in Figure 3 illustrate the harmonic oscillation case. On the one hand, they are intended to highlight the dynamic equilibrium process underlying the onset of oscillations. On the other, they give insight on the influence of the model parameters. All the drawings are for $\tau_x = 10, \quad \tau_y = 0.1$ and $\delta = 1$. The three drawings at the top are for $\gamma_{NE} = 1$ and $\gamma_{NI} = 1$. The one on the left in this subset shows the solution trajectories in the x-y plane for different initial conditions. The opposed expansive and contractive forces are highlighted by this figure. Their equilibrium results in the system evolving towards a limit cycle from any initial condition located either inside or outside it.

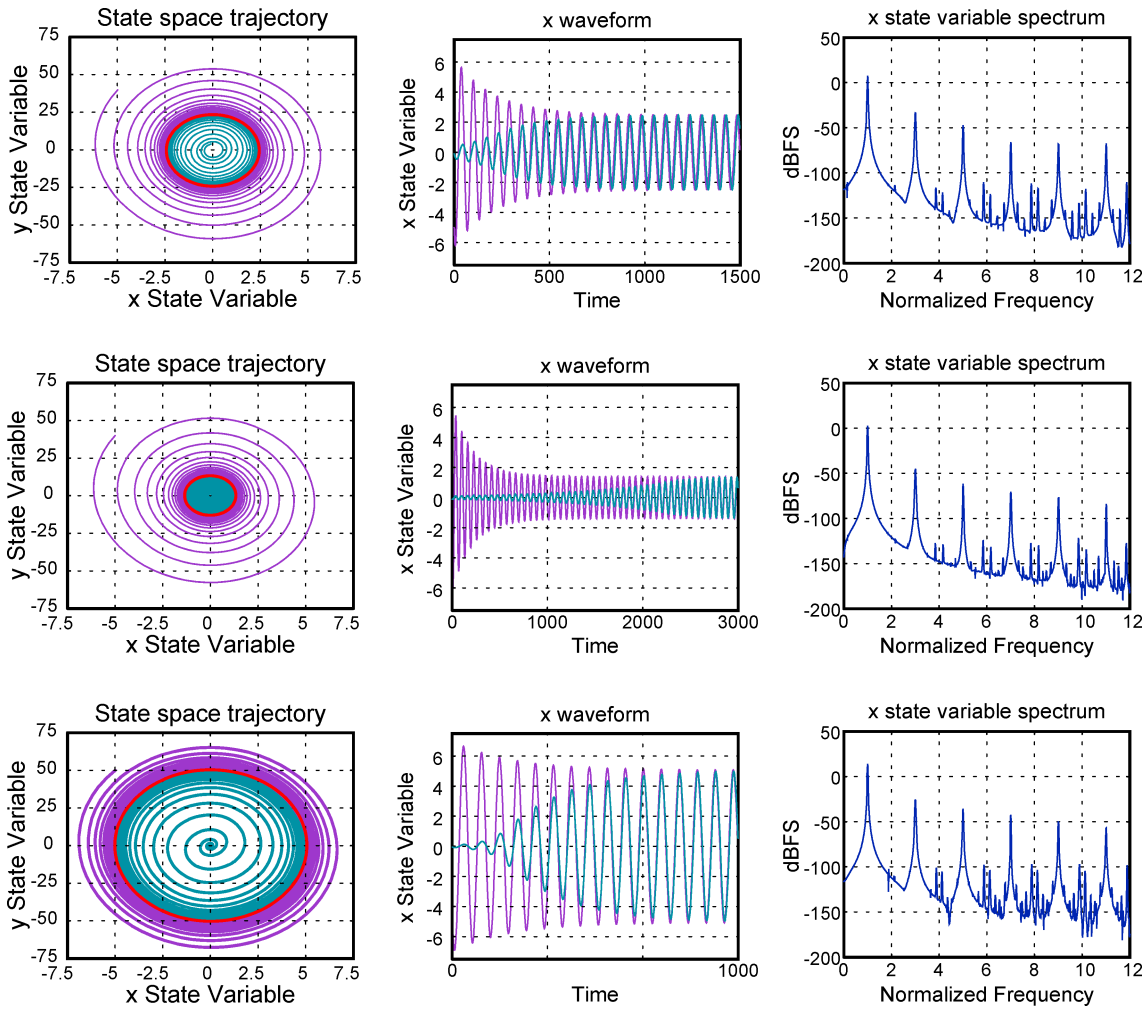

Figure 3. Trajectories, signals and spectrum for the oscillator model in the harmonic oscillation case for $\tau_x = 10$, $\tau_y = 0.1$ and $\delta = 1$. The three drawings at the top are for $\gamma_{\rm NE} = 1$ and $\gamma_{\rm NI} = 1$, those in the center row are for $\gamma_{\rm NE} = 1$ and $\gamma_{\rm NI} = 0.2$, the drawings at the bottom were obtained for $\gamma_{\rm NE} = 1$ and $\gamma_{\rm NI} = 3$. We see that the oscillation frequency is practically the same in the three cases (basically set by $\tau_0 = \sqrt{\tau_x \tau_y}$). We also observe that the larger $\gamma_{\rm NI}$, the larger the signal amplitude and distortion, while the dynamic evolution toward the limit cycle is faster.

The waveform at the center in the top set of figures shows $x(t)$ at the steady-state. Because thisxt() steady-state is obtained as the result of a nonlinear equilibrium process, this waveform is not a pure sinusoidal, but contains harmonics. The spectrum on the right shows these harmonics. The three drawings in the center row in Figure 3 are for $\gamma_{\rm NE} = 1$ and $\gamma_{\rm NI} = 0.2$. Here the frequenc is practically the same as in the previous case, although the amplitude and distortion of are $x(t)$ now smaller. On the other hand, the evolution from inside the limit cycle towards the limit cycle itself is much slower. However, the last set of drawings, for $\gamma_{\rm NE} = 1$ and $\gamma_{\rm NI} = 3$, disply, again, practically the same frequency but much larger amplitude and distortion, and a very fast evolution to the limit cycle.

The following observations on the influence of parameters can be made regarding the harmonic oscillator case:

- The oscillation frequency is basically set by $\tau_0 = \sqrt{\tau_x \tau_y}$. The voltage control of this frequency is hence achieved through electronic tuning of the time constants τ_x and τ_y For the LC circuits of Figure 2(b) and (c), the frequency can be made voltage-controlled by resorting to the use of tunable capacitors or inductors (15–24).
- On the one hand, for given values of τ_x, τ_y, $\gamma_{\rm NE}$ and δ, the larger $\gamma_{\rm NI}$, the larger the signal amplitude and the signal distortion. Also, the faster the dynamic evolution towards the limit cycle from the inside. On the other hand, for given values of τ_x, τ_y, γ_{NI} and δ, the smaller γ_{NE}, the smaller the signal distortion, although the speed of the dynamic evolution towards the limit cycle from the inside does not change with γ_{NE}. Finally, the value of δ influence either the signal amplitude, but has no influence on either the signal distortion or the speed of the evolution towards the limit cycle.

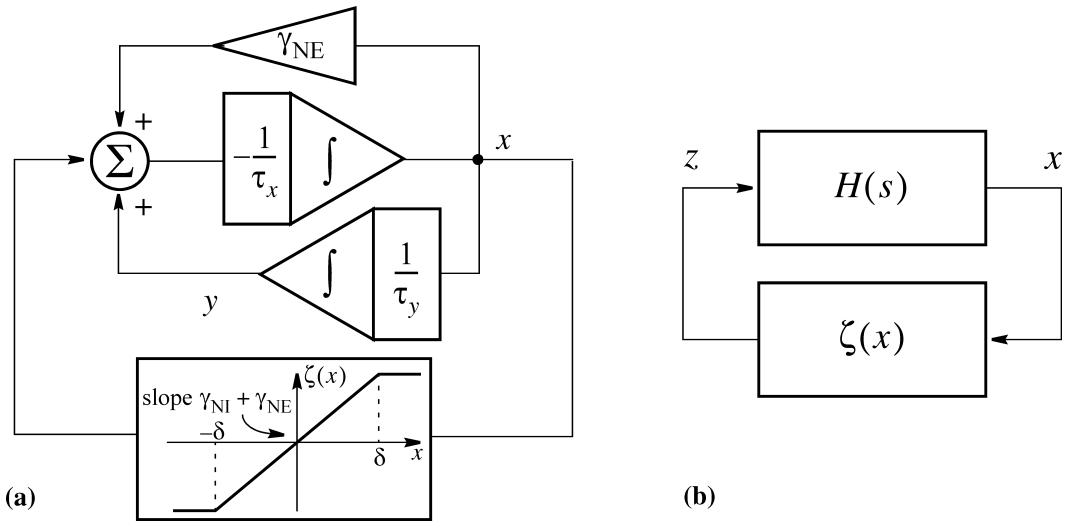

Figure 4. (a) Representation of the basic oscillator model in Figure 2(a) as the interconnection of a linear dynamic block and a nonlinear block and (b) general harmonic oscillator model with these blocks. The phase shift of the linear block is null at the oscillation frequency, and the oscillation occurs at the amplitude for which the loop gain is just unity.

General Harmonic Oscillator Model

Figure 2(a) can be redrawn as depicted in Figure 4(a), consisting of the interconnection of a linear dynamic block with transfer function in the s-domain given by

$$H(s) = \frac{X(s)}{Z(s)} = \frac{s\frac{1}{\tau_x}}{s^2 + s\frac{\gamma_{NE}}{\tau_x} + \frac{1}{\tau_x\tau_y}} \tag{7}$$

and a nonlinear block with transfer characteristics $\zeta(x)$. Note that the linear block acts as a bandpass filter with resonant frequency $\omega_0 \equiv 1/\tau_0$ and quality factor $Q = 1/(\gamma_{NE}\alpha)$.Note also that the gain of this filter at the resonant frequency is $1/\gamma_{NE}$, and that the nonlinear block gains $\gamma_{NE} + \gamma_{NI}$ inside its inner linear region.

Assume $x(t) \approx \rho\cos(\omega t)$. The system can oscillate, provided that the amplitude and the phase of this signal is maintained while the signal is being transmitted across the loop. Consider first the phase. On the one hand, the nonlinearity is static, and does not produce any phase shift. On the other hand, the phase of the linear block is null only for $\omega = \omega_0$ –which is why the oscillation actually happens at this frequency. Consider now the amplitude. On the one hand, for $\rho > \delta$, the loop has a gain of $1 + \gamma_{NI}/\gamma_{NE}$, larger than unity, so that the amplitude grows while the signal transverses the loop. On the other hand, for $\rho > \delta$, the gain is compressed due to the saturation nonlinearity. The compression increases with ρ until a critical amplitude value ρ_0 is reached where the effective gain is unity.

Figure 4(b) shows the block diagram of a generic harmonic oscillator model. Based on the explanations made for Figure 4(a) the following statements are made for this generic model:

- The phase shift of the linear block must be frequency-dependent and null at a single frequency $\omega = \omega_0$, which is the osocillation frequency. The sharper the phase-vs-frequency characteristics of the linear block around this zero-phase frequency, the larger the accuracy of the oscillation frequency setting.
- Consider now the oscillation amplitude. On the one hand, the loop gain at the zero-phase frequency must be larger than unity for low amplitudes. This ensures that the oscillations will start. On the other hand, the compression exercised by the nonlinear block must render the loop gain smaller than unity for large amplitude values. The oscillation occurs at the amplitude for which the compressed loop gain at the zero-phase frequency is just unity.

This can be applied to the *ring oscillator* structure of Figure 5(a)–commonly employed in 10 VCOs. It is composed of N identical stages, Neach with linearized transfer function (22) ,

$$F(s) = \frac{-G_m R}{1 + sRC} \tag{8}$$

connected into a feedback loop. On the one hand, note that each stage produces a phase shift of $\pi - \text{atan}(\omega RC)$; the zero-phase frequency is hence readily calculated as,

$$f_0 = \frac{1}{2\pi RC}\tan\frac{\pi}{2N}\{3 + (-1)^N\} \tag{9}$$

On the other hand, the nonlinearity, and hence the control of the oscillation amplitude, is inherent to the active devices used to realize the transconductors. For the simple circuits typically employed in these transconductors, such as for instance those in Figure 5(b), the transconduc-tance decreases with the signal amplitude. Hence, the condition for the generation of oscillations is $G_m R > 1$.

Relaxation Oscillator Case

It corresponds to α in Eq. (4) atbeing much larger than unity, i.e. to $\tau_x \ll \tau_y$. In the limit, as $\alpha \to \infty$, its factor in the top equation of Eq. (4) becomes negligible and hence,

$$y = -\xi(x) \tag{10}$$

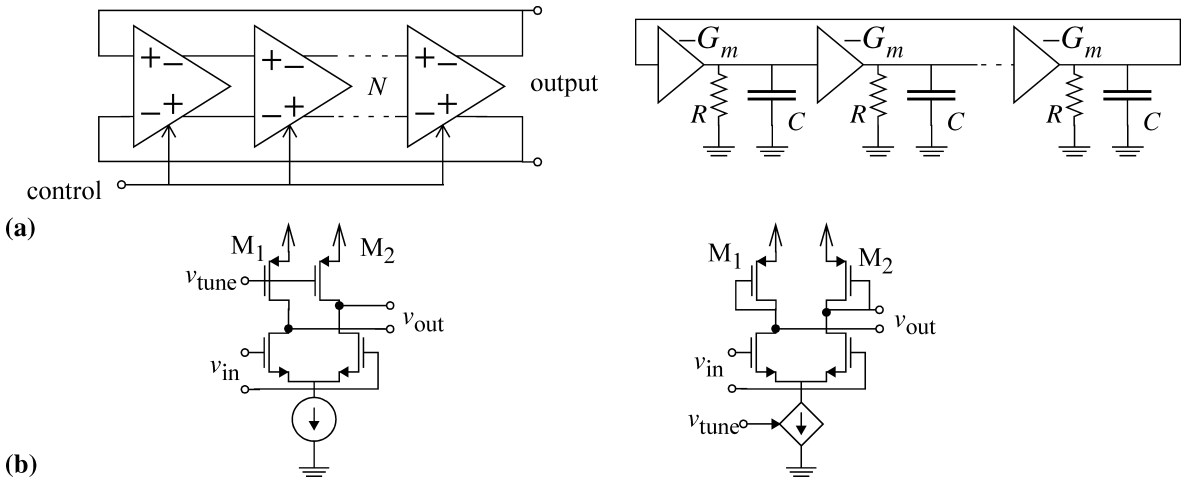

Figure 5. (a) Ring oscillator structure and its linearized model as a specific example of Figure 4. (b) Simple typical circuit realizations for the tunable transconductors.

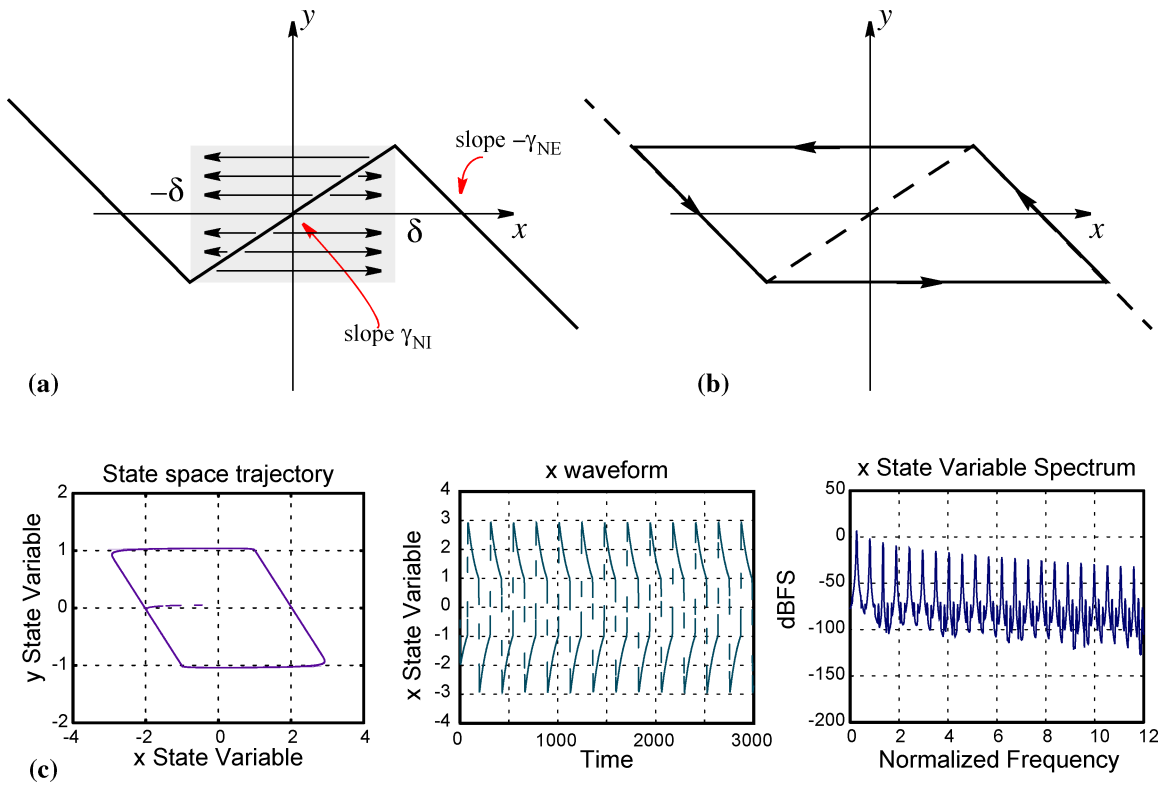

Figure 6. The limit cycle in the relaxation case fits with the nonlinear function $\xi(x)$ in (a) as depicted in (b), where we assume that the horizontal transitions occur instantaneously. The bottom drawing (c) shows the limit cycle, the *x(t)* waveform and its spectrum for $\tau_x = 0.1, \quad \tau_y = 10, \quad \delta = 1$ and $\gamma_{NE} = \gamma_{NI} = 1$.

meaning that the shape of the limit cycle fits with the nonlinear function $-\xi(x)$, drawn with a thick solid trace in Figure 6(a).

This piece of information has to be complemented with the analysis of the solution trajectories of Eq. (4) the different linear pieces of $-\xi(x)$: Let us consider first the inner piece, where $y = \gamma_{NI}x$. Analysis obtains,

$$x(\tau) \approx -\frac{1}{\gamma_{NI}}[y(0) - \gamma_{NI}x(0)]e^{\alpha\gamma_{NI}\tau}$$
$$y(\tau) \approx [y(0)]e^{\alpha\gamma_{NI}\tau} \tag{11}$$

valid for $|x| < \delta$. Note that in the limit, fo $\alpha \to \infty$, $y(\tau)$ remains practically constant while the system evolves in this inner region. Quite on the contrary, *x(t)* changes at very high speed; either decreasing, for $y(0) > \gamma_{NI}x(0)$, or increasing,

for $y(0) < \gamma_{NI}x(0)$. The arrows drawn with thin solid lines in Figure 6(a) indicate the direction and sense of the trajectories in this inner region. From this picture, it is readily inferred that the nonlinearity inner piece is not part of the limit cycle.

Let us now consider the outer pieces, where $y = -\gamma_{NE}x \mp \beta$, where the minus is for the left-hand piece, the plus for the right-hand one, and β is the absolute value of the ordinate at the origin. Analysis obtains a fast transient across a quasi-horizontal trajectory followed by a slow asymptotic behavior whose trajectory is described by

$$\begin{aligned} x(\tau) &\approx -\frac{1}{\gamma_{NE}}[y(0) - (\mp\beta)]e^{(-\frac{1}{\alpha\gamma_{NE}})\tau} \\ x(\tau) &\approx [y(0) - (\mp\beta)]e^{(-\frac{1}{\alpha\gamma_{NE}})\tau} \mp \beta \end{aligned} \tag{12}$$

Note that this slow asymptotic behavior results in trajectories which fit exactly with the corresponding outer piece of the nonlinear function.

As a summary of these considerations, the limit cycle can be built as shown in Figure 6(b), where we assume that the horizontal transitions occur instantaneously. Thus, the oscillation frequency is basically determined by the time invested in making the asymptotic evolutions on the outer pieces of the nonlinearity, which can be calculated from Eq. (12) as

$$T_c = 2\tau_y\gamma_{NE}\ln\frac{\beta + \gamma_{NI}\delta}{\beta - \gamma_{NI}\delta} \tag{13}$$

These summary considerations are confirmed by the simulations depicted in Figure 6(c), which shows the limit cycle, the *x(t)* waveform and its spectrum for $\tau_x = 0.1, \quad \tau_y = 10, \quad \delta = 1$ and $\gamma_{NE} = \gamma_{NI} = 1$.

Let us at this point explore the implications of the conditions leading to the relaxation oscillator case on the LC circuits of Figure 2(b) and (c). These conditions are met by making $C \to 0$ in the former case; and by making $L \to 0$ in the latter. For circuit implementation purposes, these negligible elements can be considered parasitics and, hence, the relaxation oscillator can be built by simply connecting either an inductor or a capacitor to a nonlinear resistor. Figure 7 shows these realizations, where the nonlinear resistor is N-shaped for Figure 7(a), and S-shaped for Figure 7(b).

CONVERTERS BASED ON MULTIVIBRATORS

Since the frequency in oscillators can be controlled by means of tunable capacitors, resistors or inductors, any oscillator can be used to translate a voltage into a frequency, provided that the voltage to be converted is that used to tune the devices (15–24). However, in the case of harmonic oscillators, these mechanisms do not provide a good enough linear dependence of the output frequency on the input voltage nor temperature stability for most voltage-to-frequency applications. They are used instead in PLL (phase locked loops) applications, many allowing nonlinearities up to several tens of percent and temperature induced variations as long as the tuning range accommodates them (23). The jitter in these circuits is also lower than in relaxation oscillators, which make them more appropriate for timing applications (11). Multivibrators have usually poor timing accuracy for frequencies above a few hundred kHzs because of the random fluctuations of the threshold levels and charging and discharging currents and their increasing importance with respect to shorter clock periods (1), but they provide the best linearity and temperature and supply stability at medium-low frequencies, as well as wide control and signal ranges (8). Since the latter are features required for voltage-to-frequency conversion, most VFCs on the market are based on multivibrators, thus we will focus on this approach in the following.

Implementations of VFCs are usually based on capacitors as energy storage elements, and the nonlinear resistor in Figure 7(b) is commonly implemented as depicted in Figure 8(a). The current switches in Figure 8(a) are set to the *Ch* or *Dh* position by the *reversal block,* corresponding to the *charging phase* and the *discharging phase* respectively. During the charging phase, the current i_C enters the capacitor input node (+) and the voltage v_C grows, while it decreases during the discharging phase, wherein the current i_D leaves the capacitor input node. The circuit operation consists in the succession of these two phases in a cyclic behavior. The period of the cycle is determined on the one hand by the value of i_C and i_D and the capacitance C associated to the *timing capacitor,* which set the rate for the voltage v_C to change inside each phase, and on the other hand by the reversal block, which senses v_C and turns the switches to the *Ch* or *Dh* positions. Assuming constant values for the currents i_C and i_D, the time intervals corresponding to the charging and discharging phases are (see Figure 8(c)) ,

$$t_C = \frac{C(v_{CH} - v_{CL})}{i_C} \quad t_D = \frac{C(v_{CH} - v_{CL})}{i_D} \tag{14}$$

where v_{CH} and v_{CL} are the top and bottom limits respectively of the voltage swing in the capacitor terminals. In the specific case of having $i = i_c = i_D$, the time invested in a cycle is

$$T_c = t_C + t_D = \frac{2C(v_{CH} - v_{CL})}{i} \tag{15}$$

where we have supposed that the delay associated with the reversal block and the current switches is negligible, which corresponds to the assumption $\tau_x \ll \tau_y$ in the previous section. Actually, the expression for T_c above is also derived from Eq. (13) by making $\gamma_{NE} \to \infty$,which provides

$$T_c = 4\tau_y\gamma_{NI} \tag{16}$$

for the time invested in completing the cyclic diagram in Figure 8(b) (see also Figure 6). Note that Eq. (16) yields Eq. (15) if γ_{NI} is obtained from Figure 8(a) as

$$\gamma_{NI} = \frac{v_{CH} - v_{CL}}{2iR} \tag{17}$$

and taking into account that $\tau_y = RC$.

The VFCs currently on the market can be classified into two major categories that follow the previous approach, the *Schmitt trigger type converters* and the *charge balancing type converters.* The main difference between both types

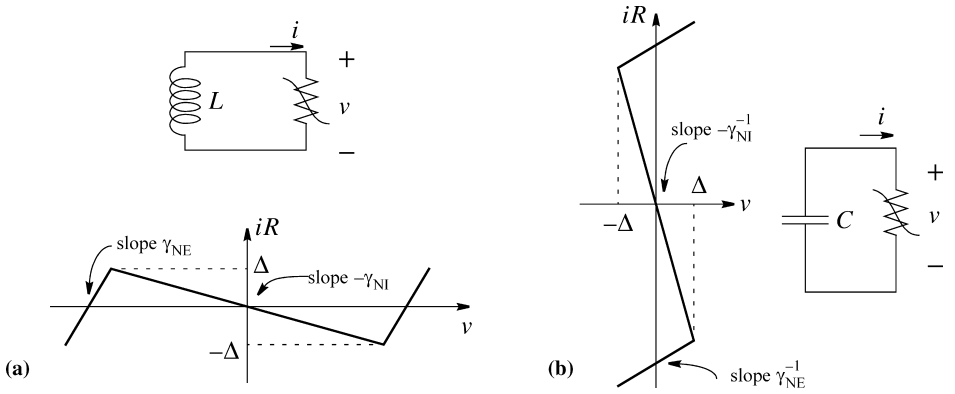

Figure 7. Simplified first-order abstractions for a relaxation oscillator. The conditions leading to the relaxation oscillator case on the LC circuits of Figure 2(b) and Figure 2(c) are met by making C -> 0 in the former case (a) and $L \rightarrow 0$ in the latter (b).

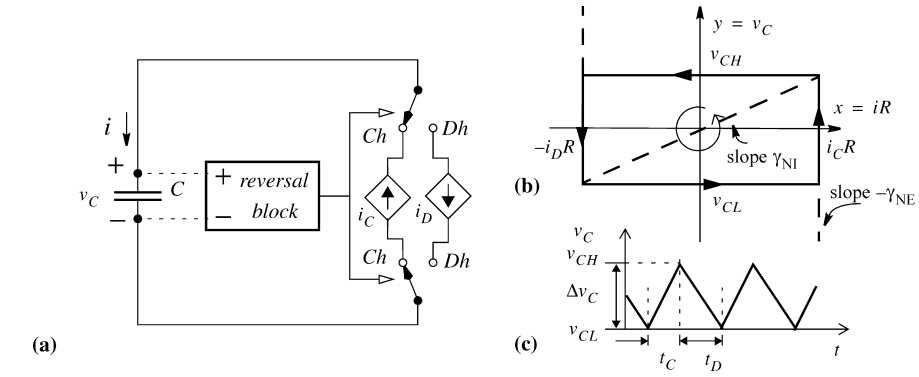

Figure 8. Realization of relaxation oscillators based on Figure 7(b). The reversal block controls the switches to alternatively charge and discharge the capacitor (a). The associated cyclic diagram corresponding to the general case in Figure 6 is shown in (b), while (c) depicts the resultant waveform.

lies in the role that the reversal block plays. In the former, the reversal block works like a Schmitt trigger, which senses $v_C(t)$ and turns the current switch to the position *Ch* or *Dh* any time it reaches the low v_{CL} and high v_{CH} threshold values respectively. Thus, the reversal block imposes the thresholds v_{CH} and v_{CL}, and sets directly the voltage swing $(v_{CH} - v_{CL})$ in the CLacitor during the circuit operation. Eq. (14) applies here and the frequency of the waveform associated to v_C is controlled by means of voltage controlled current sources, thus making $i_C = K_C v_{in}$ and $i_D = K_D v_{in}$ obtain

$$f = \frac{1}{t_C + t_D} = \frac{K_C K_D v_{in}}{(K_C + KD)C(v_{CH} - v_{CL})} \tag{18}$$

where v_{in} is the input voltage that is converted into the frequency f. In the particular case of having $K_C = K_D$, we get a symmetrical triaKC=KDngular shaped periodic signal.

On the other hand, in the charge-balancing type converters, the reversal block does not impose lower and upper limits or thresholds to the voltage drop in the capacitor, but a fixed duration of the charging phase T_0. These circuits also are built to fulfill $i_C = i_0 - i_D$, where i_0 is a constant current. The basic working principles are similar to those in the Schmitt trigger converters, and the circuit evolves in a cycle with successive charging and discharging phases. Let us begin in a certain point inside the discharging phase. The voltage v_C ramps down until it equals a lower threshold v_{CL}. At this time, the switch is turned to *Ch* by the reversal block and the capacitor is charged but now for a fixed period T_0. Thus, the voltage v_C changes an amount given by

$$\Delta v_C = \frac{i_C T_0}{C} = \frac{(i_0 - i_D)T_0}{C} \tag{19}$$

Once this charging phase is concluded, the switch is set to *Dh* by the reversal block and the capacitor is discharged by i_D until the lower threshold is reached again, hence the voltage v_C falls an amount of Δv_C and the duration of this phase is

$$t_D = \frac{C\Delta v_C}{i_D} = (\frac{i_0}{i_D} - 1)T_0 \tag{20}$$

since T_0 and i_0 are constant values, the frequency is changed by tuning i_D in Eq. (20). If $i_D = K_D v_{in}$, we obtain the following expression for the frequency of $v_C(t)$,

$$f = \frac{1}{t_C + t_D} = \frac{i_D}{i_0 T_0} = \frac{K_D v_{in}}{i_0 T_0} \tag{21}$$

In the following we will show implementations of these two classes of converters and we will discuss design issues and non idealities.

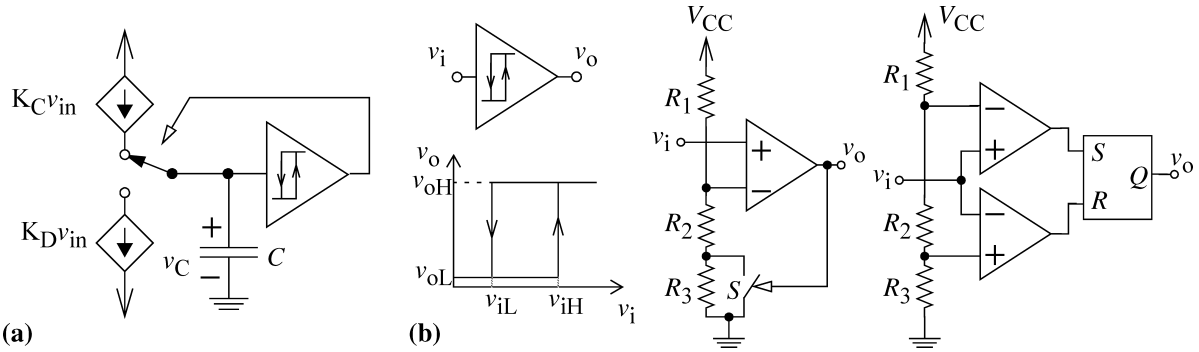

Figure 9. (a) Direct implementation of a Schmitt trigger type VFC converter, where the reversal block in Figure 8 is implemented by a Schmitt trigger circuit.(b) Two realizations of the Schmitt trigger block.

SCHMITT TRIGGER TYPE CONVERTERS

Direct Implementation

Figure 9(a) shows a straightforward implementation of a Schmitt trigger type converter with a grounded capacitor. Two possible realizations of the Schmitt trigger block are also depicted in Figure 9(b) (14). In the single-comparator-type Schmitt trigger on the left of Figure 9(b), for very low values of v_i the comparator output is low and the current switch is open, thus the voltage reference at the inverting input is

$$v_{iH} = V_{CC}\frac{R_2 + R_3}{R_1 + R_2 + R_3} \tag{22}$$

For increasing values of the input voltage, eventually the reference in Eq. (22) is crossed and the comparator output changes and turns the switch on, thus the resistor R_3 is short circuited. Hence, if the input voltage decreases at this point, the new reference voltage at the inverting input of the comparator is

$$v_{iL} = V_{CC}\frac{R_2}{R_1 + R_2} \tag{23}$$

Note that Eq. (22) and Eq. (23) constitute the high and low threshold voltages, respectively, of the single-comparator Schmitt trigger. The main drawback of this circuit is that the parasitic capacitors at the nodes between the resistors have to be charged and discharged every time the switch is closed or opened, which is a time-consuming task and causes errors that limit the high frequency capability of the circuit. A better behavior is obtained by using two comparators and fixed voltage references to define the threshold values. The right part of Figure 9(b) shows the dual-comparator Schmitt trigger which is based on this approach and whose threshold voltages are determined by the resistor ladder as

$$v_{iL} = V_{CC}\frac{R_3}{R_1 + R_2 + R_3} \quad v_{iH} = V_{CC}\frac{R_2 + R_3}{R_1 + R_2 + R_3} \tag{24}$$

Besides other general limitations that will be seen later, the basic disadvantage of this strategy is the poor supply voltage stability, due to the dependence of the threshold values on V_{CC}. Table 1 shows the typical performance parameters associated to the NE566[4], which follows the direct approach in Figure 9(a) and whose maximum drift with supply voltage is 2%/V.

Emitter-coupled multivibrator

Instead of a grounded capacitor, the circuit in Figure 10 uses a floating one which is charged and discharged by means of the bias current sources i_C and i_D. Basically, the circuit fixes the voltage at one terminal of the capacitor, for instance, the emitter of Q_3, to a nearly constant voltage V_M, while the other terminal is connected to the current source i_C that charges it. Eventually, the voltage in the latter drops enough to allow the base-to-emitter voltage of Q_2 to reach the transistor threshold, which causes the voltage at the base of Q_3 to fall and the transistor is turned off. The voltage at the emitter of Q_2 is now fixed to two base-to-emitter drops below the supply voltage and the capacitor is being discharged by i_D. Since the circuit is symmetrical, the process is repeated periodically. Let us split the cycle in periods related to important events in order to derive the expression of the output wave frequency:

- Figure 10(b) shows the circuit working somewhere in the cycle with the transistor $Q_2$and the diode D_1 in the cut-off region, which is indicated by using a white trace. Consider the clamping block in Figure 10(a) formed by one diode and one resistor in parallel. The voltage drop across this block is depicted in Figure 10(a), as well as the response to a step in the current I_D. As long as Q_2 is off, the voltage across the block equals zero if we neglect the base and leakage currents. Since Q_1 and Q_3 are on, the voltage at node B is clamped to $V_M = V_{CC} - 2\,V_{B\,Eon}$ approximately. On the other hand, the current source i_C is charging the capacitor with a constant current, thus the voltage at the emitter of Q_2 falls to a lower threshold V_L beyond which Q_2 is not longer cut-off. Since D_2 and Q_4 are on, such a limit is given by the equation,

$$V_L = V_{CC} - (V_{D2} + V_{BEQ4} + V_{BEQ2}) \approx V_{CC} - 3\,V_{B\,Eon} \tag{25}$$

- Once the voltage at node A reaches V_L, the transistor Q_2 turns on and its collector current makes the voltage drop across the left clamping block rise to V_{BEcon}, thus the base of Q_1 drops to $V_{CC} - V_{B\,Eon}$ and the emitter of Q_1 follows this voltage, hence the voltage at the base of Q_3 is now $V_{CC} - 2V_{B\,Eon}$. Since its emitter was fixed

Table 1. Typical performance parameters of the NE566

Maximum operating frequency	1MHz
Sweep range	10:1
Frequency drift with supply voltage	0.2 %/V
Frequency drift with temperature	600 ppm/°C
FM distortion (±10%deviation)	0.4%

Table 2. Typical performance parameters of the AD537 JD

Frequency range	0kHz to 150kHz
Nonlinearity ($f$max = 100kHz)	0.15%
Error drift with temperature (0° to 70°C)	50 ppm/°C
Error drift with supply voltage ($f$max < 100kHz)	0.01%/V

Table 3. Typical performance parameters of the AD VFC32KN

Frequency range	0kHz to 500kHz
Nonlinearity ($f$max = 500kHz)	0.05%
Error drift with temperature (0° to 70°C)	75 ppm/°C
Error drift with supply voltage (max)	0.015% of FSR%

Table 4. Typical performance parameters of the AD652 JP

Gain Temperature Coefficient	
fCLOCK = 200kHz	± 25ppm/°C
fCLOCK = 4MHz	± 25ppm/°C
Linearity Error	
fCLOCK = 200kHz	± 0.002%
fCLOCK = 4MHz	± 0.02%
Power Supply Rejection Ratio	0.001 %/V

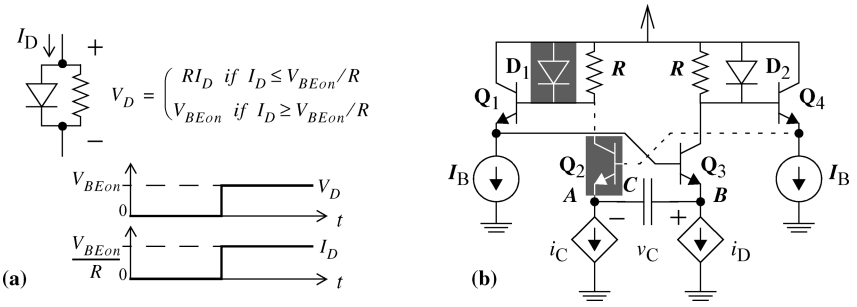

Figure 10. Emitter-coupled multivibrator. The clamping block in (a) causes a voltage drop of value V_{BEon} for a current $I_D \ge V_{BEon}/R$, that makes the basis voltage of Q_2 fall, thus it is cut-off and the capacitor is charged through . The situation reiCmains until the voltage drop at the emitter of Q_2 is low enough to turn on Q_2, thus the clamping block at the top-left corner cuts-off Q_3 and the situation is reversed. The process is repeated cyclically.

to the same voltage, the transistor Q_3 turns off. Note that at this point, the voltage drop across the capacitor is $V_C = V_B - V_A = V_{BEon}$

- Since Q_3 is cut off, its collector current vanishes and the voltage drop across the right clamping block goes down to zero. As a consequence, the voltage at node A is pulled up to the value $V_{CC} - 2V_{BEon}$. On the other hand, since the switching time is very short, the capacitor remains charged and the voltage increment is translated into an increment in the voltage at node B, which reaches the value,

$$V_H = V_{CC} - V_{BEon} \tag{26}$$

- Note that the situation is symmetrical to that in the first point, but now the voltage at nodeA remains constant while the current source i_D discharges the capacitor, which is equivalent to the initial point above.

From the previous discussion we conclude that in each charging or discharging phase, the voltage at one capacitor terminal A or B remains constant, while the other changes from the voltage V_H to V_L. It is then easy to derive the voltage increment in the capacitor,

$$\Delta v_C = v_{CH} - v_{CL} = (V_H - V_M) - (V_L - V_M) = 2V_{BEon} \tag{27}$$

Since the problem is equivalent to that treated in the previous section, equation Eq. (18) is also valid here and the

frequency of oscillation is given by the expression,

$$f = \frac{K v_{in}}{4CV_{BEon}} \tag{28}$$

where K_C=K_D=K.

Improved emitter-coupled multivibrator

Since the base-to-emitter voltage has a strong temperature coefficient, the circuit in Figure 10 has as a main drawback the dependence of Eq. (28) on the temperature. One strategy to compensate this dependence consists of making that the current that charges and discharges the capacitor is dependent on the temperature for cancelling the global dependence (14). Such an approach achieves circuits whose output frequency does not change with the temperature for v_{in}=0, while there is a dependence for values of v_{in} different from zero. Another strategy tries to make $\Delta v_C = v_{CH} - v_{CL}$ equal to a quantity very stable under temperature variations. That is the strategy followed in the circuit of Figure 11, which basically works in the same way as the previous one in Figure 10. The main difference consists in the change of the voltage values used to clamp the collectors of Q_1 and Q_2. For this purpose, the simple diodes in Figure 10 are substituted by a more complex circuitry depicted at the top of Figure 11. In addition to the current sources, the circuit uses two reference voltages to implement the strategy: a very stable voltage reference V_R, and the reference voltage $V_{CC} - 2V_{BEon}$ generated by D_5 and D_6. In addition, one diode bridge derives the voltages at the collectors of Q_1 and Q_2 from these references. Figure 11 illustrates the same situation as in Figure 10, where Q_1 was cut-off, the voltage at node B was fixed, and the capacitor was being charged by i_C. The same process is going on now in Figure 11 where the devices in white are off, but the voltages at the collectors of Q_1 and $Q_2$are set to $V_{CC} - V_{BEon}$ and $V_{CC} - V_R - V_{BEon}$, respectively, by the above referred top circuitry. Taking into account the voltage drops across the emitter followers as well as that in Q_2, the voltage at B is

$$V_M = V_{CC} - 3\,V_{BEon} \tag{29}$$

and the voltage atA beyond which Q_1 is not off anymore is

$$V_L = V_{CC} - V_R - 3\,V_{BEon} \tag{30}$$

When this limit is reached, the situation is reversed, Q_1 is turned on and Q_2 is turned off. At this point, the voltage across the capacitor is $v_C = V_B - V_A = V_M - V_L = V_R$, and the final voltage at B after the switching will be

$$V_H = V_M + V_R = V_{CC} - 3V_{BEon} + V_R \tag{31}$$

Now from Eqs. (29), (30) and (31) $\Delta v_C = v_{CH} - v_{CL} = (V_H - V_M) - (V_L - V_M) = 2V_R$ and Eq. (18) reduces to

$$f = \frac{K\,V_{in}}{4CV_R} \tag{32}$$

The frequency of oscillation can now be stable if V_R is designed carefully to have a low temperature coefficient, which is described later. Table 2 shows some typical parameters of the AD537JD (2). The data refer to the current-to-frequency converter block without taking into account the deviations introduced by the voltage-to-current converter at input.

The other major class of commercial voltage-to-frequency converters are based on a charge balancing system. As said in Section 3, these circuits are characterized by having a fixed length in time in the charging phase. We can classify them into two major categories, those based on one-shot timers and those which are synchronized to a clock signal.

Charge balancing converters based on one-shot timers

Figure 12 illustrates a typical implementation of these converters, whose working principle we now describe. Suppose that $v_C \le v_{in}$, then the comparator provides a high output. As a consequence, the one-shot timer output rises and the current switch is set to the *Ch* position. This behavior of the one-shot continues under the start-up conditions or in the case of a change in the input voltage, and the frequency of the timer output signal is zero. Once the condition $v_C > v_{in}$ is reached, the one-shot is reset and the current switch is set to the *Dh* position, thus the capacitor is discharged through R. However, as soon as the condition $v_C \le v_{in}$ is fulfilled again, the timer is triggered and the switch is turned to *Ch* again to allow the current flow into the integrator. This time the one-shot timer operates as usual and generates a pulse of fixed duration t_{os}, thus a packet of charge is injected in the RC integrator and v_C ramps upward by an amount

$$\Delta v_C = t_{os}\frac{dv_c}{dt} = t_{os}\frac{(i_0 - i_D)}{C} \tag{33}$$

which is enough to make $v_C > v_{in}$, thus the one-shot is reset and the capacitor is discharged again until v_C reaches v_{in}. If $\Delta v_C \ll v_C$, we can approximate $i_D \approx v_{in}/R$, which is a constant current that discharges C, thus the time t_D is given by

$$t_D \approx \frac{|\Delta v_C|}{|\frac{dv_C}{dt}|} = \frac{t_{os}((i_0 - i_D)/C)}{\frac{i_D}{C}} = t_{os}(\frac{i_0 R}{v_{in}} - 1) \tag{34}$$

The cycle is repeated again as soon as v_C equals v_{in}, thus the output of the one-shot timer is a periodic signal whose frequency is

$$f = \frac{1}{t_{os} + t_D} = \frac{v_{in}}{t_{os} i_0 R} \tag{35}$$

Note that this coincides with Eq. (21) for $K_D = 1/R$ and $T_0 = t_{os}$. The circuit in Figure 12 has two main drawbacks. First, the change of v_C causes an error in the charging current due to the finite output impedance of the current source that generates it, as well as in the discharging current i_D, which is not constant as supposed above. Second, the passive RC integrator is very slow, especially for large input voltage changes, which require a large amount of charge to be injected in or extracted from the capacitor. Both aspects can be improved by using an active integrator, as Figure 13 depicts (3–27). The negative feedback provides low impedance at the inverting input terminal of the integrator, whose voltage remains nearly constant, thus the error in the charging and discharging currents is reduced. Equations Eq. (33)-Eq. (35) are valid in Figure 13(b), but now $i_D = v_{in}/R$ 'exactly'. With respect to Figure 13(a), v_C

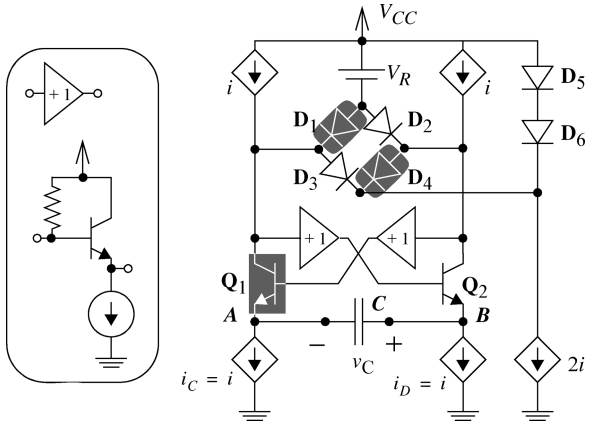

Figure 11. Improved emitter-coupled multivibrator. The clamping circuitry is redesigned to make the voltage variations at the capacitor depend on a voltage (V_R) very stable against temperature changes, thus the frequency drift with temperature is improved.

V. Charge balancing type converters

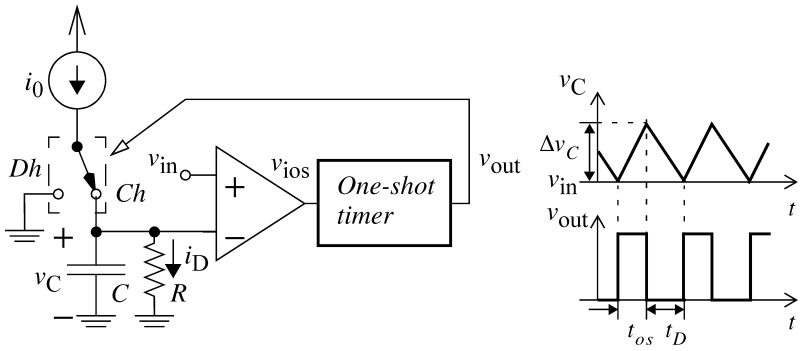

Figure 12. Basic diagram of a charge-balancing converter based on a one-shot timer. The charging phase has fixed length in time, which is the width of the pulse generated by the one-shot timer (t_{os}) when it is triggered by the comparator. For $\Delta v_C \ll v_C$, the average voltage at the comparator inverting input is v_{in}, thus $i_D \approx v_{in}/R$. The average current injected in the bottom integrator must equal i_D and depends on the rate the one-shot is triggered with, hence this rate depends on v_{in}.

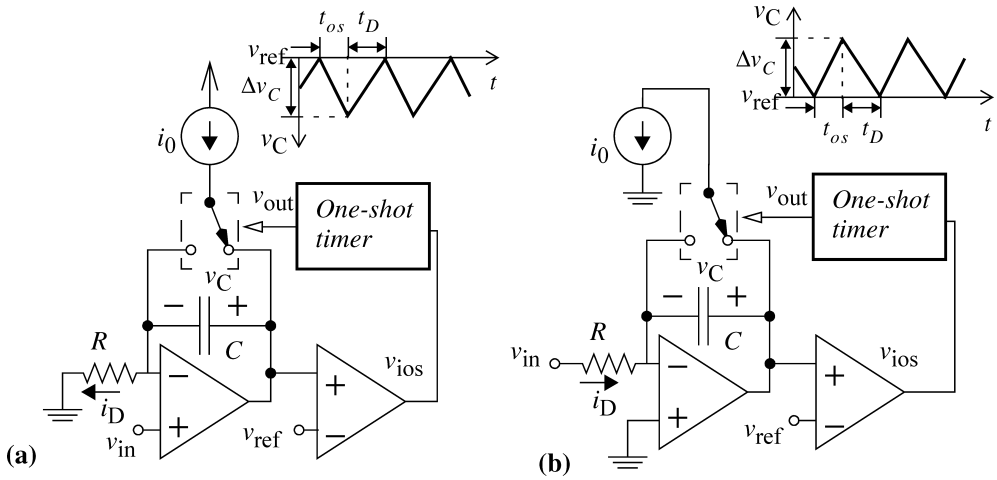

Figure 13. Improved converters based on one-shot timers. The use of active integrators instead of the passive one in Figure 12 achieves smaller errors and improves the dynamic response.

diminishes in the reset mode, thus the derivative in Eq. (33) is negative, as is the voltage increment, but Eq. (34) and Eq. (35) are valid. In both cases, the output current of the op amp in the integrator is the same for the charging and the discharging modes, which improves the dynamic response because this minimizes the transients. In addition, Figure 13(a) provides high impedance for the input terminal, which can be useful for applications with low load requirements. Finally, note that the capacitance of the integrating capacitor does not appear in Eq. (35), thus it

does not influence directly the output frequency. However, it certainly influences the shape of $v_C(t)$, because if C is too small, Δv_C in Eq. (33) could become too large and exceed the linear range of the integrator. In (16), a nonlinearity error of ± 0.024% FS (f= 10Hz to 11 kHz) is reported for the approach in Figure 12, while it is reduced to 0.006% FS for the improved converter in Figure 13(b).

The input voltage offset V_{off} of the comparator in Figure 12 and the integrators in Figure 13 introduces an error $\varepsilon_f = |\frac{V_{off}}{t_{os} i_0 R}|$ in the expected off frequency - an effect that can be significant, especially for low frequencies, in terms of relative error. On the other hand, precision and low temperature coefficient current sources to derive i_o are generated on-chip by means of a voltage band-gap reference and a precision voltage-to-current conversion circuit (see Section 7), while further reflections and replications should also be carried out by cascode current mirrors. Nevertheless, accuracy as well as high frequency capability of these converters is primarily determined by the precision of the one-shot section.

Figure 14 shows the simplest form of an exponential-ramp-type one-shot timer (14). The principle of operation is as follows. As long as the flip-flop is reset (low input), the voltage at the output $\overline{Q}$ is high and the current switch (which can be implemented in the simplest way by a grounded transistor) is open, thus the voltage drop in the capacitor is zero. If the circuit is triggered by a high input, the outputs Q and $\overline{Q}$ of the flip-flop are set to a high and a low voltage respectively, thus the switch is turned off and the capacitor is charged through R, and v_{Cos} grows exponentially with a time constant of RC_{os}. However, as soon as the reference voltage at the non-inverting input (which is determined by the voltage divider formed by R_a and R_b) is reached, the comparator output changes to a low voltage value and the flip-flop is reset, hence the switch is closed and the capacitor is discharged quickly. Simple calculations on the circuit formed by the supply voltage source, R and C_{os} provides

$$t_{os} = RC_{os}\ln(1 + \frac{R_b}{R_a}) \tag{36}$$

The voltage divider formed by R_a and R_b is usually implemented on-chip and the accuracy obtained for the ratio R_b/R_a is within ±1%, and does not depe±1nd on the temperature. Thus, the precision, as well as the temperature stability in the expected t_{os} are mainly determined by the resistor R and the capacitor. However, for small values of t_{os}, the time delays in the input comparator, the flip-flop and the switch limit the accuracy. In addition, for low frequencies the leakage currents in the capacitor and the switch introduce an error in the timing prediction.

Table 3 shows some typical performance parameters of the monolithic converter ADVFC32KN (4).

Synchronized charge balancing type converters

Further improvements can be achieved by replacing the one-shot timer by circuitry clocked by a precise oscillator, usually a crystal one, which determines the charging phase duration (5). Figure 15 shows the circuit which results from substituting the one-shot timer with a block composed of one bistable and one AND logic gate, which works as follows. If the integrator output crosses the threshold v_{ref}, the comparator places a high value at the bistable input (suppose that $\overline{Q}$ is high). However, the output does not follow it immediately as in Figure 13(b), but it is synchronized with the clock by the flip-flop and changes at the next clock rising edge. At the same time, the output complement (low value) is put at the flip-flop input by the feed-back loop, thus the output will go back down at the next rising edge of the clock and the duration of the output pulse is just one clock cycle. Note that the circuit operates in the charging phase as long as the output is high, thus T_{CLK} replaces t_{os} in the equations Eq. (33), Eq. (34) and Eq. (35), which remain valid. However, since the output is now synchronized, its frequency must be a multiple of the clock frequency ,

$$f = \frac{1}{T_{CLK} + T_{CLK} \times i_S(\frac{t_D}{T_{CLK}})} = \frac{1}{T_{CLK}[1 + i_S(\frac{i_0 R}{v_{in}} - 1)]} \tag{37}$$

where i_s in Eq. (37) means the next superior integer of the argument. Table 4 shows some typical performance parameters of the synchronized converter AD652JP(5).

In addition to other design issues that will be discussed in the next section, Figure 15 has a specific problem to solve due to the lack of synchronism between the input voltage and the clock. The latter could cause that the comparator output changes at the same time as the clock arrives at the D flip-flop. Since the latter are usually designed to work synchronously, a setup time must be respected for the input signal to change before the clock edge, otherwise there could be metastability problems that do not guarantee a correct value of the flop output, thus t_C can be shorter or larger and the circuit does not work properly. Is it possible to avoid this problem by building the D flip-flop with two flip-flops in cascade or with a flip-flop and a latch in cascade (5), like the right part of Figure 15 shows, where the clock edge for both flops is delayed. The simplest way to have delayed edges for both flops consists in using the clock falling edge to trigger the first flip-flop, while the second flop is triggered by the rising edge, thus they are delayed half a clock cycle. With this strategy, the metastability of the first flip-flop has ended by the time the second flip-flop is clocked, and the pulse width of the output is a clock cycle, thus there is not error in t_C.

Sigma-delta modulators

Figure 16 shows a first-order sigma-delta modulator. It basically consists in a loop with a 1-bit analog to digital converter, which is the latched comparator, and a 1-bit digital to analog converter in the feedback path. Provided the loop has enough gain, the difference between the analog input and the D/A converter output is minimized and the average value of the D/A output must approach that of the input signal. Similarly, the averaging of the comparator output provides a digital word that represents the analog input. This averaging is described later as part of the processing required to obtain a digital word from the frequency output of a VFC (digital processing in Section 7), thus sigma-delta modulators can be viewed as synchronized charge-balancing voltage to frequency converters (the charge is injected into or removed from the integrator for the DAC

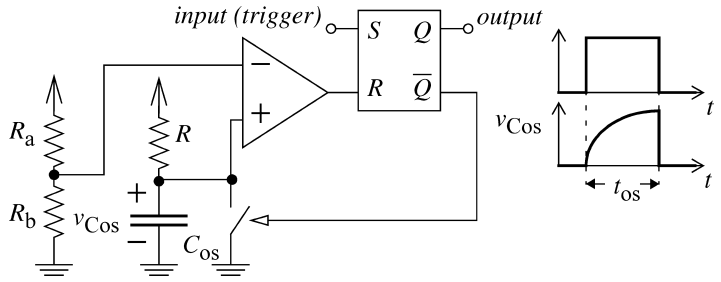

Figure 14. Exponential-ramp-type one-shot timer

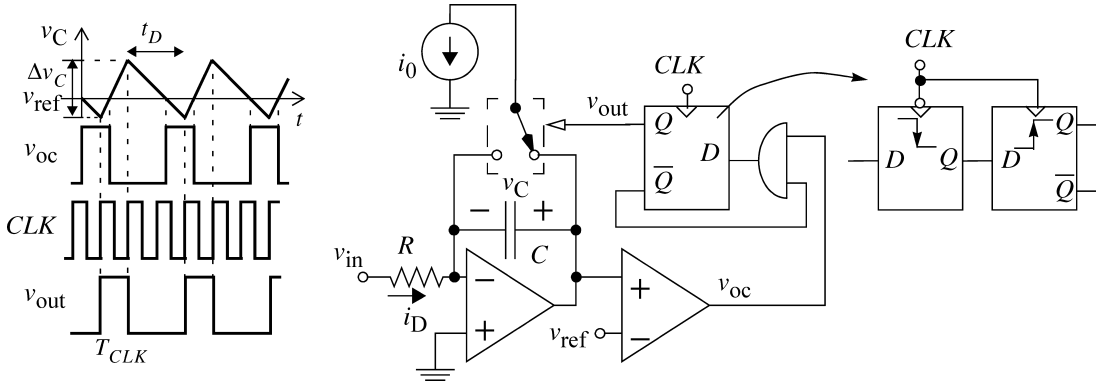

Figure 15. Synchronized charge balancing converter. The one-shot timer is replaced by externally clocked circuitry. The charging phase length is now fixed by the clock period, which is supposed very accurate.

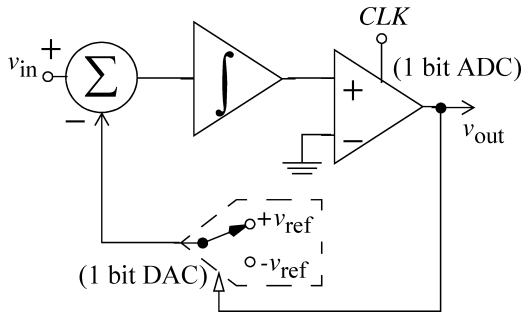

Figure 16. Sigma-delta modulator as synchronized charge-balancing voltage to frequency converter.

output to track the input voltage). In fact, the transfer function of the AD7740 (6) is $f = 0.1\ f_{CLK} + 0.8(v_{in}/v_{ref})\ f_{CLK}$.

Since sigma-delta modulators can be built currently with cheap CMOS technology, the main advantage of this approach is the cost. The AD7741 (7) with 0.012% Nonlinearity at 2.75MHz of FoutMax costs five times less than the synchronous AD652 with 0.02% Nonlinearity at 2MHz of FoutMax. In addition, they need fewer external components.

DESIGN ISSUES AND LIMITATIONS OF CONVERTERS BASED ON MULTIVIBRATORS

Although some design aspects relative to the design and non-idealities have already been discussed in previous sections, for more clarity, some others regarding all the converters based on relaxation oscillators are examined here. Specifically, note that Eq. (15) and Eq. (18) have been derived without taking into account the deviations from the ideal case. Let us now show some real implementations of formerly ideal blocks and discuss deviations from the ideal case and their consequences in the output wave shape.

Implementation of the Voltage Controlled Current Sources

Many VFCs described above use voltage controlled current sources to implement the charging and discharging currents in Figure 8, where $i_C = K_C v_{in}$ and $i_D = K_D v_{in}$. such proportional relationship is obtained readily with a resistor, but a transistor is needed to isolate the control node from the output, which is depicted in Figure 17(a). Such a circuit provides the reference current ,

$$i_{ref} = \frac{v_{in} - v_{BEon}}{R} - i_B \tag{38}$$

which acts as charging or discharging current. However, note that this circuit provides a current that is not proportional to v_{in}, but contains an offset that equals $-(v_{BEon}/R +$

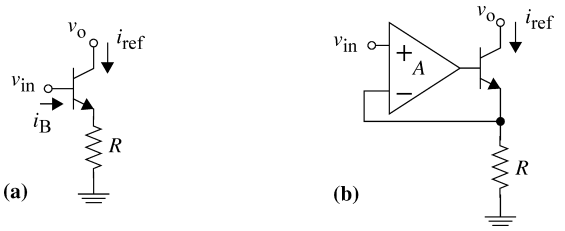

Figure 17. Controlled current source implementation

i_B). Besides modifying the intended proportional relationship, the added term has a strong temperature coefficient, since the base to emitter voltage varies with the temperature as -2mV/°C.

A common alternative for eliminating the dependence of $i_{\rm ref}$ on $V_{\rm BEon}$ places the transistor in a negative feedback loop as Figure 17(b) illustrates. If we neglect the base current, the output reference current for this circuit is

$$i_{ref} = \frac{A}{(A+1)R}\, v_{in} - \frac{v_{BEon}}{(A+1)R} \tag{39}$$

Note that for $A \gg 1$ the term depending on $V_{\rm BEon}$ vanishes and the reference current equals

$$i_{ref} \approx \frac{v_{in}}{R} \tag{40}$$

which is proportional to $v_{\rm in}$. The higher the value of the input amplifierA, the larger the accuracy of Eq. (40). In addition, a MOS transistor can replace the bipolar one in Figure 17(b) to reduce the error introduced by neglecting the base current, due to the high impedance associated to the gate of MOS transistors.

Finite output resistance of the constant currents

The current source depicted in Figure 17(b) still has a non-ideal behavior that can introduce deviations in the expected output current. Specifically, since the collector current depends on the collector-to-emitter voltage drop because of the B JT base length modulation, the current $i_{\rm ref}$ varies with v_o and this causes an error if the output node directly drives the terminals of the capacitor in Figure 8, because the voltage drop in the capacitor changes as a consequence of the circuit operation. We can model this dependence on the output node voltage by means of a resistor in parallel with an ideal current source whose value is the expected one. This is illustrated in Figure 18, where the Thevenin equivalent is also depicted. If the circuit is now connected to the timing capacitor, the voltage v_C does not follow a linear behavior with *t,* but a well-known exponential behavior. As a consequence, the time to charge or discharge the capacitor an amount Δv_C is longer than expected, which is indicated in Figure 18(a) by means of the error ε_t. For the circuits described above, this means longer periods or lower frequencies than those in the ideal case. In order to improve the output impedance of the current source, several cascode configurations have been reported (13). Some usual ones are depicted in Figure 18(b), where the current i '$_{\rm ref}$ equals $i_{\rm ref}$, but the output resistance the circuit in Figure 17.

Dependence of the Frequency on Temperature and Voltage Supply Variations

The temperature stability of the converter output frequency depends on many factors, some of which have already been discussed above. First, in order to improve the temperature stability we should avoid circuits like that in Figure 10 whose output frequency depends directly on parameters like $V_{\rm BEon}$ that has a large temperature coefficient. Other circuits described above must still be designed carefully to avoid drift.

First, voltage references and charging currents have a large influence on the temperature stability. For instance, the voltage source $V_{\rm R}$ in the equation Eq. (32) must be designed to compensate the temperature dependence. Figure 19(a) shows an example circuit able to generate a reference voltage $V_{\rm R}$ with a low temperature coefficient (13). Such a circuit takes advantage of the different sign of the temperature coefficients associated to the voltage-to-emitter drop in a BJT and the thermal voltage $V_{\rm T}$. The box in Figure 19(b) encloses a circuit able to generate a current that is proportional to $V_{\rm T}$. As long as the voltage at both output terminals A_1 and A_2 is the same, i.e. $V_{A1} = V_{A2}$, the current I_2 is given by the equation

$$I_2 = \frac{(V_{BEQ1} - V_{BEQ2})}{R_2} = \frac{V_T}{R_2}\ln(\frac{nI_1}{I_2}) \tag{41}$$

Two possible approaches to force $V_{\rm A1}$=$V_{\rm A2}$ are illustrated in Figure 19(b). The circuit at the top of Figure 19(b) uses a negative feedback loop with an operational amplifier that ensures zero differential input, thus $V_{\rm A}1$=$V_{\rm A2}$. Taking into account that the voltage drop across resistors *R1* and $\rm R_3$ is the same, we can derive the following expression for $V_{\rm R}$ in Figure 19(b)

$$V_R = V_{BEQ1} + \frac{R_3 V_T}{R_2}\ln(\frac{nR_3}{R_1}) \tag{42}$$

Another strategy uses cascode transistors to get $V_{\rm A}1$=$V_{\rm A2}$. This is the approach followed by the circuit at the bottom of Figure 19(b), where the reference voltage is

$$V_R = V_{BEQ3} + \frac{R_3 V_T}{R_2}\ln(n) \tag{43}$$

The reference voltage in Eq. (42) and Eq. (43) is made independent of the temperature variations by choosing properly the circuit and device parameters to achieve $\frac{dV_R}{dT}\,|_{T=T_0} = 0$ (see (13) for more details).

On the other hand, stable current sources can be obtained by driving the circuit in Figure 17(b) with a stable voltage source like that in Fig. 19, which is the strategy followed by many commercial VFCs like the AD537(2).

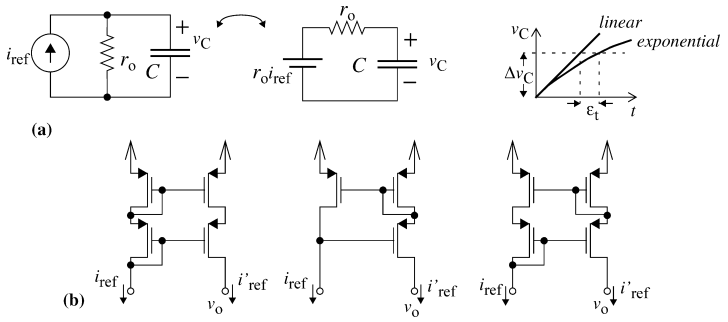

Figure 18. Current source finite output resistance: timing error (a) and common cascode strategies to increase the output resistance (b).

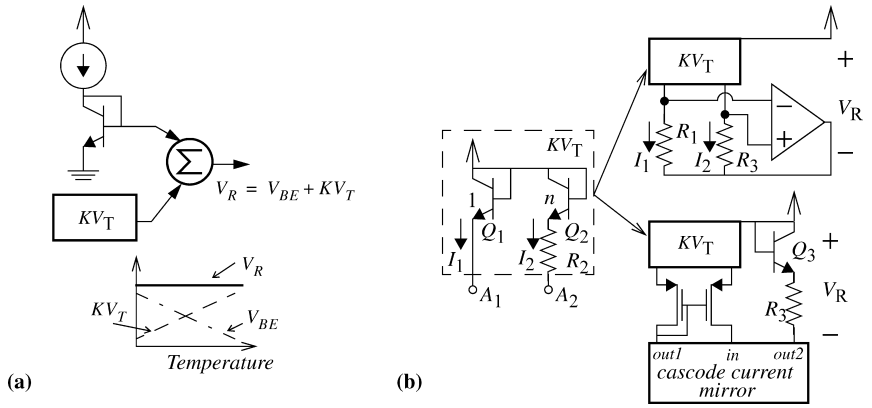

Figure 19. Band-gap reference voltage. (a) The voltages V_{BE} and V_{T} have temperature VTcoefficients of opposite sign, thus they compensate the global dependence of V_{R} .(b) Two realizations of this approachVR.

Another element that affects the temperature stability is the dependence on the temperature of the Schmitt trigger thresholds, specifically that of the difference $\Delta v_C = v_{CH} - v_{CL}$ in Eq. (15). We have already discussed the particular case of the emitter-coupled circuit in Figure 11. With regard to the direct implementation in Figure 9, the reference voltages and the comparator offsets are the main sources of drift. Contributions to global drift are in both cases a few tens of ppm◦/C.

In the case of the charge-balancing converters, note that Δv_C is determined mainly by the charging and discharging currents and by the parameter T_0 in Eq. (21). The drift of T_0 in converters based on one-shot timers is due mainly to the resistance R and the capacitance C_{os} in Eq. (36) and Figure 14, which are usually external in most commercial VFCs. Finally, the stability of $\mathrm{T}_0$is obviously improved when such a parameter is determined by a precise external clock as in the synchronous converters.

On the other hand, frequency drift with the supply voltage is also mainly due to variations of the charging and discharging currents as well as that of Δv_C. Band-gap references like those described above also provide supply independent biasing.

Finite Sensing Node Impedance and Leakage Currents

Note that Figure 8 assumes infinite impedance in the reversal block sensing input nodes. Real implementations however do not usually present such a feature. Specifically, if the reversal block is built with bipolar transistors in the input stage, bias currents have to be provided from the input to the sensing nodes. Such currents are usually in the range of a few hundred nano-amperes and add to or subtract from charging and discharging currents. MOS transistors can be used instead, to implement almost infinite input impedance thanks to the isolation provided by the gate oxide. In addition, junction leakage or dielectric absorption currents can also be added to or subtracted from charging currents, thus also affecting the output frequency. However, these currents are commonly at a low nanoampere range. Hence, errors due to these base and leakage currents can be usually tolerated as long as the charging and discharging currents are in the range of $\geq 10\mu A$ (14).

Finite Switching Times

The switching times in Figure 8 have been neglected in the computation of the output frequency in Eq. (18). However, they are not zero in real implementations and limit the frequency capability of the converter. The elements that contribute to the delay in switching are mainly the length of the feedback path and the delays of the blocks along it, while the gain of the active devices, the parasitic capacitances and the internal current levels determine such delays.

Output Interfacing

The output stage of the commercial VFCs is designed to allow easy interfacing to all digital logic families. Hence, BJT open collector or both uncommitted collector and emit-

ter interfaces are provided. External pull-up resistors and proper biasing complete the interface and determine the rise times and output logic levels that are adequate for each specific application. Internally, some interface circuitry is needed to drive the base of the output BJT for circuits like that on the right of Figure 11 (2), while it is not necessary in one-shot based converters like those in (3, 25), whose one-shot output drives it directly. Synchronous converters also may use a one-shot timer to drive the output transistor, which allows the pulse width of the frequency output to be controlled by means of an external capacitor.

External Component Selection

Timing capacitors in the converters described above, as well as resistors in Figs. 12,14 and 15 are usually external components in commercially available VFCs. Special care must be taken to select these components in order to preserve performance. High linearity and low temperature coefficients for the resistors and the capacitors are required. In addition, the latter should not leak, since dielectric absorption can affect the linearity and offset of the transfer function.

FREQUENCY TO VOLTAGE CONVERSION

The complementary operation of that carried out by the voltage to frequency converters is the frequency to voltage conversion, which is performed by the $\underline{F}requency - to - \underline{V}oltage\underline{C}onverters$ (FVCs). This task can be often implemented by the same ICs that perform the V/F conversion, and it is applicable in areas like telemetry, motor speed control, as well as to build interfaces for sensors whose output is in the form of a variable frequency or pulse train (14, 19). Figure 20(a) shows how this conversion can be accomplished by means of an integrator and a current switch that is driven by the frequency signal in the so called pulse integrating FVCs. The switch can also be driven by the output of a one-shot timer (see Figure 20(a)), which reduces the integration time, thus allowing small increments in the output voltage without needing too large capacitors. The average output voltage in Figure 20(a) can be calculated by taking into account that in the steady state the whole current will flow through the resistor R thus

$$v_{out} = -Ri_0 t_{os}\ f_{in} \tag{44}$$

where $i_0 t_{os} f_{\rm in}$ is the average current injected by thi0tosfine top current source in the integrator. A simpler passive integrator could be used instead of the active one in Figure 20(a), but the latter reduces the error caused by the finite output impedance of the current source (this can also be accomplished by means of cascode transistors (20)) and speeds up the converter response time.

Since the current is injected in the integrator in packets of size $i_0 t_{\rm Os}$, the output voltage has an ac ripple riding on it whose peak-to-peak value is

$$(\Delta v_{out})_{p\,p} = \frac{i_o t_{os}}{C} \tag{45}$$

It is possible to reduce the ripple by increasing the capacitance C in Eq. (45), but it also will enlarge the time constant associated to the integrator $\tau = RC$, thus the response time is slow. This is a common trade-off in the design of these circuits. One strategy to reduce the ripple while keeping the dynamic response consists in filtering the output. As reported in (20), a passive RC filter exhibits low ripple at all frequencies, but it is slow. The lowest ripple at high frequencies is achieved by an active filter, which also provides much faster step response than the RC filter. Finally, is it possible to cascade a second active filter on the converter's output to reduce the ripple at moderate frequencies.

Another approach to convert a frequency into a voltage is implemented by the phase-locked-loop type FVCs (21). Figure 20(b) shows a phase-locked loop (PLL), which basically works as follows. The frequency and phase detector provides an output voltage which is proportional to the difference between the output and input signal phases. After filtering, this voltage is converted back into the output frequency by a V/F converter. The feedback loop locks the phase difference between both input and output signals. The filter output voltage is proportional to the deviations of the frequency of the input signal, thus the circuit also performs a frequency-to-voltage conversion. This converter operates over a wide frequency range of 1 or 2 or 3 decades and responds quickly to frequency changes while it does not have ant inherent ripple.

Finally, pulse-integrating converters are open-loop versions of the charge balancing type converters in Section 5, thus their accuracy, linearity and stability are basically the same as those obtainable from their related VFCs. With respect to Figure 20(b), the high linearity provided by the VFC, which is not required for most PLL applications, is exploited here to get an ultra-linear FVC.

APPLICATIONS

This section describes some typical applications of the voltage-to-frequency converters, which we classify in five major fields: telemetry and remote control, isolation, digital processing, communication and signal processing, and artificial neural networks.

Telemetry and remote control

Data acquisition of remote sensors is often not possible without transforming the dc sensor output signal, because it is physically unreachable or because of the vulnerability of dc signals to be degraded when they have to travel long distances through noisy channels (10–19). Once converted to frequency signals, they can be transmitted by wires, radio or fiber optic links and processed digitally or converted back into a dc signal to drive an actuator. The latter is performed by a frequency-to-voltage converter ,

Isolation

Some applications require galvanic isolation of the sensor and the data processing unit in order to prevent unreasonable current leakage, or to prevent damage due to high bias voltages which are often of several volts. Typical isolation interfaces use magnetic or optical couplers (10, 17) like those depicted in Figure 22.

$$v_{out} = -Ri_0 t_{os} f_{in}$$

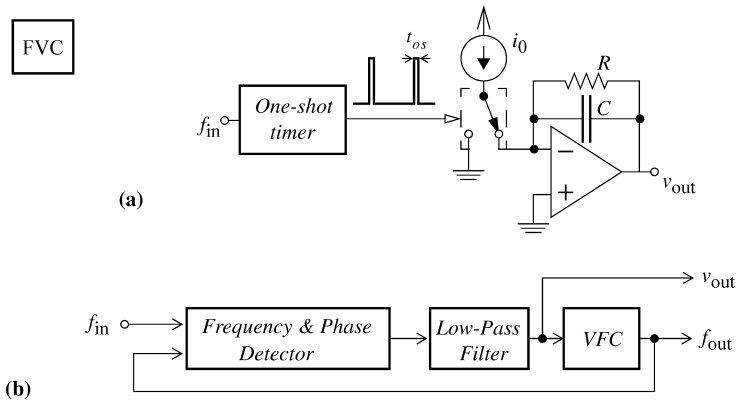

Figure 20. Frequency-to-Voltage converters. (a) Pulse-integrating converters, where the charge packets are injected in the integrator at a rate determined by the input frequency. (b) Phase-locked-loop type converters, where the low-pass filter output voltage in a PLL is proportional to the deviations of the input signal frequency.

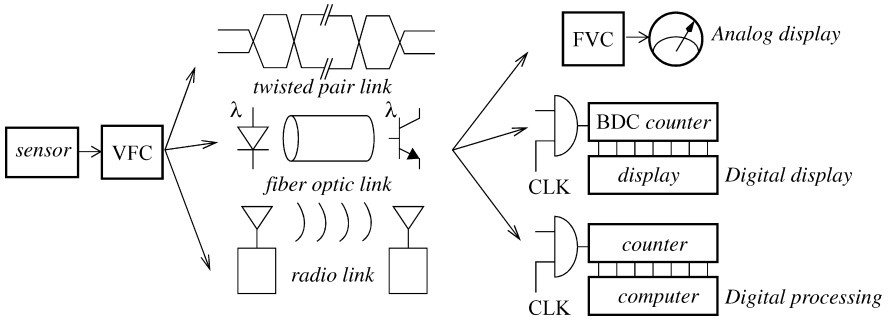

Figure 21. Telemetry with VFC. The voltage signal from a sensor is translated into a frequency signal to be transmitted through twisted pair, fiber optic or radio links. On the other side, the signal can be converted back into a voltage to drive an analog display or an actuator, or can be processed digitally.

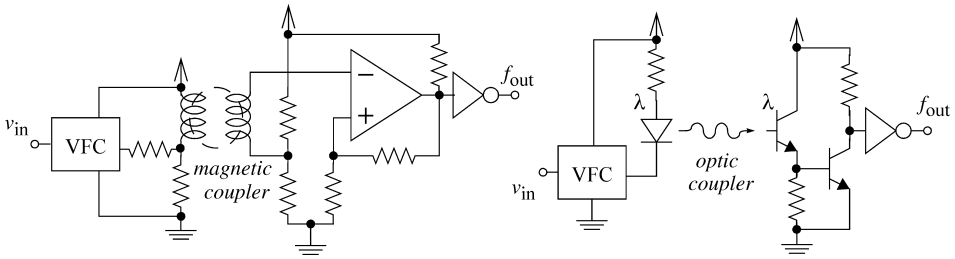

Figure 22. Isolation with VFCs. The frequency signal from a VFC can be transmitted through magnetic (a) or optic (b) couplers to implement galvanic isolation, thus preventing damage due to high bias voltages, or unreasonable current leakage.

Digital Processing

The output frequency signal from a VFC can be easily translated into a digital code in order to be processed, stored or displayed by conventional digital circuits and systems (9–28).

Actually, this procedure implements an A/D converter while transforming the dc input of the VFC into a digital word. Figure 23(a) shows the simplest way to carry out this A/D conversion, where a counter, which is only enabled for a given interval T_G named *gate time,* counts the transitions of the input signal. Thus, after this known period, the counter stores the decimal value $N = f \times T_G$, which encodes the input voltage in a binary number. Another approach is illustrated in Figure 23(b) and uses two counters, one to count the transitions of the input signal, and the other to act as a timer that generates an interruption to a microcomputer that reads the content of the first counter and resets it. In both cases, if $FS = f_{\max} - f_{\min}$ is the full fmin frequency range, the resolution of the A/D converters will be

$$n = \log_2(FS \times T_G) \tag{46}$$

where n is the number of bits of the output digital word. Hence, the larger the gate time, the larger the resolution, which is also limited by the resolution of the VFC. Commercial VFCs provide resolutions as high as 13 bits. Note

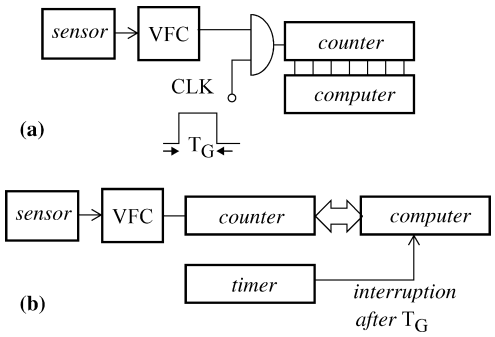

Figure 23. Digital processing of the output frequency signal of a VFC. The transitions in a fixed time interval T_G (T_G) are counted and the average frequency is computed.

that the input frequency must remain constant during the gate time for proper conversion, otherwise an average of the input frequency is computed. In addition, since the input signal and the clock are not synchronized, one cycle of the frequency signal can be lost or counted if the transition is just after or before the edge of the clock signal, which causes an error of ± 1 in the result stored in the counter.

Communication and Signal Processing

Since voltage-to-frequency converters are actually VCOs, they can be used in phase-locked loops in applications such as jitter reduction, skew suppression, frequency synthesis, clock recovery or FM modulation (23). However, special care must be taken in order to reduce the jitter and enhance the spectral purity of the output signal, like the use of differential mode in signal and control paths and guard rings to isolate the noise sources. High linearity is not a key issue in PLL applications, except that described in the Section 6, where nonlinearity degrades the loop stability but can be of several tens of percent. Higher linearity is required for FM modulation, where distortion in the detected signal must be below 1%. Figure 20(b) depicts a PLL that uses a voltage-to-frequency converter as a voltage controlled oscillator.

[i] In practice, the excitations may not strictly be dc, but ac signals whose frequency is smaller, commonly much smaller, than that of the signal generated by the circuit.

[ii] The dynamic range can be expressed in a number of equivalent bits b by using the following expression $DR = 6.02 \cdot b + 1.76$. Thus, 60dB dynamic range corresponds to an equivalent resolution of 9.7bits.

[iii] In the electronic implementations of Figure 2(b) and (c), the negative slope is caused by a negative resistance. This negative resistance injects energy into the two other circuit components, namely the inductor and the capacitor. Because these latter elements do not dissipate energy, but simply store it, the total energy becomes increased and this manifests itself as an increase of the signal amplitude. On the other hand, the positive slope is caused by a positive resistance which dissipates part of the energy stored in the energy-storage part of the circuit. At the equilibrium there is balance between the energy injected and the energy dissipated, the circuit energy remains unchanged and the movement is due to a continuous interchange of this energy between the inductor and the capacitor.

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[iv] This device is obsolete, but its data are still a good example of the performance obtained with this implementation.

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